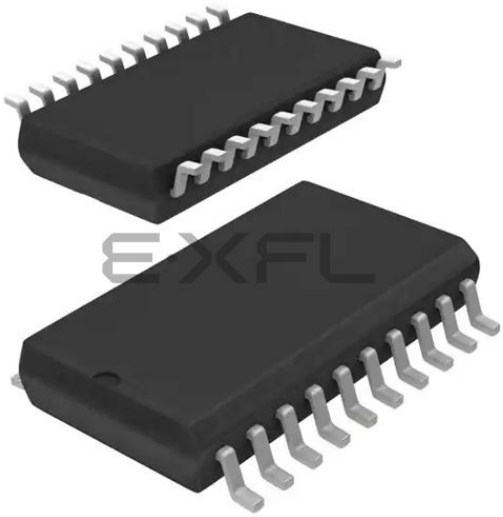

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	USI
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny861a-sur

be used. If a reset occurs while a write operation is in progress, the write operation will be completed provided that the power supply voltage is sufficient.

5.4 I/O Memory

The I/O space definition of the ATtiny261A/461A/861A is shown in “Register Summary” on page 277.

All I/Os and peripherals are placed in the I/O space. All I/O locations may be accessed using the LD/LDS/LDD and ST/STS/STD instructions, enabling data transfer between the 32 general purpose working registers and the I/O space. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions. Refer to the instruction set section for more details. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses.

For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

Some of the Status Flags are cleared by writing a logical one to them. Note that, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work on registers in the address range 0x00 to 0x1F, only.

The I/O and Peripherals Control Registers are explained in later sections.

5.4.1 General Purpose I/O Registers

The ATtiny261A/461A/861A contains three General Purpose I/O Registers. These registers can be used for storing any information, and they are particularly useful for storing global variables and Status Flags. General Purpose I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI, CBI, SBIS, and SBIC instructions.

5.5 Register Description

5.5.1 EEARH – EEPROM Address Register

Bit	7	6	5	4	3	2	1	0	
0x1F (0x3F)	–	–	–	–	–	–	–	EEAR8	EEARH
Read/Write	R	R	R	R	R	R	R	R/W	
Initial Value	0	0	0	0	0	0	0	X/0	

- **Bits 7:1 – Res: Reserved Bits**

These bits are reserved and will always read as zero.

- **Bit 0 – EEAR8: EEPROM Address**

This is the most significant EEPROM address bit of ATtiny861A. In devices with less EEPROM, i.e. ATtiny261A/ATtiny461A, this bit is reserved and will always read zero. The initial value of the EEPROM Address Register (EEAR) is undefined and a proper value must therefore be written before the EEPROM is accessed.

10.2.2 Alternate Functions of Port B

The Port B pins with alternate function are shown in Table 10-6.

Table 10-6. Port B Pins Alternate Functions

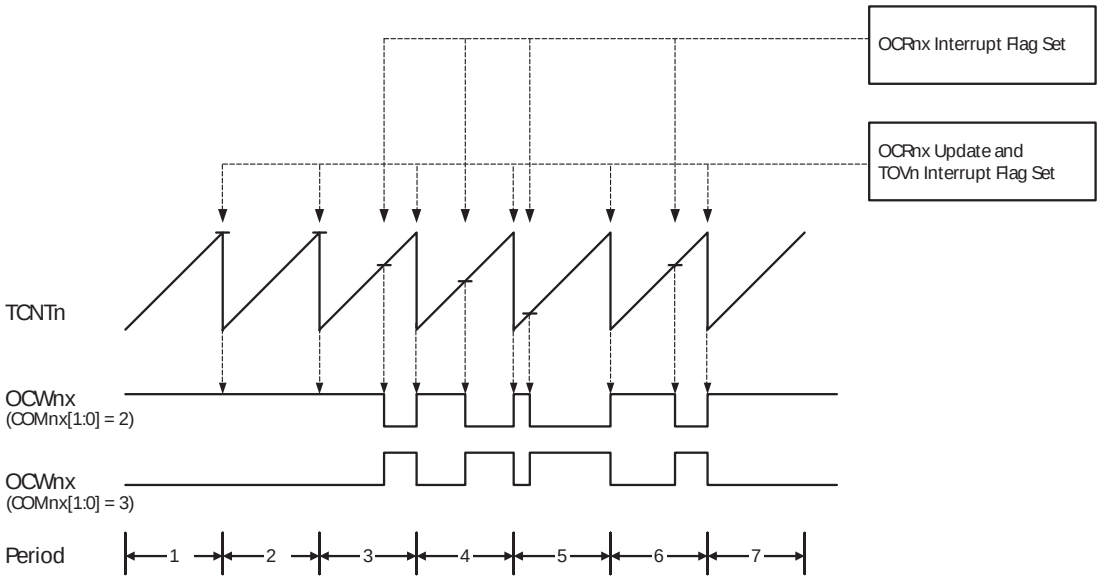
Port Pin	Alternate Function
PB7	$\overline{\text{RESET}}$: Reset pin dW: debugWire I/O ADC10: ADC Input Channel 10 PCINT15: Pin Change Interrupt 0, Source 15
PB6	ADC9: ADC Input Channel 9 T0: Timer/Counter0 Clock Source INT0: External Interrupt 0 Input PCINT14: Pin Change Interrupt 0, Source 14
PB5	XTAL2: Crystal Oscillator Output CLKO: System Clock Output OC1D: Timer/Counter1 Compare Match D Output ADC8: ADC Input Channel 8 PCINT13: Pin Change Interrupt 0, Source 13
PB4	XTAL1: Crystal Oscillator Input CLKI: External Clock Input $\overline{\text{OC1D}}$: Inverted Timer/Counter1 Compare Match D Output ADC7: ADC Input Channel 7 PCINT12: Pin Change Interrupt 0, Source 12
PB3	OC1B: Timer/Counter1 Compare Match B Output PCINT11: Pin Change Interrupt 0, Source 11
PB2	USCK: USI Clock (Three Wire Mode) SCL : USI Clock (Two Wire Mode) $\overline{\text{OC1B}}$: Inverted Timer/Counter1 Compare Match B Output PCINT10: Pin Change Interrupt 0, Source 10
PB1	DO: USI Data Output (Three Wire Mode) OC1A: Timer/Counter1 Compare Match A Output PCINT9: Pin Change Interrupt 1, Source 9
PB0	DI: USI Data Input (Three Wire Mode) SDA: USI Data Input (Two Wire Mode) $\overline{\text{OC1A}}$: Inverted Timer/Counter1 Compare Match A Output PCINT8: Pin Change Interrupt 1, Source 8

- **Port B, Bit 7 – $\overline{\text{RESET}}$/dW/ADC10/PCINT15**
  - RESET, Reset pin: When the RSTDISBL Fuse is programmed, this pin functions as a normal I/O pin, and the part will have to rely on Power-on Reset and Brown-out Reset as its reset sources. When the RSTDISBL Fuse is unprogrammed, the reset circuitry is connected to the pin, and the pin can not be used as an I/O pin.
  - If PB7 is used as a reset pin, DDB7, PORTB7 and PINB7 will all read 0.
  - dW: When the debugWIRE Enable (DWEN) Fuse is programmed and Lock bits are unprogrammed, the RESET port pin is configured as a wire-AND (open-drain) bi-directional I/O pin with pull-up enabled and becomes the communication gateway between target and emulator.

DAC applications. High frequency allows physically small sized external components (coils, capacitors), and therefore reduces total system cost.

The timing diagram for the fast PWM mode is shown in Figure 12-12. The counter is incremented until the counter value matches the TOP value. The counter is then cleared at the following timer clock cycle. The TCNT1 value is in the timing diagram shown as a histogram for illustrating the single-slope operation. The diagram includes the Waveform Output in non-inverted and inverted Compare Output modes. The small horizontal line marks on the TCNT1 slopes represent Compare Matches between OCR1x and TCNT1.

Figure 12-12. Fast PWM Mode, Timing Diagram



The Timer/Counter Overflow Flag (TOV1) is set each time the counter reaches TOP. If the interrupt is enabled, the interrupt handler routine can be used for updating the compare value.

In fast PWM mode, the compare unit allows generation of PWM waveforms on the OC1x pins. Setting the COM1x[1:0] bits to two will produce a non-inverted PWM and setting the COM1x[1:0] to three will produce an inverted PWM output. Setting the COM1x[1:0] bits to one will enable complementary Compare Output mode and produce both the non-inverted (OC1x) and inverted output ($\overline{OC1x}$). The actual value will only be visible on the port pin if the data direction for the port pin is set as output. The PWM waveform is generated by setting (or clearing) the Waveform Output (OCW1x) at the Compare Match between OCR1x and TCNT1, and clearing (or setting) the Waveform Output at the timer clock cycle the counter is cleared (changes from TOP to BOTTOM).

The PWM frequency for the output can be calculated by the following equation:

$$f_{OCnxPWM} = \frac{f_{clkT1}}{N}$$

The *N* variable represents the number of steps in single-slope operation. The value of *N* equals either to the TOP value.

The extreme values for the OCR1C Register represents special cases when generating a PWM waveform output in the fast PWM mode. If the OCR1C is set equal to BOTTOM, the output will be a narrow spike for each MAX+1 timer clock cycle. Setting the OCR1C equal to MAX will result

Table 13-1. Relationship between USIWM[1:0] and USI Operation (Continued)

USIWM1	USIWM0	Description
1	0	Two-wire mode. Uses SDA (DI) and SCL (USCK) pins (1). The *Serial Data* (SDA) and the *Serial Clock* (SCL) pins are bi-directional and use open-collector output drives. The output drivers are enabled by setting the corresponding bit for SDA and SCL in the DDRA register. When the output driver is enabled for the SDA pin, the output driver will force the line SDA low if the output of the USI Data Register or the corresponding bit in the PORTA register is zero. Otherwise, the SDA line will not be driven (i.e., it is released). When the SCL pin output driver is enabled the SCL line will be forced low if the corresponding bit in the PORTA register is zero, or by the start detector. Otherwise the SCL line will not be driven. The SCL line is held low when a start detector detects a start condition and the output is enabled. Clearing the Start Condition Flag (USISIF) releases the line. The SDA and SCL pin inputs is not affected by enabling this mode. Pull-ups on the SDA and SCL port pin are disabled in Two-wire mode.
1	1	Two-wire mode. Uses SDA and SCL pins. Same operation as in two-wire mode above, except that the SCL line is also held low when a counter overflow occurs, and until the Counter Overflow Flag (USIOIF) is cleared.

Note: 1. The DI and USCK pins are renamed to *Serial Data* (SDA) and *Serial Clock* (SCL) respectively to avoid confusion between the modes of operation.

- **Bits 3:2 – USICS[1:0]: Clock Source Select**

These bits set the clock source for the USI Data Registerr and counter. The data output latch ensures that the output is changed at the opposite edge of the sampling of the data input (DI/SDA) when using external clock source (USCK/SCL). When software strobe or Timer/Counter0 Compare Match clock option is selected, the output latch is transparent and therefore the output is changed immediately. Clearing the USICS[1:0] bits enables software strobe option. When using this option, writing a one to the USICLK bit clocks both the USI Data Register and the counter. For external clock source (USICS1 = 1), the USICLK bit is no longer used as a strobe, but selects between external clocking and software clocking by the USITC strobe bit.

Table 13-2 on page 134 shows the relationship between the USICS[1:0] and USICLK setting and clock source used for the USI Data Register and the 4-bit counter.

Table 13-2. Relations between the USICS[1:0] and USICLK Setting

USICS1	USICS0	USICLK	USI Data Register Clock Source	4-bit Counter Clock Source
0	0	0	No Clock	No Clock
0	0	1	Software clock strobe (USICLK)	Software clock strobe (USICLK)
0	1	X	Timer/Counter0 Compare Match	Timer/Counter0 Compare Match
1	0	0	External, positive edge	External, both edges

reference may be decoupled by an external capacitor at the AREF pin to improve noise immunity.

The analog input channel and differential gain are selected by writing to the MUX[5:0] bits in ADMUX. Any of the 11 ADC input pins ADC[10:0] can be selected as single ended inputs to the ADC. The positive and negative inputs to the differential gain amplifier are described in Table 15-5.

If differential channels are selected, the differential gain stage amplifies the voltage difference between the selected input pair by the selected gain factor, 1x, 8x, 20x or 32x, according to the setting of the MUX[5:0] bits in ADMUX and the GSEL bit in ADCSRB. This amplified value then becomes the analog input to the ADC. If single ended channels are used, the gain amplifier is bypassed altogether.

If the same ADC input pin is selected as both the positive and negative input to the differential gain amplifier, the remaining offset in the gain stage and conversion circuitry can be measured directly as the result of the conversion. This figure can be subtracted from subsequent conversions with the same gain setting to reduce offset error to below 1 LSW.

The on-chip temperature sensor is selected by writing the code “111111” to the MUX[5:0] bits in ADMUX register when the ADC11 channel is used as an ADC input.

The ADC is enabled by setting the ADC Enable bit, ADEN in ADCSRA. Voltage reference and input channel selections will not go into effect until ADEN is set. The ADC does not consume power when ADEN is cleared, so it is recommended to switch off the ADC before entering power saving sleep modes.

The ADC generates a 10-bit result which is presented in the ADC Data Registers, ADCH and ADCL. By default, the result is presented right adjusted, but can optionally be presented left adjusted by setting the ADLAR bit in ADMUX.

If the result is left adjusted and no more than 8-bit precision is required, it is sufficient to read ADCH. Otherwise, ADCL must be read first, then ADCH, to ensure that the content of the data registers belongs to the same conversion. Once ADCL is read, ADC access to data registers is blocked. This means that if ADCL has been read, and a conversion completes before ADCH is read, neither register is updated and the result from the conversion is lost. When ADCH is read, ADC access to the ADCH and ADCL Registers is re-enabled.

The ADC has its own interrupt which can be triggered when a conversion completes. When ADC access to the data registers is prohibited between reading of ADCH and ADCL, the interrupt will trigger even if the result is lost.

15.4 Starting a Conversion

A single conversion is started by writing a logical one to the ADC Start Conversion bit, ADSC. This bit stays high as long as the conversion is in progress and will be cleared by hardware when the conversion is completed. If a different data channel is selected while a conversion is in progress, the ADC will finish the current conversion before performing the channel change.

Alternatively, a conversion can be triggered automatically by various sources. Auto Triggering is enabled by setting the ADC Auto Trigger Enable bit, ADATE in ADCSRA. The trigger source is selected by setting the ADC Trigger Select bits, ADTS in ADCSRB (see description of the ADTS bits for a list of the trigger sources). When a positive edge occurs on the selected trigger signal, the ADC prescaler is reset and a conversion is started. This provides a method of starting conversions at fixed intervals. If the trigger signal still is set when the conversion completes, a new

selection. Since the next conversion has already started automatically, the next result will reflect the previous channel selection. Subsequent conversions will reflect the new channel selection.

15.6.2 ADC Voltage Reference

The conversion range of the ADC is defined by the voltage reference (V_{REF}). Single ended channels that exceed V_{REF} will result in codes close to 0x3FF. V_{REF} can be selected as either V_{CC}, or internal 1.1V / 2.56V voltage reference, or external AREF pin. The first conversion result after switching voltage reference source may be inaccurate, and the user is advised to discard this result.

15.7 ADC Noise Canceler

The ADC features a noise canceler that enables conversion during sleep mode. This reduces noise induced from the CPU core and other I/O peripherals. The noise canceler can be used with ADC Noise Reduction and Idle mode. To make use of this feature, the following procedure should be used:

- Make sure that the ADC is enabled and is not busy converting. Single Conversion mode must be selected and the ADC conversion complete interrupt must be enabled.
- Enter ADC Noise Reduction mode (or Idle mode). The ADC will start a conversion once the CPU has been halted.
- If no other interrupts occur before the ADC conversion completes, the ADC interrupt will wake up the CPU and execute the ADC Conversion Complete interrupt routine. If another interrupt wakes up the CPU before the ADC conversion is complete, it will be executed, and an ADC Conversion Complete interrupt request will be generated when the ADC conversion completes. The CPU will remain in active mode until a new sleep command is executed.

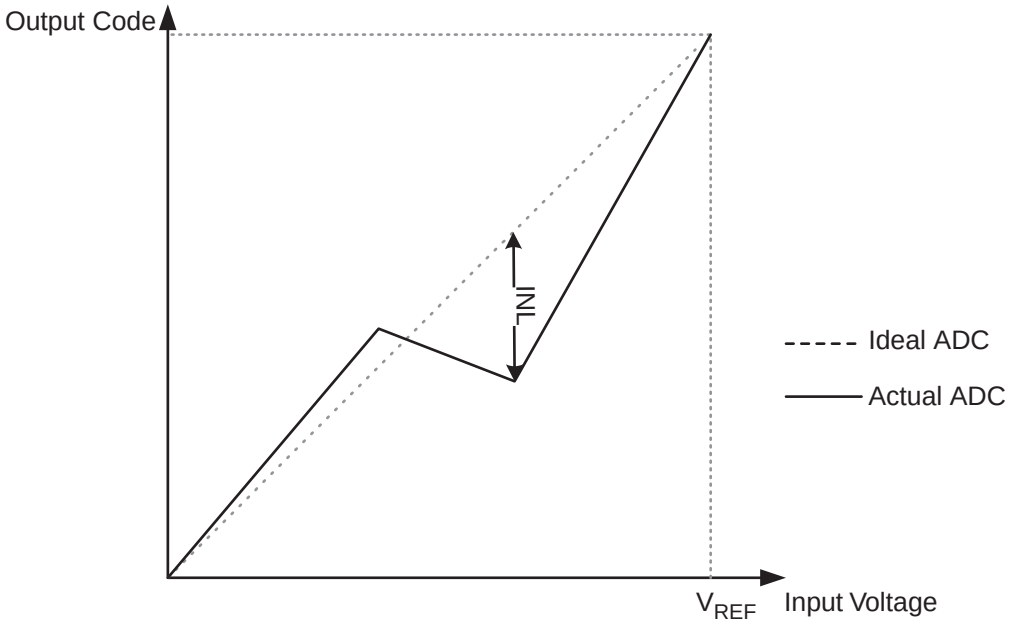
Note that the ADC will not automatically be turned off when entering other sleep modes than Idle mode and ADC Noise Reduction mode. The user is advised to write zero to ADEN before entering such sleep modes to avoid excessive power consumption.

15.8 Analog Input Circuitry

The analog input circuitry for single ended channels is illustrated in Figure 15-8 An analog source applied to ADCn is subjected to the pin capacitance and input leakage of that pin, regardless of whether that channel is selected as input for the ADC. When the channel is selected, the source must drive the S/H capacitor through the series resistance (combined resistance in the input path).

- Integral Non-linearity (INL): After adjusting for offset and gain error, the INL is the maximum deviation of an actual transition compared to an ideal transition for any code. Ideal value: 0 LSB.

Figure 15-11. Integral Non-linearity (INL)



- Differential Non-linearity (DNL): The maximum deviation of the actual code width (the interval between two adjacent transitions) from the ideal code width (1 LSB). Ideal value: 0 LSB.

Figure 15-12. Differential Non-linearity (DNL)

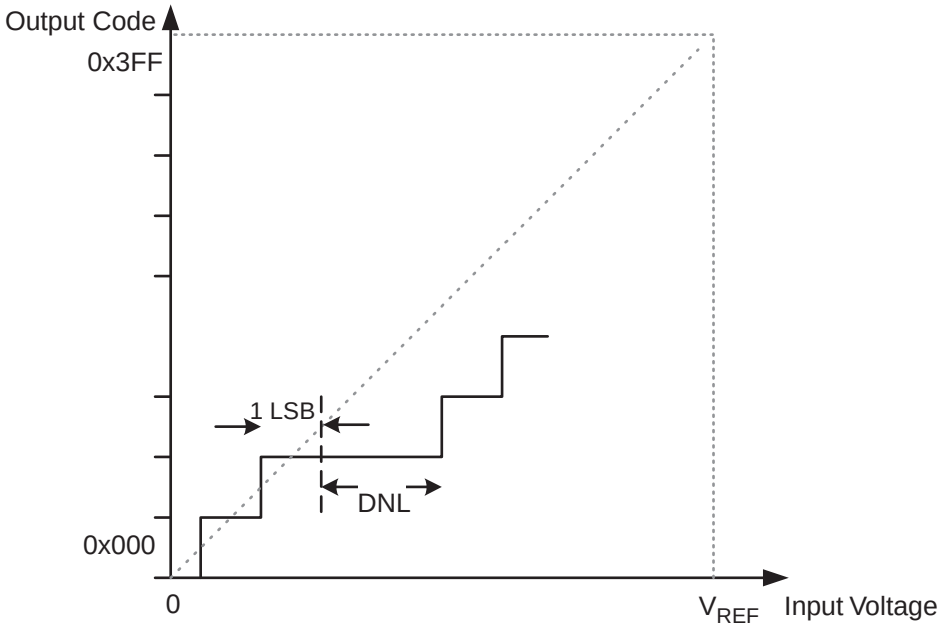


Table 18-5. Fuse Low Byte

Fuse Low Byte	Bit No	Description	Default Value
CKDIV8 (1)	7	Divide clock by 8	0 (programmed)
CKOUT (2)	6	Clock Output Enable	1 (unprogrammed)
SUT1	5	Select start-up time	1 (unprogrammed) (3)
SUT0	4	Select start-up time	0 (programmed) (3)
CKSEL3	3	Select Clock source	0 (programmed) (4)
CKSEL2	2	Select Clock source	0 (programmed) (4)
CKSEL1	1	Select Clock source	1 (unprogrammed) (4)
CKSEL0	0	Select Clock source	0 (programmed) (4)

Notes:
1. See "System Clock Prescaler" on page 31 for details.
2. Allows system clock to be output on pin. See "Clock Output Buffer" on page 32 for details.
3. The default value results in maximum start-up time for the default clock source. See Table 6-7 on page 28 for details.
4. The default setting results in internal oscillator @ 8.0 MHz. See Table 6-6 on page 28 for details.

Note that fuse bits are locked if Lock Bit 1 (LB1) is programmed. Fuse bits should be programmed before lock bits. The status of fuse bits is not affected by chip erase.

Fuse bits can also be read by device firmware. See section "Reading Fuse and Lock Bits from Software" on page 165.

18.2.1 Latching of Fuses

Fuse values are latched when the device enters programming mode and changes to fuse values have no effect until the part leaves programming mode. This does not apply to the EESAVE Fuse which will take effect once it is programmed. Fuses are also latched on power-up.

18.3 Signature Bytes

All Atmel microcontrollers have a three-byte signature code which identifies the device. This code can be read in both serial and High-voltage Programming mode, also when the device is locked. The three bytes reside in a separate address space. The signature bytes are given in Table 18-6.

Table 18-6. Device ID

	Signature Bytes Address		
Parts	0x000	0x001	0x002
ATtiny261A	0x1E	0x91	0x0C
ATtiny461A	0x1E	0x92	0x08
ATtiny861A	0x1E	0x93	0x0D

18.4 Calibration Byte

The signature area has one byte of calibration data for the internal oscillator. This byte resides in the high byte of address 0x000. During reset, this byte is automatically written into the OSCCAL Register to ensure correct frequency of the calibrated oscillator.

18.5 Page Size

Table 18-7. No. of Words in a Page and No. of Pages in the Flash

Device	Flash Size	Page Size	PCWORD	No. of Pages	PCPAGE	PCMSB
ATtiny261A	1K words (2K bytes)	16 words	PC[3:0]	64	PC[9:4]	9
ATtiny461A	2K words (4K bytes)	32 words	PC[4:0]	64	PC[10:5]	10
ATtiny861A	4K words (8K bytes)	32 words	PC[4:0]	128	PC[11:5]	11

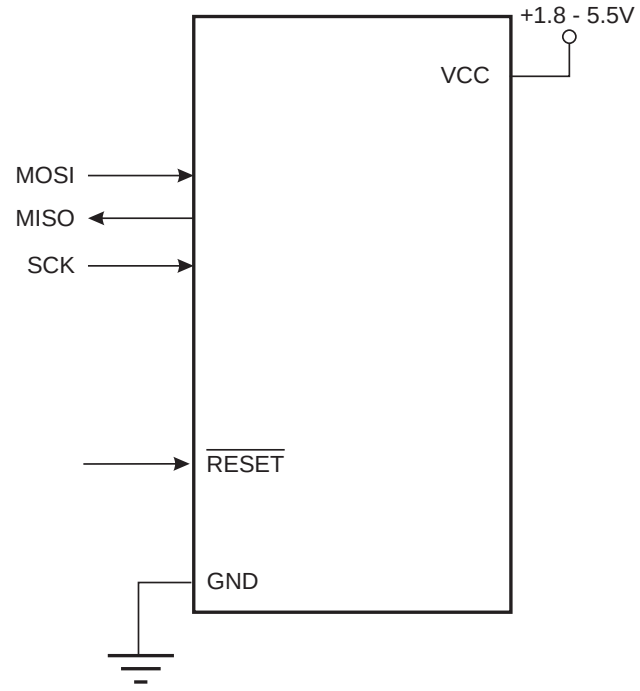
Table 18-8. No. of Words in a Page and No. of Pages in the EEPROM

Device	EEPROM Size	Page Size	PCWORD	No. of Pages	PCPAGE	EEAMSB
ATtiny261A	128 bytes	4 bytes	EEA[1:0]	32	EEA[6:2]	6
ATtiny461A	256 bytes	4 bytes	EEA[1:0]	64	EEA[7:2]	7
ATtiny861A	512 bytes	4 bytes	EEA[1:0]	128	EEA[8:2]	8

18.6 Serial Programming

Both the Flash and EEPROM memory arrays can be programmed using the serial SPI bus while $\overline{\text{RESET}}$ is pulled to GND. The serial interface consists of pins SCK, MOSI (input) and MISO (output). See Figure 18-1.

Figure 18-1. Serial Programming and Verify



Note: If the device is clocked by the internal Oscillator, there is no need to connect a clock source to the CLKI pin.

19.7 Analog Comparator Characteristics

Table 19-10. Analog Comparator Characteristics, T_A = -40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{AIO}	Input Offset Voltage	V_{CC} = 5V, VIN = V_{CC} / 2		< 10	40	mV
I_{LAC}	Input Leakage Current	V_{CC} = 5V, VIN = V_{CC} / 2	-50		50	nA
t_{APD}	Analog Propagation Delay (from saturation to slight overdrive)	V_{CC} = 2.7V		750		ns
		V_{CC} = 4.0V		500		
	Analog Propagation Delay (large step change)	V_{CC} = 2.7V		100		
		V_{CC} = 4.0V		75		
t_{DPD}	Digital Propagation Delay	V_{CC} = 1.8V - 5.5		1	2	CLK

19.8 Serial Programming Characteristics

Figure 19-3. Serial Programming Waveforms

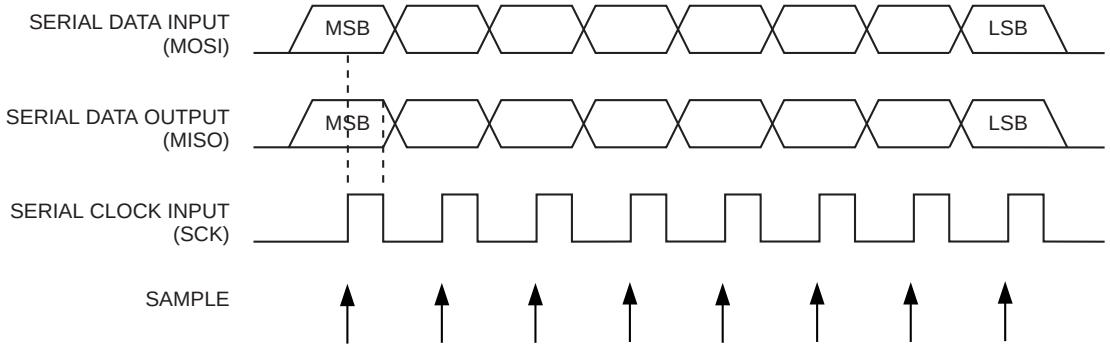


Figure 19-4. Serial Programming Timing

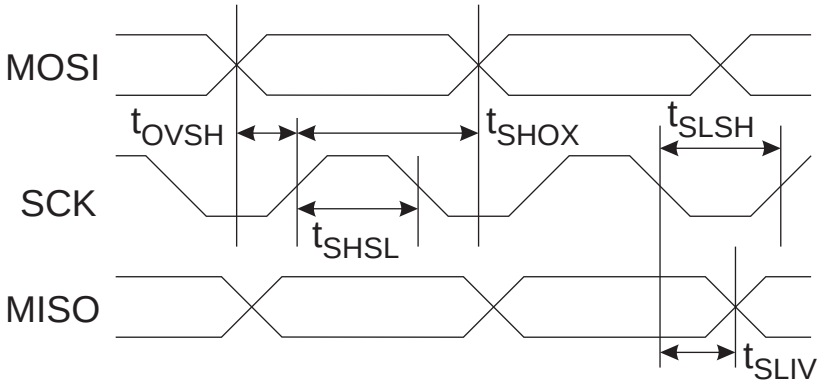


Table 19-12. Parallel Programming Characteristics, V_{CC} = 5V ± 10% (Continued)

Symbol	Parameter	Min	Typ	Max	Units
t_{XLXH}	XTAL1 Low to XTAL1 High	200			ns
t_{XHXL}	XTAL1 Pulse Width High	150			ns
t_{XLDX}	Data and Control Hold after XTAL1 Low	67			ns
t_{XLWL}	XTAL1 Low to $\overline{WR}$ Low	0			ns
t_{BVPH}	BS1 Valid before PAGEL High	67			ns
t_{PHPL}	PAGEL Pulse Width High	150			ns
t_{PLBX}	BS1 Hold after PAGEL Low	67			ns
t_{WLBX}	BS2/1 Hold after $\overline{WR}$ Low	67			ns
t_{PLWL}	PAGEL Low to $\overline{WR}$ Low	67			ns
t_{BVWL}	BS1 Valid to $\overline{WR}$ Low	67			ns
t_{WLWH}	$\overline{WR}$ Pulse Width Low	150			ns
t_{WLRL}	$\overline{WR}$ Low to RDY/$\overline{BSY}$ Low	0		1	µs
t_{WLRH}	$\overline{WR}$ Low to RDY/$\overline{BSY}$ High(1)	3.7		4.5	ms
t_{WLRH_CE}	$\overline{WR}$ Low to RDY/$\overline{BSY}$ High for Chip Erase(2)	7.5		9	ms
t_{XLOL}	XTAL1 Low to $\overline{OE}$ Low	0			ns
t_{BVDV}	BS1 Valid to DATA valid	0		250	ns
t_{OLDV}	$\overline{OE}$ Low to DATA Valid			250	ns
t_{OHDZ}	$\overline{OE}$ High to DATA Tri-stated			250	ns

Notes: 1. t_{WLRH} is valid for the Write Flash, Write EEPROM, Write Fuse bits and Write Lock bits commands.

2. t_{WLRH_CE} is valid for the Chip Erase command.

Figure 20-39. V_{IH}: Input Threshold Voltage vs. V_{CC} (Reset Pin, Read as '1')

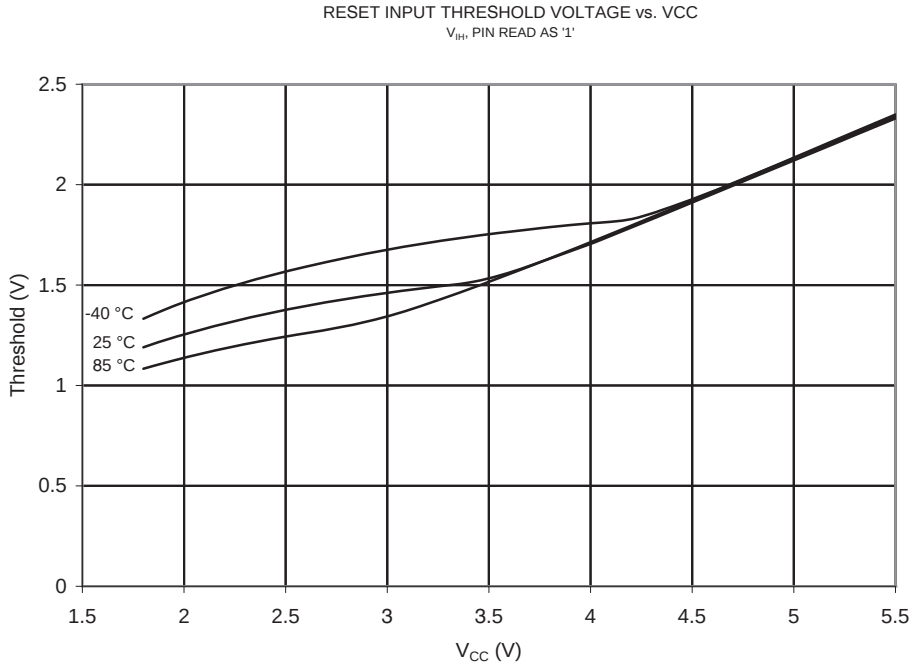


Figure 20-40. V_{IL}: Input Threshold Voltage vs. V_{CC} (Reset Pin, Read as '0')

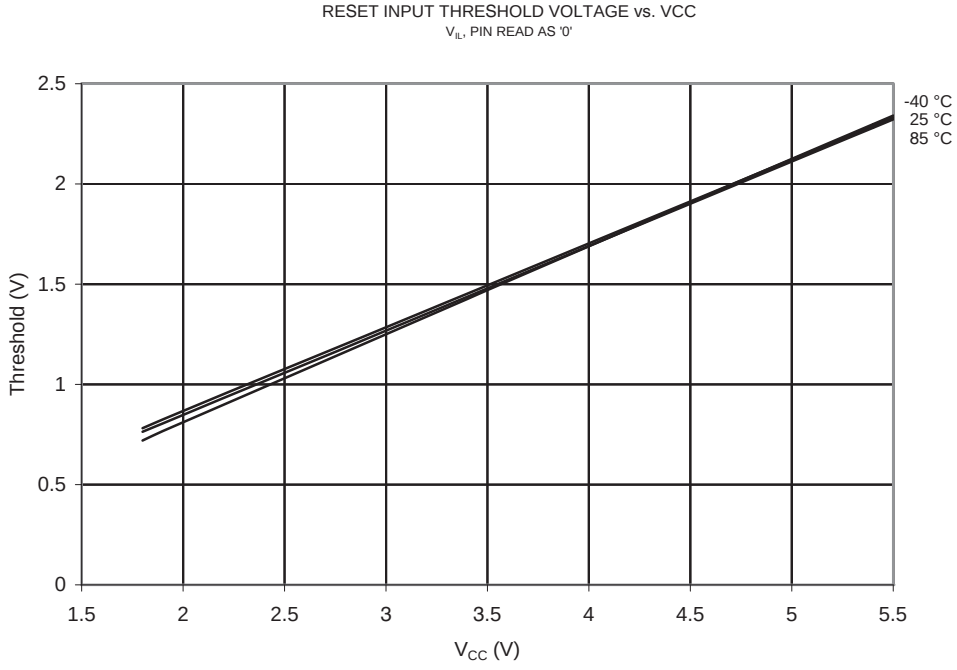


Figure 20-72. Pull-Up Resistor Current vs. Input Voltage (I/O Pin, V_{CC} = 3V)

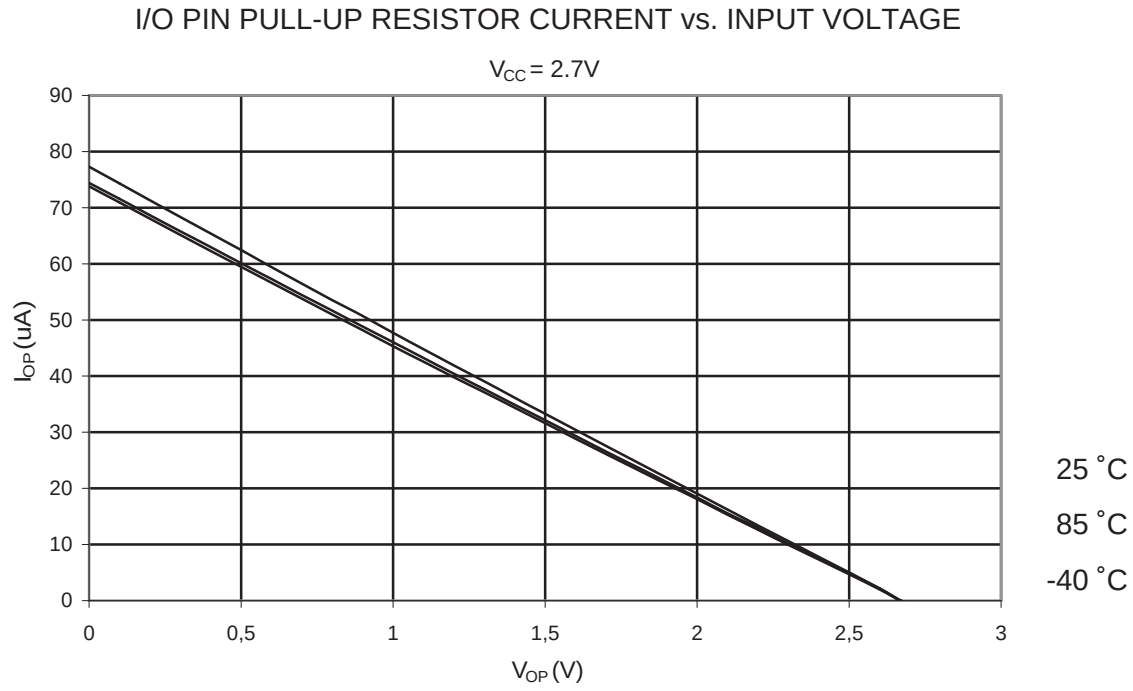


Figure 20-73. Pull-Up Resistor Current vs. Input Voltage (I/O Pin, V_{CC} = 5V)

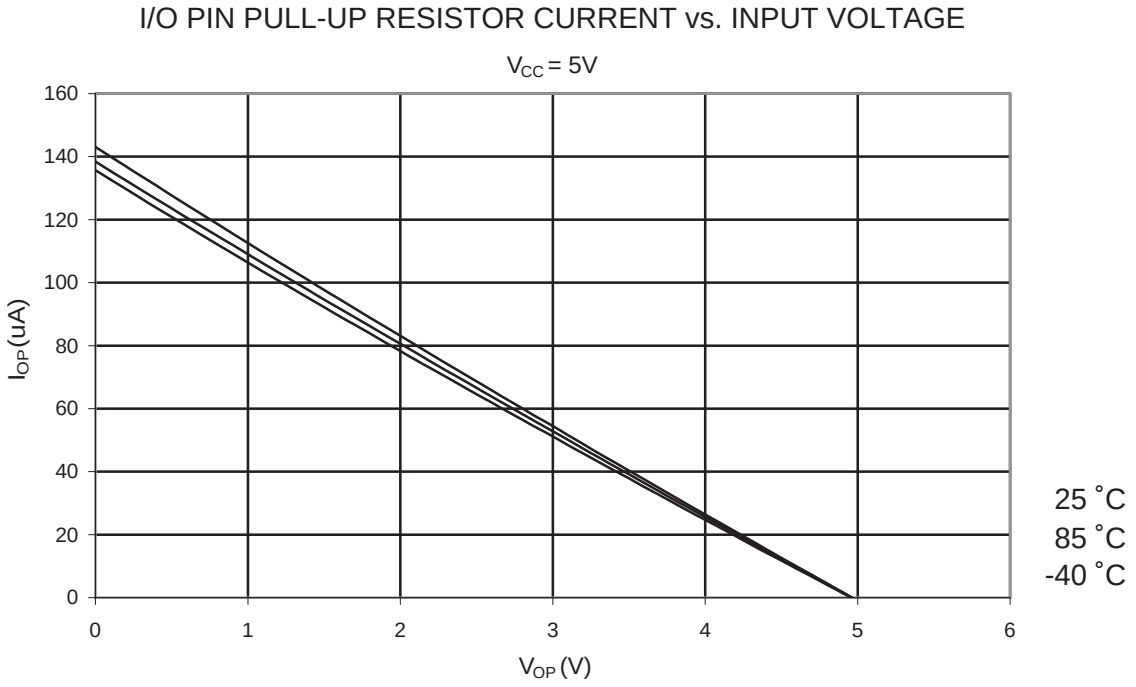


Figure 20-74. Pull-Up Resistor Current vs. Input Voltage (Reset Pin, V_{CC} = 1.8V)

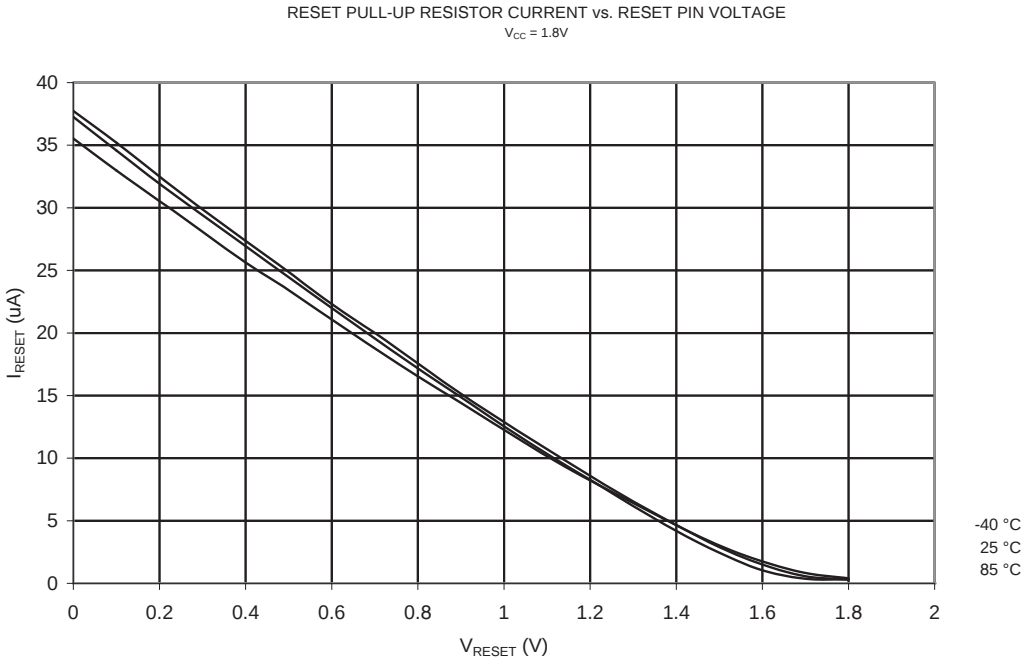


Figure 20-75. Pull-Up Resistor Current vs. Input Voltage (Reset Pin, V_{CC} = 3V)

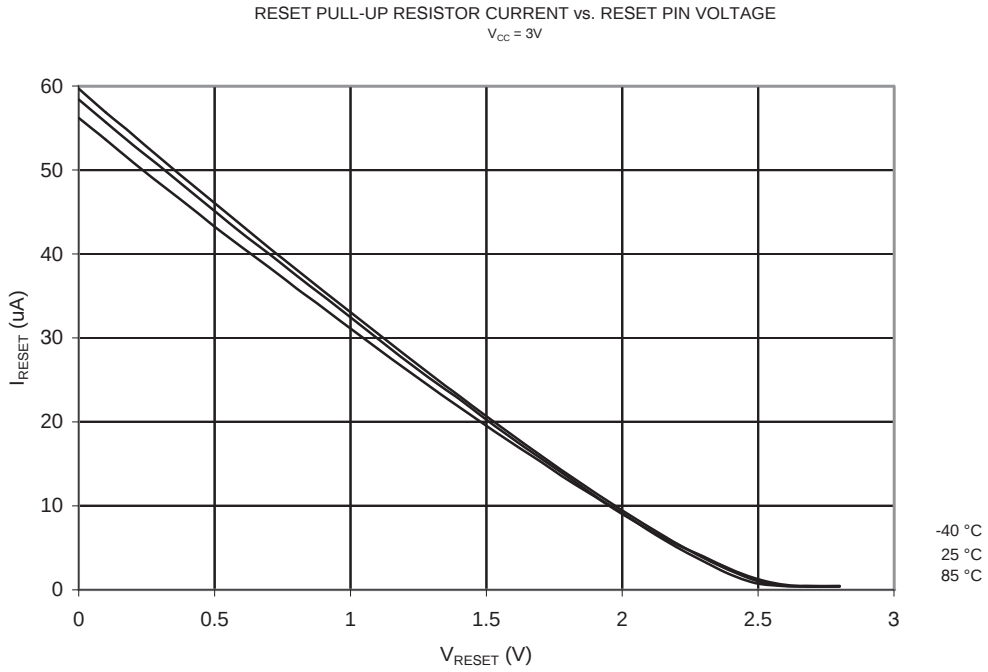


Figure 20-111. Idle Supply Current vs. V_{CC} (Internal Calibrated Oscillator, 1 MHz)

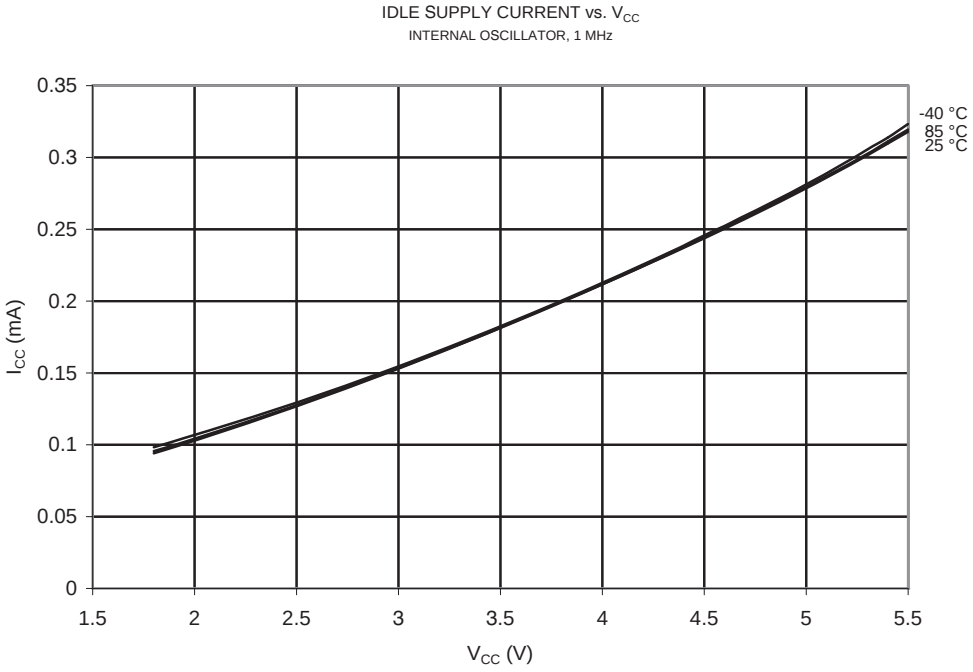


Figure 20-112. Idle Supply Current vs. V_{CC} (Internal Calibrated Oscillator, 128 kHz)

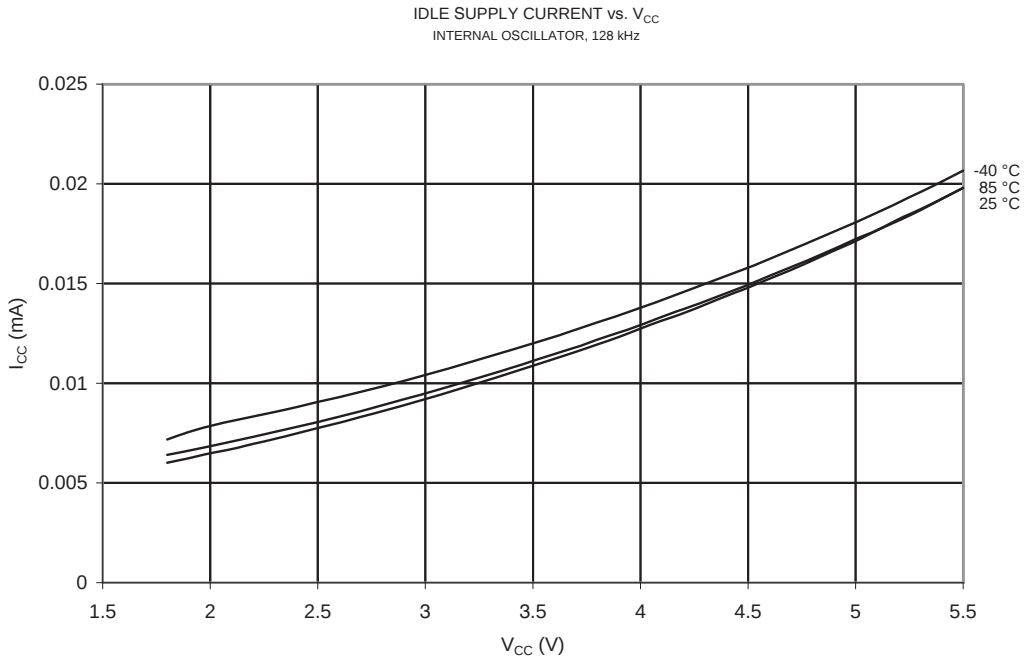


Figure 20-119. Timer/Counter1 Current vs. V_{CC}

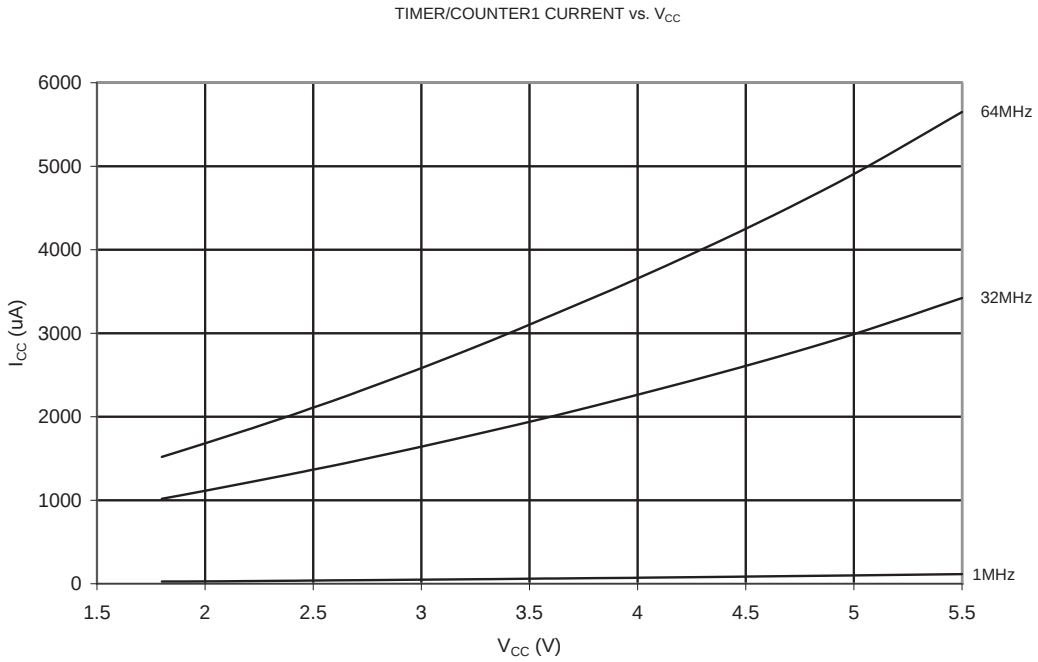


Figure 20-120. Brownout Detector Current vs. V_{CC}

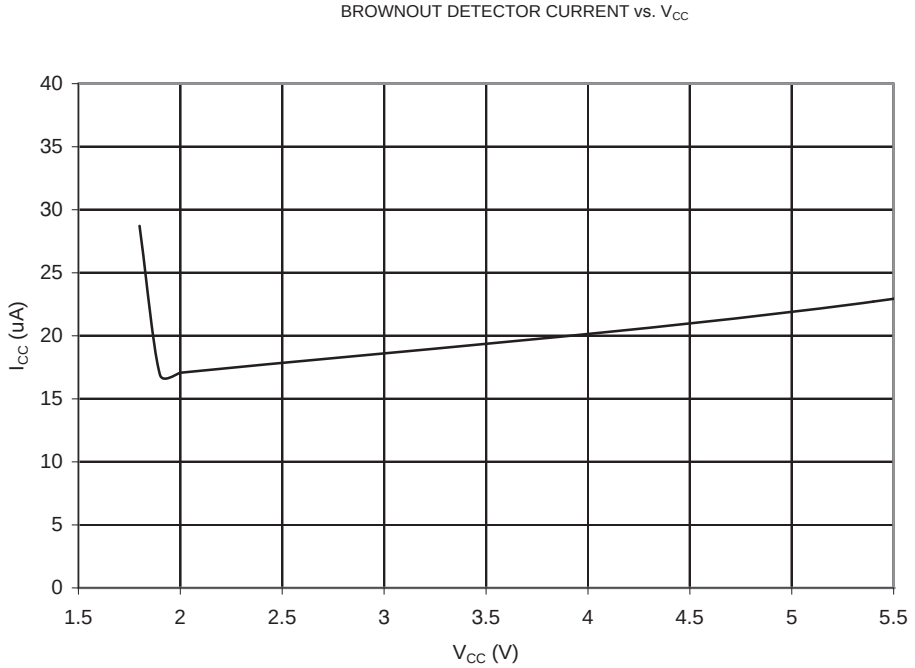
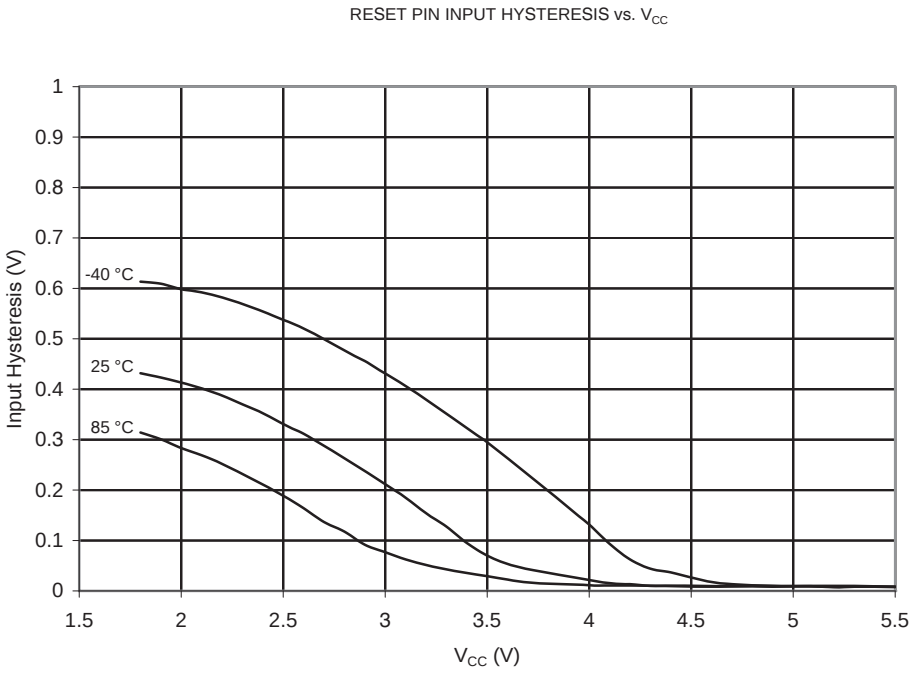


Figure 20-143. V_{IH}-V_{IL}: Input Hysteresis vs. V_{CC} (Reset Pin)



20.4.9 BOD, Bandgap and Reset

Figure 20-144. BOD Threshold vs. Temperature (BOD Level set to 4.3V)

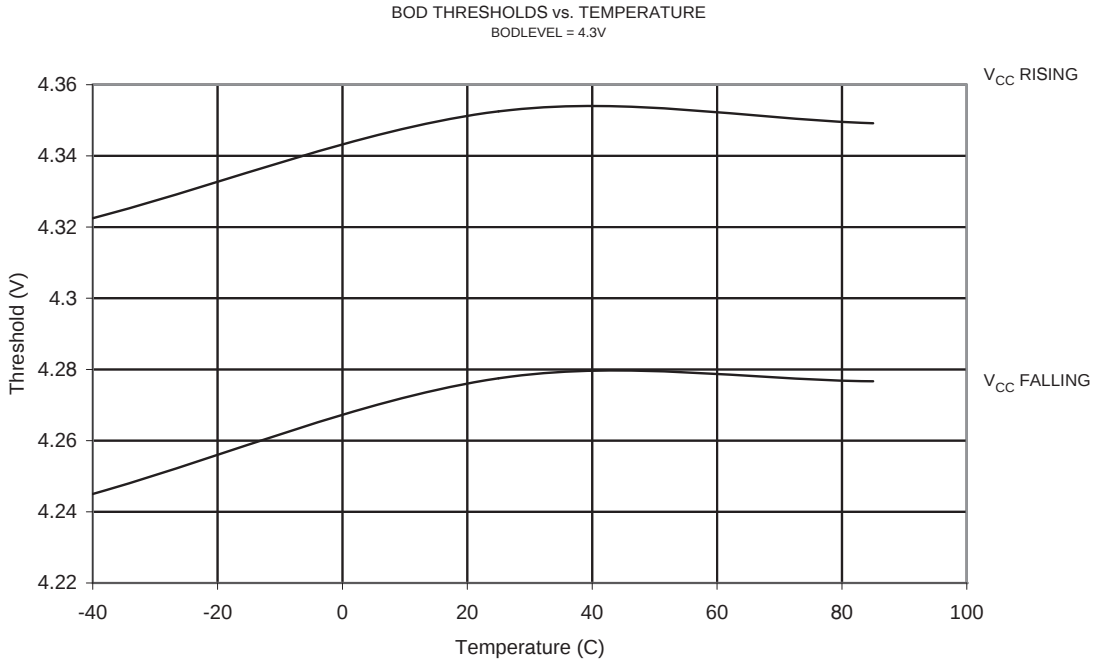


Figure 20-153. Frequency of Calibrated 8.0 MHz Oscillator vs. OSCCAL Value