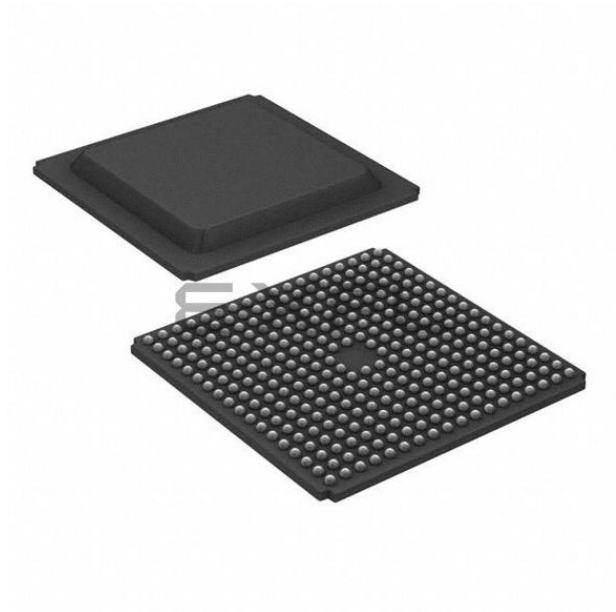
AMD Xilinx - XC3S1000-4FG320C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1920
Number of Logic Elements/Cells	17280
Total RAM Bits	442368
Number of I/O	221
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1000-4fg320c

Spartan-3 FPGA Design Documentation

The functionality of the Spartan®-3 FPGA family is described in the following documents. The topics covered in each guide are listed.

- UG331: *Spartan-3 Generation FPGA User Guide*
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Software Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
- UG332: *Spartan-3 Generation Configuration User Guide*
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx Platform Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples

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For specific hardware examples, see the Spartan-3 FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- Spartan-3 FPGA Starter Kit Board page
  http://www.xilinx.com/s3starter
- UG130: *Spartan-3 FPGA Starter Kit User Guide*

According to Figure 7, the clock line OTCLK1 connects the CK inputs of the upper registers on the output and three-state paths. Similarly, OTCLK2 connects the CK inputs for the lower registers on the output and three-state paths. The upper and lower registers on the input path have independent clock lines: ICLK1 and ICLK2. The enable line OCE connects the CE inputs of the upper and lower registers on the output path. Similarly, TCE connects the CE inputs for the register pair on the three-state path and ICE does the same for the register pair on the input path. The Set/Reset (SR) line entering the IOB is common to all six registers, as is the Reverse (REV) line.

Each storage element supports numerous options in addition to the control over signal polarity described in the IOB Overview section. These are described in Table 6.

Table 6: **Storage Element Options**

Option Switch	Function	Specificity
FF/Latch	Chooses between an edge-sensitive flip-flop or a level-sensitive latch	Independent for each storage element.
SYNC/ASYNC	Determines whether SR is synchronous or asynchronous	Independent for each storage element.
SRHIGH/SRLOW	Determines whether SR acts as a Set, which forces the storage element to a logic “1" (SRHIGH) or a Reset, which forces a logic “0” (SRLOW).	Independent for each storage element, except when using FDDR. In the latter case, the selection for the upper element (OFF1 or TFF2) applies to both elements.
INIT1/INIT0	In the event of a Global Set/Reset, after configuration or upon activation of the GSR net, this switch decides whether to set or reset a storage element. By default, choosing SRLOW also selects INIT0; choosing SRHIGH also selects INIT1.	Independent for each storage element, except when using FDDR. In the latter case, selecting INIT0 for one element applies to both elements (even though INIT1 is selected for the other).

Double-Data-Rate Transmission

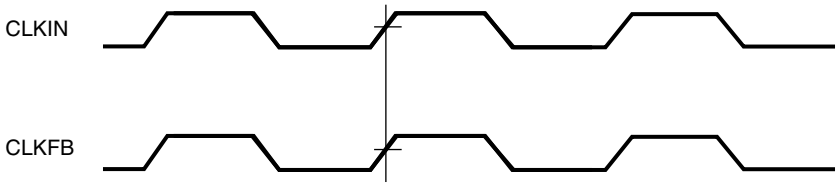
Double-Data-Rate (DDR) transmission describes the technique of synchronizing signals to both the rising and falling edges of the clock signal. Spartan-3 devices use register-pairs in all three IOB paths to perform DDR operations.

The pair of storage elements on the IOB’s Output path (OFF1 and OFF2), used as registers, combine with a special multiplexer to form a DDR D-type flip-flop (FDDR). This primitive permits DDR transmission where output data bits are synchronized to both the rising and falling edges of a clock. It is possible to access this function by placing either an FDDRRSE or an FDDRCPE component or symbol into the design. DDR operation requires two clock signals (50% duty cycle), one the inverted form of the other. These signals trigger the two registers in alternating fashion, as shown in Figure 8. Commonly, the Digital Clock Manager (DCM) generates the two clock signals by mirroring an incoming signal, then shifting it 180 degrees. This approach ensures minimal skew between the two signals.

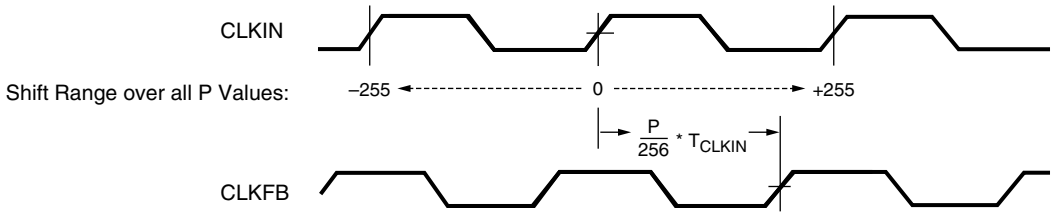
The storage-element-pair on the Three-State path (TFF1 and TFF2) can also be combined with a local multiplexer to form an FDDR primitive. This permits synchronizing the output enable to both the rising and falling edges of a clock. This DDR operation is realized in the same way as for the output path.

The storage-element-pair on the input path (IFF1 and IFF2) allows an I/O to receive a DDR signal. An incoming DDR clock signal triggers one register and the inverted clock signal triggers the other register. In this way, the registers take turns capturing bits of the incoming DDR data signal.

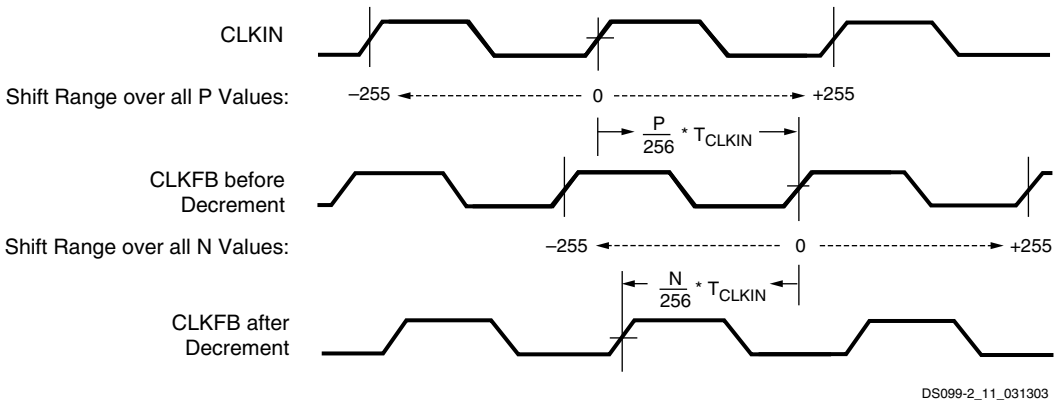
a. CLKOUT_PHASE_SHIFT = NONE



b. CLKOUT_PHASE_SHIFT = FIXED



c. CLKOUT_PHASE_SHIFT = VARIABLE



Notes:

1. P represents the integer value ranging from –255 to +255 to which the PHASE_SHIFT attribute is assigned.
2. N is an integer value ranging from –255 to +255 that represents the net phase shift effect from a series of increment and/or decrement operations.
   N = {Total number of increments} – {Total number of decrements}
   A positive value for N indicates a net increment; a negative value indicates a net decrement.

Figure 23: **Phase Shifter Waveforms**

The Status Logic Component

The Status Logic component not only reports on the state of the DCM but also provides a means of resetting the DCM to an initial known state. The signals associated with the Status Logic component are described in Table 22.

As a rule, the Reset (RST) input is asserted only upon configuring the device or changing the CLKIN frequency. A DCM reset does not affect attribute values (e.g., CLKFX_MULTIPLY and CLKFX_DIVIDE). If not used, RST must be tied to GND.

The eight bits of the STATUS bus are defined in Table 23.

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

- **Advance:** Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur. Use as estimates, not for production.
- **Preliminary:** Based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reported delays is greatly reduced compared to Advance data. Use as estimates, not for production.
- **Production:** These specifications are approved only after silicon has been characterized over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Parameter values are considered stable with no future changes expected.

  Production-quality systems must only use FPGA designs compiled with a Production status speed file. FPGA designs using a less mature speed file designation should only be used during system prototyping or preproduction qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **The following applies unless otherwise noted: The parameter values published in this module apply to all Spartan®-3 devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.** All parameters representing voltages are measured with respect to GND.

Mask and Fab Revisions

Some specifications list different values for one or more mask or fab revisions, indicated by the device top marking (see Package Marking, page 5). The revision differences involve the power ramp rates, differential DC specifications, and DCM characteristics. The most recent revision (mask rev E and GQ fab/geometry code) is errata-free with improved specifications than earlier revisions.

Mask rev E with fab rev GQ has been shipping since 2005 (see XCN05009) and has been 100% of Xilinx Spartan-3 device shipments since 2006. SCD 0974 was provided to ensure the receipt of the rev E silicon, but it is no longer needed. Parts ordered under the SCD appended “0974” to the standard part number. For example, “XC3S50-4VQ100C” became “XC3S50-4VQ100C0974”.

Table 28: **Absolute Maximum Ratings**

Symbol	Description	Conditions		Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND			–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage relative to GND			–0.5	3.00	V
V_{CCO}	Output driver supply voltage relative to GND			–0.5	3.75	V
V_{REF}	Input reference voltage relative to GND			–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND(2,4)	Driver in a high-impedance state	Commercial	–0.95	4.4	V
			Industrial	–0.85	4.3	
	Voltage applied to all Dedicated pins relative to GND(3)		All temp. ranges	–0.5	V_{CCAUX} + 0.5	V

Table 28: **Absolute Maximum Ratings *(Cont'd)***

Symbol	Description	Conditions	Min	Max	Units
I_{IK}	Input clamp current per I/O pin	–0.5 V < V_{IN} < (V_{CCO} + 0.5 V)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage pins relative to GND	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{SOL}	Soldering temperature(4)		–	220	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. All User I/O and Dual-Purpose pins (DIN/D0, D1–D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B) draw power from the V_{CCO} power rail of the associated bank. Keeping VIN within 500 mV of the associated V_{CCO} rails or ground rail ensures that the internal diode junctions that exist between each of these pins and the V_{CCO} and GND rails do not turn on. Table 32 specifies the V_{CCO} range used to determine the max limit. Input voltages outside the –0.5V to V_{CCO}+0.5V voltage range are permissible provided that the I_{IK} input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Prolonged exposure to such current may compromise device reliability. A sustained current of 10 mA will not compromise device reliability. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Generation FPGAs* for more details. The VIN limits apply to both the DC and AC components of signals. Simple application solutions are available that show how to handle overshoot/undershoot as well as achieve PCI compliance. Refer to the following application notes: XAPP457, *Powering and Configuring Spartan-3 Generation FPGAs in Compliant PCI Applications* and XAPP659, *Virtex®-II Pro / Virtex-II Pro X 3.3V I/O Design Guidelines*.
3. All Dedicated pins (M0–M2, CCLK, PROG_B, DONE, HSWAP_EN, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} rail do not turn on. Table 32 specifies the V_{CCAUX} range used to determine the max limit. When V_{CCAUX} is at its maximum recommended operating level (2.625V), V_{IN} max < 3.125V. As long as the V_{IN} max specification is met, oxide stress is not possible. For information concerning the use of 3.3V signals, see the 3.3V-Tolerant Configuration Interface, page 47. See also XAPP459.
4. For soldering guidelines, see UG112, *Device Packaging and Thermal Characteristics* and XAPP427, *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Table 29: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO4T}	Threshold for the V_{CCO} Bank 4 supply	0.4	1.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order. When applying V_{CCINT} power before V_{CCAUX} power, the FPGA may draw a *surplus* current in addition to the quiescent current levels specified in Table 34. Applying V_{CCAUX} eliminates the surplus current. The FPGA does not use any of the surplus current for the power-on process. For this power sequence, make sure that regulators with foldback features will not shut down inadvertently.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 4, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.
3. If a brown-out condition occurs where V_{CCAUX} or V_{CCINT} drops below the retention voltage indicated in Table 31, then V_{CCAUX} or V_{CCINT} must drop below the minimum power-on reset voltage in order to clear out the device configuration content.

Table 42: **Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Hold Times						
T_{IOICKP}	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(3), IOBDELAY = NONE	XC3S50	-0.55	-0.55	ns
			XC3S200	-0.29	-0.29	ns
			XC3S400	-0.29	-0.29	ns
			XC3S1000	-0.55	-0.55	ns
			XC3S1500	-0.55	-0.55	ns
			XC3S2000	-0.55	-0.55	ns
			XC3S4000	-0.61	-0.61	ns
			XC3S5000	-0.68	-0.68	ns
$T_{IOICKPD}$	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(3), IOBDELAY = IFD	XC3S50	-2.74	-2.74	ns
			XC3S200	-3.00	-3.00	ns
			XC3S400	-2.90	-2.90	ns
			XC3S1000	-3.24	-3.24	ns
			XC3S1500	-3.55	-3.55	ns
			XC3S2000	-4.57	-4.57	ns
			XC3S4000	-4.96	-4.96	ns
			XC3S5000	-5.09	-5.09	ns
Set/Reset Pulse Width						
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB		All	0.66	0.76	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 44.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 44. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS33	Slow	2 mA	6.38	7.34	ns
		4 mA	4.83	5.55	ns
		6 mA	4.01	4.61	ns
		8 mA	3.92	4.51	ns
		12 mA	2.91	3.35	ns
		16 mA	2.81	3.23	ns
		24 mA	2.49	2.86	ns
	Fast	2 mA	3.86	4.44	ns
		4 mA	1.87	2.15	ns
		6 mA	0.62	0.71	ns
		8 mA	0.61	0.70	ns
		12 mA	0.16	0.19	ns
		16 mA	0.14	0.16	ns
		24 mA	0.06	0.07	ns
LVDCI_33			0.28	0.32	ns
LVDCI_DV2_33			0.26	0.30	ns
LVTTL	Slow	2 mA	7.27	8.36	ns
		4 mA	4.94	5.69	ns
		6 mA	3.98	4.58	ns
		8 mA	3.98	4.58	ns
		12 mA	2.97	3.42	ns
		16 mA	2.84	3.26	ns
		24 mA	2.65	3.04	ns
	Fast	2 mA	4.32	4.97	ns
		4 mA	1.87	2.15	ns
		6 mA	1.27	1.47	ns
		8 mA	1.19	1.37	ns
		12 mA	0.42	0.48	ns
		16 mA	0.27	0.32	ns
		24 mA	0.16	0.18	ns

Table 48: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
DIFF_SSTL2_II	-	V_{ICM} – 0.75	V_{ICM} + 0.75	50	1.25	V_{ICM}
DIFF_SSTL2_II_DCI						

Notes:

1. Descriptions of the relevant symbols are as follows:
   VREF – The reference voltage for setting the input switching threshold
   VICM – The common mode input voltage
   VM – Voltage of measurement point on signal transition
   VL – Low-level test voltage at Input pin
   VH – High-level test voltage at Input pin
   RT – Effective termination resistance, which takes on a value of 1MW when no parallel termination is required
   VT – Termination voltage
2. The load capacitance (CL) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Using IBIS Models to Simulate Load Conditions in Application

IBIS Models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 48, V_T, R_T, and V_M. Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF}, is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link.

http://www.xilinx.com/support/download/index.htm

Simulate delays for a given application according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 35. Use parameter values V_T, R_T, and V_M from Table 48. C_{REF} is zero.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase (or decrease) in delay should be added to (or subtracted from) the appropriate Output standard adjustment (Table 47) to yield the worst-case delay of the PCB trace.

Table 70: **Spartan-3 FPGA Pin Definitions**

Pin Name	Direction	Description
I/O: General-purpose I/O pins		
I/O	User-defined as input, output, bidirectional, three-state output, open-drain output, open-source output	**User I/O:** Unrestricted single-ended user-I/O pin. Supports all I/O standards except the differential standards.
I/O_Lxxy_#	User-defined as input, output, bidirectional, three-state output, open-drain output, open-source output	**User I/O, Half of Differential Pair:** Unrestricted single-ended user-I/O pin or half of a differential pair. Supports all I/O standards including the differential standards.
DUAL: Dual-purpose configuration pins		
IO_Lxxy_#/DIN/D0, IO_Lxxy_#/D1, IO_Lxxy_#/D2, IO_Lxxy_#/D3, IO_Lxxy_#/D4, IO_Lxxy_#/D5, IO_Lxxy_#/D6, IO_Lxxy_#/D7	Input during configuration Possible bidirectional I/O after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Configuration Data Port:** In Parallel (SelectMAP) modes, D0-D7 are byte-wide configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained via the Persist bitstream option. In Serial modes, DIN (D0) serves as the single configuration data input. This pin becomes a user I/O after configuration unless retained by the Persist bitstream option.
IO_Lxxy_#/CS_B	Input during Parallel mode configuration Possible input after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Chip Select for Parallel Mode Configuration:** In Parallel (SelectMAP) modes, this is the active-Low Chip Select signal. This pin becomes a user I/O after configuration unless the SelectMAP port is retained via the Persist bitstream option.
IO_Lxxy_#/RDWR_B	Input during Parallel mode configuration Possible input after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Read/Write Control for Parallel Mode Configuration:** In Parallel (SelectMAP) modes, this is the active-Low Write Enable, active-High Read Enable signal. This pin becomes a user I/O after configuration unless the SelectMAP port is retained via the Persist bitstream option.
IO_Lxxy_#/ BUSY/DOUT	Output during configuration Possible output after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Configuration Data Rate Control for Parallel Mode, Serial Data Output for Serial Mode:** In Parallel (SelectMAP) modes, BUSY throttles the rate at which configuration data is loaded. This pin becomes a user I/O after configuration unless the SelectMAP port is retained via the Persist bitstream option. In Serial modes, DOUT provides preamble and configuration data to downstream devices in a multi-FPGA daisy-chain. This pin becomes a user I/O after configuration.
IO_Lxxy_#/INIT_B	Bidirectional (open-drain) during configuration User I/O after configuration	**Initializing Configuration Memory/Detected Configuration Error:** When Low, this pin indicates that configuration memory is being cleared. When held Low, this pin delays the start of configuration. After this pin is released or configuration memory is cleared, the pin goes High. During configuration, a Low on this output indicates that a configuration data error occurred. This pin always has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM during configuration, regardless of the HSWAP_EN pin. This pin becomes a user I/O after configuration.
DCI: Digitally Controlled Impedance reference resistor input pins		
IO_Lxxy_#/VRN_# or IO/VRN_#	Input when using DCI Otherwise, same as I/O	**DCI Reference Resistor for NMOS I/O Transistor (per bank):** If using DCI, a 1% precision impedance-matching resistor is connected between this pin and the VCCO supply for this bank. Otherwise, this pin is a user I/O.
IO_Lxxy_#/VRP_# or IO/VRP_#	Input when using DCI Otherwise, same as I/O	**DCI Reference Resistor for PMOS I/O Transistor (per bank):** If using DCI, a 1% precision impedance-matching resistor is connected between this pin and the ground supply. Otherwise, this pin is a user I/O.

The 1% precision impedance-matching resistor attached to the VRN_# pin controls the pull-down impedance of NMOS transistor in the input or output buffer. Consequently, the VRN_# pin must connect to VCCO. The 'N' character in "VRN" indicates that this pin controls the I/O buffer's NMOS transistor impedance. The VRN_# pin is only used for split termination.

Each VRN or VRP reference input requires its own resistor. A single resistor cannot be shared between VRN or VRP pins associated with different banks.

During configuration, these pins behave exactly like user-I/O pins. The associated DCI behavior is not active or valid until after configuration completes.

Also see Digitally Controlled Impedance (DCI), page 16.

DCI Termination Types

If the I/O in an I/O bank do not use the DCI feature, then no external resistors are required and both the VRP_# and VRN_# pins are available for user I/O, as shown in section [a] of Figure 42.

If the I/O standards within the associated I/O bank require single termination—such as GTL_DCI, GTLP_DCI, or HSTL_III_DCI—then only the VRP_# signal connects to a 1% precision impedance-matching resistor, as shown in section [b] of Figure 42. A resistor is not required for the VRN_# pin.

Finally, if the I/O standards with the associated I/O bank require split termination—such as HSTL_I_DCI, SSTL2_I_DCI, SSTL2_II_DCI, or LVDS_25_DCI and LVDSEXT_25_DCI receivers—then both the VRP_# and VRN_# pins connect to separate 1% precision impedance-matching resistors, as shown in section [c] of Figure 42. Neither pin is available for user I/O.

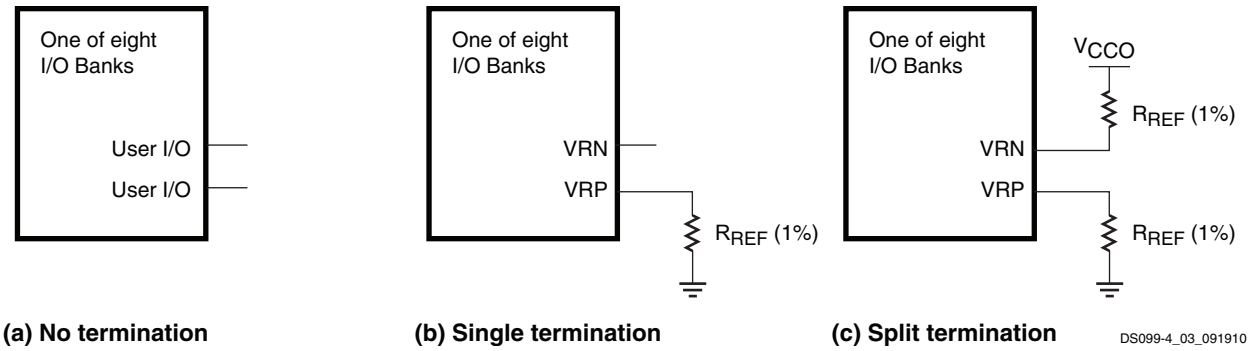


Figure 42: **DCI Termination Types**

GCLK: Global Clock Buffer Inputs or General-Purpose I/O Pins

These pins are user-I/O pins unless they specifically connect to one of the eight low-skew global clock buffers on the device, specified using the IBUFG primitive.

There are eight GCLK pins per device and two each appear in the top-edge banks, Bank 0 and 1, and the bottom-edge banks, Banks 4 and 5. See Figure 40 for a picture of bank labeling.

During configuration, these pins behave exactly like user-I/O pins.

Also see Global Clock Network, page 42.

CONFIG: Dedicated Configuration Pins

The dedicated configuration pins control the configuration process and are not available as user-I/O pins. Every package has seven dedicated configuration pins. All CONFIG-type pins are powered by the +2.5V VCCAUX supply.

Also see Configuration, page 46.

Table 85: **Maximum User I/Os by Package**

Device	Package	Maximum User I/Os	Maximum Differential Pairs	All Possible I/O Pins by Type					N.C.
				I/O	DUAL	DCI	VREF	GCLK	
XC3S50	VQ100	63	29	22	12	14	7	8	0
XC3S200	VQ100	63	29	22	12	14	7	8	0
XC3S50	CP132(1)	89	44	44	12	14	11	8	0
XC3S50	TQ144	97	46	51	12	14	12	8	0
XC3S200	TQ144	97	46	51	12	14	12	8	0
XC3S400	TQ144	97	46	51	12	14	12	8	0
XC3S50	PQ208	124	56	72	12	16	16	8	17
XC3S200	PQ208	141	62	83	12	16	22	8	0
XC3S400	PQ208	141	62	83	12	16	22	8	0
XC3S200	FT256	173	76	113	12	16	24	8	0
XC3S400	FT256	173	76	113	12	16	24	8	0
XC3S1000	FT256	173	76	113	12	16	24	8	0
XC3S400	FG320	221	100	156	12	16	29	8	0
XC3S1000	FG320	221	100	156	12	16	29	8	0
XC3S1500	FG320	221	100	156	12	16	29	8	0
XC3S400	FG456	264	116	196	12	16	32	8	69
XC3S1000	FG456	333	149	261	12	16	36	8	0
XC3S1500	FG456	333	149	261	12	16	36	8	0
XC3S2000	FG456	333	149	261	12	16	36	8	0
XC3S1000	FG676	391	175	315	12	16	40	8	98
XC3S1500	FG676	487	221	403	12	16	48	8	2
XC3S2000	FG676	489	221	405	12	16	48	8	0
XC3S4000	FG676	489	221	405	12	16	48	8	0
XC3S5000	FG676	489	221	405	12	16	48	8	0
XC3S2000	FG900	565	270	481	12	16	48	8	68
XC3S4000	FG900	633	300	549	12	16	48	8	0
XC3S5000	FG900	633	300	549	12	16	48	8	0
XC3S4000	FG1156(1)	712	312	621	12	16	55	8	73
XC3S5000	FG1156(1)	784	344	692	12	16	56	8	1

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Electronic versions of the package pinout tables and footprints are available for download from the Xilinx website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs. Download the files from the following location:

http://www.xilinx.com/support/documentation/data_sheets/s3_pin.zip

FG320: 320-lead Fine-pitch Ball Grid Array

The 320-lead fine-pitch ball grid array package, FG320, supports three different Spartan-3 devices, including the XC3S400, the XC3S1000, and the XC3S1500. The footprint for all three devices is identical, as shown in Table 98 and Figure 50.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

All the package pins appear in Table 98 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 98: **FG320 Package Pinout**

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
0	IO	D9	I/O
0	IO	E7	I/O
0	IO/VREF_0	B3	VREF
0	IO/VREF_0	D6	VREF
0	IO_L01N_0/VRP_0	A2	DCI
0	IO_L01P_0/VRN_0	A3	DCI
0	IO_L09N_0	B4	I/O
0	IO_L09P_0	C4	I/O
0	IO_L10N_0	C5	I/O
0	IO_L10P_0	D5	I/O
0	IO_L15N_0	A4	I/O
0	IO_L15P_0	A5	I/O
0	IO_L25N_0	B5	I/O
0	IO_L25P_0	B6	I/O
0	IO_L27N_0	C7	I/O
0	IO_L27P_0	D7	I/O
0	IO_L28N_0	C8	I/O
0	IO_L28P_0	D8	I/O
0	IO_L29N_0	E8	I/O
0	IO_L29P_0	F8	I/O
0	IO_L30N_0	A7	I/O
0	IO_L30P_0	A8	I/O
0	IO_L31N_0	B9	I/O
0	IO_L31P_0/VREF_0	A9	VREF
0	IO_L32N_0/GCLK7	E9	GCLK
0	IO_L32P_0/GCLK6	F9	GCLK
0	VCCO_0	B8	VCCO
0	VCCO_0	C6	VCCO
0	VCCO_0	G8	VCCO

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
2	IO_L20N_2	E17	I/O
2	IO_L20P_2	E18	I/O
2	IO_L21N_2	F15	I/O
2	IO_L21P_2	E15	I/O
2	IO_L22N_2	F14	I/O
2	IO_L22P_2	G14	I/O
2	IO_L23N_2/VREF_2	G18	VREF
2	IO_L23P_2	F17	I/O
2	IO_L24N_2	G15	I/O
2	IO_L24P_2	G16	I/O
2	IO_L27N_2	H13	I/O
2	IO_L27P_2	H14	I/O
2	IO_L34N_2/VREF_2	H16	VREF
2	IO_L34P_2	H15	I/O
2	IO_L35N_2	H17	I/O
2	IO_L35P_2	H18	I/O
2	IO_L39N_2	J18	I/O
2	IO_L39P_2	J17	I/O
2	IO_L40N_2	J15	I/O
2	IO_L40P_2/VREF_2	J14	VREF
2	VCCO_2	F16	VCCO
2	VCCO_2	H12	VCCO
2	VCCO_2	J12	VCCO
3	IO	K15	I/O
3	IO_L01N_3/VRP_3	T17	DCI
3	IO_L01P_3/VRN_3	T16	DCI
3	IO_L16N_3	T18	I/O
3	IO_L16P_3	U18	I/O
3	IO_L17N_3	P16	I/O
3	IO_L17P_3/VREF_3	R16	VREF
3	IO_L19N_3	R17	I/O
3	IO_L19P_3	R18	I/O
3	IO_L20N_3	P18	I/O
3	IO_L20P_3	P17	I/O
3	IO_L21N_3	P15	I/O
3	IO_L21P_3	N15	I/O
3	IO_L22N_3	M14	I/O
3	IO_L22P_3	N14	I/O
3	IO_L23N_3	M15	I/O
3	IO_L23P_3/VREF_3	M16	VREF

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
2	IO_L21P_2	IO_L21P_2	E22	I/O
2	IO_L22N_2	IO_L22N_2	G17	I/O
2	IO_L22P_2	IO_L22P_2	G18	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	F19	VREF
2	IO_L23P_2	IO_L23P_2	G19	I/O
2	IO_L24N_2	IO_L24N_2	F20	I/O
2	IO_L24P_2	IO_L24P_2	F21	I/O
2	N.C. (◆)	IO_L26N_2	G20	I/O
2	N.C. (◆)	IO_L26P_2	H19	I/O
2	IO_L27N_2	IO_L27N_2	G21	I/O
2	IO_L27P_2	IO_L27P_2	G22	I/O
2	N.C. (◆)	IO_L28N_2	H18	I/O
2	N.C. (◆)	IO_L28P_2	J17	I/O
2	N.C. (◆)	IO_L29N_2	H21	I/O
2	N.C. (◆)	IO_L29P_2	H22	I/O
2	N.C. (◆)	IO_L31N_2	J18	I/O
2	N.C. (◆)	IO_L31P_2	J19	I/O
2	N.C. (◆)	IO_L32N_2	J21	I/O
2	N.C. (◆)	IO_L32P_2	J22	I/O
2	N.C. (◆)	IO_L33N_2	K17	I/O
2	N.C. (◆)	IO_L33P_2	K18	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	K19	VREF
2	IO_L34P_2	IO_L34P_2	K20	I/O
2	IO_L35N_2	IO_L35N_2	K21	I/O
2	IO_L35P_2	IO_L35P_2	K22	I/O
2	IO_L38N_2	IO_L38N_2	L17	I/O
2	IO_L38P_2	IO_L38P_2	L18	I/O
2	IO_L39N_2	IO_L39N_2	L19	I/O
2	IO_L39P_2	IO_L39P_2	L20	I/O
2	IO_L40N_2	IO_L40N_2	L21	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	L22	VREF
2	VCCO_2	VCCO_2	H17	VCCO
2	VCCO_2	VCCO_2	H20	VCCO
2	VCCO_2	VCCO_2	J16	VCCO
2	VCCO_2	VCCO_2	K16	VCCO
2	VCCO_2	VCCO_2	L16	VCCO
3	IO	IO	Y21	I/O
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	Y20	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	Y19	DCI
3	IO_L16N_3	IO_L16N_3	W22	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
6	IO_L20N_6	IO_L20N_6	IO_L20N_6	IO_L20N_6	IO_L20N_6	V7	I/O
6	IO_L20P_6	IO_L20P_6	IO_L20P_6	IO_L20P_6	IO_L20P_6	U7	I/O
6	IO_L21N_6	IO_L21N_6	IO_L21N_6	IO_L21N_6	IO_L21N_6	V5	I/O
6	IO_L21P_6	IO_L21P_6	IO_L21P_6	IO_L21P_6	IO_L21P_6	V4	I/O
6	IO_L22N_6	IO_L22N_6	IO_L22N_6	IO_L22N_6	IO_L22N_6	V3	I/O
6	IO_L22P_6	IO_L22P_6	IO_L22P_6	IO_L22P_6	IO_L22P_6	V2	I/O
6	IO_L23N_6	IO_L23N_6	IO_L23N_6	IO_L23N_6	IO_L23N_6	U6	I/O
6	IO_L23P_6	IO_L23P_6	IO_L23P_6	IO_L23P_6	IO_L23P_6	U5	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	U4	VREF
6	IO_L24P_6	IO_L24P_6	IO_L24P_6	IO_L24P_6	IO_L24P_6	U3	I/O
6	IO_L26N_6	IO_L26N_6	IO_L26N_6	IO_L26N_6	IO_L26N_6	U2	I/O
6	IO_L26P_6	IO_L26P_6	IO_L26P_6	IO_L26P_6	IO_L26P_6	U1	I/O
6	IO_L27N_6	IO_L27N_6	IO_L27N_6	IO_L27N_6	IO_L27N_6	T8	I/O
6	IO_L27P_6	IO_L27P_6	IO_L27P_6	IO_L27P_6	IO_L27P_6	T7	I/O
6	IO_L28N_6	IO_L28N_6	IO_L28N_6	IO_L28N_6	IO_L28N_6	T6	I/O
6	IO_L28P_6	IO_L28P_6	IO_L28P_6	IO_L28P_6	IO_L28P_6	T5	I/O
6	IO_L29N_6	IO_L29N_6	IO_L29N_6	IO_L29N_6	IO_L29N_6	T2	I/O
6	IO_L29P_6	IO_L29P_6	IO_L29P_6	IO_L29P_6	IO_L29P_6	T1	I/O
6	IO_L31N_6	IO_L31N_6	IO_L31N_6	IO_L31N_6	IO_L31N_6	R8	I/O
6	IO_L31P_6	IO_L31P_6	IO_L31P_6	IO_L31P_6	IO_L31P_6	R7	I/O
6	IO_L32N_6	IO_L32N_6	IO_L32N_6	IO_L32N_6	IO_L32N_6	R6	I/O
6	IO_L32P_6	IO_L32P_6	IO_L32P_6	IO_L32P_6	IO_L32P_6	R5	I/O
6	IO_L33N_6	IO_L33N_6	IO_L33N_6	IO_L33N_6	IO_L33N_6	T4	I/O
6	IO_L33P_6	IO_L33P_6	IO_L33P_6	IO_L33P_6	IO_L33P_6	R3	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	R2	VREF
6	IO_L34P_6	IO_L34P_6	IO_L34P_6	IO_L34P_6	IO_L34P_6	R1	I/O
6	IO_L35N_6	IO_L35N_6	IO_L35N_6	IO_L35N_6	IO_L35N_6	P8	I/O
6	IO_L35P_6	IO_L35P_6	IO_L35P_6	IO_L35P_6	IO_L35P_6	P7	I/O
6	IO_L38N_6	IO_L38N_6	IO_L38N_6	IO_L38N_6	IO_L38N_6	P6	I/O
6	IO_L38P_6	IO_L38P_6	IO_L38P_6	IO_L38P_6	IO_L38P_6	P5	I/O
6	IO_L39N_6	IO_L39N_6	IO_L39N_6	IO_L39N_6	IO_L39N_6	P4	I/O
6	IO_L39P_6	IO_L39P_6	IO_L39P_6	IO_L39P_6	IO_L39P_6	P3	I/O
6	IO_L40N_6	IO_L40N_6	IO_L40N_6	IO_L40N_6	IO_L40N_6	P2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	P1	VREF
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	P9	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	P10	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	R9	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	T3	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	T9	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	U8	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	V8	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	Y3	VCCO
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	F5	DCI

User I/Os by Bank

Table 104 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1000 in the FG676 package. Similarly, Table 105 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1500 in the FG676 package. Finally, Table 106 shows the same information for the XC3S2000, XC3S4000, and XC3S5000 in the FG676 package.

Table 104: **User I/Os Per Bank for XC3S1000 in FG676 Package**

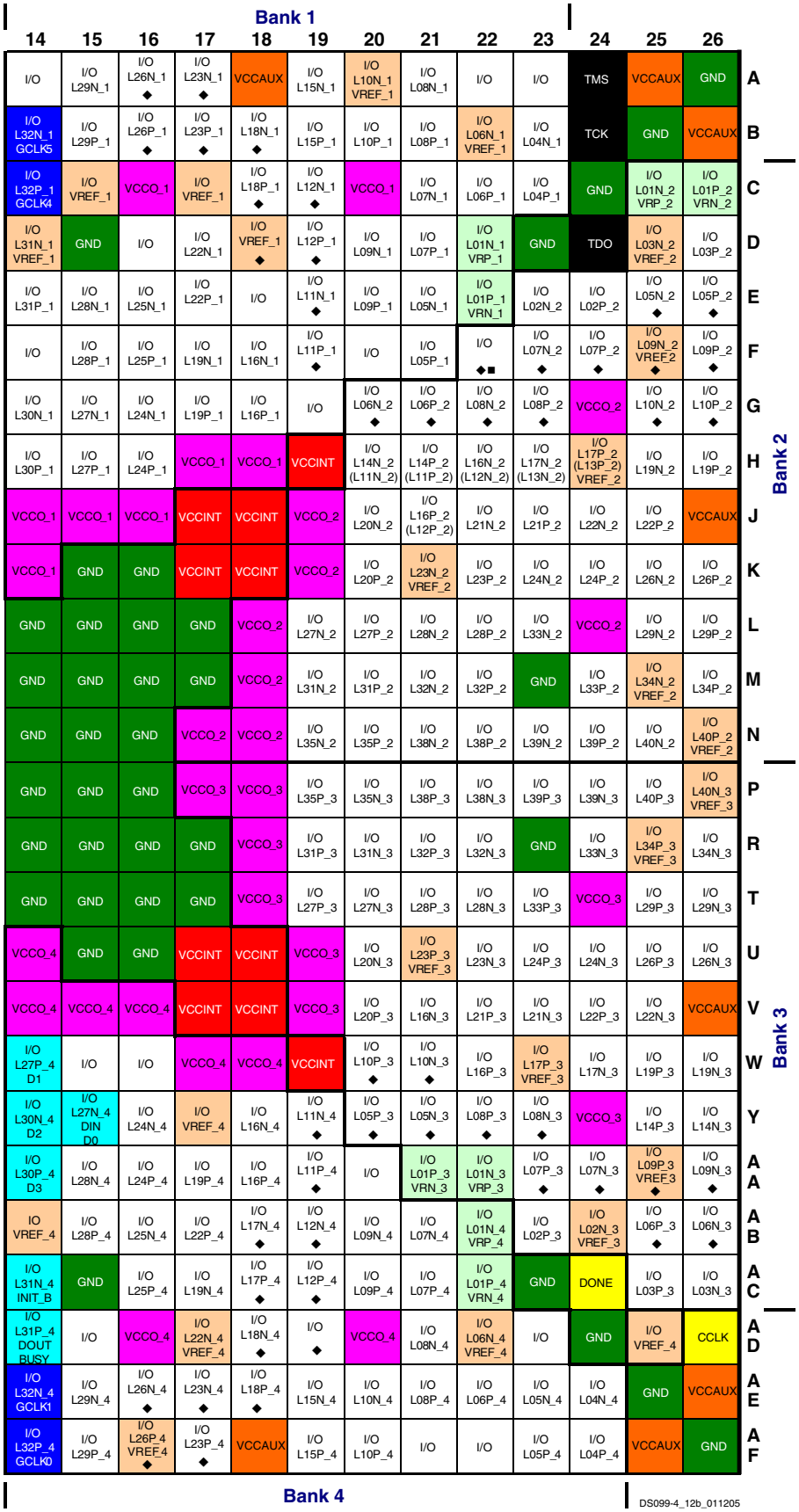
Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	49	40	0	2	5	2
	1	50	41	0	2	5	2
Right	2	48	41	0	2	5	0
	3	48	41	0	2	5	0
Bottom	4	50	35	6	2	5	2
	5	50	35	6	2	5	2
Left	6	48	41	0	2	5	0
	7	48	41	0	2	5	0

Table 105: **User I/Os Per Bank for XC3S1500 in FG676 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	62	52	0	2	6	2
	1	61	51	0	2	6	2
Right	2	60	52	0	2	6	0
	3	60	52	0	2	6	0
Bottom	4	63	47	6	2	6	2
	5	61	45	6	2	6	2
Left	6	60	52	0	2	6	0
	7	60	52	0	2	6	0

Table 106: **User I/Os Per Bank for XC3S2000, XC3S4000, and XC3S5000 in FG676 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	62	52	0	2	6	2
	1	61	51	0	2	6	2
Right	2	61	53	0	2	6	0
	3	60	52	0	2	6	0
Bottom	4	63	47	6	2	6	2
	5	61	45	6	2	6	2
Left	6	61	53	0	2	6	0
	7	60	52	0	2	6	0



Right Half of Package (Top View)

Notes:

1. Differential pair assignments shown in parentheses on balls H20, H21, H22, H23, H24, and J21 are for XC3S4000 only.
2. Differential pair assignments for the XC3S5000 are different on 15 balls (see Table 103 for details.)

Figure 54: FG676 Package Footprint (Top View) Continued

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
5	VCCO_5	VCCO_5	AJ13	VCCO
5	VCCO_5	VCCO_5	AL11	VCCO
5	VCCO_5	VCCO_5	AL16	VCCO
5	VCCO_5	VCCO_5	AM4	VCCO
5	VCCO_5	VCCO_5	AM8	VCCO
5	VCCO_5	VCCO_5	AN13	VCCO
6	IO	IO	AH1	I/O
6	IO	IO	AH2	I/O
6	IO	IO	V9	I/O
6	IO	IO	V10	I/O
6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	AM2	DCI
6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	AM1	DCI
6	IO_L02N_6	IO_L02N_6	AL2	I/O
6	IO_L02P_6	IO_L02P_6	AL1	I/O
6	IO_L03N_6/VREF_6	IO_L03N_6/VREF_6	AK3	VREF
6	IO_L03P_6	IO_L03P_6	AK2	I/O
6	IO_L04N_6	IO_L04N_6	AJ4	I/O
6	IO_L04P_6	IO_L04P_6	AJ3	I/O
6	IO_L05N_6	IO_L05N_6	AJ2	I/O
6	IO_L05P_6	IO_L05P_6	AJ1	I/O
6	IO_L06N_6	IO_L06N_6	AH6	I/O
6	IO_L06P_6	IO_L06P_6	AH5	I/O
6	IO_L07N_6	IO_L07N_6	AG6	I/O
6	IO_L07P_6	IO_L07P_6	AG5	I/O
6	IO_L08N_6	IO_L08N_6	AG2	I/O
6	IO_L08P_6	IO_L08P_6	AG1	I/O
6	IO_L09N_6/VREF_6	IO_L09N_6/VREF_6	AF7	VREF
6	IO_L09P_6	IO_L09P_6	AF6	I/O
6	IO_L10N_6	IO_L10N_6	AG4	I/O
6	IO_L10P_6	IO_L10P_6	AF4	I/O
6	IO_L11N_6	IO_L11N_6	AF3	I/O
6	IO_L11P_6	IO_L11P_6	AF2	I/O
6	IO_L12N_6	IO_L12N_6	AF8	I/O
6	IO_L12P_6	IO_L12P_6	AE9	I/O
6	IO_L13N_6	IO_L13N_6	AE8	I/O
6	IO_L13P_6/VREF_6	IO_L13P_6/VREF_6	AE7	VREF
6	IO_L14N_6	IO_L14N_6	AE6	I/O
6	IO_L14P_6	IO_L14P_6	AE5	I/O
6	IO_L15N_6	IO_L15N_6	AE4	I/O
6	IO_L15P_6	IO_L15P_6	AE3	I/O

User I/Os by Bank

Note: The FG(G)1156 package is discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Table 111 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S4000 in the FG1156 package. Similarly, Table 112 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S5000 in the FG1156 package.

Table 111: **User I/Os Per Bank for XC3S4000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	90	79	0	2	7	2
	1	90	79	0	2	7	2
Right	2	88	80	0	2	6	0
	3	88	79	0	2	7	0
Bottom	4	90	73	6	2	7	2
	5	90	73	6	2	7	2
Left	6	88	79	0	2	7	0
	7	88	79	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

Table 112: **User I/Os Per Bank for XC3S5000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	100	89	0	2	7	2
	1	100	89	0	2	7	2
Right	2	96	87	0	2	7	0
	3	96	87	0	2	7	0
Bottom	4	100	83	6	2	7	2
	5	100	83	6	2	7	2
Left	6	96	87	0	2	7	0
	7	96	87	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

Revision History

Date	Version	Description
04/03/03	1.0	Initial Xilinx release.
04/21/03	1.1	Added information on the VQ100 package footprint, including a complete pinout table (Table 87) and footprint diagram (Figure 44). Updated Table 85 with final I/O counts for the VQ100 package. Also added final differential I/O pair counts for the TQ144 package. Added clarifying comments to HSWAP_EN pin description on page 119. Updated the footprint diagram for the FG900 package shown in Figure 55a and Figure 55b. Some thick lines separating I/O banks were incorrect. Made cosmetic changes to Figure 40, Figure 42, and Figure 43. Updated Xilinx hypertext links. Added XC3S200 and XC3S400 to Pin Name column in Table 91.
05/12/03	1.1.1	AM32 pin was missing GND label in FG1156 package diagram (Figure 53).
07/11/03	1.1.2	Corrected misspellings of GCLK in Table 69 and Table 70. Changed CMOS25 to LVCMOS25 in Dual-Purpose Pin I/O Standard During Configuration section. Clarified references to Module 2. For XC3S5000 in FG1156 package, corrected N.C. symbol to a black square in Table 110, key, and package drawing.
07/29/03	1.2	Corrected pin names on FG1156 package. Some package balls incorrectly included LVDS pair names. The affected balls on the FG1156 package include G1, G2, G33, G34, U9, U10, U25, U26, V9, V10, V25, V26, AH1, AH2, AH33, AH34. The number of LVDS pairs is unaffected. Modified affected balls and re-sorted rows in Table 110. Updated affected balls in Figure 53. Also updated ASCII and Excel electronic versions of FG1156 pinout.
08/19/03	1.2.1	Removed 100 MHz ConfigRate option in CCLK: Configuration Clock section and in Table 80. Added note that TDO is a totem-pole output in Table 77.
10/09/03	1.2.2	Some pins had incorrect bank designations and were improperly sorted in Table 93. No pin names or functions changed. Renamed DCI_IN to DCI and added black diamond to N.C. pins in Table 93. In Figure 47, removed some extraneous text from pin 106 and corrected spelling of pins 45, 48, and 81.
12/17/03	1.3	Added FG320 pin tables and pinout diagram (FG320: 320-lead Fine-pitch Ball Grid Array). Made cosmetic changes to the TQ144 footprint (Figure 46), the PQ208 footprint (Figure 47), the FG676 footprint (Figure 53), and the FG900 footprint (Figure 55). Clarified wording in Precautions When Using the JTAG Port in 3.3V Environments section.
02/27/04	1.4	Clarified wording in Using JTAG Port After Configuration section. In Table 81, reduced package height for FG320 and increased maximum I/O values for the FG676, FG900, and FG1156 packages.
07/13/04	1.5	Added information on lead-free (Pb-free) package options to the Package Overview section plus Table 81 and Table 83. Clarified the VRN_# reference resistor requirements for I/O standards that use single termination as described in the DCI Termination Types section and in Figure 42b. Graduated from Advance Product Specification to Product Specification.
08/24/04	1.5.1	Removed XC3S2000 references from FG1156: 1156-lead Fine-pitch Ball Grid Array.
01/17/05	1.6	Added XC3S50 in CP132 package option. Added XC3S2000 in FG456 package option. Added XC3S4000 in FG676 package option. Added Selecting the Right Package Option section. Modified or added Table 81, Table 83, Table 84, Table 85, Table 89, Table 90, Table 100, Table 102, Table 103, Table 106, Figure 45, and Figure 53.
08/19/05	1.7	Removed term “weak” from the description of pull-up and pull-down resistors. Added IDCODE Register values. Added signal integrity precautions to CCLK: Configuration Clock and indicated that CCLK should be treated as an I/O during Master mode in Table 79.
04/03/06	2.0	Added Package Thermal Characteristics. Updated Figure 41 to make it a more obvious example. Added detail about which pins have dedicated pull-up resistors during configuration, regardless of the HSWAP_EN value to Table 70 and to Pin Behavior During Configuration. Updated Precautions When Using the JTAG Port in 3.3V Environments.
04/26/06	2.1	Corrected swapped data row in Table 86. The Theta-JA with zero airflow column was swapped with the Theta-JC column. Made additional notations on CONFIG and JTAG pins that have pull-up resistors during configuration, regardless of the HSWAP_EN input.
05/25/07	2.2	Added link on page 128 to Material Declaration Data Sheets. Corrected units typo in Table 74. Added Note 1 to Table 103 about VREF for XC3S1500 in FG676.