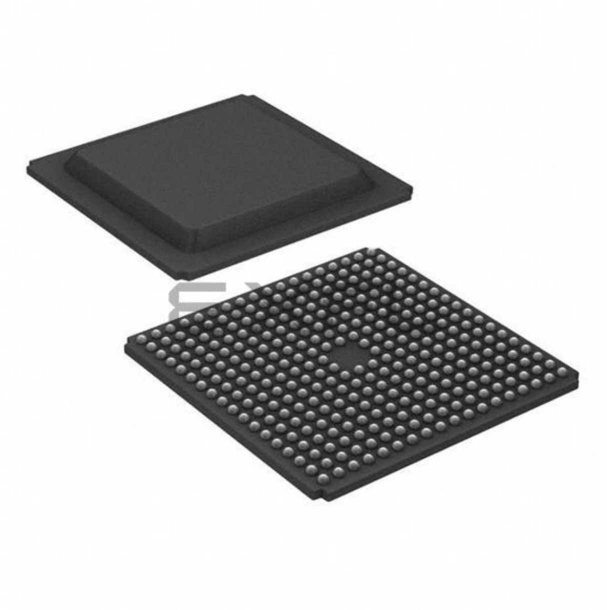
AMD Xilinx - XC3S1000-4FG320I Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1920
Number of Logic Elements/Cells	17280
Total RAM Bits	442368
Number of I/O	221
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1000-4fg320i

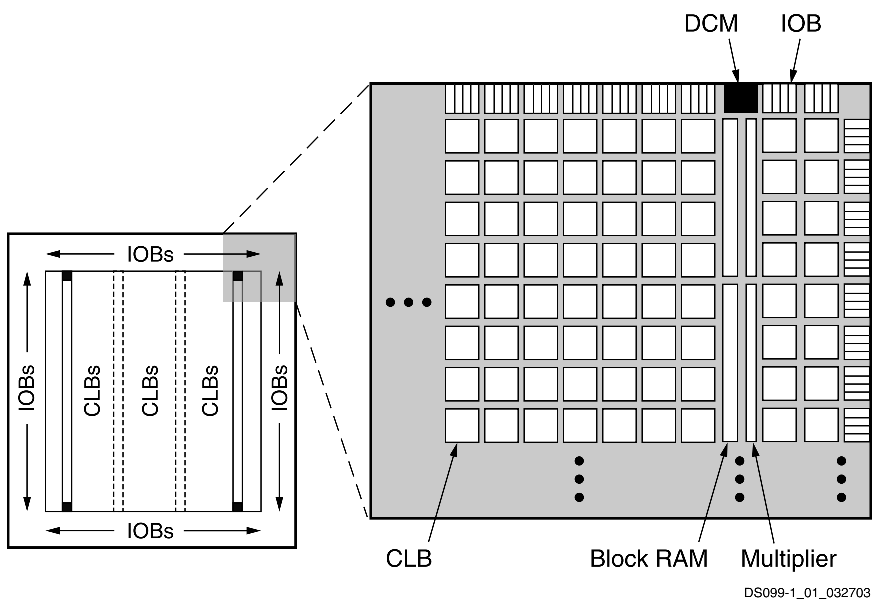
Architectural Overview

The Spartan-3 family architecture consists of five fundamental programmable functional elements:

- Configurable Logic Blocks (CLBs) contain RAM-based Look-Up Tables (LUTs) to implement logic and storage elements that can be used as flip-flops or latches. CLBs can be programmed to perform a wide variety of logical functions as well as to store data.
- Input/Output Blocks (IOBs) control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Twenty-six different signal standards, including eight high-performance differential standards, are available as shown in Table 2. Double Data-Rate (DDR) registers are included. The Digitally Controlled Impedance (DCI) feature provides automatic on-chip terminations, simplifying board designs.
- Block RAM provides data storage in the form of 18-Kbit dual-port blocks.
- Multiplier blocks accept two 18-bit binary numbers as inputs and calculate the product.
- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. The XC3S50 has a single column of block RAM embedded in the array. Those devices ranging from the XC3S200 to the XC3S2000 have two columns of block RAM. The XC3S4000 and XC3S5000 devices have four RAM columns. Each column is made up of several 18-Kbit RAM blocks; each block is associated with a dedicated multiplier. The DCMs are positioned at the ends of the outer block RAM columns.

The Spartan-3 family features a rich network of traces and switches that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The two additional block RAM columns of the XC3S4000 and XC3S5000 devices are shown with dashed lines. The XC3S50 has only the block RAM column on the far left.

Figure 1: **Spartan-3 Family Architecture**

Configuration

Spartan-3 FPGAs are programmed by loading configuration data into robust reprogrammable static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. Before powering on the FPGA, configuration data is stored externally in a PROM or some other nonvolatile medium either on or off the board. After applying

Table 13: **Block RAM Port Signals *(Cont'd)***

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Data Output Bus	DOA	DOB	Output	Basic data access occurs whenever WE is inactive. The DO outputs mirror the data stored in the addressed memory location. Data access with WE asserted is also possible if one of the following two attributes is chosen: WRITE_FIRST and READ_FIRST. WRITE_FIRST simultaneously presents the new input data on the DO output port and writes the data to the address RAM location. READ_FIRST presents the previously stored RAM data on the DO output port while writing new data to RAM. A third attribute, NO_CHANGE, latches the DO outputs upon the assertion of WE. It is possible to configure a port's total data path width (w) to be 1, 2, 4, 9, 18, or 36 bits. This selection applies to both the DI and DO paths. See the DI signal description.
Parity Data Output(s)	DOPA	DOPB	Output	Parity inputs represent additional bits included in the data input path to support error detection. The number of parity bits "p" included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 14.
Write Enable	WEA	WEB	Input	When asserted together with EN, this input enables the writing of data to the RAM. In this case, the data access attributes WRITE_FIRST, READ_FIRST or NO_CHANGE determines if and how data is updated on the DO outputs. See the DO signal description. When WE is inactive with EN asserted, read operations are still possible. In this case, a transparent latch passes data from the addressed memory location to the DO outputs.
Clock Enable	ENA	ENB	Input	When asserted, this input enables the CLK signal to synchronize Block RAM functions as follows: the writing of data to the DI inputs (when WE is also asserted), the updating of data at the DO outputs as well as the setting/resetting of the DO output latches. When de-asserted, the above functions are disabled.
Set/Reset	SSRA	SSRB	Input	When asserted, this pin forces the DO output latch to the value that the SRVAL attribute is set to. A Set/Reset operation on one port has no effect on the other ports functioning, nor does it disturb the memory's data contents. It is synchronized to the CLK signal.
Clock	CLKA	CLKB	Input	This input accepts the clock signal to which read and write operations are synchronized. All associated port inputs are required to meet setup times with respect to the clock signal's active edge. The data output bus responds after a clock-to-out delay referenced to the clock signal's active edge.

Port Aspect Ratios

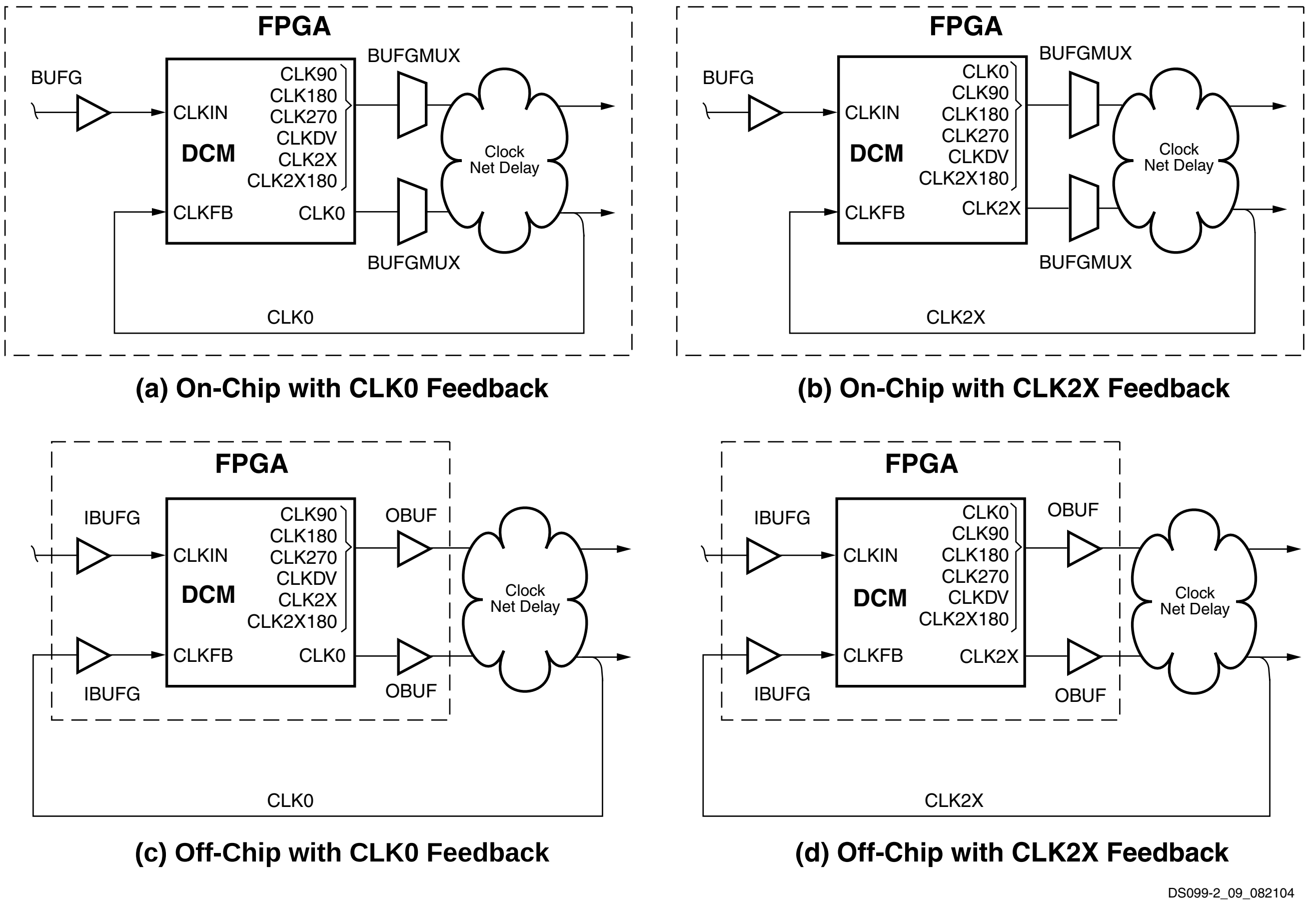
On a given port, it is possible to select a number of different possible widths ($w - p$) for the DI/DO buses as shown in Table 14. These two buses always have the same width. This data bus width selection is independent for each port. If the data bus width of Port A differs from that of Port B, the Block RAM automatically performs a bus-matching function. When data are written to a port with a narrow bus, then read from a port with a wide bus, the latter port will effectively combine "narrow" words to form "wide" words. Similarly, when data are written into a port with a wide bus, then read from a port with a narrow bus, the latter port will divide "wide" words to form "narrow" words. When the data bus width is eight bits or greater, extra parity bits become available. The width of the total data path (w) is the sum of the DI/DO bus width and any parity bits (p).

The width selection made for the DI/DO bus determines the number of address lines according to the relationship expressed below:

$$r = 14 - [\log(w-p)/\log(2)] \quad \textit{Equation 1}$$

In turn, the number of address lines delimits the total number (n) of addressable locations or depth according to the following equation:

$$n = 2^r \quad \textit{Equation 2}$$



Notes:

1. In the Low Frequency mode, all seven DLL outputs are available. In the High Frequency mode, only the CLK0, CLK180, and CLKDV outputs are available.

Figure 21: **Input Clock, Output Clock, and Feedback Connections for the DLL**

In the on-chip synchronization case (the [a] and [b] sections of Figure 21), it is possible to connect any of the DLL's seven output clock signals through general routing resources to the FPGA's internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. As shown in the [a] section of Figure 21, the feedback loop is created by routing CLK0 (or CLK2X, in the [b] section) to a global clock net, which in turn drives the CLKFB input.

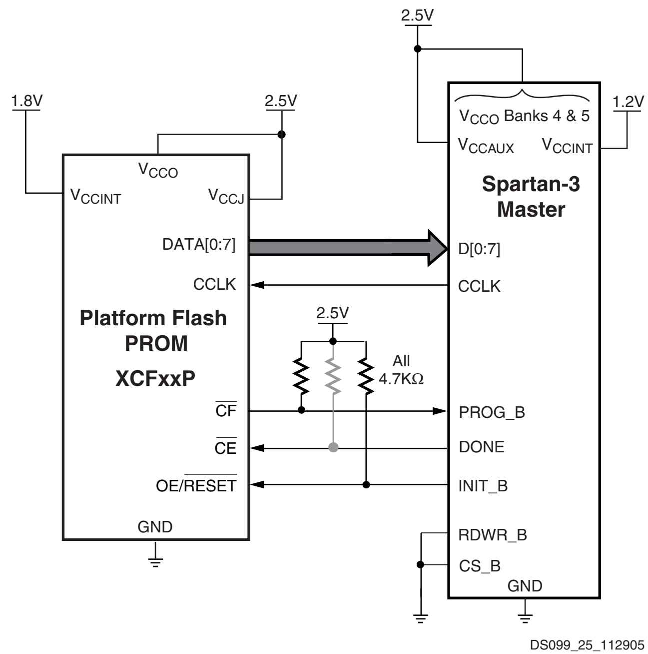
In the off-chip synchronization case (the [c] and [d] sections of Figure 21), CLK0 (or CLK2X) plus any of the DLL's other output clock signals exit the FPGA using output buffers (OBUF) to drive an external clock network plus registers on the board. As shown in the [c] section of Figure 21, the feedback loop is formed by feeding CLK0 (or CLK2X, in the [d] section) back into the FPGA using an IBUFG, which directly accesses the global clock network, or an IBUF. Then, the global clock net is connected directly to the CLKFB input.

DLL Frequency Modes

The DLL supports two distinct operating modes, High Frequency and Low Frequency, with each specified over a different clock frequency range. The DLL_FREQUENCY_MODE attribute chooses between the two modes. When the attribute is set to LOW, the Low Frequency mode permits all seven DLL clock outputs to operate over a low-to-moderate frequency range. When the attribute is set to HIGH, the High Frequency mode allows the CLK0, CLK180 and CLKDV outputs to operate at the highest possible frequencies. The remaining DLL clock outputs are not available for use in High Frequency mode.

Accommodating High Input Frequencies

If the frequency of the CLKIN signal is high such that it exceeds the maximum permitted, divide it down to an acceptable value using the CLKIN_DIVIDE_BY_2 attribute. When this attribute is set to TRUE, the CLKIN frequency is divided by a factor of two just as it enters the DCM.



Notes:

1. There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.

Figure 28: **Connection Diagram for Master Parallel Configuration**

Master Parallel Mode

In this mode, the FPGA configures from byte-wide data, and the FPGA supplies the CCLK configuration clock. In Master configuration modes, CCLK behaves as a bidirectional I/O pin. Timing is similar to the Slave Parallel mode except that CCLK is supplied by the FPGA. The device connections are shown in Figure 28.

Boundary-Scan (JTAG) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the FPGA. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). FPGA configuration using the Boundary-Scan mode is compatible with the IEEE Std 1149.1-1993 standard and IEEE Std 1532 for In-System Configurable (ISC) devices.

Configuration through the boundary-scan port is always available, regardless of the selected configuration mode. In some cases, however, the mode pin setting may affect proper programming of the device due to various interactions. For example, if the mode pins are set to Master Serial or Master Parallel mode, and the associated PROM is already programmed with a valid configuration image, then there is potential for configuration interference between the JTAG and PROM data. Selecting the Boundary-Scan mode disables the other modes and is the most reliable mode when programming via JTAG.

Configuration Sequence

The configuration of Spartan-3 devices is a three-stage process that occurs after Power-On Reset or the assertion of PROG_B. POR occurs after the V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 4 supplies have reached their respective maximum input threshold levels (see Table 29, page 59). After POR, the three-stage process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process. A flow diagram for the configuration sequence of the Serial and Parallel modes is shown in Figure 29. The flow diagram for the Boundary-Scan configuration sequence appears in Figure 30.

Simultaneously Switching Output Guidelines

This section provides guidelines for the maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins, of a given output signal standard, that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 49 and Table 50 provide the essential SSO guidelines. For each device/package combination, Table 49 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and will possibly not match the physical number of pairs. For each output signal standard and drive strength, Table 50 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The Table 50 guidelines are categorized by package style. Multiply the appropriate numbers from Table 49 and Table 50 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines may result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 49 x Table 50

The recommended maximum SSO values assume that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The number of SSOs allowed for quad-flat packages (VQ, TQ, PQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 49: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	VQ100	CP132[1][2]	TQ144[1]	PQ208	FT256	FG320	FG456	FG676	FG900	FG1156[2]
XC3S50	1	1.5	1.5	2	–	–	–	–	–	–
XC3S200	1	–	1.5	2	3	–	–	–	–	–
XC3S400	–	–	1.5	2	3	3	5	–	–	–
XC3S1000	–	–	–	–	3	3	5	5	–	–
XC3S1500	–	–	–	–	–	3	5	6	–	–
XC3S2000	–	–	–	–	–	–	5	6	9	–
XC3S4000	–	–	–	–	–	–	–	6	10	12
XC3S5000	–	–	–	–	–	–	–	6	10	12

Notes:

1. The V_{CCO} lines for the pair of banks on each side of the CP132 and TQ144 packages are internally tied together. Each pair of interconnected banks shares three V_{CCO}/GND pairs. Consequently, the per bank number is 1.5.
2. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.
3. The information in this table also applies to Pb-free packages.

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package				
			VQ100	TQ144	PQ208	CP132	FT256, FG320, FG456, FG676, FG900, FG1156
LVCMOS33	Slow	2	34	24	24	52	76
		4	17	14	14	26	46
		6	17	11	11	26	27
		8	10	10	10	13	20
		12	9	9	9	13	13
		16	8	8	8	8	10
		24	8	8	8	8	9
	Fast	2	20	20	20	26	44
		4	15	15	15	15	26
		6	11	11	11	13	16
		8	10	10	10	10	12
		12	8	8	8	8	10
		16	8	8	8	8	8
		24	7	7	7	7	7
LVDCI_33			10	10	10	10	10
LVDCI_DV2_33			10	10	10	10	10
HSLVDCI_33			10	10	10	10	10
LVTTL	Slow	2	34	25	25	52	60
		4	17	16	16	26	41
		6	17	15	15	26	29
		8	12	12	12	13	22
		12	10	10	10	13	13
		16	10	10	10	10	11
		24	8	8	8	8	9
	Fast	2	20	20	20	26	34
		4	13	13	13	13	20
		6	11	11	11	13	15
		8	10	10	10	10	12
		12	9	9	9	9	10
		16	8	8	8	8	9
		24	7	7	7	7	7

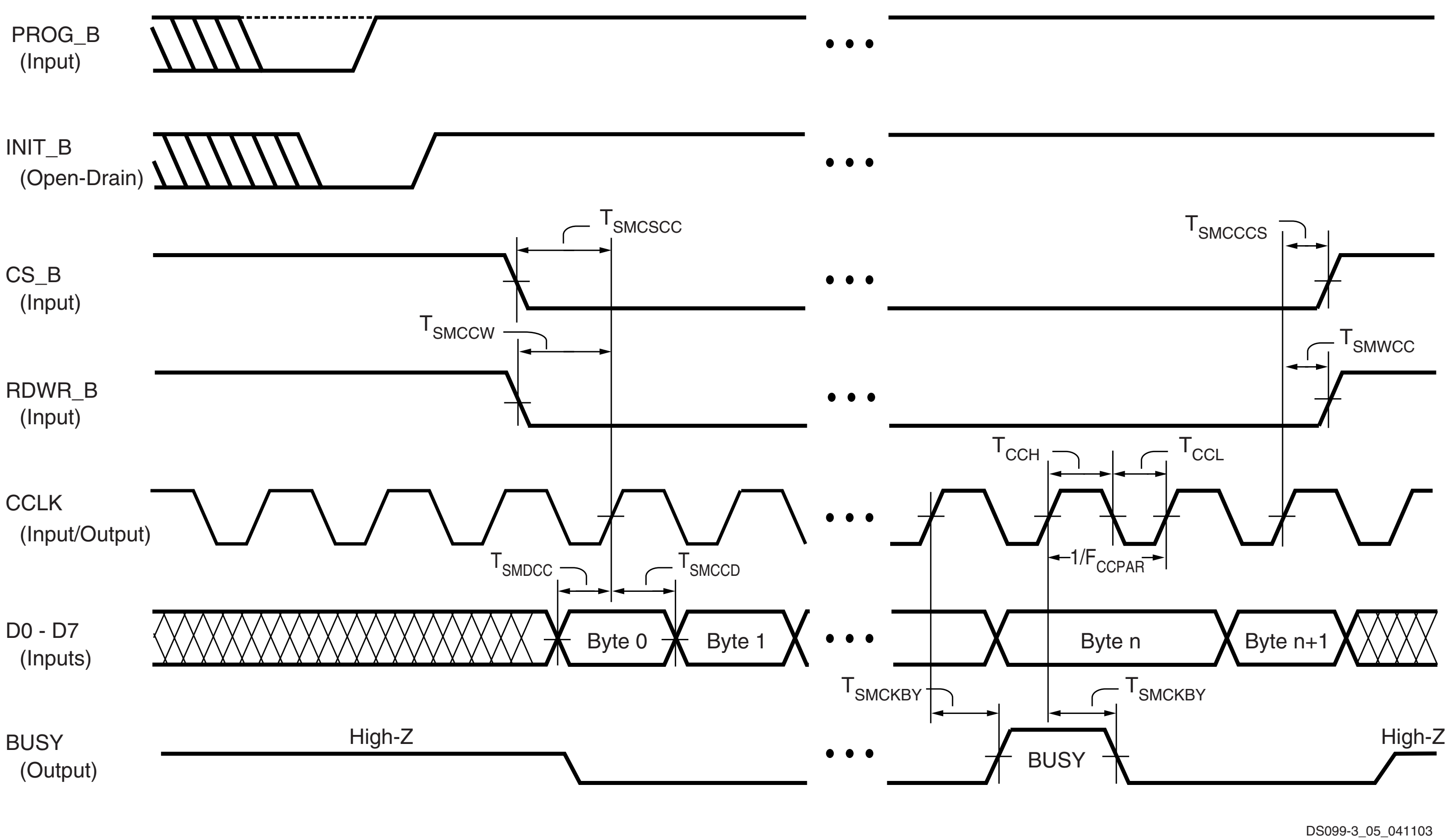


Figure 38: **Waveforms for Master and Slave Parallel Configuration**

Table 67: **Timing for the Master and Slave Parallel Configuration Modes**

Symbol	Description	Slave/ Master	All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin	Slave	–	12.0	ns
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	Both	10.0	–	ns
T_{SMCSCC}	The time from the setup of a logic level at the CS_B pin to the rising transition at the CCLK pin		10.0	–	ns
T_{SMCCW}(3)	The time from the setup of a logic level at the RDWR_B pin to the rising transition at the CCLK pin		10.0	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins	Both	0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CS_B pin		0	–	ns
T_{SMWCC}(3)	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns

Spartan-3 FPGA Family: Pinout Descriptions

DS099 (v3.0) October 29, 2012 **Product Specification**

Introduction

This data sheet module describes the various pins on a Spartan®-3 FPGA and how they connect to the supported component packages.

- The Pin Types section categorizes all of the FPGA pins by their function type.
- The Pin Definitions section provides a top-level description for each pin on the device.
- The Detailed, Functional Pin Descriptions section offers significantly more detail about each pin, especially for the dual- or special-function pins used during device configuration.
- Some pins have associated behavior that is controlled by settings in the configuration bitstream. These options are described in the Bitstream Options section.
- The Package Overview section describes the various packaging options available for Spartan-3 FPGAs. Detailed pin list tables and footprint diagrams are provided for each package solution.

Pin Descriptions

Pin Types

A majority of the pins on a Spartan-3 FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3 device packages, as outlined in Table 69. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 69: **Types of Pins on Spartan-3 FPGAs**

Pin Type/ Color Code	Description	Pin Name
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO, IO_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. There are 12 dual-purpose configuration pins on every package. The INIT_B pin has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM during configuration.	IO_Lxxy_#/DIN/D0, IO_Lxxy_#/D1, IO_Lxxy_#/D2, IO_Lxxy_#/D3, IO_Lxxy_#/D4, IO_Lxxy_#/D5, IO_Lxxy_#/D6, IO_Lxxy_#/D7, IO_Lxxy_#/CS_B, IO_Lxxy_#/RDWR_B, IO_Lxxy_#/BUSY/DOUT, IO_Lxxy_#/INIT_B
CONFIG	Dedicated configuration pin. Not available as a user-I/O pin. Every package has seven dedicated configuration pins. These pins are powered by VCCAUX and have a dedicated internal pull-up resistor to VCCAUX during configuration.	CCLK, DONE, M2, M1, M0, PROG_B, HSWAP_EN
JTAG	Dedicated JTAG pin. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX and have a dedicated internal pull-up resistor to VCCAUX during configuration.	TDI, TMS, TCK, TDO
DCI	Dual-purpose pin that is either a user-I/O pin or used to calibrate output buffer impedance for a specific bank using Digital Controlled Impedance (DCI). There are two DCI pins per I/O bank.	IO/VRN_# IO_Lxxy_#/VRN_# IO/VRP_# IO_Lxxy_#/VRP_#

Table 79: **Pin Behavior After Power-Up, During Configuration *(Cont'd)***

Pin Name	Configuration Mode Settings <M2:M1:M0>					Bitstream Configuration Option
	Serial Modes		SelectMap Parallel Modes		JTAG Mode <1:0:1>	
	Master <0:0:0>	Slave <1:1:1>	Master <0:1:1>	Slave <1:1:0>		
IO_Lxxy_#/ D5			D5 (I/O)	D5 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D6			D6 (I/O)	D6 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D7			D7 (I/O)	D7 (I/O)		Persist UnusedPin
IO_Lxxy_#/ CS_B			CS_B (I)	CS_B (I)		Persist UnusedPin
IO_Lxxy_#/ RDWR_B			RDWR_B (I)	RDWR_B (I)		Persist UnusedPin
IO_Lxxy_#/ BUSY/DOUT	DOUT (O)	DOUT (O)	BUSY (O)	BUSY (O)		Persist UnusedPin
DUAL: Dual-purpose configuration pins (INIT_B has a pull-up resistor to VCCO_4 or VCCO_BOTTOM always active during configuration, regardless of HSWAP_EN pin)						
IO_Lxxy_#/ INIT_B	INIT_B (I/OD)	INIT_B (I/OD)	INIT_B (I/OD)	INIT_B (I/OD)		UnusedPin
DCI: Digitally Controlled Impedance reference resistor input pins						
IO_Lxxy_#/ VRN_#						UnusedPin
IO/VRN_#						UnusedPin
IO_Lxxy_#/ VRP_#						UnusedPin
IO/VRP_#						UnusedPin
GCLK: Global clock buffer inputs						
IO_Lxxy_#/ GCLK0 through GCLK7						UnusedPin
VREF: I/O bank input reference voltage pins						
IO_Lxxy_#/ VREF_#						UnusedPin
IO/VREF_#						UnusedPin
CONFIG: Dedicated configuration pins (pull-up resistor to VCCAUX always active during configuration, regardless of HSWAP_EN pin)						
CCLK	CCLK (I/O)	CCLK (I)	CCLK (I/O)	CCLK (I)		CclkPin ConfigRate
PROG_B	PROG_B (I) (pull-up)	PROG_B (I) (pull-up)	PROG_B (I) (pull-up)	PROG_B (I) (pull-up)	PROG_B (I), Via JPROG_B instruction	ProgPin
DONE	DONE (I/OD)	DONE (I/OD)	DONE (I/OD)	DONE (I/OD)	DONE (I/OD)	DriveDone DonePin DonePipe
M2	M2=0 (I)	M2=1 (I)	M2=0 (I)	M2=1 (I)	M2=1 (I)	M2Pin
M1	M1=0 (I)	M1=1 (I)	M1=1 (I)	M1=1 (I)	M1=0 (I)	M1Pin
M0	M0=0 (I)	M0=1 (I)	M0=1 (I)	M0=0 (I)	M0=1 (I)	M0Pin
HSWAP_EN	HSWAP_EN (I)	HSWAP_EN (I)	HSWAP_EN (I)	HSWAP_EN (I)	HSWAP_EN (I)	HswapenPin

TQ144 Footprint

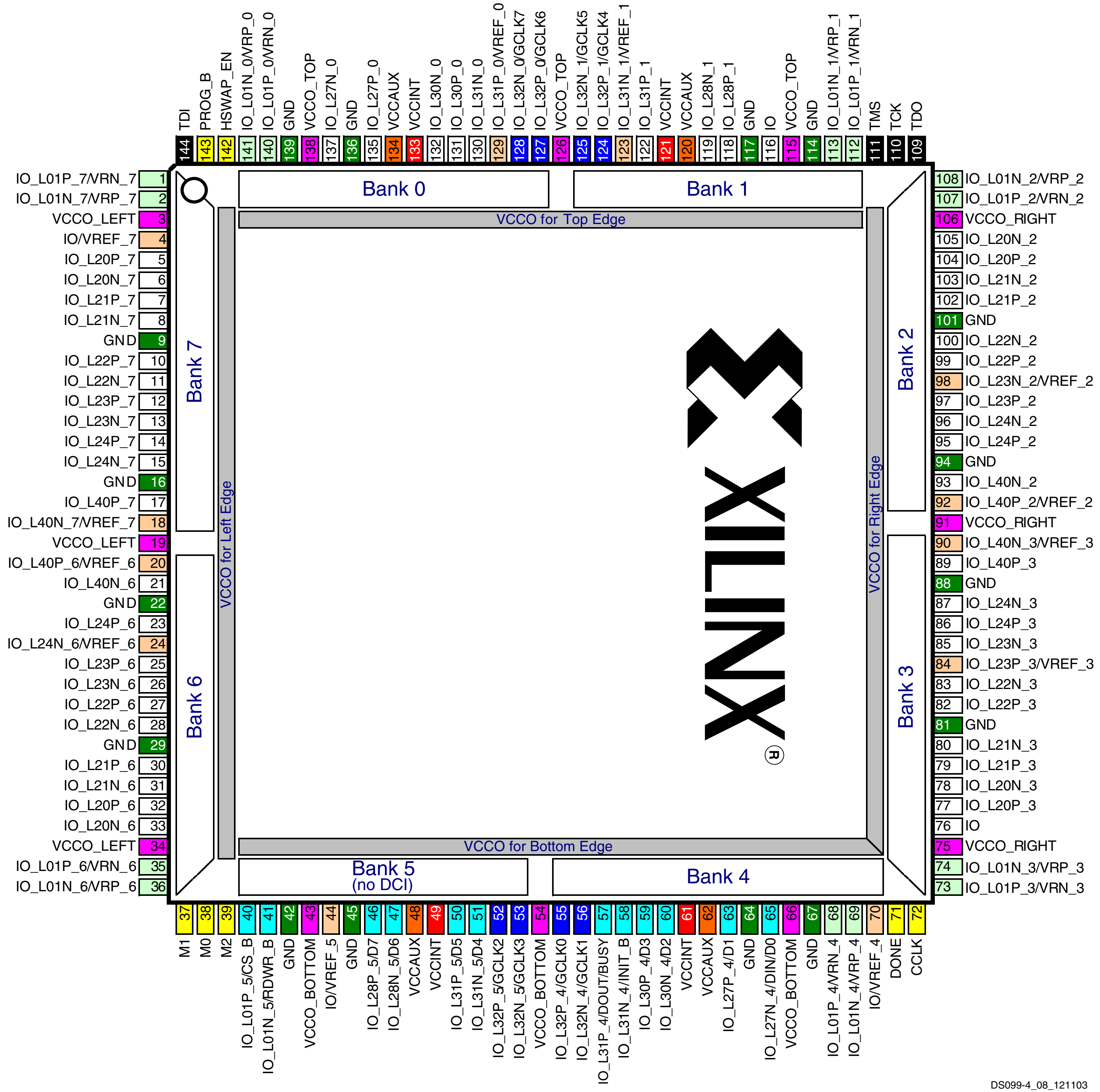


Figure 46: **TQ144 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

51	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	12	**VREF:** User I/O or input voltage reference for bank
14	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input	12	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	16	**GND:** Ground	4	**VCCAUX:** Auxiliary voltage supply (+2.5V)

Table 93: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
3	IO_L20P_3	IO_L20P_3	P114	I/O
3	IO_L21N_3	IO_L21N_3	P117	I/O
3	IO_L21P_3	IO_L21P_3	P116	I/O
3	IO_L22N_3	IO_L22N_3	P120	I/O
3	IO_L22P_3	IO_L22P_3	P119	I/O
3	IO_L23N_3	IO_L23N_3	P123	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	P122	VREF
3	IO_L24N_3	IO_L24N_3	P125	I/O
3	IO_L24P_3	IO_L24P_3	P124	I/O
3	N.C. (◆)	IO_L39N_3	P128	I/O
3	N.C. (◆)	IO_L39P_3	P126	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	P131	VREF
3	IO_L40P_3	IO_L40P_3	P130	I/O
3	VCCO_3	VCCO_3	P110	VCCO
3	VCCO_3	VCCO_3	P127	VCCO
4	IO	IO	P93	I/O
4	N.C. (◆)	IO	P97	I/O
4	IO/VREF_4	IO/VREF_4	P85	VREF
4	N.C. (◆)	IO/VREF_4	P96	VREF
4	IO/VREF_4	IO/VREF_4	P102	VREF
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	P101	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	P100	DCI
4	IO_L25N_4	IO_L25N_4	P95	I/O
4	IO_L25P_4	IO_L25P_4	P94	I/O
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	P92	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	P90	DUAL
4	IO_L30N_4/D2	IO_L30N_4/D2	P87	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	P86	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	P83	DUAL
4	IO_L31P_4/DOUT/BUSY	IO_L31P_4/DOUT/BUSY	P81	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	P80	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	P79	GCLK
4	VCCO_4	VCCO_4	P84	VCCO
4	VCCO_4	VCCO_4	P98	VCCO
5	IO	IO	P63	I/O
5	IO	IO	P71	I/O
5	IO/VREF_5	IO/VREF_5	P78	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	P58	DUAL
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	P57	DUAL
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	P62	DCI

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
6	IO_L16P_6	N3	I/O
6	IO_L17N_6	N2	I/O
6	IO_L17P_6/VREF_6	N1	VREF
6	IO_L19N_6	M4	I/O
6	IO_L19P_6	M3	I/O
6	IO_L20N_6	M2	I/O
6	IO_L20P_6	M1	I/O
6	IO_L21N_6	L5	I/O
6	IO_L21P_6	L4	I/O
6	IO_L22N_6	L3	I/O
6	IO_L22P_6	L2	I/O
6	IO_L23N_6	K5	I/O
6	IO_L23P_6	K4	I/O
6	IO_L24N_6/VREF_6	K3	VREF
6	IO_L24P_6	K2	I/O
6	IO_L39N_6	J4	I/O
6	IO_L39P_6	J3	I/O
6	IO_L40N_6	J2	I/O
6	IO_L40P_6/VREF_6	J1	VREF
6	VCCO_6	J5	VCCO
6	VCCO_6	J6	VCCO
6	VCCO_6	K6	VCCO
7	IO	G2	I/O
7	IO_L01N_7/VRP_7	C1	DCI
7	IO_L01P_7/VRN_7	B1	DCI
7	IO_L16N_7	C2	I/O
7	IO_L16P_7/VREF_7	C3	VREF
7	IO_L17N_7	D1	I/O
7	IO_L17P_7	D2	I/O
7	IO_L19N_7/VREF_7	E3	VREF
7	IO_L19P_7	D3	I/O
7	IO_L20N_7	E1	I/O
7	IO_L20P_7	E2	I/O
7	IO_L21N_7	F4	I/O
7	IO_L21P_7	E4	I/O
7	IO_L22N_7	F2	I/O
7	IO_L22P_7	F3	I/O
7	IO_L23N_7	G5	I/O
7	IO_L23P_7	F5	I/O
7	IO_L24N_7	G3	I/O

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
4	IO_L31P_4/ DOUT/BUSY	V10	DUAL
4	IO_L32N_4/GCLK1	N10	GCLK
4	IO_L32P_4/GCLK0	P10	GCLK
4	VCCO_4	M10	VCCO
4	VCCO_4	M11	VCCO
4	VCCO_4	T13	VCCO
4	VCCO_4	U11	VCCO
5	IO	N8	I/O
5	IO	P8	I/O
5	IO	U6	I/O
5	IO/VREF_5	R9	VREF
5	IO_L01N_5/RDWR_B	V3	DUAL
5	IO_L01P_5/CS_B	V2	DUAL
5	IO_L06N_5	T5	I/O
5	IO_L06P_5	T4	I/O
5	IO_L10N_5/VRP_5	V4	DCI
5	IO_L10P_5/VRN_5	U4	DCI
5	IO_L15N_5	R6	I/O
5	IO_L15P_5	R5	I/O
5	IO_L16N_5	V5	I/O
5	IO_L16P_5	U5	I/O
5	IO_L27N_5/VREF_5	P6	VREF
5	IO_L27P_5	P7	I/O
5	IO_L28N_5/D6	R7	DUAL
5	IO_L28P_5/D7	T7	DUAL
5	IO_L29N_5	V8	I/O
5	IO_L29P_5/VREF_5	V7	VREF
5	IO_L30N_5	R8	I/O
5	IO_L30P_5	T8	I/O
5	IO_L31N_5/D4	U9	DUAL
5	IO_L31P_5/D5	V9	DUAL
5	IO_L32N_5/GCLK3	N9	GCLK
5	IO_L32P_5/GCLK2	P9	GCLK
5	VCCO_5	M8	VCCO
5	VCCO_5	M9	VCCO
5	VCCO_5	T6	VCCO
5	VCCO_5	U8	VCCO
6	IO	K6	I/O
6	IO_L01N_6/VRP_6	T3	DCI

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	W9	VREF
5	IO_L27P_5	IO_L27P_5	V9	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	AB9	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	AA9	DUAL
5	IO_L29N_5	IO_L29N_5	Y10	I/O
5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	W10	VREF
5	IO_L30N_5	IO_L30N_5	AB10	I/O
5	IO_L30P_5	IO_L30P_5	AA10	I/O
5	IO_L31N_5/D4	IO_L31N_5/D4	W11	DUAL
5	IO_L31P_5/D5	IO_L31P_5/D5	V11	DUAL
5	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	AA11	GCLK
5	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	Y11	GCLK
5	VCCO_5	VCCO_5	T9	VCCO
5	VCCO_5	VCCO_5	T10	VCCO
5	VCCO_5	VCCO_5	T11	VCCO
5	VCCO_5	VCCO_5	U8	VCCO
5	VCCO_5	VCCO_5	Y8	VCCO
6	IO	IO	Y1	I/O
6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	Y3	DCI
6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	Y2	DCI
6	IO_L16N_6	IO_L16N_6	W4	I/O
6	IO_L16P_6	IO_L16P_6	W3	I/O
6	IO_L17N_6	IO_L17N_6	W2	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	W1	VREF
6	IO_L19N_6	IO_L19N_6	V5	I/O
6	IO_L19P_6	IO_L19P_6	U5	I/O
6	IO_L20N_6	IO_L20N_6	V4	I/O
6	IO_L20P_6	IO_L20P_6	V3	I/O
6	IO_L21N_6	IO_L21N_6	V2	I/O
6	IO_L21P_6	IO_L21P_6	V1	I/O
6	IO_L22N_6	IO_L22N_6	T6	I/O
6	IO_L22P_6	IO_L22P_6	T5	I/O
6	IO_L23N_6	IO_L23N_6	U4	I/O
6	IO_L23P_6	IO_L23P_6	T4	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	U3	VREF
6	IO_L24P_6	IO_L24P_6	U2	I/O
6	N.C. (◆)	IO_L26N_6	T3	I/O
6	N.C. (◆)	IO_L26P_6	R4	I/O
6	IO_L27N_6	IO_L27N_6	T2	I/O
6	IO_L27P_6	IO_L27P_6	T1	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
2	N.C. (◆)	IO_L06N_2	IO_L06N_2	IO_L06N_2	IO_L06N_2	G20	I/O
2	N.C. (◆)	IO_L06P_2	IO_L06P_2	IO_L06P_2	IO_L06P_2	G21	I/O
2	N.C. (◆)	IO_L07N_2	IO_L07N_2	IO_L07N_2	IO_L07N_2	F23	I/O
2	N.C. (◆)	IO_L07P_2	IO_L07P_2	IO_L07P_2	IO_L07P_2	F24	I/O
2	N.C. (◆)	IO_L08N_2	IO_L08N_2	IO_L08N_2	IO_L08N_2	G22	I/O
2	N.C. (◆)	IO_L08P_2	IO_L08P_2	IO_L08P_2	IO_L08P_2	G23	I/O
2	N.C. (◆)	IO_L09N_2/VREF_2[(1)]	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	F25	VREF[(1)]
2	N.C. (◆)	IO_L09P_2	IO_L09P_2	IO_L09P_2	IO_L09P_2	F26	I/O
2	N.C. (◆)	IO_L10N_2	IO_L10N_2	IO_L10N_2	IO_L10N_2	G25	I/O
2	N.C. (◆)	IO_L10P_2	IO_L10P_2	IO_L10P_2	IO_L10P_2	G26	I/O
2	IO_L14N_2	IO_L14N_2	IO_L14N_2[(2)]	IO_L11N_2[(2)]	IO_L11N_2	H20	I/O
2	IO_L14P_2	IO_L14P_2	IO_L14P_2[(2)]	IO_L11P_2[(2)]	IO_L11P_2	H21	I/O
2	IO_L16N_2	IO_L16N_2	IO_L16N_2[(2)]	IO_L12N_2[(2)]	IO_L12N_2	H22	I/O
2	IO_L16P_2	IO_L16P_2	IO_L16P_2[(2)]	IO_L12P_2[(2)]	IO_L12P_2	J21	I/O
2	IO_L17N_2	IO_L17N_2	IO_L17N_2[(2)]	IO_L13N_2[(2)]	IO[(3)]	H23	I/O
2	IO_L17P_2/VREF_2	IO_L17P_2/VREF_2	IO_L17P_2[(2)]/VREF_2	IO_L13P_2[(2)]/VREF_2	IO/VREF_2[(3)]	H24	VREF
2	IO_L19N_2	IO_L19N_2	IO_L19N_2	IO_L19N_2	IO_L19N_2	H25	I/O
2	IO_L19P_2	IO_L19P_2	IO_L19P_2	IO_L19P_2	IO_L19P_2	H26	I/O
2	IO_L20N_2	IO_L20N_2	IO_L20N_2	IO_L20N_2	IO_L20N_2	J20	I/O
2	IO_L20P_2	IO_L20P_2	IO_L20P_2	IO_L20P_2	IO_L20P_2	K20	I/O
2	IO_L21N_2	IO_L21N_2	IO_L21N_2	IO_L21N_2	IO_L21N_2	J22	I/O
2	IO_L21P_2	IO_L21P_2	IO_L21P_2	IO_L21P_2	IO_L21P_2	J23	I/O
2	IO_L22N_2	IO_L22N_2	IO_L22N_2	IO_L22N_2	IO_L22N_2	J24	I/O
2	IO_L22P_2	IO_L22P_2	IO_L22P_2	IO_L22P_2	IO_L22P_2	J25	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	K21	VREF
2	IO_L23P_2	IO_L23P_2	IO_L23P_2	IO_L23P_2	IO_L23P_2	K22	I/O
2	IO_L24N_2	IO_L24N_2	IO_L24N_2	IO_L24N_2	IO_L24N_2	K23	I/O
2	IO_L24P_2	IO_L24P_2	IO_L24P_2	IO_L24P_2	IO_L24P_2	K24	I/O
2	IO_L26N_2	IO_L26N_2	IO_L26N_2	IO_L26N_2	IO_L26N_2	K25	I/O
2	IO_L26P_2	IO_L26P_2	IO_L26P_2	IO_L26P_2	IO_L26P_2	K26	I/O
2	IO_L27N_2	IO_L27N_2	IO_L27N_2	IO_L27N_2	IO_L27N_2	L19	I/O
2	IO_L27P_2	IO_L27P_2	IO_L27P_2	IO_L27P_2	IO_L27P_2	L20	I/O
2	IO_L28N_2	IO_L28N_2	IO_L28N_2	IO_L28N_2	IO_L28N_2	L21	I/O
2	IO_L28P_2	IO_L28P_2	IO_L28P_2	IO_L28P_2	IO_L28P_2	L22	I/O
2	IO_L29N_2	IO_L29N_2	IO_L29N_2	IO_L29N_2	IO_L29N_2	L25	I/O
2	IO_L29P_2	IO_L29P_2	IO_L29P_2	IO_L29P_2	IO_L29P_2	L26	I/O
2	IO_L31N_2	IO_L31N_2	IO_L31N_2	IO_L31N_2	IO_L31N_2	M19	I/O
2	IO_L31P_2	IO_L31P_2	IO_L31P_2	IO_L31P_2	IO_L31P_2	M20	I/O
2	IO_L32N_2	IO_L32N_2	IO_L32N_2	IO_L32N_2	IO_L32N_2	M21	I/O
2	IO_L32P_2	IO_L32P_2	IO_L32P_2	IO_L32P_2	IO_L32P_2	M22	I/O
2	IO_L33N_2	IO_L33N_2	IO_L33N_2	IO_L33N_2	IO_L33N_2	L23	I/O
2	IO_L33P_2	IO_L33P_2	IO_L33P_2	IO_L33P_2	IO_L33P_2	M24	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AB5	DUAL
5	IO_L04N_5	IO_L04N_5	IO_L04N_5	IO_L04N_5	IO_L04N_5	AE4	I/O
5	IO_L04P_5	IO_L04P_5	IO_L04P_5	IO_L04P_5	IO_L04P_5	AD4	I/O
5	IO_L05N_5	IO_L05N_5	IO_L05N_5	IO_L05N_5	IO_L05N_5	AB6	I/O
5	IO_L05P_5	IO_L05P_5	IO_L05P_5	IO_L05P_5	IO_L05P_5	AA6	I/O
5	IO_L06N_5	IO_L06N_5	IO_L06N_5	IO_L06N_5	IO_L06N_5	AE5	I/O
5	IO_L06P_5	IO_L06P_5	IO_L06P_5	IO_L06P_5	IO_L06P_5	AD5	I/O
5	IO_L07N_5	IO_L07N_5	IO_L07N_5	IO_L07N_5	IO_L07N_5	AD6	I/O
5	IO_L07P_5	IO_L07P_5	IO_L07P_5	IO_L07P_5	IO_L07P_5	AC6	I/O
5	IO_L08N_5	IO_L08N_5	IO_L08N_5	IO_L08N_5	IO_L08N_5	AF6	I/O
5	IO_L08P_5	IO_L08P_5	IO_L08P_5	IO_L08P_5	IO_L08P_5	AE6	I/O
5	IO_L09N_5	IO_L09N_5	IO_L09N_5	IO_L09N_5	IO_L09N_5	AC7	I/O
5	IO_L09P_5	IO_L09P_5	IO_L09P_5	IO_L09P_5	IO_L09P_5	AB7	I/O
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	AF7	DCI
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	AE7	DCI
5	N.C. (◆)	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	AB8	VREF
5	N.C. (◆)	IO_L11P_5	IO_L11P_5	IO_L11P_5	IO_L11P_5	AA8	I/O
5	N.C. (◆)	IO_L12N_5	IO_L12N_5	IO_L12N_5	IO_L12N_5	AD8	I/O
5	N.C. (◆)	IO_L12P_5	IO_L12P_5	IO_L12P_5	IO_L12P_5	AC8	I/O
5	IO_L15N_5	IO_L15N_5	IO_L15N_5	IO_L15N_5	IO_L15N_5	AF8	I/O
5	IO_L15P_5	IO_L15P_5	IO_L15P_5	IO_L15P_5	IO_L15P_5	AE8	I/O
5	IO_L16N_5	IO_L16N_5	IO_L16N_5	IO_L16N_5	IO_L16N_5	AA9	I/O
5	IO_L16P_5	IO_L16P_5	IO_L16P_5	IO_L16P_5	IO_L16P_5	Y9	I/O
5	N.C. (◆)	IO_L18N_5	IO_L18N_5	IO_L18N_5	IO_L18N_5	AE9	I/O
5	N.C. (◆)	IO_L18P_5	IO_L18P_5	IO_L18P_5	IO_L18P_5	AD9	I/O
5	IO_L19N_5	IO_L19N_5	IO_L19N_5	IO_L19N_5	IO_L19N_5	AA10	I/O
5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	Y10	VREF
5	IO_L22N_5	IO_L22N_5	IO_L22N_5	IO_L22N_5	IO_L22N_5	AC10	I/O
5	IO_L22P_5	IO_L22P_5	IO_L22P_5	IO_L22P_5	IO_L22P_5	AB10	I/O
5	N.C. (◆)	IO_L23N_5	IO_L23N_5	IO_L23N_5	IO_L23N_5	AF10	I/O
5	N.C. (◆)	IO_L23P_5	IO_L23P_5	IO_L23P_5	IO_L23P_5	AE10	I/O
5	IO_L24N_5	IO_L24N_5	IO_L24N_5	IO_L24N_5	IO_L24N_5	Y11	I/O
5	IO_L24P_5	IO_L24P_5	IO_L24P_5	IO_L24P_5	IO_L24P_5	W11	I/O
5	IO_L25N_5	IO_L25N_5	IO_L25N_5	IO_L25N_5	IO_L25N_5	AB11	I/O
5	IO_L25P_5	IO_L25P_5	IO_L25P_5	IO_L25P_5	IO_L25P_5	AA11	I/O
5	N.C. (◆)	IO_L26N_5	IO_L26N_5	IO_L26N_5	IO_L26N_5	AF11	I/O
5	N.C. (◆)	IO_L26P_5	IO_L26P_5	IO_L26P_5	IO_L26P_5	AE11	I/O
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	Y12	VREF
5	IO_L27P_5	IO_L27P_5	IO_L27P_5	IO_L27P_5	IO_L27P_5	W12	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	AB12	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	AA12	DUAL
5	IO_L29N_5	IO_L29N_5	IO_L29N_5	IO_L29N_5	IO_L29N_5	AF12	I/O

FG676 Footprint

Left Half of Package (Top View)

XC3S1000 (391 max. user I/O)

315	**I/O:** Unrestricted, general-purpose user I/O
40	**VREF:** User I/O or input voltage reference for bank
98	**N.C.:** Unconnected pins for XC3S1000 (◆)

XC3S1500 (487 max user I/O)

403	**I/O:** Unrestricted, general-purpose user I/O
48	**VREF:** User I/O or input voltage reference for bank
2	**N.C.:** Unconnected pins for XC3S1500 (■)

XC3S2000, XC3S4000, XC3S5000 (489 max user I/O)

405	**I/O:** Unrestricted, general-purpose user I/O
48	**VREF:** User I/O or input voltage reference for bank
0	**N.C.:** No unconnected pins

All devices

12	**DUAL:** Configuration pin, then possible user I/O
8	**GCLK:** User I/O or global clock buffer input
16	**DCI:** User I/O or reference resistor input for bank
7	**CONFIG:** Dedicated configuration pins
4	**JTAG:** Dedicated JTAG port pins
20	**VCCINT:** Internal core voltage supply (+1.2V)
64	**VCCO:** Output voltage supply for bank
16	**VCCAUX:** Auxiliary voltage supply (+2.5V)
76	**GND:** Ground

Bank 0 (top, columns 7–13); Bank 7 (left, rows A–N); Bank 6 (left, rows P–AF); Bank 5 (bottom, columns 4–13)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	VCCAUX	I/O	I/O L05P_0 VREF_0	I/O	I/O	I/O L10P_0	I/O L15P_0	VCCAUX	I/O L23P_0 ◆	I/O L26P_0 VREF_0 ◆	I/O L29P_0	I/O L32P_0 GCLK6
B	VCCAUX	GND	I/O VREF_0	I/O L05N_0	I/O L06P_0	I/O L08P_0	I/O L10N_0	I/O L15N_0	I/O L18P_0 ◆	I/O L23N_0 ◆	I/O L26N_0 ◆	I/O L29N_0	I/O L32N_0 GCLK7
C	TDI	HSWAP_EN	GND	I/O	I/O L06N_0	I/O L08N_0	VCCO_0	I/O ◆	I/O L18N_0 ◆	I/O L22P_0	VCCO_0	I/O	I/O L31P_0 VREF_0
D	I/O L03N_7 VREF_7	I/O L03P_7	PROG_B	GND	I/O L01P_0 VRN_0	I/O L07P_0	I/O L09P_0	I/O L12P_0 ◆	I/O L17P_0 ◆	I/O L22N_0	I/O L25P_0	GND	I/O L31N_0
E	I/O L06N_7	I/O L06P_7 ◆	I/O L02N_7	I/O L02P_7	I/O L01N_0 VRP_0	I/O L07N_0	I/O L09N_0	I/O L12N_0 ◆	I/O L17N_0 ◆	I/O L19P_0	I/O L25N_0	I/O L28P_0	I/O
F	I/O L09N_7 ◆	I/O L09P_7 ◆	I/O L07N_7 ◆	I/O L07P_7 ◆	I/O L01N_7 VRP_7	I/O L01P_7 VRN_7	I/O VREF_0	I/O L11P_0 ◆	I/O L16P_0	I/O L19N_0	I/O L24P_0	I/O L28N_0	I/O L30P_0
G	I/O L14N_7	I/O L14P_7	VCCO_7	I/O L08N_7 ◆	I/O L08P_7 ◆	I/O L05N_7 ◆	I/O L05P_7 ◆	I/O L11N_0 ◆	I/O L16N_0	I/O VREF_0	I/O L24N_0	I/O L27N_0	I/O L30N_0
H	I/O L19N_7 VREF_7	I/O L19P_7	I/O L17N_7	I/O L17P_7	I/O L16P_7 VREF_7	I/O L10N_7 ◆	I/O L10P_7 VREF_7 ◆	VCCINT	VCCO_0	VCCO_0	I/O	I/O	I/O L27P_0
J	VCCAUX	I/O L22N_7	I/O L22P_7	I/O L21N_7	I/O L21P_7	I/O L16N_7	I/O L20P_7	VCCO_7	VCCINT	VCCINT	VCCO_0	VCCO_0	VCCO_0
K	I/O L26N_7	I/O L26P_7	I/O L24N_7	I/O L24P_7	I/O L23N_7	I/O L23P_7	I/O L20N_7	VCCO_7	VCCINT	VCCINT	GND	GND	VCCO_0
L	I/O L29N_7	I/O L29P_7	VCCO_7	I/O L33P_7	I/O L28N_7	I/O L28P_7	I/O L27N_7	I/O L27P_7 VREF_7	VCCO_7	GND	GND	GND	GND
M	I/O L34N_7	I/O L34P_7	I/O L33N_7	GND	I/O L32P_7	I/O L32N_7	I/O L31N_7	I/O L31P_7	VCCO_7	GND	GND	GND	GND
N	I/O L40N_7 VREF_7	I/O L40P_7	I/O L39N_7	I/O L39P_7	I/O L38N_7	I/O L38P_7	I/O L35N_7	I/O L35P_7	VCCO_7	VCCO_7	GND	GND	GND
P	I/O L40P_6 VREF_6	I/O L40N_6	I/O L39P_6	I/O L39N_6	I/O L38P_6	I/O L38N_6	I/O L35P_6	I/O L35N_6	VCCO_6	VCCO_6	GND	GND	GND
R	I/O L34P_6	I/O L34N_6 VREF_6	I/O L33P_6	GND	I/O L32P_6	I/O L32N_6	I/O L31P_6	I/O L31N_6	VCCO_6	GND	GND	GND	GND
T	I/O L29P_6	I/O L29N_6	VCCO_6	I/O L33N_6	I/O L28P_6	I/O L28N_6	I/O L27P_6	I/O L27N_6	VCCO_6	GND	GND	GND	GND
U	I/O L26P_6	I/O L26N_6	I/O L24P_6	I/O L24N_6 VREF_6	I/O L23P_6	I/O L23N_6	I/O L20P_6	VCCO_6	VCCINT	VCCINT	GND	GND	VCCO_5
V	VCCAUX	I/O L22P_6	I/O L22N_6	I/O L21P_6	I/O L21N_6	I/O L16N_6	I/O L20N_6	VCCO_6	VCCINT	VCCINT	VCCO_5	VCCO_5	VCCO_5
W	I/O L19P_6	I/O L19N_6	I/O L17P_6 VREF_6	I/O L17N_6	I/O L16P_6	I/O L14P_6	I/O L14N_6	VCCINT	VCCO_5	VCCO_5	I/O L24P_5	I/O L27P_5	I/O L30P_5
Y	I/O L10P_6 ◆	I/O L10N_6 ◆	VCCO_6	I/O L08P_6 ◆	I/O L08N_6 ◆	I/O L06P_6 ◆	I/O L06N_6 ◆	I/O	I/O L16P_5	I/O L19P_5 VREF_5	I/O L24N_5	I/O L27N_5 VREF_5	I/O L30N_5
AA	I/O L09P_6 ◆	I/O L09N_6 VREF_6 ◆	I/O L07P_6 ◆	I/O L07N_6 ◆	I/O ◆■	I/O L05P_5	I/O	I/O L11P_5 ◆	I/O L16N_5	I/O L19N_5	I/O L25P_5	I/O L28P_5 D7	I/O
AB	I/O L05P_6 ◆	I/O L05N_6 ◆	I/O L02P_6	I/O L02N_6	I/O L01P_5 CS_B	I/O L05N_5	I/O L09P_5	I/O L11N_5 VREF_5 ◆	I/O	I/O L22P_5	I/O L25N_5	I/O L28N_5 D6	I/O L31P_5 D5
AC	I/O L03P_6	I/O L03N_6 VREF_6	M1	GND	I/O L01N_5 RDWR_B	I/O L07P_5	I/O L09N_5	I/O L12P_5 ◆	I/O ◆	I/O L22N_5	I/O	GND	I/O L31N_5 D4
AD	I/O L01P_6 VRN_6	I/O L01N_6 VRP_6	GND	I/O L04P_5	I/O L06P_5	I/O L07N_5	VCCO_5	I/O L12N_5 ◆	I/O L18P_5 ◆	I/O	VCCO_5	I/O	I/O L32P_5 GCLK2
AE	VCCAUX	GND	M0	I/O L04N_5	I/O L06N_5	I/O L08P_5	I/O L10P_5 VRN_5	I/O L15P_5	I/O L18N_5 ◆	I/O L23P_5 ◆	I/O L26P_5 ◆	I/O L29P_5 VREF_5	I/O L32N_5 GCLK3
AF	GND	VCCAUX	M2	I/O	I/O VREF_5	I/O L08N_5	I/O L10N_5 VRP_5	I/O L15N_5	VCCAUX	I/O L23N_5 ◆	I/O L26N_5 ◆	I/O L29N_5	I/O VREF_5

DS099-4_12a_030203

Figure 53: **FG676 Package Footprint (Top View)**

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	AE14	VREF
5	IO_L27P_5	IO_L27P_5	AE13	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	AJ14	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	AH14	DUAL
5	IO_L29N_5	IO_L29N_5	AC15	I/O
5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	AB15	VREF
5	IO_L30N_5	IO_L30N_5	AD15	I/O
5	IO_L30P_5	IO_L30P_5	AD14	I/O
5	IO_L31N_5/D4	IO_L31N_5/D4	AG15	DUAL
5	IO_L31P_5/D5	IO_L31P_5/D5	AF15	DUAL
5	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	AJ15	GCLK
5	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	AH15	GCLK
5	N.C. (◆)	IO_L35N_5	AK7	I/O
5	N.C. (◆)	IO_L35P_5	AJ7	I/O
5	N.C. (◆)	IO_L36N_5	AD8	I/O
5	N.C. (◆)	IO_L36P_5	AC8	I/O
5	N.C. (◆)	IO_L37N_5	AF8	I/O
5	N.C. (◆)	IO_L37P_5	AE8	I/O
5	N.C. (◆)	IO_L38N_5	AH8	I/O
5	N.C. (◆)	IO_L38P_5	AG8	I/O
5	VCCO_5	VCCO_5	AH5	VCCO
5	VCCO_5	VCCO_5	AF7	VCCO
5	VCCO_5	VCCO_5	AD9	VCCO
5	VCCO_5	VCCO_5	AH9	VCCO
5	VCCO_5	VCCO_5	AB11	VCCO
5	VCCO_5	VCCO_5	Y12	VCCO
5	VCCO_5	VCCO_5	Y13	VCCO
5	VCCO_5	VCCO_5	AD13	VCCO
5	VCCO_5	VCCO_5	AH13	VCCO
5	VCCO_5	VCCO_5	Y14	VCCO
6	IO	IO	AB6	I/O
6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	AH2	DCI
6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	AH1	DCI
6	IO_L02N_6	IO_L02N_6	AG4	I/O
6	IO_L02P_6	IO_L02P_6	AG3	I/O
6	IO_L03N_6/VREF_6	IO_L03N_6/VREF_6	AG2	VREF
6	IO_L03P_6	IO_L03P_6	AG1	I/O
6	IO_L04N_6	IO_L04N_6	AF2	I/O
6	IO_L04P_6	IO_L04P_6	AF1	I/O
6	IO_L05N_6	IO_L05N_6	AF4	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	GND	GND	K30	GND
N/A	GND	GND	P30	GND
N/A	GND	GND	U30	GND
N/A	GND	GND	AA30	GND
N/A	GND	GND	AE30	GND
N/A	GND	GND	AJ30	GND
N/A	GND	GND	AK30	GND
N/A	GND	GND	AK2	GND
N/A	VCCAUX	VCCAUX	F4	VCCAUX
N/A	VCCAUX	VCCAUX	K4	VCCAUX
N/A	VCCAUX	VCCAUX	P4	VCCAUX
N/A	VCCAUX	VCCAUX	U4	VCCAUX
N/A	VCCAUX	VCCAUX	AA4	VCCAUX
N/A	VCCAUX	VCCAUX	AE4	VCCAUX
N/A	VCCAUX	VCCAUX	D6	VCCAUX
N/A	VCCAUX	VCCAUX	AG6	VCCAUX
N/A	VCCAUX	VCCAUX	D10	VCCAUX
N/A	VCCAUX	VCCAUX	AG10	VCCAUX
N/A	VCCAUX	VCCAUX	D14	VCCAUX
N/A	VCCAUX	VCCAUX	AG14	VCCAUX
N/A	VCCAUX	VCCAUX	D17	VCCAUX
N/A	VCCAUX	VCCAUX	AG17	VCCAUX
N/A	VCCAUX	VCCAUX	D21	VCCAUX
N/A	VCCAUX	VCCAUX	AG21	VCCAUX
N/A	VCCAUX	VCCAUX	D25	VCCAUX
N/A	VCCAUX	VCCAUX	AG25	VCCAUX
N/A	VCCAUX	VCCAUX	F27	VCCAUX
N/A	VCCAUX	VCCAUX	K27	VCCAUX
N/A	VCCAUX	VCCAUX	P27	VCCAUX
N/A	VCCAUX	VCCAUX	U27	VCCAUX
N/A	VCCAUX	VCCAUX	AA27	VCCAUX
N/A	VCCAUX	VCCAUX	AE27	VCCAUX
N/A	VCCINT	VCCINT	L11	VCCINT
N/A	VCCINT	VCCINT	R11	VCCINT
N/A	VCCINT	VCCINT	T11	VCCINT
N/A	VCCINT	VCCINT	Y11	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	N12	VCCINT
N/A	VCCINT	VCCINT	P12	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L24P_3	IO_L24P_3	AC26	I/O
3	IO_L26N_3	IO_L26N_3	AA28	I/O
3	IO_L26P_3	IO_L26P_3	AA27	I/O
3	IO_L27N_3	IO_L27N_3	AA30	I/O
3	IO_L27P_3	IO_L27P_3	AA29	I/O
3	IO_L28N_3	IO_L28N_3	AA32	I/O
3	IO_L28P_3	IO_L28P_3	AA31	I/O
3	IO_L29N_3	IO_L29N_3	AA34	I/O
3	IO_L29P_3	IO_L29P_3	AA33	I/O
3	IO_L30N_3	IO_L30N_3	Y29	I/O
3	IO_L30P_3	IO_L30P_3	Y28	I/O
3	IO_L31N_3	IO_L31N_3	Y32	I/O
3	IO_L31P_3	IO_L31P_3	Y31	I/O
3	IO_L32N_3	IO_L32N_3	Y34	I/O
3	IO_L32P_3	IO_L32P_3	Y33	I/O
3	IO_L33N_3	IO_L33N_3	W25	I/O
3	IO_L33P_3	IO_L33P_3	Y26	I/O
3	IO_L34N_3	IO_L34N_3	W29	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	W28	VREF
3	IO_L35N_3	IO_L35N_3	W33	I/O
3	IO_L35P_3	IO_L35P_3	W32	I/O
3	IO_L37N_3	IO_L37N_3	V28	I/O
3	IO_L37P_3	IO_L37P_3	V27	I/O
3	IO_L38N_3	IO_L38N_3	V30	I/O
3	IO_L38P_3	IO_L38P_3	V29	I/O
3	IO_L39N_3	IO_L39N_3	V32	I/O
3	IO_L39P_3	IO_L39P_3	V31	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	V34	VREF
3	IO_L40P_3	IO_L40P_3	V33	I/O
3	N.C. (◆)	IO_L41N_3	AH32	I/O
3	N.C. (◆)	IO_L41P_3	AH31	I/O
3	N.C. (◆)	IO_L44N_3	AD29	I/O
3	N.C. (◆)	IO_L44P_3	AD28	I/O
3	IO_L45N_3	IO_L45N_3	AC34	I/O
3	IO_L45P_3	IO_L45P_3	AC33	I/O
3	IO_L46N_3	IO_L46N_3	AB28	I/O
3	IO_L46P_3	IO_L46P_3	AB27	I/O
3	IO_L47N_3	IO_L47N_3	AB32	I/O
3	IO_L47P_3	IO_L47P_3	AB31	I/O
3	IO_L48N_3	IO_L48N_3	AA24	I/O