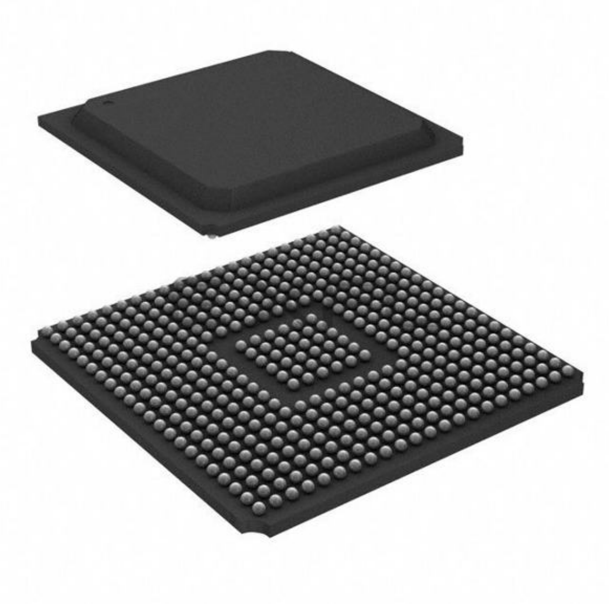

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1920
Number of Logic Elements/Cells	17280
Total RAM Bits	442368
Number of I/O	333
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1000-4fg456c

In contrast, the 144-pin Thin Quad Flat Pack (TQ144) package and the 132-pin Chip-Scale Package (CP132) tie V_{CCO} together internally for the pair of banks on each side of the device. For example, the V_{CCO} Bank 0 and the V_{CCO} Bank 1 lines are tied together. The interconnected bank-pairs are 0/1, 2/3, 4/5, and 6/7. As a result, Spartan-3 devices in the CP132 and TQ144 packages support four independent V_{CCO} supplies.

Note: The CP132 package is discontinued. See http://www.xilinx.com/support/documentation /spartan-3_customer_notices.htm.

Spartan-3 FPGA Compatibility

Within the Spartan-3 family, all devices are pin-compatible by package. When the need for future logic resources outgrows the capacity of the Spartan-3 device in current use, a larger device in the same package can serve as a direct replacement. Larger devices may add extra V_{REF} and V_{CCO} lines to support a greater number of I/Os. In the larger device, more pins can convert from user I/Os to V_{REF} lines. Also, additional V_{CCO} lines are bonded out to pins that were "not connected" in the smaller device. Thus, it is important to plan for future upgrades at the time of the board's initial design by laying out connections to the extra pins.

The Spartan-3 family is not pin-compatible with any previous Xilinx FPGA family or with other platforms among the Spartan-3 Generation FPGAs.

Rules Concerning Banks

When assigning I/Os to banks, it is important to follow the following V_{CCO} rules:

- Leave no V_{CCO} pins unconnected on the FPGA.
- Set all V_{CCO} lines associated with the (interconnected) bank to the same voltage level.
- The V_{CCO} levels used by all standards assigned to the I/Os of the (interconnected) bank(s) must agree. The Xilinx development software checks for this. Tables 8, 9, and 10 describe how different standards use the V_{CCO} supply.
- Only one of the following standards is allowed on outputs per bank: LVDS, LDT, LVDS_EXT, or RSDS. This restriction is for the eight banks in each device, even if the V_{CCO} levels are shared across banks, as in the CP132 and TQ144 packages.
- If none of the standards assigned to the I/Os of the (interconnected) bank(s) uses V_{CCO}, tie all associated V_{CCO} lines to 2.5V.
- In general, apply 2.5V to V_{CCO} Bank 4 from power-on to the end of configuration. Apply the same voltage to V_{CCO} Bank 5 during parallel configuration or a Readback operation. For information on how to program the FPGA using 3.3V signals and power, see the 3.3V-Tolerant Configuration Interface section.

If any of the standards assigned to the Inputs of the bank use V_{REF}, then observe the following additional rules:

- Connect *all* V_{REF} pins within the bank to the same voltage level.
- The V_{REF} levels used by all standards assigned to the Inputs of the bank must agree. The Xilinx development software checks for this. Tables 8 and 10 describe how different standards use the V_{REF} supply.

If none of the standards assigned to the Inputs of a bank use V_{REF} for biasing input switching thresholds, all associated V_{REF} pins function as User I/Os.

Exceptions to Banks Supporting I/O Standards

Bank 5 of any Spartan-3 device in a VQ100, CP132, or TQ144 package does not support DCI signal standards. In this case, bank 5 has neither VRN nor VRP pins.

Furthermore, banks 4 and 5 of any Spartan-3 device in a VQ100 package do not support signal standards using V_{REF} (see Table 8). In this case, the two banks do not have any V_{REF} pins.

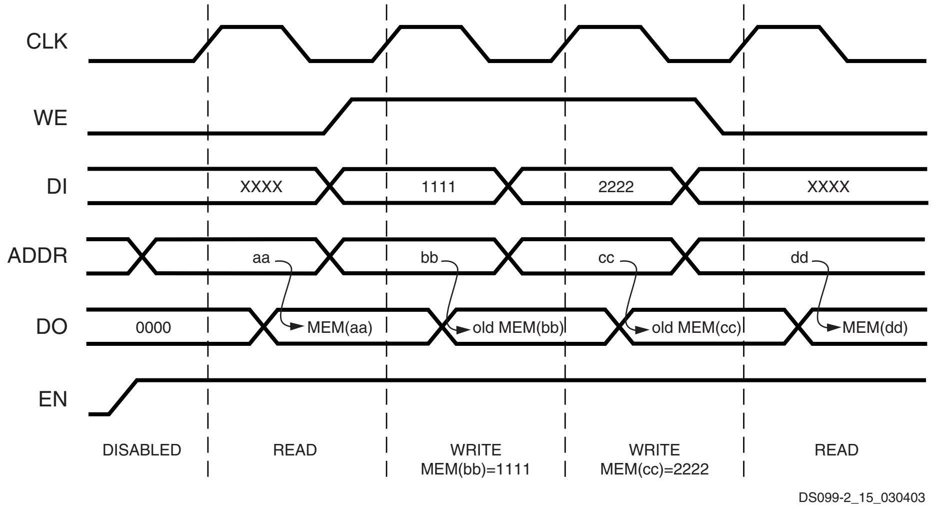


Figure 16: **Waveforms of Block RAM Data Operations with READ_FIRST Selected**

Choosing a third attribute called NO_CHANGE puts the DO outputs in a latched state when asserting WE. Under this condition, the DO outputs will retain the data driven just before WE was asserted. NO_CHANGE timing is shown in the portion of Figure 17 during which WE is High.

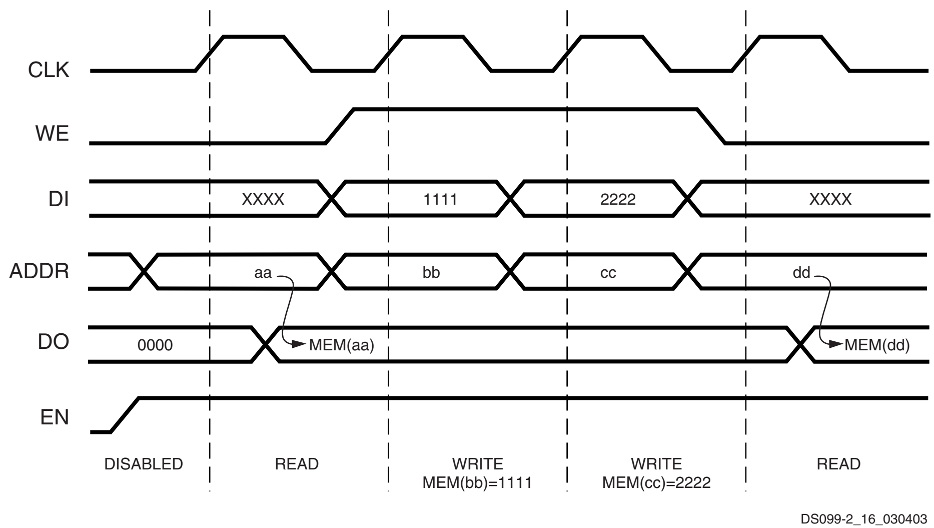


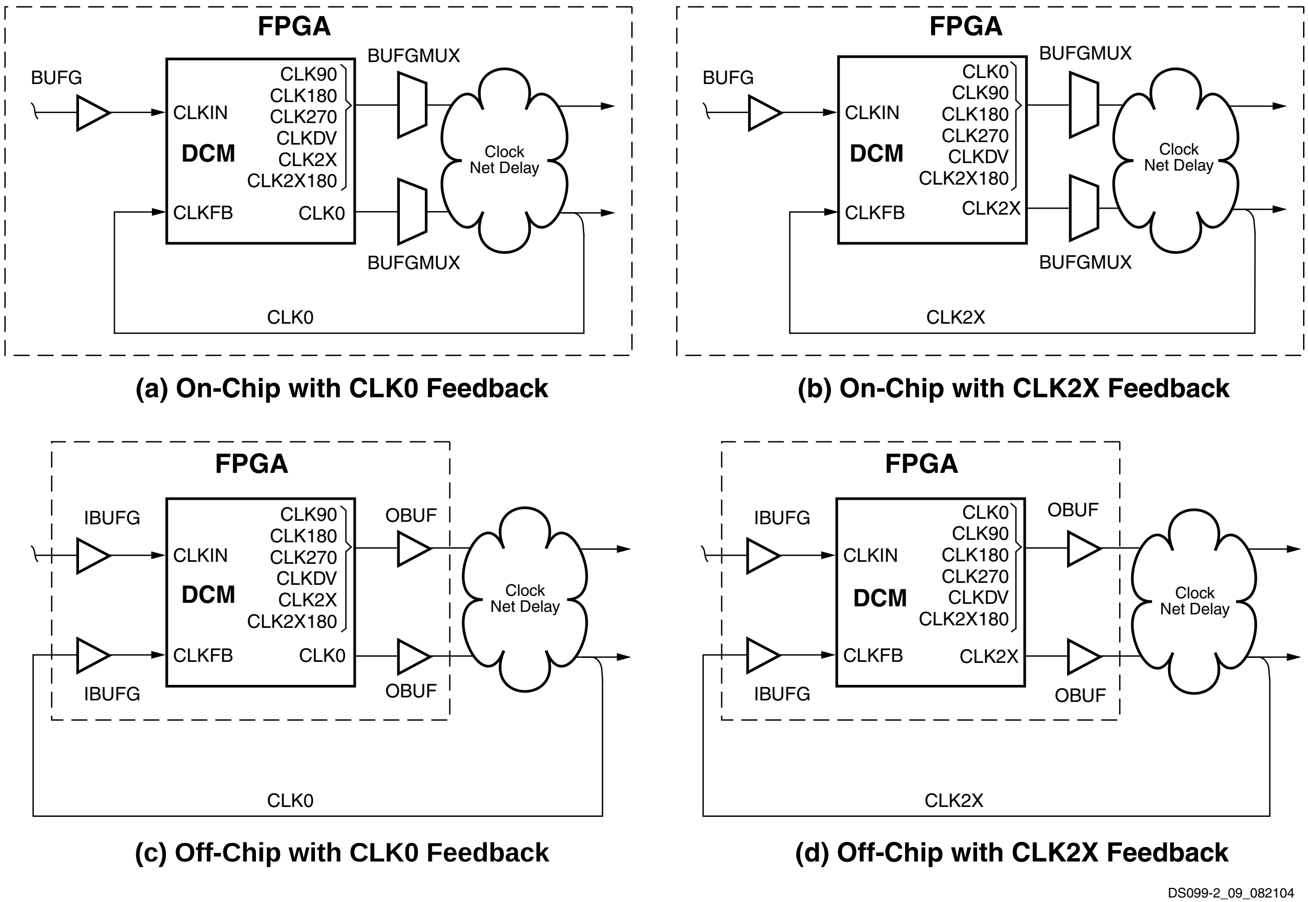
Figure 17: **Waveforms of Block RAM Data Operations with NO_CHANGE Selected**

Dedicated Multipliers

All Spartan-3 devices provide embedded multipliers that accept two 18-bit words as inputs to produce a 36-bit product. This section provides an introduction to multipliers. For further details, refer to the chapter entitled “Using Embedded Multipliers” in UG331.

The input buses to the multiplier accept data in two’s-complement form (either 18-bit signed or 17-bit unsigned). One such multiplier is matched to each block RAM on the die. The close physical proximity of the two ensures efficient data handling. Cascading multipliers permits multiplicands more than three in number as well as wider than 18-bits. The multiplier is placed in a design using one of two primitives: an asynchronous version called MULT18X18 and a version with a register called MULT18X18S, as shown in Figure 18. The signals for these primitives are defined in Table 15.

The CORE Generator system produces multipliers based on these primitives that can be configured to suit a wide range of requirements.



Notes:

1. In the Low Frequency mode, all seven DLL outputs are available. In the High Frequency mode, only the CLK0, CLK180, and CLKDV outputs are available.

Figure 21: **Input Clock, Output Clock, and Feedback Connections for the DLL**

In the on-chip synchronization case (the [a] and [b] sections of Figure 21), it is possible to connect any of the DLL's seven output clock signals through general routing resources to the FPGA's internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. As shown in the [a] section of Figure 21, the feedback loop is created by routing CLK0 (or CLK2X, in the [b] section) to a global clock net, which in turn drives the CLKFB input.

In the off-chip synchronization case (the [c] and [d] sections of Figure 21), CLK0 (or CLK2X) plus any of the DLL's other output clock signals exit the FPGA using output buffers (OBUF) to drive an external clock network plus registers on the board. As shown in the [c] section of Figure 21, the feedback loop is formed by feeding CLK0 (or CLK2X, in the [d] section) back into the FPGA using an IBUFG, which directly accesses the global clock network, or an IBUF. Then, the global clock net is connected directly to the CLKFB input.

DLL Frequency Modes

The DLL supports two distinct operating modes, High Frequency and Low Frequency, with each specified over a different clock frequency range. The DLL_FREQUENCY_MODE attribute chooses between the two modes. When the attribute is set to LOW, the Low Frequency mode permits all seven DLL clock outputs to operate over a low-to-moderate frequency range. When the attribute is set to HIGH, the High Frequency mode allows the CLK0, CLK180 and CLKDV outputs to operate at the highest possible frequencies. The remaining DLL clock outputs are not available for use in High Frequency mode.

Accommodating High Input Frequencies

If the frequency of the CLKIN signal is high such that it exceeds the maximum permitted, divide it down to an acceptable value using the CLKIN_DIVIDE_BY_2 attribute. When this attribute is set to TRUE, the CLKIN frequency is divided by a factor of two just as it enters the DCM.

Table 52: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	–	1.87	–	2.15	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	0.46	–	0.52	–	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.46	–	0.53	–	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.33	–	0.37	–	ns
Hold Times						
T_{DH}, T_{AH}, T_{WH}	Hold time of the BX, BY data inputs, the F/G address inputs, or the write enable input after the active transition at the CLK input of the distributed RAM	0	–	0	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.85	–	0.97	–	ns

Table 53: **CLB Shift Register Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	–	3.30	–	3.79	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.46	–	0.52	–	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0	–	0	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.85	–	0.97	–	ns

HSWAP_EN: Disable Pull-up Resistors During Configuration

As shown in Table 76, a Low on this asynchronous pin enables pull-up resistors on all user I/Os not actively involved in the configuration process, although only until device configuration completes. A High disables the pull-up resistors during configuration, which is the desired state for some applications.

The dedicated configuration CONFIG pins (CCLK, DONE, PROG_B, HSWAP_EN, M2, M1, M0), the JTAG pins (TDI, TMS, TCK, TDO) and the INIT_B always have active pull-up resistors during configuration, regardless of the value on HSWAP_EN.

After configuration, HSWAP_EN becomes a "don't care" input and any pull-up resistors previously enabled by HSWAP_EN are disabled. If a user I/O in the application requires a pull-up resistor after configuration, place a PULLUP primitive on the associated I/O pin or, for some pins, set the associated bitstream generator option.

Table 76: **HSWAP_EN Encoding**

HSWAP_EN	Function
During Configuration	
0	Enable pull-up resistors on all pins not actively involved in the configuration process. Pull-ups are only active until configuration completes. See Table 79.
1	No pull-up resistors during configuration.
After Configuration, User Mode	
X	This pin has no function except during device configuration.

Notes:
1. X = don't care, either 0 or 1.

The Bitstream generator option HswapenPin determines whether a pull-up resistor to VCCAUX, a pull-down resistor, or no resistor is present on HSWAP_EN after configuration.

JTAG: Dedicated JTAG Port Pins

Table 77: **JTAG Pin Descriptions**

Pin Name	Direction	Description	Bitstream Generation Option
TCK	Input	**Test Clock:** The TCK clock signal synchronizes all boundary scan operations on its rising edge.	The BitGen option **TckPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.
TDI	Input	**Test Data Input:** TDI is the serial data input for all JTAG instruction and data registers. This input is sampled on the rising edge of TCK.	The BitGen option **TdiPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.
TMS	Input	**Test Mode Select:** The TMS input controls the sequence of states through which the JTAG TAP state machine passes. This input is sampled on the rising edge of TCK.	The BitGen option **TmsPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.
TDO	Output	**Test Data Output:** The TDO pin is the data output for all JTAG instruction and data registers. This output is sampled on the rising edge of TCK. The TDO output is an active totem-pole driver and is not like the open-collector TDO output on Virtex®-II Pro FPGAs.	The BitGen option **TdoPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.

These pins are dedicated connections to the four-wire IEEE 1532/IEEE 1149.1 JTAG port, shown in Figure 43 and described in Table 77. The JTAG port is used for boundary-scan testing, device configuration, application debugging, and possibly an additional serial port for the application. These pins are dedicated and are not available as user-I/O pins. Every package has four dedicated JTAG pins and these pins are powered by the +2.5V VCCAUX supply.

For additional information on JTAG configuration, see Boundary-Scan (JTAG) Mode, page 50.

Table 79: **Pin Behavior After Power-Up, During Configuration *(Cont'd)***

Pin Name	Configuration Mode Settings <M2:M1:M0>					Bitstream Configuration Option
	Serial Modes		SelectMap Parallel Modes		JTAG Mode <1:0:1>	
	Master <0:0:0>	Slave <1:1:1>	Master <0:1:1>	Slave <1:1:0>		
VCCO: I/O bank output voltage supply pins						
VCCO_4 (for DUAL pins)	Same voltage as external interface	Same voltage as external interface	Same voltage as external interface	Same voltage as external interface	VCCO_4	N/A
VCCO_5 (for DUAL pins)	VCCO_5	VCCO_5	Same voltage as external interface	Same voltage as external interface	VCCO_5	N/A
VCCO_#	VCCO_#	VCCO_#	VCCO_#	VCCO_#	VCCO_#	N/A
VCCAUX: Auxiliary voltage supply pins						
VCCAUX	+2.5V	+2.5V	+2.5V	+2.5V	+2.5V	N/A
VCCINT: Internal core voltage supply pins						
VCCINT	+1.2V	+1.2V	+1.2V	+1.2V	+1.2V	N/A
GND: Ground supply pins						
GND	GND	GND	GND	GND	GND	N/A

Notes:

1. #= I/O bank number, an integer from 0 to 7.
2. (I) = input, (O) = output, (OD) = open-drain output, (I/O) = bidirectional, (I/OD) = bidirectional with open-drain output. Open-drain output requires pull-up to create logic High level.
3. Shaded cell indicates that the pin is high-impedance during configuration. To enable a soft pull-up resistor during configuration, drive or tie HSWAP_EN Low.

Bitstream Options

Table 80 lists the various bitstream options that affect pins on a Spartan-3 FPGA. The table shows the names of the affected pins, describes the function of the bitstream option, the name of the bitstream generator option variable, and the legal values for each variable. The default option setting for each variable is indicated with bold, underlined text.

Table 80: **Bitstream Options Affecting Spartan-3 Device Pins**

Affected Pin Name(s)	Bitstream Generation Function	Option Variable Name	Values (**Default**)
All unused I/O pins of type I/O, DUAL, GCLK, DCI, VREF	For all I/O pins that are unused in the application after configuration, this option defines whether the I/Os are individually tied to VCCO via a pull-up resistor, tied ground via a pull-down resistor, or left floating. If left floating, the unused pins should be connected to a defined logic level, either from a source internal to the FPGA or external.	UnusedPin	• **Pulldown** • Pullup • Pullnone
IO_Lxxy_#/DIN, IO_Lxxy_#/DOUT, IO_Lxxy_#/INIT_B	Serial configuration mode: If set to Yes, then these pins retain their functionality after configuration completes, allowing for device (re-)configuration. Readback is not supported in with serial mode.	Persist	• **No** • Yes
IO_Lxxy_#/D0, IO_Lxxy_#/D1, IO_Lxxy_#/D2, IO_Lxxy_#/D3, IO_Lxxy_#/D4, IO_Lxxy_#/D5, IO_Lxxy_#/D6, IO_Lxxy_#/D7, IO_Lxxy_#/CS_B, IO_Lxxy_#/RDWR_B, IO_Lxxy_#/BUSY, IO_Lxxy_#/INIT_B	Parallel configuration mode (also called SelectMAP): If set to Yes, then these pins retain their SelectMAP functionality after configuration completes, allowing for device readback and for partial or complete (re-)configuration.	Persist	• **No** • Yes

Table 89: **CP132 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	CP132 Ball	Type
6	IO_L22N_6	K1	I/O
6	IO_L22P_6	J3	I/O
6	IO_L23N_6	J2	I/O
6	IO_L23P_6	J1	I/O
6	IO_L24N_6/VREF_6	H3	VREF
6	IO_L24P_6	H2	I/O
6	IO_L40N_6	H1	I/O
6	IO_L40P_6/VREF_6	G3	VREF
7	IO_L01N_7/VRP_7	B2	DCI
7	IO_L01P_7/VRN_7	B1	DCI
7	IO_L21N_7	C1	I/O
7	IO_L21P_7	D3	I/O
7	IO_L22N_7	D1	I/O
7	IO_L22P_7	D2	I/O
7	IO_L23N_7	E2	I/O
7	IO_L23P_7	E3	I/O
7	IO_L24N_7	F3	I/O
7	IO_L24P_7	E1	I/O
7	IO_L40N_7/VREF_7	G1	VREF
7	IO_L40P_7	F2	I/O
0,1	VCCO_TOP	B12	VCCO
0,1	VCCO_TOP	A4	VCCO
0,1	VCCO_TOP	B8	VCCO
2,3	VCCO_RIGHT	D13	VCCO
2,3	VCCO_RIGHT	H13	VCCO
2,3	VCCO_RIGHT	M12	VCCO
4,5	VCCO_BOTTOM	N7	VCCO
4,5	VCCO_BOTTOM	P11	VCCO
4,5	VCCO_BOTTOM	N3	VCCO
6,7	VCCO_LEFT	G2	VCCO
6,7	VCCO_LEFT	L2	VCCO
6,7	VCCO_LEFT	C3	VCCO
N/A	GND	B4	GND
N/A	GND	B9	GND
N/A	GND	C2	GND
N/A	GND	C12	GND
N/A	GND	D14	GND
N/A	GND	F1	GND
N/A	GND	J14	GND
N/A	GND	L1	GND

Table 91: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
2	IO_L23N_2/VREF_2	P98	VREF
2	IO_L23P_2	P97	I/O
2	IO_L24N_2	P96	I/O
2	IO_L24P_2	P95	I/O
2	IO_L40N_2	P93	I/O
2	IO_L40P_2/VREF_2	P92	VREF
3	IO	P76	I/O
3	IO_L01N_3/VRP_3	P74	DCI
3	IO_L01P_3/VRN_3	P73	DCI
3	IO_L20N_3	P78	I/O
3	IO_L20P_3	P77	I/O
3	IO_L21N_3	P80	I/O
3	IO_L21P_3	P79	I/O
3	IO_L22N_3	P83	I/O
3	IO_L22P_3	P82	I/O
3	IO_L23N_3	P85	I/O
3	IO_L23P_3/VREF_3	P84	VREF
3	IO_L24N_3	P87	I/O
3	IO_L24P_3	P86	I/O
3	IO_L40N_3/VREF_3	P90	VREF
3	IO_L40P_3	P89	I/O
4	IO/VREF_4	P70	VREF
4	IO_L01N_4/VRP_4	P69	DCI
4	IO_L01P_4/VRN_4	P68	DCI
4	IO_L27N_4/DIN/D0	P65	DUAL
4	IO_L27P_4/D1	P63	DUAL
4	IO_L30N_4/D2	P60	DUAL
4	IO_L30P_4/D3	P59	DUAL
4	IO_L31N_4/INIT_B	P58	DUAL
4	IO_L31P_4/DOUT/BUSY	P57	DUAL
4	IO_L32N_4/GCLK1	P56	GCLK
4	IO_L32P_4/GCLK0	P55	GCLK
5	IO/VREF_5	P44	VREF
5	IO_L01N_5/RDWR_B	P41	DUAL
5	IO_L01P_5/CS_B	P40	DUAL
5	IO_L28N_5/D6	P47	DUAL
5	IO_L28P_5/D7	P46	DUAL
5	IO_L31N_5/D4	P51	DUAL
5	IO_L31P_5/D5	P50	DUAL
5	IO_L32N_5/GCLK3	P53	GCLK

Table 93: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
7	IO_L21N_7	IO_L21N_7	P13	I/O
7	IO_L21P_7	IO_L21P_7	P12	I/O
7	IO_L22N_7	IO_L22N_7	P16	I/O
7	IO_L22P_7	IO_L22P_7	P15	I/O
7	IO_L23N_7	IO_L23N_7	P19	I/O
7	IO_L23P_7	IO_L23P_7	P18	I/O
7	IO_L24N_7	IO_L24N_7	P21	I/O
7	IO_L24P_7	IO_L24P_7	P20	I/O
7	N.C. (◆)	IO_L39N_7	P24	I/O
7	N.C. (◆)	IO_L39P_7	P22	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	P27	VREF
7	IO_L40P_7	IO_L40P_7	P26	I/O
7	VCCO_7	VCCO_7	P6	VCCO
7	VCCO_7	VCCO_7	P23	VCCO
N/A	GND	GND	P1	GND
N/A	GND	GND	P186	GND
N/A	GND	GND	P195	GND
N/A	GND	GND	P202	GND
N/A	GND	GND	P163	GND
N/A	GND	GND	P170	GND
N/A	GND	GND	P179	GND
N/A	GND	GND	P134	GND
N/A	GND	GND	P145	GND
N/A	GND	GND	P151	GND
N/A	GND	GND	P157	GND
N/A	GND	GND	P112	GND
N/A	GND	GND	P118	GND
N/A	GND	GND	P129	GND
N/A	GND	GND	P82	GND
N/A	GND	GND	P91	GND
N/A	GND	GND	P99	GND
N/A	GND	GND	P105	GND
N/A	GND	GND	P53	GND
N/A	GND	GND	P59	GND
N/A	GND	GND	P66	GND
N/A	GND	GND	P75	GND
N/A	GND	GND	P30	GND
N/A	GND	GND	P41	GND
N/A	GND	GND	P47	GND
N/A	GND	GND	P8	GND

FT256: 256-lead Fine-pitch Thin Ball Grid Array

The 256-lead fine-pitch thin ball grid array package, FT256, supports three different Spartan-3 devices, including the XC3S200, the XC3S400, and the XC3S1000. The footprints for all three devices are identical, as shown in Table 96 and Figure 49.

All the package pins appear in Table 96 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 96: **FT256 Package Pinout**

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
0	IO	A5	I/O
0	IO	A7	I/O
0	IO/VREF_0	A3	VREF
0	IO/VREF_0	D5	VREF
0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L25N_0	C5	I/O
0	IO_L25P_0	B5	I/O
0	IO_L27N_0	E6	I/O
0	IO_L27P_0	D6	I/O
0	IO_L28N_0	C6	I/O
0	IO_L28P_0	B6	I/O
0	IO_L29N_0	E7	I/O
0	IO_L29P_0	D7	I/O
0	IO_L30N_0	C7	I/O
0	IO_L30P_0	B7	I/O
0	IO_L31N_0	D8	I/O
0	IO_L31P_0/VREF_0	C8	VREF
0	IO_L32N_0/GCLK7	B8	GCLK
0	IO_L32P_0/GCLK6	A8	GCLK
0	VCCO_0	E8	VCCO
0	VCCO_0	F7	VCCO
0	VCCO_0	F8	VCCO
1	IO	A9	I/O
1	IO	A12	I/O
1	IO	C10	I/O
1	IO/VREF_1	D12	VREF
1	IO_L01N_1/VRP_1	A14	DCI
1	IO_L01P_1/VRN_1	B14	DCI

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
7	IO_L24P_7	G4	I/O
7	IO_L39N_7	H3	I/O
7	IO_L39P_7	H4	I/O
7	IO_L40N_7/VREF_7	H1	VREF
7	IO_L40P_7	G1	I/O
7	VCCO_7	G6	VCCO
7	VCCO_7	H5	VCCO
7	VCCO_7	H6	VCCO
N/A	GND	A1	GND
N/A	GND	A16	GND
N/A	GND	B2	GND
N/A	GND	B9	GND
N/A	GND	B15	GND
N/A	GND	F6	GND
N/A	GND	F11	GND
N/A	GND	G7	GND
N/A	GND	G8	GND
N/A	GND	G9	GND
N/A	GND	G10	GND
N/A	GND	H2	GND
N/A	GND	H7	GND
N/A	GND	H8	GND
N/A	GND	H9	GND
N/A	GND	H10	GND
N/A	GND	J7	GND
N/A	GND	J8	GND
N/A	GND	J9	GND
N/A	GND	J10	GND
N/A	GND	J15	GND
N/A	GND	K7	GND
N/A	GND	K8	GND
N/A	GND	K9	GND
N/A	GND	K10	GND
N/A	GND	L6	GND
N/A	GND	L11	GND
N/A	GND	R2	GND
N/A	GND	R8	GND
N/A	GND	R15	GND
N/A	GND	T1	GND

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	M25	VREF
2	IO_L34P_2	IO_L34P_2	IO_L34P_2	IO_L34P_2	IO_L34P_2	M26	I/O
2	IO_L35N_2	IO_L35N_2	IO_L35N_2	IO_L35N_2	IO_L35N_2	N19	I/O
2	IO_L35P_2	IO_L35P_2	IO_L35P_2	IO_L35P_2	IO_L35P_2	N20	I/O
2	IO_L38N_2	IO_L38N_2	IO_L38N_2	IO_L38N_2	IO_L38N_2	N21	I/O
2	IO_L38P_2	IO_L38P_2	IO_L38P_2	IO_L38P_2	IO_L38P_2	N22	I/O
2	IO_L39N_2	IO_L39N_2	IO_L39N_2	IO_L39N_2	IO_L39N_2	N23	I/O
2	IO_L39P_2	IO_L39P_2	IO_L39P_2	IO_L39P_2	IO_L39P_2	N24	I/O
2	IO_L40N_2	IO_L40N_2	IO_L40N_2	IO_L40N_2	IO_L40N_2	N25	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	N26	VREF
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	G24	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	J19	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	K19	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	L18	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	L24	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	M18	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	N17	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	N18	VCCO
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	AA22	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	AA21	DCI
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	AB24	VREF
3	IO_L02P_3	IO_L02P_3	IO_L02P_3	IO_L02P_3	IO_L02P_3	AB23	I/O
3	IO_L03N_3	IO_L03N_3	IO_L03N_3	IO_L03N_3	IO_L03N_3	AC26	I/O
3	IO_L03P_3	IO_L03P_3	IO_L03P_3	IO_L03P_3	IO_L03P_3	AC25	I/O
3	N.C. (◆)	IO_L05N_3	IO_L05N_3	IO_L05N_3	IO_L05N_3	Y21	I/O
3	N.C. (◆)	IO_L05P_3	IO_L05P_3	IO_L05P_3	IO_L05P_3	Y20	I/O
3	N.C. (◆)	IO_L06N_3	IO_L06N_3	IO_L06N_3	IO_L06N_3	AB26	I/O
3	N.C. (◆)	IO_L06P_3	IO_L06P_3	IO_L06P_3	IO_L06P_3	AB25	I/O
3	N.C. (◆)	IO_L07N_3	IO_L07N_3	IO_L07N_3	IO_L07N_3	AA24	I/O
3	N.C. (◆)	IO_L07P_3	IO_L07P_3	IO_L07P_3	IO_L07P_3	AA23	I/O
3	N.C. (◆)	IO_L08N_3	IO_L08N_3	IO_L08N_3	IO_L08N_3	Y23	I/O
3	N.C. (◆)	IO_L08P_3	IO_L08P_3	IO_L08P_3	IO_L08P_3	Y22	I/O
3	N.C. (◆)	IO_L09N_3	IO_L09N_3	IO_L09N_3	IO_L09N_3	AA26	I/O
3	N.C. (◆)	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	AA25	VREF
3	N.C. (◆)	IO_L10N_3	IO_L10N_3	IO_L10N_3	IO_L10N_3	W21	I/O
3	N.C. (◆)	IO_L10P_3	IO_L10P_3	IO_L10P_3	IO_L10P_3	W20	I/O
3	IO_L14N_3	IO_L14N_3	IO_L14N_3	IO_L14N_3	IO_L14N_3	Y26	I/O
3	IO_L14P_3	IO_L14P_3	IO_L14P_3	IO_L14P_3	IO_L14P_3	Y25	I/O
3	IO_L16N_3	IO_L16N_3	IO_L16N_3	IO_L16N_3	IO_L16N_3	V21	I/O
3	IO_L16P_3	IO_L16P_3	IO_L16P_3	IO_L16P_3	IO_L16P_3	W22	I/O
3	IO_L17N_3	IO_L17N_3	IO_L17N_3	IO_L17N_3	IO_L17N_3	W24	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	W23	VREF

User I/Os by Bank

Table 104 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1000 in the FG676 package. Similarly, Table 105 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1500 in the FG676 package. Finally, Table 106 shows the same information for the XC3S2000, XC3S4000, and XC3S5000 in the FG676 package.

Table 104: **User I/Os Per Bank for XC3S1000 in FG676 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	49	40	0	2	5	2
	1	50	41	0	2	5	2
Right	2	48	41	0	2	5	0
	3	48	41	0	2	5	0
Bottom	4	50	35	6	2	5	2
	5	50	35	6	2	5	2
Left	6	48	41	0	2	5	0
	7	48	41	0	2	5	0

Table 105: **User I/Os Per Bank for XC3S1500 in FG676 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	62	52	0	2	6	2
	1	61	51	0	2	6	2
Right	2	60	52	0	2	6	0
	3	60	52	0	2	6	0
Bottom	4	63	47	6	2	6	2
	5	61	45	6	2	6	2
Left	6	60	52	0	2	6	0
	7	60	52	0	2	6	0

Table 106: **User I/Os Per Bank for XC3S2000, XC3S4000, and XC3S5000 in FG676 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	62	52	0	2	6	2
	1	61	51	0	2	6	2
Right	2	61	53	0	2	6	0
	3	60	52	0	2	6	0
Bottom	4	63	47	6	2	6	2
	5	61	45	6	2	6	2
Left	6	61	53	0	2	6	0
	7	60	52	0	2	6	0

Right Half of Package (Top View)

Bank 1 (top, columns 14–23) · Bank 2 (right, rows A–N) · Bank 3 (right, rows P–AC) · Bank 4 (bottom, columns 14–24)

	14	15	16	17	18	19	20	21	22	23	24	25	26
A	I/O	I/O L29N_1	I/O L26N_1 ◆	I/O L23N_1 ◆	VCCAUX	I/O L15N_1	I/O L10N_1 VREF_1	I/O L08N_1	I/O	I/O	TMS	VCCAUX	GND
B	I/O L32N_1 GCLK5	I/O L29P_1	I/O L26P_1 ◆	I/O L23P_1 ◆	I/O L18N_1 ◆	I/O L15P_1	I/O L10P_1	I/O L08P_1	I/O L06N_1 VREF_1	I/O L04N_1	TCK	GND	VCCAUX
C	I/O L32P_1 GCLK4	I/O VREF_1	VCCO_1	I/O VREF_1	I/O L18P_1 ◆	I/O L12N_1 ◆	VCCO_1	I/O L07N_1	I/O L06P_1	I/O L04P_1	GND	I/O L01N_2 VRP_2	I/O L01P_2 VRN_2
D	I/O L31N_1 VREF_1	GND	I/O	I/O L22N_1	I/O VREF_1 ◆	I/O L12P_1 ◆	I/O L09N_1	I/O L07P_1	I/O L01N_1 VRP_1	GND	TDO	I/O L03N_2 VREF_2	I/O L03P_2
E	I/O L31P_1	I/O L28N_1	I/O L25N_1	I/O L22P_1	I/O	I/O L11N_1 ◆	I/O L09P_1	I/O L05N_1	I/O L01P_1 VRN_1	I/O L02N_2	I/O L02P_2	I/O L05N_2 ◆	I/O L05P_2 ◆
F	I/O	I/O L28P_1	I/O L25P_1	I/O L19N_1	I/O L16N_1	I/O L11P_1 ◆	I/O	I/O L05P_1	I/O ◆■	I/O L07N_2 ◆	I/O L07P_2 ◆	I/O L09N_2 VREF_2 ◆	I/O L09P_2 ◆
G	I/O L30N_1	I/O L27N_1	I/O L24N_1	I/O L19P_1	I/O L16P_1	I/O	I/O L06N_2 ◆	I/O L06P_2 ◆	I/O L08N_2 ◆	I/O L08P_2 ◆	VCCO_2	I/O L10N_2 ◆	I/O L10P_2 ◆
H	I/O L30P_1	I/O L27P_1	I/O L24P_1	VCCO_1	VCCO_1	VCCINT	I/O L14N_2 (L11N_2)	I/O L14P_2 (L11P_2)	I/O L16N_2 (L12N_2)	I/O L17N_2 (L13N_2)	I/O L17P_2 (L13P_2) VREF_2	I/O L19N_2	I/O L19P_2
J	VCCO_1	VCCO_1	VCCO_1	VCCINT	VCCINT	VCCO_2	I/O L20N_2	I/O L16P_2 (L12P_2)	I/O L21N_2	I/O L21P_2	I/O L22N_2	I/O L22P_2	VCCAUX
K	VCCO_1	GND	GND	VCCINT	VCCINT	VCCO_2	I/O L20P_2	I/O L23N_2 VREF_2	I/O L23P_2	I/O L24N_2	I/O L24P_2	I/O L26N_2	I/O L26P_2
L	GND	GND	GND	GND	VCCO_2	I/O L27N_2	I/O L27P_2	I/O L28N_2	I/O L28P_2	I/O L33N_2	VCCO_2	I/O L29N_2	I/O L29P_2
M	GND	GND	GND	GND	VCCO_2	I/O L31N_2	I/O L31P_2	I/O L32N_2	I/O L32P_2	GND	I/O L33P_2	I/O L34N_2 VREF_2	I/O L34P_2
N	GND	GND	GND	VCCO_2	VCCO_2	I/O L35N_2	I/O L35P_2	I/O L38N_2	I/O L38P_2	I/O L39N_2	I/O L39P_2	I/O L40N_2	I/O L40P_2 VREF_2
P	GND	GND	GND	VCCO_3	VCCO_3	I/O L35P_3	I/O L35N_3	I/O L38P_3	I/O L38N_3	I/O L39P_3	I/O L39N_3	I/O L40P_3	I/O L40N_3 VREF_3
R	GND	GND	GND	GND	VCCO_3	I/O L31P_3	I/O L31N_3	I/O L32P_3	I/O L32N_3	GND	I/O L33N_3	I/O L34P_3 VREF_3	I/O L34N_3
T	GND	GND	GND	GND	VCCO_3	I/O L27P_3	I/O L27N_3	I/O L28P_3	I/O L28N_3	I/O L33P_3	VCCO_3	I/O L29P_3	I/O L29N_3
U	VCCO_4	GND	GND	VCCINT	VCCINT	VCCO_3	I/O L20N_3	I/O L23P_3 VREF_3	I/O L23N_3	I/O L24P_3	I/O L24N_3	I/O L26P_3	I/O L26N_3
V	VCCO_4	VCCO_4	VCCO_4	VCCINT	VCCINT	VCCO_3	I/O L20P_3	I/O L16N_3	I/O L21P_3	I/O L21N_3	I/O L22P_3	I/O L22N_3	VCCAUX
W	I/O L27P_4 D1	I/O	I/O	VCCO_4	VCCO_4	VCCINT	I/O L10P_3 ◆	I/O L10N_3 ◆	I/O L16P_3	I/O L17P_3 VREF_3	I/O L17N_3	I/O L19P_3	I/O L19N_3
Y	I/O L30N_4 D2	I/O L27N_4 DIN D0	I/O L24N_4	I/O VREF_4	I/O L16N_4	I/O L11N_4 ◆	I/O L05P_3 ◆	I/O L05N_3 ◆	I/O L08P_3 ◆	I/O L08N_3 ◆	VCCO_3	I/O L14P_3	I/O L14N_3
AA	I/O L30P_4 D3	I/O L28N_4	I/O L24P_4	I/O L19P_4	I/O L16P_4	I/O L11P_4 ◆	I/O	I/O L01P_3 VRN_3	I/O L01N_3 VRP_3	I/O L07P_3 ◆	I/O L07N_3 ◆	I/O L09P_3 VREF_3 ◆	I/O L09N_3 ◆
AB	IO VREF_4	I/O L28P_4	I/O L25N_4	I/O L22P_4	I/O L17N_4 ◆	I/O L12N_4 ◆	I/O L09N_4	I/O L07N_4	I/O L01N_4 VRP_4	I/O L02P_3	I/O L02N_3 VREF_3	I/O L06P_3 ◆	I/O L06N_3 ◆
AC	I/O L31N_4 INIT_B	GND	I/O L25P_4	I/O L19N_4	I/O L17P_4 ◆	I/O L12P_4 ◆	I/O L09P_4	I/O L07P_4	I/O L01P_4 VRN_4	GND	DONE	I/O L03P_3	I/O L03N_3
AD	I/O L31P_4 DOUT BUSY	I/O	VCCO_4	I/O L22N_4 VREF_4	I/O L18N_4 ◆	I/O ◆	VCCO_4	I/O L08N_4	I/O L06N_4 VREF_4	I/O	GND	I/O VREF_4	CCLK
AE	I/O L32N_4 GCLK1	I/O L29N_4	I/O L26N_4 ◆	I/O L23N_4 ◆	I/O L18P_4 ◆	I/O L15N_4	I/O L10N_4	I/O L08P_4	I/O L06P_4	I/O L05N_4	I/O L04N_4	GND	VCCAUX
AF	I/O L32P_4 GCLK0	I/O L29P_4	I/O L26P_4 VREF_4 ◆	I/O L23P_4 ◆	VCCAUX	I/O L15P_4	I/O L10P_4	I/O	I/O	I/O L05P_4	I/O L04P_4	VCCAUX	GND

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Figure 54: FG676 Package Footprint (Top View) Continued

Notes:

1. Differential pair assignments shown in parentheses on balls H20, H21, H22, H23, H24, and J21 are for XC3S4000 only.
2. Differential pair assignments for the XC3S5000 are different on 15 balls (see Table 103 for details.)

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO_L30N_0	IO_L30N_0	G15	I/O
0	IO_L30P_0	IO_L30P_0	F15	I/O
0	IO_L31N_0	IO_L31N_0	D15	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C15	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B15	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A15	GCLK
0	N.C. (◆)	IO_L35N_0	B7	I/O
0	N.C. (◆)	IO_L35P_0	A7	I/O
0	N.C. (◆)	IO_L36N_0	G7	I/O
0	N.C. (◆)	IO_L36P_0	H8	I/O
0	N.C. (◆)	IO_L37N_0	E9	I/O
0	N.C. (◆)	IO_L37P_0	D9	I/O
0	N.C. (◆)	IO_L38N_0	B9	I/O
0	N.C. (◆)	IO_L38P_0	A9	I/O
0	VCCO_0	VCCO_0	C5	VCCO
0	VCCO_0	VCCO_0	E7	VCCO
0	VCCO_0	VCCO_0	C9	VCCO
0	VCCO_0	VCCO_0	G9	VCCO
0	VCCO_0	VCCO_0	J11	VCCO
0	VCCO_0	VCCO_0	L12	VCCO
0	VCCO_0	VCCO_0	C13	VCCO
0	VCCO_0	VCCO_0	G13	VCCO
0	VCCO_0	VCCO_0	L13	VCCO
0	VCCO_0	VCCO_0	L14	VCCO
1	IO	IO	E25	I/O
1	IO	IO	J21	I/O
1	IO	IO	K20	I/O
1	IO	IO	F18	I/O
1	IO	IO	F16	I/O
1	IO	IO	A16	I/O
1	IO/VREF_1	IO/VREF_1	J17	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	A27	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B27	DCI
1	IO_L02N_1	IO_L02N_1	D26	I/O
1	IO_L02P_1	IO_L02P_1	C27	I/O
1	IO_L03N_1	IO_L03N_1	A26	I/O
1	IO_L03P_1	IO_L03P_1	B26	I/O
1	IO_L04N_1	IO_L04N_1	B25	I/O
1	IO_L04P_1	IO_L04P_1	C25	I/O
1	IO_L05N_1	IO_L05N_1	F24	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
4	IO_L31P_4/DOUT/BUSY	IO_L31P_4/DOUT/BUSY	AH16	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	AJ16	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	AK16	GCLK
4	N.C. (◆)	IO_L33N_4	AH25	I/O
4	N.C. (◆)	IO_L33P_4	AJ25	I/O
4	N.C. (◆)	IO_L34N_4	AE25	I/O
4	N.C. (◆)	IO_L34P_4	AE24	I/O
4	N.C. (◆)	IO_L35N_4	AG24	I/O
4	N.C. (◆)	IO_L35P_4	AH24	I/O
4	N.C. (◆)	IO_L38N_4	AJ24	I/O
4	N.C. (◆)	IO_L38P_4	AK24	I/O
4	VCCO_4	VCCO_4	Y17	VCCO
4	VCCO_4	VCCO_4	Y18	VCCO
4	VCCO_4	VCCO_4	AD18	VCCO
4	VCCO_4	VCCO_4	AH18	VCCO
4	VCCO_4	VCCO_4	Y19	VCCO
4	VCCO_4	VCCO_4	AB20	VCCO
4	VCCO_4	VCCO_4	AD22	VCCO
4	VCCO_4	VCCO_4	AH22	VCCO
4	VCCO_4	VCCO_4	AF24	VCCO
4	VCCO_4	VCCO_4	AH26	VCCO
5	IO	IO	AE6	I/O
5	IO	IO	AB10	I/O
5	IO	IO	AA11	I/O
5	IO	IO	AA15	I/O
5	IO	IO	AE15	I/O
5	IO/VREF_5	IO/VREF_5	AH4	VREF
5	IO/VREF_5	IO/VREF_5	AK15	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	AK4	DUAL
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AJ4	DUAL
5	IO_L02N_5	IO_L02N_5	AK5	I/O
5	IO_L02P_5	IO_L02P_5	AJ5	I/O
5	IO_L03N_5	IO_L03N_5	AF6	I/O
5	IO_L03P_5	IO_L03P_5	AG5	I/O
5	IO_L04N_5	IO_L04N_5	AJ6	I/O
5	IO_L04P_5	IO_L04P_5	AH6	I/O
5	IO_L05N_5	IO_L05N_5	AE7	I/O
5	IO_L05P_5	IO_L05P_5	AD7	I/O
5	IO_L06N_5	IO_L06N_5	AH7	I/O
5	IO_L06P_5	IO_L06P_5	AG7	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L48P_3	IO_L48P_3	AB24	I/O
3	N.C. (◆)	IO_L49N_3	AA26	I/O
3	N.C. (◆)	IO_L49P_3	AA25	I/O
3	IO_L50N_3	IO_L50N_3	Y25	I/O
3	IO_L50P_3	IO_L50P_3	Y24	I/O
3	N.C. (◆)	IO_L51N_3	V24	I/O
3	N.C. (◆)	IO_L51P_3	W24	I/O
3	VCCO_3	VCCO_3	AA23	VCCO
3	VCCO_3	VCCO_3	AB23	VCCO
3	VCCO_3	VCCO_3	AB29	VCCO
3	VCCO_3	VCCO_3	AB33	VCCO
3	VCCO_3	VCCO_3	AD27	VCCO
3	VCCO_3	VCCO_3	AD31	VCCO
3	VCCO_3	VCCO_3	AG28	VCCO
3	VCCO_3	VCCO_3	AG32	VCCO
3	VCCO_3	VCCO_3	AL32	VCCO
3	VCCO_3	VCCO_3	W23	VCCO
3	VCCO_3	VCCO_3	W31	VCCO
3	VCCO_3	VCCO_3	Y23	VCCO
3	VCCO_3	VCCO_3	Y27	VCCO
4	IO	IO	AD18	I/O
4	IO	IO	AD19	I/O
4	IO	IO	AD20	I/O
4	IO	IO	AD22	I/O
4	IO	IO	AE18	I/O
4	IO	IO	AE19	I/O
4	IO	IO	AE22	I/O
4	N.C. (◆)	IO	AE24	I/O
4	IO	IO	AF24	I/O
4	N.C. (◆)	IO	AF26	I/O
4	IO	IO	AG26	I/O
4	IO	IO	AG27	I/O
4	IO	IO	AJ27	I/O
4	IO	IO	AJ29	I/O
4	IO	IO	AK25	I/O
4	IO	IO	AN26	I/O
4	IO/VREF_4	IO/VREF_4	AF21	VREF
4	IO/VREF_4	IO/VREF_4	AH23	VREF
4	IO/VREF_4	IO/VREF_4	AK18	VREF
4	IO/VREF_4	IO/VREF_4	AL30	VREF

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
4	VCCO_4	VCCO_4	AC19	VCCO
4	VCCO_4	VCCO_4	AC20	VCCO
4	VCCO_4	VCCO_4	AC21	VCCO
4	VCCO_4	VCCO_4	AC22	VCCO
4	VCCO_4	VCCO_4	AG20	VCCO
4	VCCO_4	VCCO_4	AG24	VCCO
4	VCCO_4	VCCO_4	AH27	VCCO
4	VCCO_4	VCCO_4	AJ22	VCCO
4	VCCO_4	VCCO_4	AL19	VCCO
4	VCCO_4	VCCO_4	AL24	VCCO
4	VCCO_4	VCCO_4	AM27	VCCO
4	VCCO_4	VCCO_4	AM31	VCCO
4	VCCO_4	VCCO_4	AN22	VCCO
5	IO	IO	AD11	I/O
5	N.C. (◆)	IO	AD12	I/O
5	IO	IO	AD14	I/O
5	IO	IO	AD15	I/O
5	IO	IO	AD16	I/O
5	IO	IO	AD17	I/O
5	IO	IO	AE14	I/O
5	IO	IO	AE16	I/O
5	N.C. (◆)	IO	AF9	I/O
5	IO	IO	AG9	I/O
5	IO	IO	AG12	I/O
5	IO	IO	AJ6	I/O
5	IO	IO	AJ17	I/O
5	IO	IO	AK10	I/O
5	IO	IO	AK14	I/O
5	IO	IO	AM12	I/O
5	IO	IO	AN9	I/O
5	IO/VREF_5	IO/VREF_5	AJ8	VREF
5	IO/VREF_5	IO/VREF_5	AL5	VREF
5	IO/VREF_5	IO/VREF_5	AP17	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	AP3	DUAL
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AN3	DUAL
5	IO_L02N_5	IO_L02N_5	AP4	I/O
5	IO_L02P_5	IO_L02P_5	AN4	I/O
5	IO_L03N_5	IO_L03N_5	AN5	I/O
5	IO_L03P_5	IO_L03P_5	AM5	I/O
5	IO_L04N_5	IO_L04N_5	AM6	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
6	IO_L37N_6	IO_L37N_6	W3	I/O
6	IO_L37P_6	IO_L37P_6	W2	I/O
6	IO_L38N_6	IO_L38N_6	V6	I/O
6	IO_L38P_6	IO_L38P_6	V5	I/O
6	IO_L39N_6	IO_L39N_6	V4	I/O
6	IO_L39P_6	IO_L39P_6	V3	I/O
6	IO_L40N_6	IO_L40N_6	V2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	V1	VREF
6	N.C. (◆)	IO_L41N_6	AH4	I/O
6	N.C. (◆)	IO_L41P_6	AH3	I/O
6	N.C. (◆)	IO_L44N_6	AD7	I/O
6	N.C. (◆)	IO_L44P_6	AD6	I/O
6	IO_L45N_6	IO_L45N_6	AC4	I/O
6	IO_L45P_6	IO_L45P_6	AC3	I/O
6	N.C. (◆)	IO_L46N_6	AA10	I/O
6	N.C. (◆)	IO_L46P_6	AA9	I/O
6	IO_L48N_6	IO_L48N_6	Y7	I/O
6	IO_L48P_6	IO_L48P_6	Y6	I/O
6	N.C. (◆)	IO_L49N_6	W11	I/O
6	N.C. (◆)	IO_L49P_6	V11	I/O
6	IO_L52N_6	IO_L52N_6	V8	I/O
6	IO_L52P_6	IO_L52P_6	V7	I/O
6	VCCO_6	VCCO_6	AA12	VCCO
6	VCCO_6	VCCO_6	AB12	VCCO
6	VCCO_6	VCCO_6	AB2	VCCO
6	VCCO_6	VCCO_6	AB6	VCCO
6	VCCO_6	VCCO_6	AD4	VCCO
6	VCCO_6	VCCO_6	AD8	VCCO
6	VCCO_6	VCCO_6	AG3	VCCO
6	VCCO_6	VCCO_6	AG7	VCCO
6	VCCO_6	VCCO_6	AL3	VCCO
6	VCCO_6	VCCO_6	W12	VCCO
6	VCCO_6	VCCO_6	W4	VCCO
6	VCCO_6	VCCO_6	Y12	VCCO
6	VCCO_6	VCCO_6	Y8	VCCO
7	IO	IO	G1	I/O
7	IO	IO	G2	I/O
7	IO	IO	U10	I/O
7	IO	IO	U9	I/O
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	C1	DCI

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	C2	DCI
7	IO_L02N_7	IO_L02N_7	D1	I/O
7	IO_L02P_7	IO_L02P_7	D2	I/O
7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	E2	VREF
7	IO_L03P_7	IO_L03P_7	E3	I/O
7	IO_L04N_7	IO_L04N_7	F3	I/O
7	IO_L04P_7	IO_L04P_7	F4	I/O
7	IO_L05N_7	IO_L05N_7	F1	I/O
7	IO_L05P_7	IO_L05P_7	F2	I/O
7	IO_L06N_7	IO_L06N_7	G5	I/O
7	IO_L06P_7	IO_L06P_7	G6	I/O
7	IO_L07N_7	IO_L07N_7	H5	I/O
7	IO_L07P_7	IO_L07P_7	H6	I/O
7	IO_L08N_7	IO_L08N_7	H1	I/O
7	IO_L08P_7	IO_L08P_7	H2	I/O
7	IO_L09N_7	IO_L09N_7	J6	I/O
7	IO_L09P_7	IO_L09P_7	J7	I/O
7	IO_L10N_7	IO_L10N_7	J4	I/O
7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	H4	VREF
7	IO_L11N_7	IO_L11N_7	J2	I/O
7	IO_L11P_7	IO_L11P_7	J3	I/O
7	IO_L12N_7	IO_L12N_7	K9	I/O
7	IO_L12P_7	IO_L12P_7	J8	I/O
7	IO_L13N_7	IO_L13N_7	K7	I/O
7	IO_L13P_7	IO_L13P_7	K8	I/O
7	IO_L14N_7	IO_L14N_7	K5	I/O
7	IO_L14P_7	IO_L14P_7	K6	I/O
7	IO_L15N_7	IO_L15N_7	K3	I/O
7	IO_L15P_7	IO_L15P_7	K4	I/O
7	IO_L16N_7	IO_L16N_7	K1	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	K2	VREF
7	IO_L17N_7	IO_L17N_7	L9	I/O
7	IO_L17P_7	IO_L17P_7	L10	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	L1	VREF
7	IO_L19P_7	IO_L19P_7	L2	I/O
7	IO_L20N_7	IO_L20N_7	M10	I/O
7	IO_L20P_7	IO_L20P_7	M11	I/O
7	IO_L21N_7	IO_L21N_7	M7	I/O
7	IO_L21P_7	IO_L21P_7	M8	I/O
7	IO_L22N_7	IO_L22N_7	M5	I/O