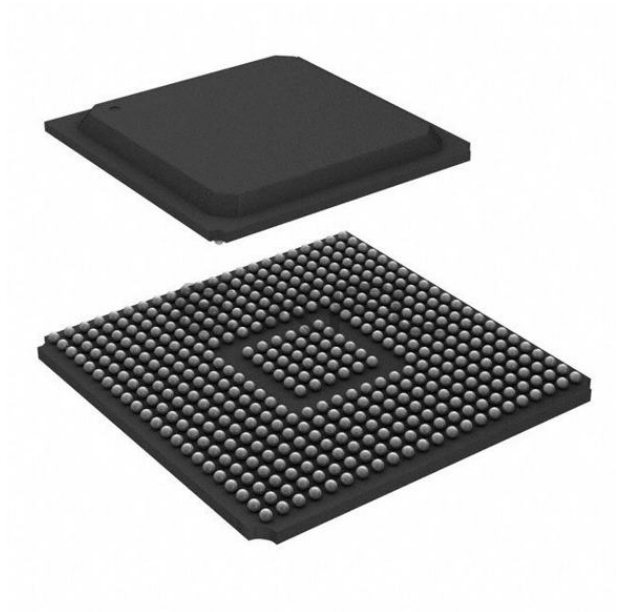
AMD Xilinx - XC3S1000-4FG456I Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1920
Number of Logic Elements/Cells	17280
Total RAM Bits	442368
Number of I/O	333
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1000-4fg456i

Table 9: **Differential I/O Standards**

Signal Standard (IOSTANDARD)	V_{CCO} (Volts)		V_{REF} for Inputs (Volts)
	For Outputs	For Inputs	
LDT_25 (ULVDS_25)	2.5	–	–
LVDS_25	2.5	–	–
BLVDS_25	2.5	–	–
LVDSEXT_25	2.5	–	–
LVPECL_25	2.5	–	–
RSDS_25	2.5	–	–
DIFF_HSTL_II_18	1.8	–	–
DIFF_SSTL2_II	2.5	–	–

Notes:

1. See Table 10 for a listing of the differential DCI standards.

The need to supply V_{REF} and V_{CCO} imposes constraints on which standards can be used in the same bank. See The Organization of IOBs into Banks section for additional guidelines concerning the use of the V_{CCO} and V_{REF} lines.

Digitally Controlled Impedance (DCI)

When the round-trip delay of an output signal—i.e., from output to input and back again—exceeds rise and fall times, it is common practice to add termination resistors to the line carrying the signal. These resistors effectively match the impedance of a device's I/O to the characteristic impedance of the transmission line, thereby preventing reflections that adversely affect signal integrity. However, with the high I/O counts supported by modern devices, adding resistors requires significantly more components and board area. Furthermore, for some packages—e.g., ball grid arrays—it may not always be possible to place resistors close to pins.

DCI answers these concerns by providing two kinds of on-chip terminations: Parallel terminations make use of an integrated resistor network. Series terminations result from controlling the impedance of output drivers. DCI actively adjusts both parallel and series terminations to accurately match the characteristic impedance of the transmission line. This adjustment process compensates for differences in I/O impedance that can result from normal variation in the ambient temperature, the supply voltage and the manufacturing process. When the output driver turns off, the series termination, by definition, approaches a very high impedance; in contrast, parallel termination resistors remain at the targeted values.

DCI is available only for certain I/O standards, as listed in Table 10. DCI is selected by applying the appropriate I/O standard extensions to symbols or components. There are five basic ways to configure terminations, as shown in Table 11. The DCI I/O standard determines which of these terminations is put into effect.

HSTL_I_DCI-, HSTL_III_DCI-, and SSTL2_I_DCI-type outputs do not require the VRN and VRP reference resistors. Likewise, LVDCI-type inputs do not require the VRN and VRP reference resistors. In a bank without any DCI I/O or a bank containing non-DCI I/O and purely HSTL_I_DCI- or HSTL_III_DCI-type outputs, or SSTL2_I_DCI-type outputs or LVDCI-type inputs, the associated VRN and VRP pins can be used as general-purpose I/O pins.

The HSLVDCI (High-Speed LVDCI) standard is intended for bidirectional use. The driver is identical to LVDCI, while the input is identical to HSTL. By using a V_{REF}-referenced input, HSLVDCI allows greater input sensitivity at the receiver than when using a single-ended LVCMOS-type receiver.

Table 10: **DCI I/O Standards**

Category of Signal Standard	Signal Standard (IOSTANDARD)	V_{CCO} (V)		V_{REF} for Inputs (V)	Termination Type	
		For Outputs	For Inputs		At Output	At Input
Single-Ended						
Gunning Transceiver Logic	GTL_DCI	1.2	1.2	0.8	Single	Single
	GTLP_DCI	1.5	1.5	1.0		
High-Speed Transceiver Logic	HSTL_I_DCI	1.5	1.5	0.75	None	Split
	HSTL_III_DCI	1.5	1.5	0.9	None	Single
	HSTL_I_DCI_18	1.8	1.8	0.9	None	Split
	HSTL_II_DCI_18 DIFF_HSTL_II_18_DCI	1.8	1.8	0.9	Split	
	HSTL_III_DCI_18	1.8	1.8	1.1	None	Single
Low-Voltage CMOS	LVDCI_15	1.5	1.5	–	Controlled impedance driver	None
	LVDCI_18	1.8	1.8	–		
	LVDCI_25	2.5	2.5	–		
	LVDCI_33(2)	3.3	3.3	–		
	LVDCI_DV2_15	1.5	1.5	–	Controlled driver with half-impedance	
	LVDCI_DV2_18	1.8	1.8	–		
	LVDCI_DV2_25	2.5	2.5	–		
	LVDCI_DV2_33	3.3	3.3	–		
Hybrid HSTL Input and LVCMOS Output	HSLVDCI_15	1.5	1.5	0.75	Controlled impedance driver	None
	HSLVDCI_18	1.8	1.8	0.9		
	HSLVDCI_25	2.5	2.5	1.25		
	HSLVDCI_33	3.3	3.3	1.65		
Stub Series Terminated Logic(3)	SSTL18_I_DCI	1.8	1.8	0.9	25Ω driver	Split
	SSTL2_I_DCI	2.5	2.5	1.25	25Ω driver	
	SSTL2_II_DCI DIFF_SSTL2_II_DCI	2.5	2.5	1.25	Split with 25Ω driver	
Differential						
Low-Voltage Differential Signaling	LVDS_25_DCI	N/A	2.5	–	None	Split on each line of pair
	LVDSEXT_25_DCI	N/A	2.5	–		

Notes:

1. DCI signal standards are not supported in Bank 5 of any Spartan-3 FPGA packaged in a VQ100, CP132, or TQ144 package.
2. Equivalent to LVTTL DCI.
3. The SSTL18_II signal standard does not have a DCI equivalent.

The DCI feature operates independently for each of the device's eight banks. Each bank has an 'N' reference pin (VRN) and a 'P' reference pin, (VRP), to calibrate driver and termination resistance. Only when using a DCI standard on a given bank do these two pins function as VRN and VRP. When not using a DCI standard, the two pins function as user I/Os. As shown in Figure 9, add an external reference resistor to pull the VRN pin up to V_{CCO} and another reference resistor to pull the VRP pin down to GND. Also see Figure 42, page 116. Both resistors have the same value—commonly 50Ω—with one-percent tolerance, which is either the characteristic impedance of the line or twice that, depending on the DCI standard in use. Standards having a symbol name that contains the letters "DV2" use a reference resistor value that is twice the line impedance. DCI adjusts the output driver impedance to match the reference resistors' value or half that, according to the standard. DCI always adjusts the on-chip termination resistors to directly match the reference resistors' value.

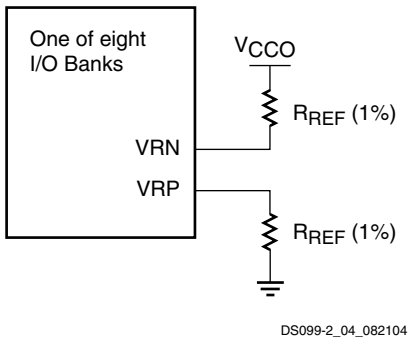


Figure 9: **Connection of Reference Resistors (R_{REF})**

The rules guiding the use of DCI standards on banks are as follows:

- No more than one DCI I/O standard with a Single Termination is allowed per bank.
- No more than one DCI I/O standard with a Split Termination is allowed per bank.
- Single Termination, Split Termination, Controlled- Impedance Driver, and Controlled-Impedance Driver with Half Impedance can co-exist in the same bank.

See also The Organization of IOBs into Banks, immediately below, and DCI: User I/O or Digitally Controlled Impedance Resistor Reference Input, page 115.

The Organization of IOBs into Banks

IOBs are allocated among eight banks, so that each side of the device has two banks, as shown in Figure 10. For all packages, each bank has independent V_{REF} lines. For example, V_{REF} Bank 3 lines are separate from the V_{REF} lines going to all other banks.

For the Very Thin Quad Flat Pack (VQ), Plastic Quad Flat Pack (PQ), Fine Pitch Thin Ball Grid Array (FT), and Fine Pitch Ball Grid Array (FG) packages, each bank has dedicated V_{CCO} lines. For example, the V_{CCO} Bank 7 lines are separate from the V_{CCO} lines going to all other banks. Thus, Spartan-3 devices in these packages support eight independent V_{CCO} supplies.

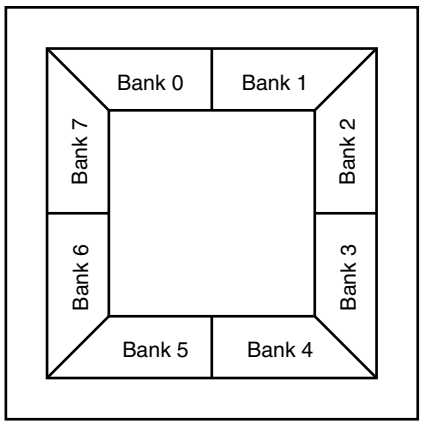


Figure 10: **Spartan-3 FPGA I/O Banks (Top View)**

Function Generator

Each of the two LUTs (F and G) in a slice have four logic inputs (A1-A4) and a single output (D). This permits any four-variable Boolean logic operation to be programmed into them. Furthermore, wide function multiplexers can be used to effectively combine LUTs within the same CLB or across different CLBs, making logic functions with still more input variables possible.

The LUTs in both the right-hand and left-hand slice-pairs not only support the logic functions described above, but also can function as ROM that is initialized with data at the time of configuration.

The LUTs in the left-hand slice-pair (even-numbered columns such as X0 in Figure 11) of each CLB support two additional functions that the right-hand slice-pair (odd-numbered columns such as X1) do not.

First, it is possible to program the “left-hand LUTs” as distributed RAM. This type of memory affords moderate amounts of data buffering anywhere along a data path. One left-hand LUT stores 16 bits. Multiple left-hand LUTs can be combined in various ways to store larger amounts of data. A dual port option combines two LUTs so that memory access is possible from two independent data lines. A Distributed ROM option permits pre-loading the memory with data during FPGA configuration.

Second, it is possible to program each left-hand LUT as a 16-bit shift register. Used in this way, each LUT can delay serial data anywhere from one to 16 clock cycles. The four left-hand LUTs of a single CLB can be combined to produce delays up to 64 clock cycles. The SHIFTIN and SHIFTOUT lines cascade LUTs to form larger shift registers. It is also possible to combine shift registers across more than one CLB. The resulting programmable delays can be used to balance the timing of data pipelines.

Block RAM Overview

All Spartan-3 devices support block RAM, which is organized as configurable, synchronous 18Kbit blocks. Block RAM stores relatively large amounts of data more efficiently than the distributed RAM feature described earlier. (The latter is better suited for buffering small amounts of data anywhere along signal paths.) This section describes basic Block RAM functions. For more information, refer to the chapter entitled “Using Block RAM” in UG331.

The aspect ratio—i.e., width vs. depth—of each block RAM is configurable. Furthermore, multiple blocks can be cascaded to create still wider and/or deeper memories.

A choice among primitives determines whether the block RAM functions as dual- or single-port memory. A name of the form RAMB16_S[w_A]_S[w_B] calls out the dual-port primitive, where the integers w_A and w_B specify the total data path width at ports w_A and w_B, respectively. Thus, a RAMB16_S9_S18 is a dual-port RAM with a 9-bit-wide Port A and an 18-bit-wide Port B. A name of the form RAMB16_S[w] identifies the single-port primitive, where the integer w specifies the total data path width of the lone port. A RAMB16_S18 is a single-port RAM with an 18-bit-wide port. Other memory functions—e.g., FIFOs, data path width conversion, ROM, etc.—are readily available using the CORE Generator™ software, part of the Xilinx development software.

Table 13: **Block RAM Port Signals *(Cont'd)***

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Data Output Bus	DOA	DOB	Output	Basic data access occurs whenever WE is inactive. The DO outputs mirror the data stored in the addressed memory location. Data access with WE asserted is also possible if one of the following two attributes is chosen: WRITE_FIRST and READ_FIRST. WRITE_FIRST simultaneously presents the new input data on the DO output port and writes the data to the address RAM location. READ_FIRST presents the previously stored RAM data on the DO output port while writing new data to RAM. A third attribute, NO_CHANGE, latches the DO outputs upon the assertion of WE. It is possible to configure a port's total data path width (w) to be 1, 2, 4, 9, 18, or 36 bits. This selection applies to both the DI and DO paths. See the DI signal description.
Parity Data Output(s)	DOPA	DOPB	Output	Parity inputs represent additional bits included in the data input path to support error detection. The number of parity bits "p" included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 14.
Write Enable	WEA	WEB	Input	When asserted together with EN, this input enables the writing of data to the RAM. In this case, the data access attributes WRITE_FIRST, READ_FIRST or NO_CHANGE determines if and how data is updated on the DO outputs. See the DO signal description. When WE is inactive with EN asserted, read operations are still possible. In this case, a transparent latch passes data from the addressed memory location to the DO outputs.
Clock Enable	ENA	ENB	Input	When asserted, this input enables the CLK signal to synchronize Block RAM functions as follows: the writing of data to the DI inputs (when WE is also asserted), the updating of data at the DO outputs as well as the setting/resetting of the DO output latches. When de-asserted, the above functions are disabled.
Set/Reset	SSRA	SSRB	Input	When asserted, this pin forces the DO output latch to the value that the SRVAL attribute is set to. A Set/Reset operation on one port has no effect on the other ports functioning, nor does it disturb the memory's data contents. It is synchronized to the CLK signal.
Clock	CLKA	CLKB	Input	This input accepts the clock signal to which read and write operations are synchronized. All associated port inputs are required to meet setup times with respect to the clock signal's active edge. The data output bus responds after a clock-to-out delay referenced to the clock signal's active edge.

Port Aspect Ratios

On a given port, it is possible to select a number of different possible widths ($w - p$) for the DI/DO buses as shown in Table 14. These two buses always have the same width. This data bus width selection is independent for each port. If the data bus width of Port A differs from that of Port B, the Block RAM automatically performs a bus-matching function. When data are written to a port with a narrow bus, then read from a port with a wide bus, the latter port will effectively combine "narrow" words to form "wide" words. Similarly, when data are written into a port with a wide bus, then read from a port with a narrow bus, the latter port will divide "wide" words to form "narrow" words. When the data bus width is eight bits or greater, extra parity bits become available. The width of the total data path (w) is the sum of the DI/DO bus width and any parity bits (p).

The width selection made for the DI/DO bus determines the number of address lines according to the relationship expressed below:

$$r = 14 - [\log(w-p)/\log(2)] \qquad \textit{Equation 1}$$

In turn, the number of address lines delimits the total number (n) of addressable locations or depth according to the following equation:

$$n = 2^r \qquad \textit{Equation 2}$$

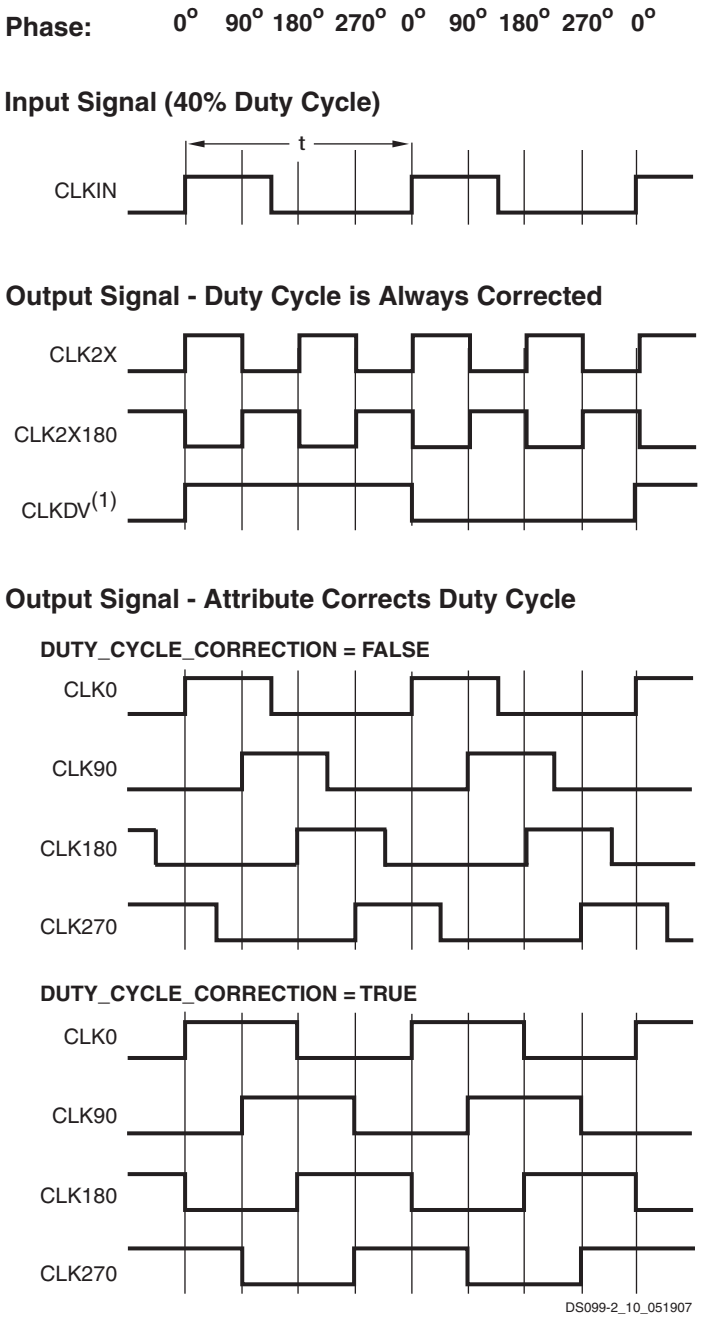


Figure 22: **Characteristics of the DLL Clock Outputs**

Digital Frequency Synthesizer (DFS)

The DFS component generates clock signals the frequency of which is a product of the clock frequency at the CLKIN input and a ratio of two user-determined integers. Because of the wide range of possible output frequencies such a ratio permits, the DFS feature provides still further flexibility than the DLL's basic synthesis options as described in the preceding section. The DFS component's two dedicated outputs, CLKFX and CLKFX180, are defined in Table 19.

The signal at the CLKFX180 output is essentially an inversion of the CLKFX signal. These two outputs always exhibit a 50% duty cycle. This is true even when the CLKIN signal does not. These DFS clock outputs are driven at the same time as the DLL's seven clock outputs.

The numerator of the ratio is the integer value assigned to the attribute CLKFX_MULTIPLY and the denominator is the integer value assigned to the attribute CLKFX_DIVIDE. These attributes are described in Table 18.

The output frequency (f_{CLKFX}) can be expressed as a function of the incoming clock frequency (f_{CLKIN}) as follows:

$$f_{CLKFX} = f_{CLKIN}(CLKFX\_MULTIPLY/CLKFX\_DIVIDE) \quad \textit{Equation 3}$$

Regarding the two attributes, it is possible to assign any combination of integer values, provided that two conditions are met:

- The two values fall within their corresponding ranges, as specified in Table 18.
- The f_{CLKFX} frequency calculated from the above expression accords with the DCM's operating frequency specifications.

For example, if CLKFX_MULTIPLY = 5 and CLKFX_DIVIDE = 3, then the frequency of the output clock signal would be 5/3 that of the input clock signal.

DFS Frequency Modes

The DFS supports two operating modes, High Frequency and Low Frequency, with each specified over a different clock frequency range. The DFS_FREQUENCY_MODE attribute chooses between the two modes. When the attribute is set to LOW, the Low Frequency mode permits the two DFS outputs to operate over a low-to-moderate frequency range. When the attribute is set to HIGH, the High Frequency mode allows both these outputs to operate at the highest possible frequencies.

DFS With or Without the DLL

The DFS component can be used with or without the DLL component:

Without the DLL, the DFS component multiplies or divides the CLKIN signal frequency according to the respective CLKFX_MULTIPLY and CLKFX_DIVIDE values, generating a clock with the new target frequency on the CLKFX and CLKFX180 outputs. Though classified as belonging to the DLL component, the CLKIN input is shared with the DFS component. This case does not employ feedback loop; therefore, it cannot correct for clock distribution delay.

With the DLL, the DFS operates as described in the preceding case, only with the additional benefit of eliminating the clock distribution delay. In this case, a feedback loop from the CLK0 output to the CLKFB input must be present.

The DLL and DFS components work together to achieve this phase correction as follows: Given values for the CLKFX_MULTIPLY and CLKFX_DIVIDE attributes, the DLL selects the delay element for which the output clock edge coincides with the input clock edge whenever mathematically possible. For example, when CLKFX_MULTIPLY = 5 and CLKFX_DIVIDE = 3, the input and output clock edges will coincide every three input periods, which is equivalent in time to five output periods.

Smaller CLKFX_MULTIPLY and CLKFX_DIVIDE values achieve faster lock times. With no factors common to the two attributes, alignment will occur once with every number of cycles equal to the CLKFX_DIVIDE value. Therefore, it is recommended that the user reduce these values by factoring wherever possible. For example, given CLKFX_MULTIPLY = 9 and CLKFX_DIVIDE = 6, removing a factor of three yields CLKFX_MULTIPLY = 3 and CLKFX_DIVIDE = 2. While both value-pairs will result in the multiplication of clock frequency by 3/2, the latter value-pair will enable the DLL to lock more quickly.

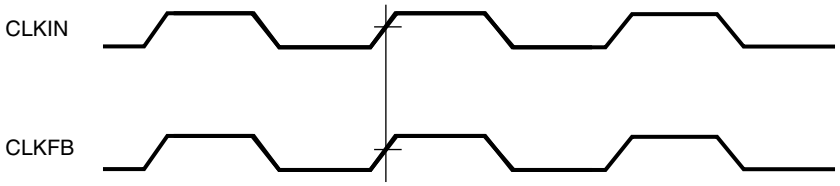
Table 18: **DFS Attributes**

Attribute	Description	Values
DFS_FREQUENCY_MODE	Chooses between High Frequency and Low Frequency modes	Low, High
CLKFX_MULTIPLY	Frequency multiplier constant	Integer from 2 to 32
CLKFX_DIVIDE	Frequency divisor constant	Integer from 1 to 32

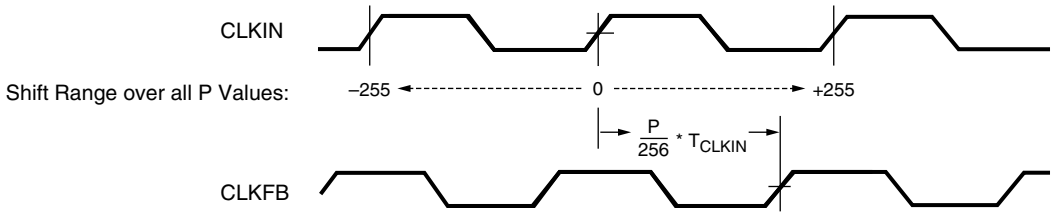
Table 19: **DFS Signals**

Signal	Direction	Description
CLKFX	Output	Multiplies the CLKIN frequency by the attribute-value ratio (CLKFX_MULTIPLY/CLKFX_DIVIDE) to generate a clock signal with a new target frequency.
CLKFX180	Output	Generates a clock signal with same frequency as CLKFX, only shifted 180° out-of-phase.

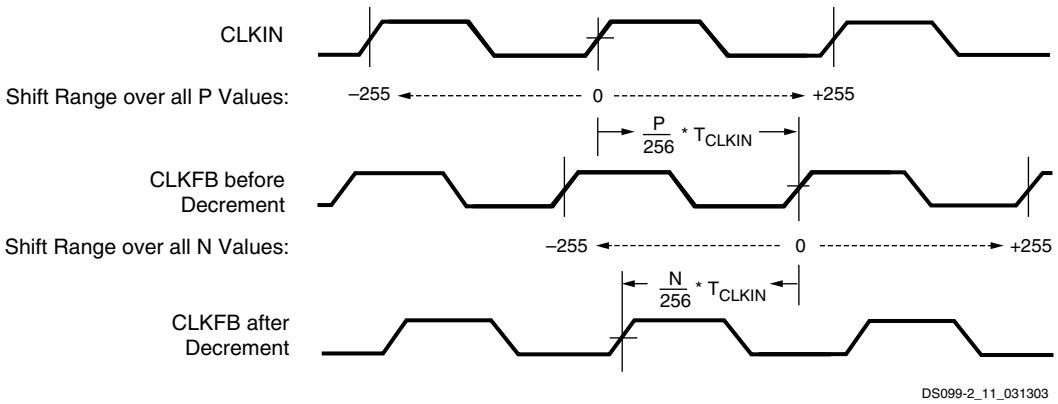
a. CLKOUT_PHASE_SHIFT = NONE



b. CLKOUT_PHASE_SHIFT = FIXED



c. CLKOUT_PHASE_SHIFT = VARIABLE



Notes:

1. P represents the integer value ranging from –255 to +255 to which the PHASE_SHIFT attribute is assigned.
2. N is an integer value ranging from –255 to +255 that represents the net phase shift effect from a series of increment and/or decrement operations.
   N = {Total number of increments} – {Total number of decrements}
   A positive value for N indicates a net increment; a negative value indicates a net decrement.

Figure 23: **Phase Shifter Waveforms**

The Status Logic Component

The Status Logic component not only reports on the state of the DCM but also provides a means of resetting the DCM to an initial known state. The signals associated with the Status Logic component are described in Table 22.

As a rule, the Reset (RST) input is asserted only upon configuring the device or changing the CLKIN frequency. A DCM reset does not affect attribute values (e.g., CLKFX_MULTIPLY and CLKFX_DIVIDE). If not used, RST must be tied to GND.

The eight bits of the STATUS bus are defined in Table 23.

Each BUFGMUX element, shown in Figure 24, is a 2-to-1 multiplexer that can receive signals from any of the four following sources:

- One of the four Global Clock inputs on the same side of the die—top or bottom—as the BUFGMUX element in use.
- Any of four nearby horizontal Double lines.
- Any of four outputs from the DCM in the right-hand quadrant that is on the same side of the die as the BUFGMUX element in use.
- Any of four outputs from the DCM in the left-hand quadrant that is on the same side of the die as the BUFGMUX element in use.

The multiplexer select line, S, chooses which of the two inputs, I0 or I1, drives the BUFGMUX's output signal, O, as described in Table 25. The switching from one clock to the other is glitchless, and done in such a way that the output High and Low times are never shorter than the shortest High or Low time of either input clock.

Table 25: **BUFGMUX Select Mechanism**

S Input	O Output
0	I0 Input
1	I1 Input

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

The BUFG clock buffer primitive drives a single clock signal onto the clock network and is essentially the same element as a BUFGMUX, just without the clock select mechanism. Similarly, the BUFGCE primitive creates an enabled clock buffer using the BUFGMUX select mechanism.

Each BUFGMUX buffers incoming clock signals to two possible destinations:

- The vertical spine belonging to the same side of the die—top or bottom—as the BUFGMUX element in use. The two spines—top and bottom—each comprise four vertical clock lines, each running from one of the BUFGMUX elements on the same side towards the center of the die. At the center of the die, clock signals reach the eight-line horizontal spine, which spans the width of the die. In turn, the horizontal spine branches out into a subsidiary clock interconnect that accesses the CLBs.
- The clock input of either DCM on the same side of the die—top or bottom—as the BUFGMUX element in use.

Use either a BUFGMUX element or a BUFG (Global Clock Buffer) element to place a Global input in the design. For the purpose of minimizing the dynamic power dissipation of the clock network, the Xilinx development software automatically disables all clock line segments that a design does not use.

A global clock line ideally drives clock inputs on the various clocked elements within the FPGA, such as CLB or IOB flip-flops or block RAMs. A global clock line also optionally drives combinatorial inputs. However, doing so provides additional loading on the clock line that might also affect clock jitter. Ideally, drive combinatorial inputs using the signal that also drives the input to the BUFGMUX or BUFG element.

For more details, refer to the chapter entitled "Using Global Clock Resources" in UG331.

Table 36: **DC Characteristics of User I/Os Using Single-Ended Standards**

Signal Standard (IOSTANDARD) and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
GTL		32	–	0.4	–
GTL_DCI		Note 3	Note 3		
GTLP		36	–	0.6	–
GTLP_DCI		Note 3	Note 3		
HSLVDCI_15		Note 3	Note 3	0.4	V_{CCO} – 0.4
HSLVDCI_18					
HSLVDCI_25					
HSLVDCI_33					
HSTL_I		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI		Note 3	Note 3		
HSTL_III		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI		Note 3	Note 3		
HSTL_I_18		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI_18		Note 3	Note 3		
HSTL_II_18		16	–16	0.4	V_{CCO} – 0.4
HSTL_II_DCI_18		Note 3	Note 3		
HSTL_III_18		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI_18		Note 3	Note 3		
LVCMOS12(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
LVCMOS15(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
LVDCI_15, LVDCI_DV2_15		Note 3	Note 3		
LVCMOS18(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
LVDCI_18, LVDCI_DV2_18		Note 3	Note 3		
LVCMOS25(4,5)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_25, LVDCI_DV2_25		Note 3	Note 3		

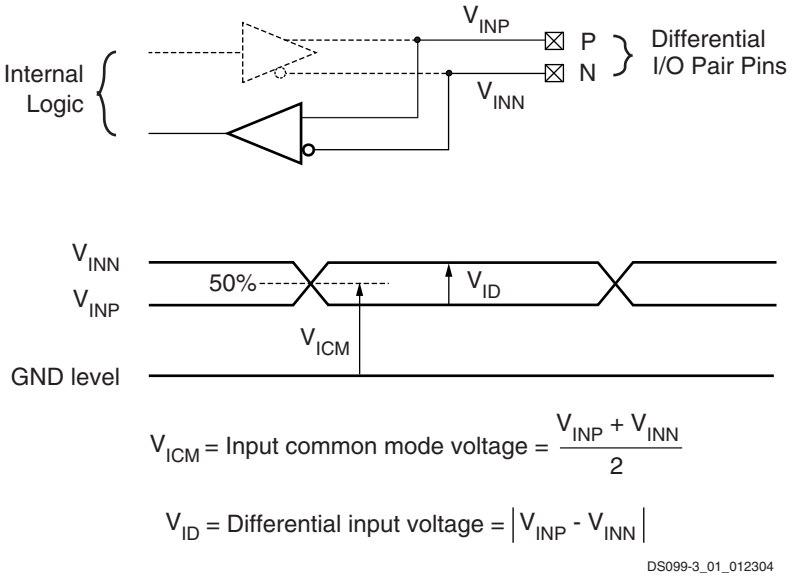


Figure 32: **Differential Input Voltages**

Table 37: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

Signal Standard (IOSTANDARD)	V_{CCO}[1]			V_{ID}[3]			V_{ICM}		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LDT_25 (ULVDS_25)	2.375	2.50	2.625	200	600	1000	0.44	0.60	0.78
LVDS_25, LVDS_25_DCI	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20
BLVDS_25	2.375	2.50	2.625	-	350	-	-	1.25	-
LVDSEXT_25, LVDSEXT_25_DCI	2.375	2.50	2.625	100	540	1000	0.30	1.20	2.20
LVPECL_25	2.375	2.50	2.625	100	-	-	0.30	1.20	2.00
RSDS_25	2.375	2.50	2.625	100	200	-	-	1.20	-
DIFF_HSTL_II_18, DIFF_HSTL_II_18_DCI	1.70	1.80	1.90	200	-	-	0.80	-	1.00
DIFF_SSTL2_II, DIFF_SSTL2_II_DCI	2.375	2.50	2.625	300	-	-	1.05	-	1.45

Notes:

1. V_{CCO} only supplies differential output drivers, not input circuits.
2. V_{REF} inputs are not used for any of the differential I/O standards.
3. V_{ID} is a differential measurement.

Switching Characteristics

All Spartan-3 devices are available in two speed grades: –4 and the higher performance –5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reported delays may still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Production-quality systems must use FPGA designs compiled using a Production status speed file. FPGAs designs using a less mature speed file designation may only be used during system prototyping or preproduction qualification. FPGA designs using Advance or Preliminary status speed files should never be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

Xilinx ISE Software Updates: http://www.xilinx.com/support/download/index.htm

All specified limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the following applies: Parameter values apply to all Spartan-3 devices. All parameters representing voltages are measured with respect to GND.

Selected timing parameters and their representative values are included below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3 FPGA v1.38 speed files are the original source for many but not all of the values. The v1.38 speed files are available in Xilinx Integrated Software Environment (ISE) software version 8.2i.

The speed grade designations for these files are shown in Table 39. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 39: **Spartan-3 FPGA Speed Grade Designations (ISE v8.2i or Later)**

Device	Advance	Preliminary	Production
XC3S50			-4, -5 (v1.37 and later)
XC3S200			
XC3S400			
XC3S1000			
XC3S1500			
XC3S2000			
XC3S4000			
XC3S5000			-4, -5 (v1.38 and later)

Table 48: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
HSTL_III_DCI_18							
LVCMOS12		-	0	1.2	1M	0	0.6
LVCMOS15		-	0	1.5	1M	0	0.75
LVDCI_15							
LVDCI_DV2_15							
HSLVDCI_15							
LVCMOS18		-	0	1.8	1M	0	0.9
LVDCI_18							
LVDCI_DV2_18							
HSLVDCI_18							
LVCMOS25		-	0	2.5	1M	0	1.25
LVDCI_25							
LVDCI_DV2_25							
HSLVDCI_25							
LVCMOS33		-	0	3.3	1M	0	1.65
LVDCI_33							
LVDCI_DV2_33							
HSLVDCI_33							
LVTTL		-	0	3.3	1M	0	1.4
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_I_DCI							
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_I_DCI							
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL2_II_DCI					50	1.25	
Differential							
LDT_25 (ULVDS_25)		-	V_{ICM} – 0.125	V_{ICM} + 0.125	60	0.6	V_{ICM}
LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_25_DCI					N/A	N/A	
BLVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
LVDSEXT_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDSEXT_25_DCI					N/A	N/A	
LVPECL_25		-	V_{ICM} – 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25		-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
DIFF_HSTL_II_18		-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.8	V_{ICM}
DIFF_HSTL_II_18_DCI							

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package				
			VQ100	TQ144	PQ208	CP132	FT256, FG320, FG456, FG676, FG900, FG1156
LVCMOS33	Slow	2	34	24	24	52	76
		4	17	14	14	26	46
		6	17	11	11	26	27
		8	10	10	10	13	20
		12	9	9	9	13	13
		16	8	8	8	8	10
		24	8	8	8	8	9
	Fast	2	20	20	20	26	44
		4	15	15	15	15	26
		6	11	11	11	13	16
		8	10	10	10	10	12
		12	8	8	8	8	10
		16	8	8	8	8	8
		24	7	7	7	7	7
LVDCI_33			10	10	10	10	10
LVDCI_DV2_33			10	10	10	10	10
HSLVDCI_33			10	10	10	10	10
LVTTL	Slow	2	34	25	25	52	60
		4	17	16	16	26	41
		6	17	15	15	26	29
		8	12	12	12	13	22
		12	10	10	10	13	13
		16	10	10	10	10	11
		24	8	8	8	8	9
	Fast	2	20	20	20	26	34
		4	13	13	13	13	20
		6	11	11	11	13	15
		8	10	10	10	10	12
		12	9	9	9	9	10
		16	8	8	8	8	9
		24	7	7	7	7	7

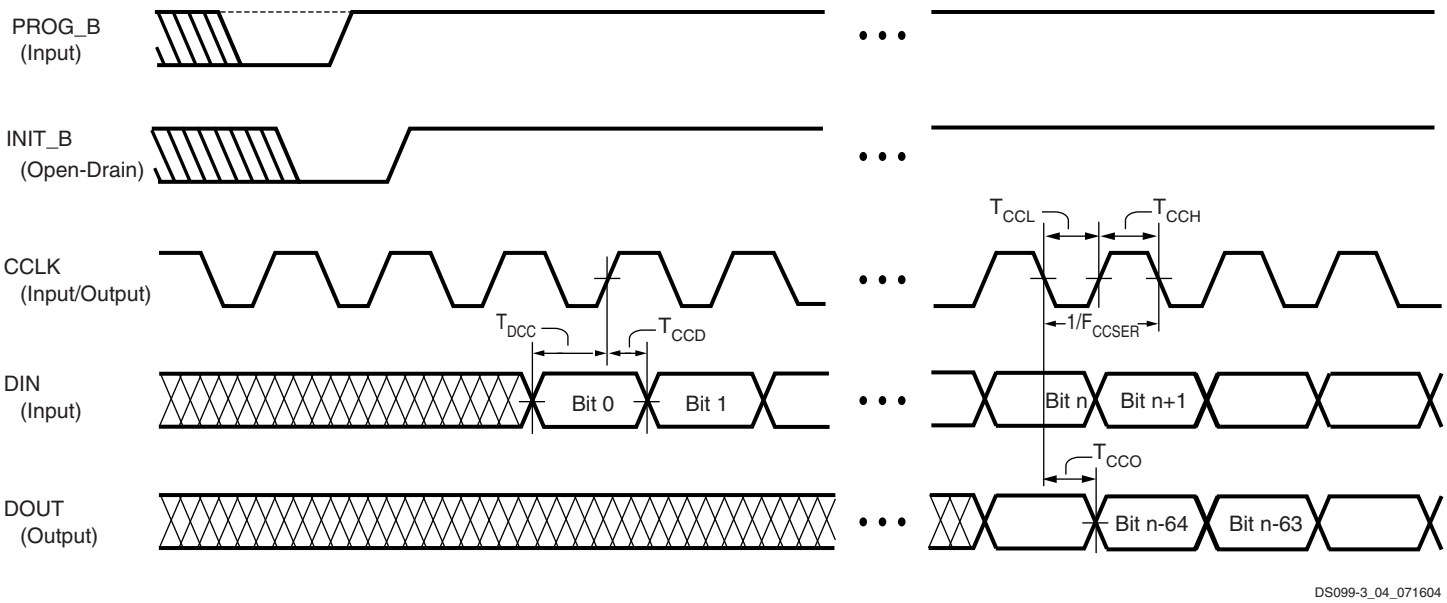


Figure 37: **Waveforms for Master and Slave Serial Configuration**

Table 66: **Timing for the Master and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	12.0	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		Both	10.0	–	ns
Hold Times						
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		Both	0	–	ns
Clock Timing						
T_{CCH}	CCLK input pin High pulse width		Slave	5.0	∞	ns
T_{CCL}	CCLK input pin Low pulse width			5.0	∞	ns
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression		0	66(2)	MHz
		With bitstream compression		0	20	MHz
		During STARTUP phase		0	50	MHz
ΔF_{CCSER}	Variation from the CCLK output frequency set using the ConfigRate BitGen option		Master	–50%	+50%	–

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

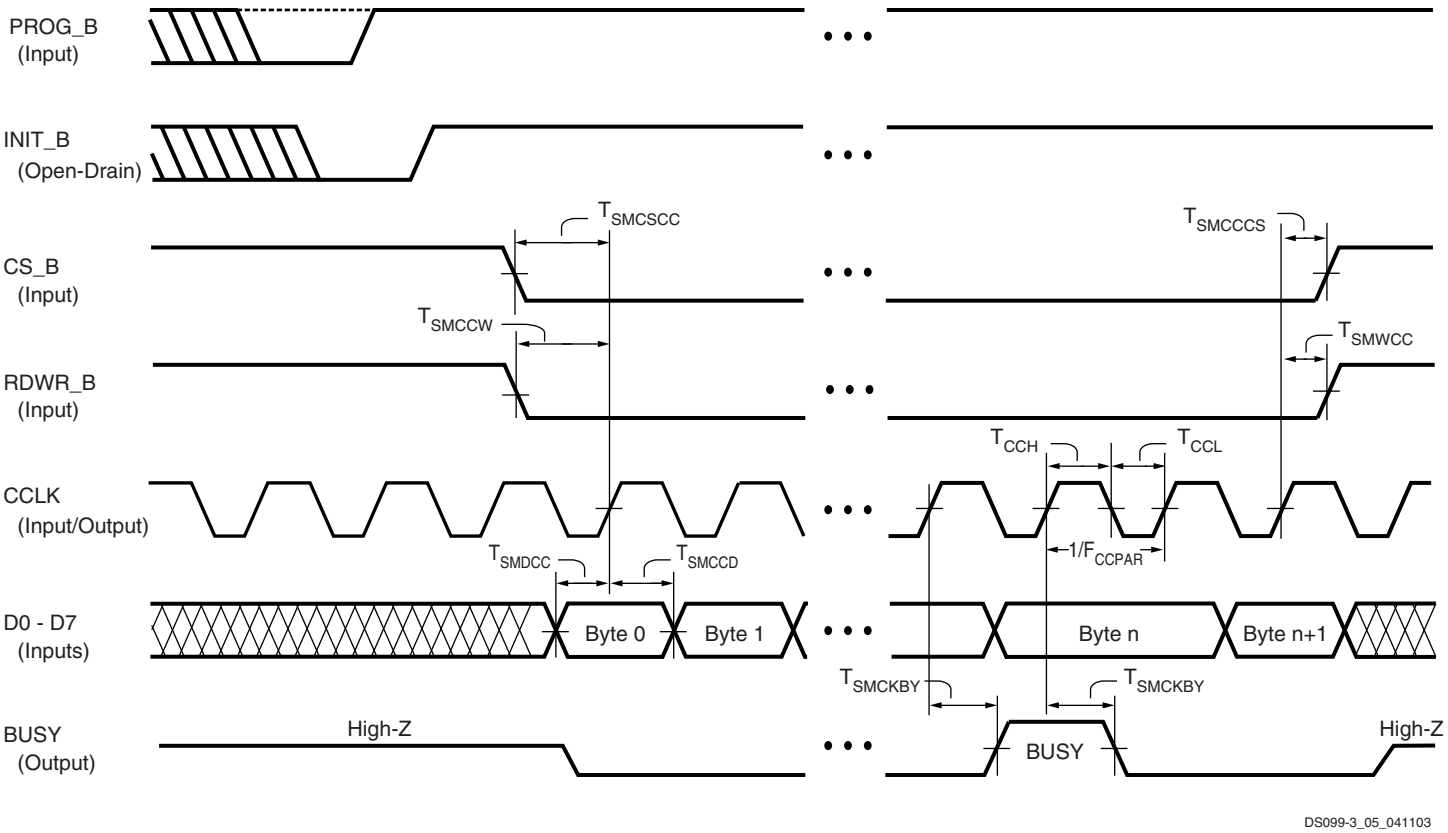


Figure 38: **Waveforms for Master and Slave Parallel Configuration**

Table 67: **Timing for the Master and Slave Parallel Configuration Modes**

Symbol	Description	Slave/ Master	All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin	Slave	–	12.0	ns
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	Both	10.0	–	ns
T_{SMCSCC}	The time from the setup of a logic level at the CS_B pin to the rising transition at the CCLK pin		10.0	–	ns
T_{SMCCW}(3)	The time from the setup of a logic level at the RDWR_B pin to the rising transition at the CCLK pin		10.0	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins	Both	0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CS_B pin		0	–	ns
T_{SMWCC}(3)	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns

FT256: 256-lead Fine-pitch Thin Ball Grid Array

The 256-lead fine-pitch thin ball grid array package, FT256, supports three different Spartan-3 devices, including the XC3S200, the XC3S400, and the XC3S1000. The footprints for all three devices are identical, as shown in Table 96 and Figure 49.

All the package pins appear in Table 96 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 96: **FT256 Package Pinout**

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
0	IO	A5	I/O
0	IO	A7	I/O
0	IO/VREF_0	A3	VREF
0	IO/VREF_0	D5	VREF
0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L25N_0	C5	I/O
0	IO_L25P_0	B5	I/O
0	IO_L27N_0	E6	I/O
0	IO_L27P_0	D6	I/O
0	IO_L28N_0	C6	I/O
0	IO_L28P_0	B6	I/O
0	IO_L29N_0	E7	I/O
0	IO_L29P_0	D7	I/O
0	IO_L30N_0	C7	I/O
0	IO_L30P_0	B7	I/O
0	IO_L31N_0	D8	I/O
0	IO_L31P_0/VREF_0	C8	VREF
0	IO_L32N_0/GCLK7	B8	GCLK
0	IO_L32P_0/GCLK6	A8	GCLK
0	VCCO_0	E8	VCCO
0	VCCO_0	F7	VCCO
0	VCCO_0	F8	VCCO
1	IO	A9	I/O
1	IO	A12	I/O
1	IO	C10	I/O
1	IO/VREF_1	D12	VREF
1	IO_L01N_1/VRP_1	A14	DCI
1	IO_L01P_1/VRN_1	B14	DCI

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
7	IO_L24P_7	G4	I/O
7	IO_L39N_7	H3	I/O
7	IO_L39P_7	H4	I/O
7	IO_L40N_7/VREF_7	H1	VREF
7	IO_L40P_7	G1	I/O
7	VCCO_7	G6	VCCO
7	VCCO_7	H5	VCCO
7	VCCO_7	H6	VCCO
N/A	GND	A1	GND
N/A	GND	A16	GND
N/A	GND	B2	GND
N/A	GND	B9	GND
N/A	GND	B15	GND
N/A	GND	F6	GND
N/A	GND	F11	GND
N/A	GND	G7	GND
N/A	GND	G8	GND
N/A	GND	G9	GND
N/A	GND	G10	GND
N/A	GND	H2	GND
N/A	GND	H7	GND
N/A	GND	H8	GND
N/A	GND	H9	GND
N/A	GND	H10	GND
N/A	GND	J7	GND
N/A	GND	J8	GND
N/A	GND	J9	GND
N/A	GND	J10	GND
N/A	GND	J15	GND
N/A	GND	K7	GND
N/A	GND	K8	GND
N/A	GND	K9	GND
N/A	GND	K10	GND
N/A	GND	L6	GND
N/A	GND	L11	GND
N/A	GND	R2	GND
N/A	GND	R8	GND
N/A	GND	R15	GND
N/A	GND	T1	GND

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
6	IO_L01P_6/VRN_6	T2	DCI
6	IO_L16N_6	U1	I/O
6	IO_L16P_6	T1	I/O
6	IO_L17N_6	R2	I/O
6	IO_L17P_6/VREF_6	R1	VREF
6	IO_L19N_6	R3	I/O
6	IO_L19P_6	P3	I/O
6	IO_L20N_6	P2	I/O
6	IO_L20P_6	P1	I/O
6	IO_L21N_6	N4	I/O
6	IO_L21P_6	P4	I/O
6	IO_L22N_6	N5	I/O
6	IO_L22P_6	M5	I/O
6	IO_L23N_6	M3	I/O
6	IO_L23P_6	M4	I/O
6	IO_L24N_6/VREF_6	N2	VREF
6	IO_L24P_6	M1	I/O
6	IO_L27N_6	L6	I/O
6	IO_L27P_6	L5	I/O
6	IO_L34N_6/VREF_6	L3	VREF
6	IO_L34P_6	L4	I/O
6	IO_L35N_6	L2	I/O
6	IO_L35P_6	L1	I/O
6	IO_L39N_6	K5	I/O
6	IO_L39P_6	K4	I/O
6	IO_L40N_6	K1	I/O
6	IO_L40P_6/VREF_6	K2	VREF
6	VCCO_6	K7	VCCO
6	VCCO_6	L7	VCCO
6	VCCO_6	N3	VCCO
7	IO	J6	I/O
7	IO_L01N_7/VRP_7	C3	DCI
7	IO_L01P_7/VRN_7	C2	DCI
7	IO_L16N_7	C1	I/O
7	IO_L16P_7/VREF_7	B1	VREF
7	IO_L17N_7	D1	I/O
7	IO_L17P_7	D2	I/O
7	IO_L19N_7/VREF_7	E3	VREF
7	IO_L19P_7	D3	I/O
7	IO_L20N_7	E2	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	GND	GND	T12	GND
N/A	GND	GND	N13	GND
N/A	GND	GND	P13	GND
N/A	GND	GND	R13	GND
N/A	GND	GND	T13	GND
N/A	GND	GND	U13	GND
N/A	GND	GND	V13	GND
N/A	GND	GND	A14	GND
N/A	GND	GND	E14	GND
N/A	GND	GND	H14	GND
N/A	GND	GND	N14	GND
N/A	GND	GND	P14	GND
N/A	GND	GND	R14	GND
N/A	GND	GND	T14	GND
N/A	GND	GND	U14	GND
N/A	GND	GND	V14	GND
N/A	GND	GND	AC14	GND
N/A	GND	GND	AF14	GND
N/A	GND	GND	AK14	GND
N/A	GND	GND	M15	GND
N/A	GND	GND	N15	GND
N/A	GND	GND	P15	GND
N/A	GND	GND	R15	GND
N/A	GND	GND	T15	GND
N/A	GND	GND	U15	GND
N/A	GND	GND	V15	GND
N/A	GND	GND	W15	GND
N/A	GND	GND	M16	GND
N/A	GND	GND	N16	GND
N/A	GND	GND	P16	GND
N/A	GND	GND	R16	GND
N/A	GND	GND	T16	GND
N/A	GND	GND	U16	GND
N/A	GND	GND	V16	GND
N/A	GND	GND	W16	GND
N/A	GND	GND	A17	GND
N/A	GND	GND	E17	GND
N/A	GND	GND	H17	GND
N/A	GND	GND	N17	GND
N/A	GND	GND	P17	GND