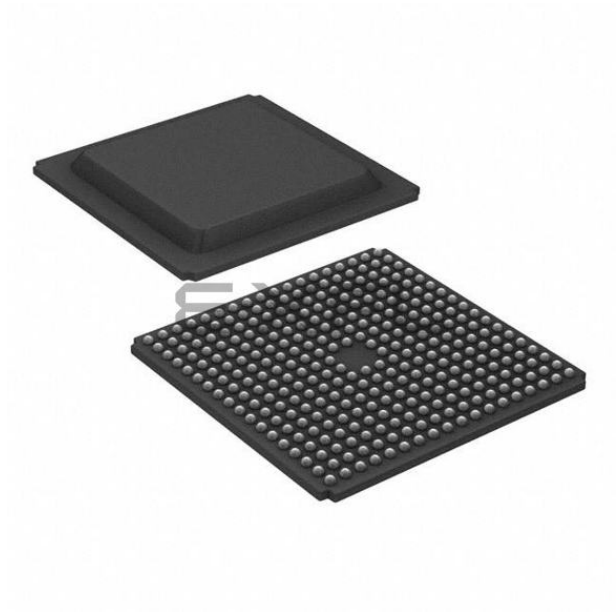
AMD Xilinx - XC3S1000-4FGG320C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1920
Number of Logic Elements/Cells	17280
Total RAM Bits	442368
Number of I/O	221
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1000-4fgg320c

According to Figure 7, the clock line OTCLK1 connects the CK inputs of the upper registers on the output and three-state paths. Similarly, OTCLK2 connects the CK inputs for the lower registers on the output and three-state paths. The upper and lower registers on the input path have independent clock lines: ICLK1 and ICLK2. The enable line OCE connects the CE inputs of the upper and lower registers on the output path. Similarly, TCE connects the CE inputs for the register pair on the three-state path and ICE does the same for the register pair on the input path. The Set/Reset (SR) line entering the IOB is common to all six registers, as is the Reverse (REV) line.

Each storage element supports numerous options in addition to the control over signal polarity described in the IOB Overview section. These are described in Table 6.

Table 6: **Storage Element Options**

Option Switch	Function	Specificity
FF/Latch	Chooses between an edge-sensitive flip-flop or a level-sensitive latch	Independent for each storage element.
SYNC/ASYNC	Determines whether SR is synchronous or asynchronous	Independent for each storage element.
SRHIGH/SRLOW	Determines whether SR acts as a Set, which forces the storage element to a logic “1" (SRHIGH) or a Reset, which forces a logic “0” (SRLOW).	Independent for each storage element, except when using FDDR. In the latter case, the selection for the upper element (OFF1 or TFF2) applies to both elements.
INIT1/INIT0	In the event of a Global Set/Reset, after configuration or upon activation of the GSR net, this switch decides whether to set or reset a storage element. By default, choosing SRLOW also selects INIT0; choosing SRHIGH also selects INIT1.	Independent for each storage element, except when using FDDR. In the latter case, selecting INIT0 for one element applies to both elements (even though INIT1 is selected for the other).

Double-Data-Rate Transmission

Double-Data-Rate (DDR) transmission describes the technique of synchronizing signals to both the rising and falling edges of the clock signal. Spartan-3 devices use register-pairs in all three IOB paths to perform DDR operations.

The pair of storage elements on the IOB’s Output path (OFF1 and OFF2), used as registers, combine with a special multiplexer to form a DDR D-type flip-flop (FDDR). This primitive permits DDR transmission where output data bits are synchronized to both the rising and falling edges of a clock. It is possible to access this function by placing either an FDDRRSE or an FDDRCPE component or symbol into the design. DDR operation requires two clock signals (50% duty cycle), one the inverted form of the other. These signals trigger the two registers in alternating fashion, as shown in Figure 8. Commonly, the Digital Clock Manager (DCM) generates the two clock signals by mirroring an incoming signal, then shifting it 180 degrees. This approach ensures minimal skew between the two signals.

The storage-element-pair on the Three-State path (TFF1 and TFF2) can also be combined with a local multiplexer to form an FDDR primitive. This permits synchronizing the output enable to both the rising and falling edges of a clock. This DDR operation is realized in the same way as for the output path.

The storage-element-pair on the input path (IFF1 and IFF2) allows an I/O to receive a DDR signal. An incoming DDR clock signal triggers one register and the inverted clock signal triggers the other register. In this way, the registers take turns capturing bits of the incoming DDR data signal.

Table 13: **Block RAM Port Signals *(Cont'd)***

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Data Output Bus	DOA	DOB	Output	Basic data access occurs whenever WE is inactive. The DO outputs mirror the data stored in the addressed memory location. Data access with WE asserted is also possible if one of the following two attributes is chosen: WRITE_FIRST and READ_FIRST. WRITE_FIRST simultaneously presents the new input data on the DO output port and writes the data to the address RAM location. READ_FIRST presents the previously stored RAM data on the DO output port while writing new data to RAM. A third attribute, NO_CHANGE, latches the DO outputs upon the assertion of WE. It is possible to configure a port's total data path width (w) to be 1, 2, 4, 9, 18, or 36 bits. This selection applies to both the DI and DO paths. See the DI signal description.
Parity Data Output(s)	DOPA	DOPB	Output	Parity inputs represent additional bits included in the data input path to support error detection. The number of parity bits "p" included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 14.
Write Enable	WEA	WEB	Input	When asserted together with EN, this input enables the writing of data to the RAM. In this case, the data access attributes WRITE_FIRST, READ_FIRST or NO_CHANGE determines if and how data is updated on the DO outputs. See the DO signal description. When WE is inactive with EN asserted, read operations are still possible. In this case, a transparent latch passes data from the addressed memory location to the DO outputs.
Clock Enable	ENA	ENB	Input	When asserted, this input enables the CLK signal to synchronize Block RAM functions as follows: the writing of data to the DI inputs (when WE is also asserted), the updating of data at the DO outputs as well as the setting/resetting of the DO output latches. When de-asserted, the above functions are disabled.
Set/Reset	SSRA	SSRB	Input	When asserted, this pin forces the DO output latch to the value that the SRVAL attribute is set to. A Set/Reset operation on one port has no effect on the other ports functioning, nor does it disturb the memory's data contents. It is synchronized to the CLK signal.
Clock	CLKA	CLKB	Input	This input accepts the clock signal to which read and write operations are synchronized. All associated port inputs are required to meet setup times with respect to the clock signal's active edge. The data output bus responds after a clock-to-out delay referenced to the clock signal's active edge.

Port Aspect Ratios

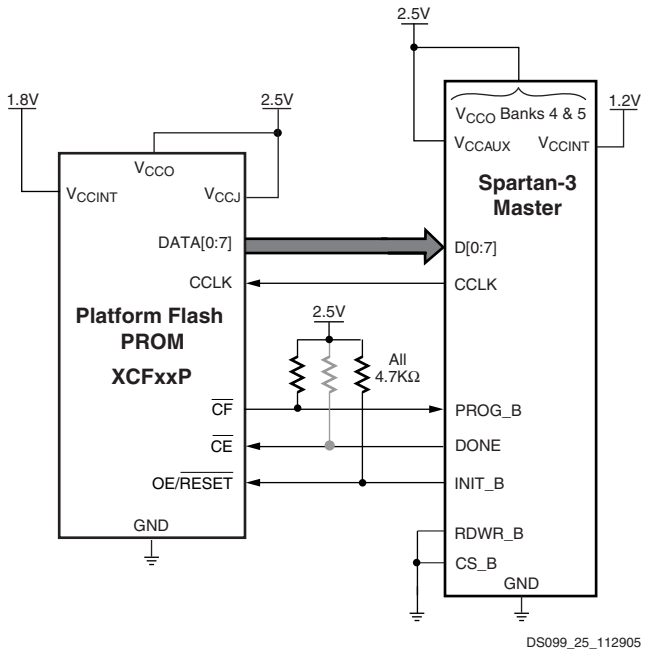
On a given port, it is possible to select a number of different possible widths ($w - p$) for the DI/DO buses as shown in Table 14. These two buses always have the same width. This data bus width selection is independent for each port. If the data bus width of Port A differs from that of Port B, the Block RAM automatically performs a bus-matching function. When data are written to a port with a narrow bus, then read from a port with a wide bus, the latter port will effectively combine "narrow" words to form "wide" words. Similarly, when data are written into a port with a wide bus, then read from a port with a narrow bus, the latter port will divide "wide" words to form "narrow" words. When the data bus width is eight bits or greater, extra parity bits become available. The width of the total data path (w) is the sum of the DI/DO bus width and any parity bits (p).

The width selection made for the DI/DO bus determines the number of address lines according to the relationship expressed below:

$$r = 14 - [\log(w-p)/\log(2)] \qquad \textit{Equation 1}$$

In turn, the number of address lines delimits the total number (n) of addressable locations or depth according to the following equation:

$$n = 2^r \qquad \textit{Equation 2}$$



Notes:

1. There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.

Figure 28: **Connection Diagram for Master Parallel Configuration**

Master Parallel Mode

In this mode, the FPGA configures from byte-wide data, and the FPGA supplies the CCLK configuration clock. In Master configuration modes, CCLK behaves as a bidirectional I/O pin. Timing is similar to the Slave Parallel mode except that CCLK is supplied by the FPGA. The device connections are shown in Figure 28.

Boundary-Scan (JTAG) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the FPGA. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). FPGA configuration using the Boundary-Scan mode is compatible with the IEEE Std 1149.1-1993 standard and IEEE Std 1532 for In-System Configurable (ISC) devices.

Configuration through the boundary-scan port is always available, regardless of the selected configuration mode. In some cases, however, the mode pin setting may affect proper programming of the device due to various interactions. For example, if the mode pins are set to Master Serial or Master Parallel mode, and the associated PROM is already programmed with a valid configuration image, then there is potential for configuration interference between the JTAG and PROM data. Selecting the Boundary-Scan mode disables the other modes and is the most reliable mode when programming via JTAG.

Configuration Sequence

The configuration of Spartan-3 devices is a three-stage process that occurs after Power-On Reset or the assertion of PROG_B. POR occurs after the V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 4 supplies have reached their respective maximum input threshold levels (see Table 29, page 59). After POR, the three-stage process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process. A flow diagram for the configuration sequence of the Serial and Parallel modes is shown in Figure 29. The flow diagram for the Boundary-Scan configuration sequence appears in Figure 30.

Initial Spartan-3 FPGA mask revisions have a limit on how fast the V_{CCO} supply can ramp. The minimum allowed V_{CCO} ramp rate appears as T_{CCO} in Table 30, page 60. The minimum rate is affected by the package inductance. Consequently, the ball grid array and chip-scale packages (CP132, FT256, FG456, FG676, and FG900) allow a faster ramp rate than the quad-flat packages (VQ100, TQ144, and PQ208).

Configuration Data Retention, Brown-Out

The FPGA's configuration data is stored in robust CMOS configuration latches. The data in these latches is retained even when the voltages drop to the minimum levels necessary to preserve RAM contents. This is specified in Table 31, page 60.

If, after configuration, the V_{CCAUX} or V_{CCINT} supply drops below its data retention voltage, clear the current device configuration using one of the following methods:

- Force the V_{CCAUX} or V_{CCINT} supply voltage below the minimum Power On Reset (POR) voltage threshold Table 29, page 59).
- Assert PROG_B Low.

The POR circuit does not monitor the VCCO_4 supply after configuration. Consequently, dropping the VCCO_4 voltage does not reset the device by triggering a Power-On Reset (POR) event.

No Internal Charge Pumps or Free-Running Oscillators

Some system applications are sensitive to sources of analog noise. Spartan-3 FPGA circuitry is fully static and does not employ internal charge pumps.

The CCLK configuration clock is active during the FPGA configuration process. After configuration completes, the CCLK oscillator is automatically disabled unless the Bitstream Generator (BitGen) option ***Persist=Yes***. See Module 4: Table 80, page 125.

Spartan-3 FPGAs optionally support a featured called Digitally Controlled Impedance (DCI). When used in an application, the DCI logic uses an internal oscillator. The DCI logic is only enabled if the FPGA application specifies an I/O standard that requires DCI (LVDCI_33, LVDCI_25, etc.). If DCI is not used, the associated internal oscillator is also disabled.

In summary, unless an application uses the ***Persist=Yes*** option or specifies a DCI I/O standard, an FPGA with no external switching remains fully static.

Switching Characteristics

All Spartan-3 devices are available in two speed grades: –4 and the higher performance –5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reported delays may still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Production-quality systems must use FPGA designs compiled using a Production status speed file. FPGAs designs using a less mature speed file designation may only be used during system prototyping or preproduction qualification. FPGA designs using Advance or Preliminary status speed files should never be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

Xilinx ISE Software Updates: http://www.xilinx.com/support/download/index.htm

All specified limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the following applies: Parameter values apply to all Spartan-3 devices. All parameters representing voltages are measured with respect to GND.

Selected timing parameters and their representative values are included below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3 FPGA v1.38 speed files are the original source for many but not all of the values. The v1.38 speed files are available in Xilinx Integrated Software Environment (ISE) software version 8.2i.

The speed grade designations for these files are shown in Table 39. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 39: **Spartan-3 FPGA Speed Grade Designations (ISE v8.2i or Later)**

Device	Advance	Preliminary	Production
XC3S50			-4, -5 (v1.37 and later)
XC3S200			
XC3S400			
XC3S1000			
XC3S1500			
XC3S2000			
XC3S4000			
XC3S5000			-4, -5 (v1.38 and later)

Table 41: **System-Synchronous Pin-to-Pin Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IOBDELAY = IFD, without DCM	XC3S50	–0.98	–0.93	ns
			XC3S200	–0.40	–0.35	ns
			XC3S400	–0.27	–0.22	ns
			XC3S1000	–1.19	–1.14	ns
			XC3S1500	–1.43	–1.38	ns
			XC3S2000	–2.33	–2.28	ns
			XC3S4000	–2.47	–2.42	ns
			XC3S5000	–2.66	–2.61	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *subtract* the appropriate adjustment from Table 44. If this is true of the data Input, *add* the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *add* the appropriate Input adjustment from Table 44. If this is true of the data Input, *subtract* the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Table 42: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Setup Times						
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2), IOBDELAY = NONE	XC3S50	1.65	1.89	ns
			XC3S200	1.37	1.57	ns
			XC3S400	1.37	1.57	ns
			XC3S1000	1.65	1.89	ns
			XC3S1500	1.65	1.89	ns
			XC3S2000	1.65	1.89	ns
			XC3S4000	1.73	1.99	ns
			XC3S5000	1.82	2.09	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the IFF's ICLK input. The Input Delay is programmed.	LVCMOS25(2), IOBDELAY = IFD	XC3S50	4.39	5.04	ns
			XC3S200	4.76	5.47	ns
			XC3S400	4.63	5.32	ns
			XC3S1000	5.02	5.76	ns
			XC3S1500	5.40	6.20	ns
			XC3S2000	6.68	7.68	ns
			XC3S4000	7.16	8.24	ns
			XC3S5000	7.33	8.42	ns

Table 70: **Spartan-3 FPGA Pin Definitions *(Cont'd)***

Pin Name	Direction	Description
TDI	Input	**JTAG Test Data Input:** TDI is the serial data input for all JTAG instruction and data registers. This pin has an internal pull-up resistor to VCCAUX during configuration.
TMS	Input	**JTAG Test Mode Select:** The serial TMS input controls the operation of the JTAG port. This pin has an internal pull-up resistor to VCCAUX during configuration.
TDO	Output	**JTAG Test Data Output:** TDO is the serial data output for all JTAG instruction and data registers. This pin has an internal pull-up resistor to VCCAUX during configuration.
VCCO: I/O bank output voltage supply pins		
VCCO_#	Supply	**Power Supply for Output Buffer Drivers (per bank):** These pins power the output drivers within a specific I/O bank.
VCCAUX: Auxiliary voltage supply pins		
VCCAUX	Supply	**Power Supply for Auxiliary Circuits:** +2.5V power pins for auxiliary circuits, including the Digital Clock Managers (DCMs), the dedicated configuration pins (CONFIG), and the dedicated JTAG pins. All VCCAUX pins must be connected.
VCCINT: Internal core voltage supply pins		
VCCINT	Supply	**Power Supply for Internal Core Logic:** +1.2V power pins for the internal logic. All pins must be connected.
GND: Ground supply pins		
GND	Supply	**Ground:** Ground pins, which are connected to the power supply's return path. All pins must be connected.
N.C.: Unconnected package pins		
N.C.		**Unconnected Package Pin:** These package pins are unconnected.

Notes:

1. All unused inputs and bidirectional pins must be tied either High or Low. For unused enable inputs, apply the level that disables the associated function. One common approach is to activate internal pull-up or pull-down resistors. An alternative approach is to externally connect the pin to either VCCO or GND.
2. All outputs are of the totem-pole type — i.e., they can drive High as well as Low logic levels — except for the cases where "Open Drain" is indicated. The latter can only drive a Low logic level and require a pull-up resistor to produce a High logic level.

Detailed, Functional Pin Descriptions

I/O Type: Unrestricted, General-purpose I/O Pins

After configuration, I/O-type pins are inputs, outputs, bidirectional I/O, three-state outputs, open-drain outputs, or open-source outputs, as defined in the application

Pins labeled "IO" support all SelectIO™ interface signal standards except differential standards. A given device at most only has a few of these pins.

A majority of the general-purpose I/O pins are labeled in the format "IO_Lxxy_#". These pins support all SelectIO signal standards, including the differential standards such as LVDS, ULVDS, BLVDS, RSDS, or LDT.

For additional information, see IOBs, page 10

Table 71: **Dual-Purpose Pins Used in Master or Slave Serial Mode**

Pin Name	Direction	Description
DIN	Input	**Serial Data Input:** During the Master or Slave Serial configuration modes, DIN is the serial configuration data input, and all data is synchronized to the rising CCLK edge. After configuration, this pin is available as a user I/O. This signal is located in Bank 4 and its output voltage determined by VCCO_4. The BitGen option ***Persist*** permits this pin to retain its configuration function in the User mode.
DOUT	Output	**Serial Data Output:** In a multi-FPGA design where all the FPGAs use serial mode, connect the DOUT output of one FPGA—in either Master or Slave Serial mode—to the DIN input of the next FPGA—in Slave Serial mode—so that configuration data passes from one to the next, in daisy-chain fashion. This "daisy chain" permits sequential configuration of multiple FPGAs. This signal is located in Bank 4 and its output voltage determined by VCCO_4. The BitGen option ***Persist*** permits this pin to retain its configuration function in the User mode.
INIT_B	Bidirectional (open-drain)	**Initializing Configuration Memory/Configuration Error:** Just after power is applied, the FPGA produces a Low-to-High transition on this pin indicating that initialization (*i.e.*, clearing) of the configuration memory has finished. Before entering the User mode, this pin functions as an open-drain output, which requires a pull-up resistor in order to produce a High logic level. In a multi-FPGA design, tie (wire AND) the INIT_B pins from all FPGAs together so that the common node transitions High only after all of the FPGAs have been successfully initialized. Externally holding this pin Low beyond the initialization phase delays the start of configuration. This action stalls the FPGA at the configuration step just before the mode select pins are sampled. During configuration, the FPGA indicates the occurrence of a data (i.e., CRC) error by asserting INIT_B Low. This signal is located in Bank 4 and its output voltage determined by VCCO_4. The BitGen option ***Persist*** permits this pin to retain its configuration function in the User mode.

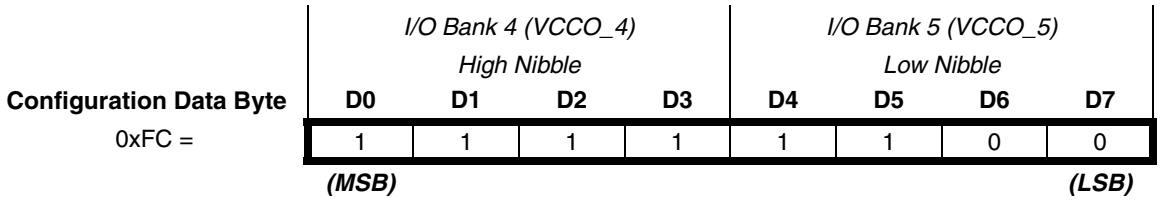


Figure 41: **Configuration Data Byte Mapping to D0-D7 Bits**

Parallel Configuration Modes (SelectMAP)

This section describes the dual-purpose configuration pins used during the Master and Slave Parallel configuration modes, sometimes also called the SelectMAP modes. In both Master and Slave Parallel configuration modes, D0-D7 form the byte-wide configuration data input. See Table 75 for Mode Select pin settings required for Parallel modes.

As shown in Figure 41, D0 is the most-significant bit while D7 is the least-significant bit. Bits D0-D3 form the high nibble of the byte and bits D4-D7 form the low nibble.

In the Parallel configuration modes, both the VCCO_4 and VCCO_5 voltage supplies are required and must both equal the voltage of the attached configuration device, typically either 2.5V or 3.3V.

Assert Low both the chip-select pin, CS_B, and the read/write control pin, RDWR_B, to write the configuration data byte presented on the D0-D7 pins to the FPGA on a rising-edge of the configuration clock, CCLK. The order of CS_B and RDWR_B does not matter, although RDWR_B must be asserted throughout the configuration process. If RDWR_B is de-asserted during configuration, the FPGA aborts the configuration operation.

After configuration, these pins are available as general-purpose user I/O. However, the SelectMAP configuration interface is optionally available for debugging and dynamic reconfiguration. To use these SelectMAP pins after configuration, set the Persist bitstream generation option.

The Readback debugging option, for example, requires the Persist bitstream generation option. During Readback mode, assert CS_B Low, along with RDWR_B High, to read a configuration data byte from the FPGA to the D0-D7 bus on a rising CCLK edge. During Readback mode, D0-D7 are output pins.

In all the cases, the configuration data and control signals are synchronized to the rising edge of the CCLK clock signal.

Table 72: **Dual-Purpose Configuration Pins for Parallel (SelectMAP) Configuration Modes *(Cont'd)***

<table>
<tr><th>Pin Name</th><th>Direction</th><th>Description</th></tr>
<tr><td>BUSY</td><td>Output</td><td>Configuration Data Rate Control for Parallel Mode:
In the Slave and Master Parallel modes, BUSY throttles the rate at which configuration data is loaded. BUSY is only necessary if CCLK operates at greater than 50 MHz. Ignore BUSY for frequencies of 50 MHz and below.
When BUSY is Low, the FPGA accepts the next configuration data byte on the next rising CCLK edge for which CS_B and RDWR_B are Low. When BUSY is High, the FPGA ignores the next configuration data byte. The next configuration data value must be held or reloaded until the next rising CCLK edge when BUSY is Low. When CS_B is High, BUSY is in a high impedance state.
<table><tr><th>BUSY</th><th>Function</th></tr><tr><td>0</td><td>The FPGA is ready to accept the next configuration data byte.</td></tr><tr><td>1</td><td>The FPGA is busy processing the current configuration data byte and is not ready to accept the next byte.</td></tr><tr><td>Hi-Z</td><td>If CS_B is High, then BUSY is high impedance.</td></tr></table>This signal is located in Bank 4 and its output voltage is determined by VCCO_4. The BitGen option Persist permits this pin to retain its configuration function in the User mode.</td></tr>
<tr><td>INIT_B</td><td>Bidirectional (open-drain)</td><td>Initializing Configuration Memory/Configuration Error (active-Low):
See description under Serial Configuration Modes, page 112.</td></tr>
</table>

JTAG Configuration Mode

In the JTAG configuration mode all dual-purpose configuration pins are unused and behave exactly like user-I/O pins, as shown in Table 79. See Table 75 for Mode Select pin settings required for JTAG mode.

Dual-Purpose Pin I/O Standard During Configuration

During configuration, the dual-purpose pins default to CMOS input and output levels for the associated VCCO voltage supply pins. For example, in the Parallel configuration modes, both VCCO_4 and VCCO_5 are required. If connected to +2.5V, then the associated pins conform to the LVCMOS25 I/O standard. If connected to +3.3V, then the pins drive LVCMOS output levels and accept either LVTTL or LVCMOS input levels.

Dual-Purpose Pin Behavior After Configuration

After the configuration process completes, these pins, if they were borrowed during configuration, become user-I/O pins available to the application. If a dual-purpose configuration pin is not used during the configuration process—*i.e.*, the parallel configuration pins when using serial mode—then the pin behaves exactly like a general-purpose I/O. See I/O Type: Unrestricted, General-purpose I/O Pins section.

DCI: User I/O or Digitally Controlled Impedance Resistor Reference Input

These pins are individual user-I/O pins unless one of the I/O standards used in the bank requires the Digitally Controlled Impedance (DCI) feature. If DCI is used, then 1% precision resistors connected to the VRP_# and VRN_# pins match the impedance on the input or output buffers of the I/O standards that use DCI within the bank. The '#' character in the pin name indicates the associated I/O bank and is an integer, 0 through 7.

There are two DCI pins per I/O bank, except in the CP132 and TQ144 packages, which do not have any DCI inputs for Bank 5.

VRP and VRN Impedance Resistor Reference Inputs

The 1% precision impedance-matching resistor attached to the VRP_# pin controls the pull-up impedance of PMOS transistor in the input or output buffer. Consequently, the VRP_# pin must connect to ground. The 'P' character in "VRP" indicates that this pin controls the I/O buffer's PMOS transistor impedance. The VRP_# pin is used for both single and split termination.

Table 87: **VQ100 Package Pinout *(Cont'd)***

Bank	XC3S50 XC3S200 Pin Name	VQ100 Pin Number	Type
6	IO_L40P_6/VREF_6	P13	VREF
6	VCCO_6	P19	VCCO
7	IO_L01N_7/VRP_7	P2	DCI
7	IO_L01P_7/VRN_7	P1	DCI
7	IO_L21N_7	P5	I/O
7	IO_L21P_7	P4	I/O
7	IO_L23N_7	P9	I/O
7	IO_L23P_7	P8	I/O
7	IO_L40N_7/VREF_7	P12	VREF
7	IO_L40P_7	P11	I/O
7	VCCO_7	P6	VCCO
N/A	GND	P3	GND
N/A	GND	P10	GND
N/A	GND	P20	GND
N/A	GND	P29	GND
N/A	GND	P41	GND
N/A	GND	P56	GND
N/A	GND	P66	GND
N/A	GND	P73	GND
N/A	GND	P82	GND
N/A	GND	P95	GND
N/A	VCCAUX	P7	VCCAUX
N/A	VCCAUX	P33	VCCAUX
N/A	VCCAUX	P58	VCCAUX
N/A	VCCAUX	P84	VCCAUX
N/A	VCCINT	P18	VCCINT
N/A	VCCINT	P45	VCCINT
N/A	VCCINT	P69	VCCINT
N/A	VCCINT	P93	VCCINT
VCCAUX	CCLK	P52	CONFIG
VCCAUX	DONE	P51	CONFIG
VCCAUX	HSWAP_EN	P98	CONFIG
VCCAUX	M0	P25	CONFIG
VCCAUX	M1	P24	CONFIG
VCCAUX	M2	P26	CONFIG
VCCAUX	PROG_B	P99	CONFIG
VCCAUX	TCK	P77	JTAG
VCCAUX	TDI	P100	JTAG

Table 93: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	P61	DCI
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	P65	VREF
5	IO_L27P_5	IO_L27P_5	P64	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	P68	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	P67	DUAL
5	IO_L31N_5/D4	IO_L31N_5/D4	P74	DUAL
5	IO_L31P_5/D5	IO_L31P_5/D5	P72	DUAL
5	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	P77	GCLK
5	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	P76	GCLK
5	VCCO_5	VCCO_5	P60	VCCO
5	VCCO_5	VCCO_5	P73	VCCO
6	N.C. (◆)	IO/VREF_6	P50	VREF
6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	P52	DCI
6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	P51	DCI
6	IO_L19N_6	IO_L19N_6	P48	I/O
6	IO_L19P_6	IO_L19P_6	P46	I/O
6	IO_L20N_6	IO_L20N_6	P45	I/O
6	IO_L20P_6	IO_L20P_6	P44	I/O
6	IO_L21N_6	IO_L21N_6	P43	I/O
6	IO_L21P_6	IO_L21P_6	P42	I/O
6	IO_L22N_6	IO_L22N_6	P40	I/O
6	IO_L22P_6	IO_L22P_6	P39	I/O
6	IO_L23N_6	IO_L23N_6	P37	I/O
6	IO_L23P_6	IO_L23P_6	P36	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	P35	VREF
6	IO_L24P_6	IO_L24P_6	P34	I/O
6	N.C. (◆)	IO_L39N_6	P33	I/O
6	N.C. (◆)	IO_L39P_6	P31	I/O
6	IO_L40N_6	IO_L40N_6	P29	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	P28	VREF
6	VCCO_6	VCCO_6	P32	VCCO
6	VCCO_6	VCCO_6	P49	VCCO
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	P3	DCI
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	P2	DCI
7	N.C. (◆)	IO_L16N_7	P5	I/O
7	N.C. (◆)	IO_L16P_7/VREF_7	P4	VREF
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	P9	VREF
7	IO_L19P_7	IO_L19P_7	P7	I/O
7	IO_L20N_7	IO_L20N_7	P11	I/O
7	IO_L20P_7	IO_L20P_7	P10	I/O

User I/Os by Bank

Table 94 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S50 in the PQ208 package. Similarly, Table 95 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S200 and XC3S400 in the PQ208 package.

Table 94: **User I/Os Per Bank for XC3S50 in PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	15	9	0	2	2	2
	1	15	9	0	2	2	2
Right	2	16	13	0	2	2	0
	3	16	12	0	2	2	0
Bottom	4	15	3	6	2	2	2
	5	15	3	6	2	2	2
Left	6	16	12	0	2	2	0
	7	16	12	0	2	2	0

Table 95: **User I/Os Per Bank for XC3S200 and XC3S400 in PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	16	9	0	2	3	2
	1	15	9	0	2	2	2
Right	2	19	14	0	2	3	0
	3	20	15	0	2	3	0
Bottom	4	17	4	6	2	3	2
	5	15	3	6	2	2	2
Left	6	19	14	0	2	3	0
	7	20	15	0	2	3	0

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
2	IO_L20N_2	E17	I/O
2	IO_L20P_2	E18	I/O
2	IO_L21N_2	F15	I/O
2	IO_L21P_2	E15	I/O
2	IO_L22N_2	F14	I/O
2	IO_L22P_2	G14	I/O
2	IO_L23N_2/VREF_2	G18	VREF
2	IO_L23P_2	F17	I/O
2	IO_L24N_2	G15	I/O
2	IO_L24P_2	G16	I/O
2	IO_L27N_2	H13	I/O
2	IO_L27P_2	H14	I/O
2	IO_L34N_2/VREF_2	H16	VREF
2	IO_L34P_2	H15	I/O
2	IO_L35N_2	H17	I/O
2	IO_L35P_2	H18	I/O
2	IO_L39N_2	J18	I/O
2	IO_L39P_2	J17	I/O
2	IO_L40N_2	J15	I/O
2	IO_L40P_2/VREF_2	J14	VREF
2	VCCO_2	F16	VCCO
2	VCCO_2	H12	VCCO
2	VCCO_2	J12	VCCO
3	IO	K15	I/O
3	IO_L01N_3/VRP_3	T17	DCI
3	IO_L01P_3/VRN_3	T16	DCI
3	IO_L16N_3	T18	I/O
3	IO_L16P_3	U18	I/O
3	IO_L17N_3	P16	I/O
3	IO_L17P_3/VREF_3	R16	VREF
3	IO_L19N_3	R17	I/O
3	IO_L19P_3	R18	I/O
3	IO_L20N_3	P18	I/O
3	IO_L20P_3	P17	I/O
3	IO_L21N_3	P15	I/O
3	IO_L21P_3	N15	I/O
3	IO_L22N_3	M14	I/O
3	IO_L22P_3	N14	I/O
3	IO_L23N_3	M15	I/O
3	IO_L23P_3/VREF_3	M16	VREF

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	M25	VREF
2	IO_L34P_2	IO_L34P_2	IO_L34P_2	IO_L34P_2	IO_L34P_2	M26	I/O
2	IO_L35N_2	IO_L35N_2	IO_L35N_2	IO_L35N_2	IO_L35N_2	N19	I/O
2	IO_L35P_2	IO_L35P_2	IO_L35P_2	IO_L35P_2	IO_L35P_2	N20	I/O
2	IO_L38N_2	IO_L38N_2	IO_L38N_2	IO_L38N_2	IO_L38N_2	N21	I/O
2	IO_L38P_2	IO_L38P_2	IO_L38P_2	IO_L38P_2	IO_L38P_2	N22	I/O
2	IO_L39N_2	IO_L39N_2	IO_L39N_2	IO_L39N_2	IO_L39N_2	N23	I/O
2	IO_L39P_2	IO_L39P_2	IO_L39P_2	IO_L39P_2	IO_L39P_2	N24	I/O
2	IO_L40N_2	IO_L40N_2	IO_L40N_2	IO_L40N_2	IO_L40N_2	N25	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	N26	VREF
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	G24	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	J19	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	K19	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	L18	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	L24	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	M18	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	N17	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	N18	VCCO
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	AA22	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	AA21	DCI
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	AB24	VREF
3	IO_L02P_3	IO_L02P_3	IO_L02P_3	IO_L02P_3	IO_L02P_3	AB23	I/O
3	IO_L03N_3	IO_L03N_3	IO_L03N_3	IO_L03N_3	IO_L03N_3	AC26	I/O
3	IO_L03P_3	IO_L03P_3	IO_L03P_3	IO_L03P_3	IO_L03P_3	AC25	I/O
3	N.C. (◆)	IO_L05N_3	IO_L05N_3	IO_L05N_3	IO_L05N_3	Y21	I/O
3	N.C. (◆)	IO_L05P_3	IO_L05P_3	IO_L05P_3	IO_L05P_3	Y20	I/O
3	N.C. (◆)	IO_L06N_3	IO_L06N_3	IO_L06N_3	IO_L06N_3	AB26	I/O
3	N.C. (◆)	IO_L06P_3	IO_L06P_3	IO_L06P_3	IO_L06P_3	AB25	I/O
3	N.C. (◆)	IO_L07N_3	IO_L07N_3	IO_L07N_3	IO_L07N_3	AA24	I/O
3	N.C. (◆)	IO_L07P_3	IO_L07P_3	IO_L07P_3	IO_L07P_3	AA23	I/O
3	N.C. (◆)	IO_L08N_3	IO_L08N_3	IO_L08N_3	IO_L08N_3	Y23	I/O
3	N.C. (◆)	IO_L08P_3	IO_L08P_3	IO_L08P_3	IO_L08P_3	Y22	I/O
3	N.C. (◆)	IO_L09N_3	IO_L09N_3	IO_L09N_3	IO_L09N_3	AA26	I/O
3	N.C. (◆)	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	AA25	VREF
3	N.C. (◆)	IO_L10N_3	IO_L10N_3	IO_L10N_3	IO_L10N_3	W21	I/O
3	N.C. (◆)	IO_L10P_3	IO_L10P_3	IO_L10P_3	IO_L10P_3	W20	I/O
3	IO_L14N_3	IO_L14N_3	IO_L14N_3	IO_L14N_3	IO_L14N_3	Y26	I/O
3	IO_L14P_3	IO_L14P_3	IO_L14P_3	IO_L14P_3	IO_L14P_3	Y25	I/O
3	IO_L16N_3	IO_L16N_3	IO_L16N_3	IO_L16N_3	IO_L16N_3	V21	I/O
3	IO_L16P_3	IO_L16P_3	IO_L16P_3	IO_L16P_3	IO_L16P_3	W22	I/O
3	IO_L17N_3	IO_L17N_3	IO_L17N_3	IO_L17N_3	IO_L17N_3	W24	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	W23	VREF

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
6	IO_L05P_6	IO_L05P_6	AE5	I/O
6	IO_L06N_6	IO_L06N_6	AE3	I/O
6	IO_L06P_6	IO_L06P_6	AE2	I/O
6	IO_L07N_6	IO_L07N_6	AD4	I/O
6	IO_L07P_6	IO_L07P_6	AD3	I/O
6	IO_L08N_6	IO_L08N_6	AD2	I/O
6	IO_L08P_6	IO_L08P_6	AD1	I/O
6	IO_L09N_6/VREF_6	IO_L09N_6/VREF_6	AD6	VREF
6	IO_L09P_6	IO_L09P_6	AC7	I/O
6	IO_L10N_6	IO_L10N_6	AC6	I/O
6	IO_L10P_6	IO_L10P_6	AC5	I/O
6	IO_L11N_6	IO_L11N_6	AC4	I/O
6	IO_L11P_6	IO_L11P_6	AC3	I/O
6	IO_L13N_6	IO_L13N_6	AC2	I/O
6	IO_L13P_6/VREF_6	IO_L13P_6/VREF_6	AC1	VREF
6	IO_L14N_6	IO_L14N_6	AB5	I/O
6	IO_L14P_6	IO_L14P_6	AB4	I/O
6	IO_L15N_6	IO_L15N_6	AB2	I/O
6	IO_L15P_6	IO_L15P_6	AB1	I/O
6	IO_L16N_6	IO_L16N_6	AB8	I/O
6	IO_L16P_6	IO_L16P_6	AA9	I/O
6	IO_L17N_6	IO_L17N_6	AA7	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	AA6	VREF
6	IO_L19N_6	IO_L19N_6	AA3	I/O
6	IO_L19P_6	IO_L19P_6	AA2	I/O
6	IO_L20N_6	IO_L20N_6	AA10	I/O
6	IO_L20P_6	IO_L20P_6	Y10	I/O
6	IO_L21N_6	IO_L21N_6	Y8	I/O
6	IO_L21P_6	IO_L21P_6	Y7	I/O
6	IO_L22N_6	IO_L22N_6	Y6	I/O
6	IO_L22P_6	IO_L22P_6	Y5	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	Y2	VREF
6	IO_L24P_6	IO_L24P_6	Y1	I/O
6	N.C. (◆)	IO_L25N_6	W9	I/O
6	N.C. (◆)	IO_L25P_6	W8	I/O
6	IO_L26N_6	IO_L26N_6	W7	I/O
6	IO_L26P_6	IO_L26P_6	W6	I/O
6	IO_L27N_6	IO_L27N_6	W4	I/O
6	IO_L27P_6	IO_L27P_6	W3	I/O
6	IO_L28N_6	IO_L28N_6	W2	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
7	IO_L23N_7	IO_L23N_7	L3	I/O
7	IO_L23P_7	IO_L23P_7	L4	I/O
7	IO_L24N_7	IO_L24N_7	L1	I/O
7	IO_L24P_7	IO_L24P_7	L2	I/O
7	N.C. (◆)	IO_L25N_7	M6	I/O
7	N.C. (◆)	IO_L25P_7	M7	I/O
7	IO_L26N_7	IO_L26N_7	M3	I/O
7	IO_L26P_7	IO_L26P_7	M4	I/O
7	IO_L27N_7	IO_L27N_7	M1	I/O
7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	M2	VREF
7	IO_L28N_7	IO_L28N_7	N10	I/O
7	IO_L28P_7	IO_L28P_7	M10	I/O
7	IO_L29N_7	IO_L29N_7	N8	I/O
7	IO_L29P_7	IO_L29P_7	N9	I/O
7	IO_L31N_7	IO_L31N_7	N1	I/O
7	IO_L31P_7	IO_L31P_7	N2	I/O
7	IO_L32N_7	IO_L32N_7	P9	I/O
7	IO_L32P_7	IO_L32P_7	P10	I/O
7	IO_L33N_7	IO_L33N_7	P6	I/O
7	IO_L33P_7	IO_L33P_7	P7	I/O
7	IO_L34N_7	IO_L34N_7	P2	I/O
7	IO_L34P_7	IO_L34P_7	P3	I/O
7	IO_L35N_7	IO_L35N_7	R9	I/O
7	IO_L35P_7	IO_L35P_7	R10	I/O
7	IO_L37N_7	IO_L37N_7	R7	I/O
7	IO_L37P_7/VREF_7	IO_L37P_7/VREF_7	R8	VREF
7	IO_L38N_7	IO_L38N_7	R5	I/O
7	IO_L38P_7	IO_L38P_7	R6	I/O
7	IO_L39N_7	IO_L39N_7	R3	I/O
7	IO_L39P_7	IO_L39P_7	R4	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	R1	VREF
7	IO_L40P_7	IO_L40P_7	R2	I/O
7	N.C. (◆)	IO_L46N_7	M8	I/O
7	N.C. (◆)	IO_L46P_7	M9	I/O
7	N.C. (◆)	IO_L49N_7	N6	I/O
7	N.C. (◆)	IO_L49P_7	M5	I/O
7	N.C. (◆)	IO_L50N_7	N4	I/O
7	N.C. (◆)	IO_L50P_7	N5	I/O
7	VCCO_7	VCCO_7	E3	VCCO
7	VCCO_7	VCCO_7	J3	VCCO

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L48P_3	IO_L48P_3	AB24	I/O
3	N.C. (◆)	IO_L49N_3	AA26	I/O
3	N.C. (◆)	IO_L49P_3	AA25	I/O
3	IO_L50N_3	IO_L50N_3	Y25	I/O
3	IO_L50P_3	IO_L50P_3	Y24	I/O
3	N.C. (◆)	IO_L51N_3	V24	I/O
3	N.C. (◆)	IO_L51P_3	W24	I/O
3	VCCO_3	VCCO_3	AA23	VCCO
3	VCCO_3	VCCO_3	AB23	VCCO
3	VCCO_3	VCCO_3	AB29	VCCO
3	VCCO_3	VCCO_3	AB33	VCCO
3	VCCO_3	VCCO_3	AD27	VCCO
3	VCCO_3	VCCO_3	AD31	VCCO
3	VCCO_3	VCCO_3	AG28	VCCO
3	VCCO_3	VCCO_3	AG32	VCCO
3	VCCO_3	VCCO_3	AL32	VCCO
3	VCCO_3	VCCO_3	W23	VCCO
3	VCCO_3	VCCO_3	W31	VCCO
3	VCCO_3	VCCO_3	Y23	VCCO
3	VCCO_3	VCCO_3	Y27	VCCO
4	IO	IO	AD18	I/O
4	IO	IO	AD19	I/O
4	IO	IO	AD20	I/O
4	IO	IO	AD22	I/O
4	IO	IO	AE18	I/O
4	IO	IO	AE19	I/O
4	IO	IO	AE22	I/O
4	N.C. (◆)	IO	AE24	I/O
4	IO	IO	AF24	I/O
4	N.C. (◆)	IO	AF26	I/O
4	IO	IO	AG26	I/O
4	IO	IO	AG27	I/O
4	IO	IO	AJ27	I/O
4	IO	IO	AJ29	I/O
4	IO	IO	AK25	I/O
4	IO	IO	AN26	I/O
4	IO/VREF_4	IO/VREF_4	AF21	VREF
4	IO/VREF_4	IO/VREF_4	AH23	VREF
4	IO/VREF_4	IO/VREF_4	AK18	VREF
4	IO/VREF_4	IO/VREF_4	AL30	VREF

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	VCCAUX	VCCAUX	Y5	VCCAUX
N/A	VCCINT	VCCINT	AA13	VCCINT
N/A	VCCINT	VCCINT	AA22	VCCINT
N/A	VCCINT	VCCINT	AB13	VCCINT
N/A	VCCINT	VCCINT	AB14	VCCINT
N/A	VCCINT	VCCINT	AB15	VCCINT
N/A	VCCINT	VCCINT	AB16	VCCINT
N/A	VCCINT	VCCINT	AB19	VCCINT
N/A	VCCINT	VCCINT	AB20	VCCINT
N/A	VCCINT	VCCINT	AB21	VCCINT
N/A	VCCINT	VCCINT	AB22	VCCINT
N/A	VCCINT	VCCINT	AC12	VCCINT
N/A	VCCINT	VCCINT	AC17	VCCINT
N/A	VCCINT	VCCINT	AC18	VCCINT
N/A	VCCINT	VCCINT	AC23	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	M23	VCCINT
N/A	VCCINT	VCCINT	N13	VCCINT
N/A	VCCINT	VCCINT	N14	VCCINT
N/A	VCCINT	VCCINT	N15	VCCINT
N/A	VCCINT	VCCINT	N16	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	N20	VCCINT
N/A	VCCINT	VCCINT	N21	VCCINT
N/A	VCCINT	VCCINT	N22	VCCINT
N/A	VCCINT	VCCINT	P13	VCCINT
N/A	VCCINT	VCCINT	P22	VCCINT
N/A	VCCINT	VCCINT	R13	VCCINT
N/A	VCCINT	VCCINT	R22	VCCINT
N/A	VCCINT	VCCINT	T13	VCCINT
N/A	VCCINT	VCCINT	T22	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT
N/A	VCCINT	VCCINT	U23	VCCINT
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	V23	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	W22	VCCINT
N/A	VCCINT	VCCINT	Y13	VCCINT

FG1156 Footprint

Top Left Corner of FG1156 Package (Top View)

XC3S4000 (712 max. user I/O)

621 **I/O:** Unrestricted, general-purpose user I/O

55 **VREF:** User I/O or input voltage reference for bank

73 **N.C.:** Unconnected pins for XC3S4000 (◆)

XC3S5000 (784 max. user I/O)

692 **I/O:** Unrestricted, general-purpose user I/O

56 **VREF:** User I/O or input voltage reference for bank

1 **N.C.:** Unconnected pins for XC3S5000 (■)

Bank 0

Bank 7

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	GND	GND	I/O L01P_0 VRN_0	I/O L02P_0	GND	I/O L05P_0 VREF_0	I/O L34P_0 ◆	I/O L36P_0	GND	I/O L38P_0	I/O L40P_0 ◆	I/O L15P_0	GND	I/O L22P_0	I/O L26P_0 VREF_0	GND	I/O L32P_0 GCLK6
B	GND	GND	I/O L01N_0 VRP_0	I/O L02N_0	I/O L03P_0	I/O L05N_0	I/O L34N_0 ◆	I/O L36N_0	I/O	I/O L38N_0	I/O L40N_0 ◆	I/O L15N_0	VCCO_0	I/O L22N_0	I/O L26N_0	I/O L28P_0	I/O L32N_0 GCLK7
C	I/O L01N_7 VRP_7	I/O L01P_7 VRN_7	GND	VCCO_0	I/O L03N_0	I/O L04P_0	I/O L33P_0 ◆	VCCO_0	I/O L08P_0	I/O L37P_0	GND	I/O L14P_0	I/O L17P_0	I/O L21P_0	I/O L25P_0	I/O L28N_0	I/O L31P_0 VREF_0
D	I/O L02N_7	I/O L02P_7	VCCO_7	PROG_B	IO VREF_0	I/O L04N_0	I/O L33N_0 ◆	I/O L35P_0	I/O L08N_0	I/O L37N_0	VCCO_0	I/O L14N_0	I/O L17N_0	I/O L21N_0	I/O L25N_0	VCCO_0	I/O L31N_0
E	GND	I/O L03N_7 VREF_7	I/O L03P_7	TDI	GND	VCCAUX	I/O L06P_0	I/O L35N_0	GND	IO VREF_0	VCCAUX	I/O L13P_0	GND	I/O L20P_0	VCCAUX	GND	I/O
F	I/O L05N_7	I/O L05P_7	I/O L04N_7	I/O L04P_7	VCCAUX	I/O	I/O L06N_0	I/O	I/O L07P_0	I/O L10P_0	I/O L39P_0 ◆	I/O L13N_0	VCCO_0	I/O L20N_0	I/O L24P_0	I/O L27P_0	I/O L30P_0
G	I/O	I/O	I/O L41N_7 ◆	I/O L41P_7 ◆	I/O L06N_7	I/O L06P_7	GND	VCCO_0	I/O L07N_0	I/O L10N_0	I/O L39N_0 ◆	I/O	I/O L16P_0	I/O L19P_0	I/O L24N_0	I/O L27N_0	I/O L30N_0
H	I/O L08N_7	I/O L08P_7	VCCO_7	I/O L10P_7 VREF_7	I/O L07N_7	I/O L07P_7	VCCO_7	I/O	I/O	I/O L09P_0	VCCO_0	I/O L12P_0	I/O L16N_0	I/O L19N_0	VCCO_0	VCCAUX	I/O L29P_0
J	GND	I/O L11N_7	I/O L11P_7	I/O L10N_7	GND	I/O L09N_7	I/O L09P_7	I/O L12P_7	I/O ◆	I/O L09N_0	I/O	I/O L12N_0	GND	IO VREF_0	I/O L23P_0	GND	I/O L29N_0
K	I/O L16N_7	I/O L16P_7 VREF_7	I/O L15N_7	I/O L15P_7	I/O L14N_7	I/O L14P_7	I/O L13N_7	I/O L13P_7	I/O L12N_7	GND	I/O ◆	I/O L11P_0	I/O	I/O L18P_0	I/O L23N_0	I/O	I/O
L	I/O L19N_7 VREF_7	I/O L19P_7	GND	VCCO_7	VCCAUX	I/O L44N_7 ◆	I/O L44P_7 ◆	VCCO_7	I/O L17N_7	I/O L17P_7	HSWAP_ EN	I/O L11N_0	I/O	I/O L18N_0	IO VREF_0	I/O	I/O
M	I/O L45N_7	I/O L45P_7	I/O L23N_7	I/O L23P_7	I/O L22N_7	I/O L22P_7	I/O L21N_7	I/O L21P_7	I/O L24P_7	I/O L20N_7	I/O L20P_7	VCCINT	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCINT
N	GND	VCCO_7	I/O L25N_7	I/O L25P_7	GND	VCCO_7	I/O L46N_7	I/O L46P_7	GND	I/O L24N_7	I/O L26P_7	VCCO_7	VCCINT	VCCINT	VCCINT	VCCINT	GND
P	I/O L49N_7	I/O L49P_7	I/O L29N_7	I/O L29P_7	I/O L28N_7	I/O L28P_7	I/O L27N_7	I/O L27P_7 VREF_7	I/O L47N_7 ◆	I/O L47P_7 ◆	I/O L26N_7	VCCO_7	VCCINT	GND	GND	GND	GND
R	I/O L32N_7	I/O L32P_7	I/O L31N_7	I/O L31P_7	VCCAUX	I/O L30N_7	I/O L30P_7	VCCO_7	I/O L33P_7	I/O L50N_7	I/O L50P_7	VCCO_7	VCCINT	GND	GND	GND	GND
T	GND	I/O L35N_7	I/O L35P_7	VCCO_7	GND	I/O L34N_7	I/O L34P_7	VCCAUX	GND	I/O L33N_7	I/O L51P_7 ◆	VCCO_7	VCCINT	GND	GND	GND	GND
U	I/O L40N_7 VREF_7	I/O L40P_7	I/O L39N_7	I/O L39P_7	I/O L38N_7	I/O L38P_7	I/O L37N_7	I/O L37P_7 VREF_7	I/O	I/O	I/O L51N_7 ◆	VCCINT	GND	GND	GND	GND	GND

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Figure 57: **FG1156 Package Footprint (Top View)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
V	I/O L40P_6 VREF_6	I/O L40N_6	I/O L39P_6	I/O L39N_6	I/O L38P_6	I/O L38N_6	I/O L52P_6	I/O L52N_6	I/O	I/O	I/O L49P_6 ◆	VCCINT	GND	GND	GND	GND	GND
W	GND	I/O L37P_6	I/O L37N_6	VCCO_6	GND	I/O L36P_6	I/O L36N_6	VCCAUX	GND	I/O L35P_6	I/O L49N_6 ◆	VCCO_6	VCCINT	GND	GND	GND	GND
Y	I/O L34P_6	I/O L34N_6 VREF_6	I/O L33P_6	I/O L33N_6	VCCAUX	I/O L48P_6	I/O L48N_6	VCCO_6	I/O L35N_6	I/O L32P_6	I/O L32N_6	VCCO_6	VCCINT	GND	GND	GND	GND
AA	I/O L31P_6	I/O L31N_6	I/O L30P_6	I/O L30N_6	I/O L29P_6	I/O L29N_6	I/O L28P_6	I/O L28N_6	I/O L46P_6 ◆	I/O L46N_6 ◆	I/O L27P_6	VCCO_6	VCCINT	GND	GND	GND	GND
AB	GND	VCCO_6	I/O L26P_6	I/O L26N_6	GND	VCCO_6	I/O L25P_6	I/O L25N_6	GND	I/O L24P_6	I/O L27N_6	VCCO_6	VCCINT	VCCINT	VCCINT	VCCINT	GND
AC	I/O L23P_6	I/O L23N_6	I/O L45P_6	I/O L45N_6	I/O L22P_6	I/O L22N_6	I/O L21P_6	I/O L21N_6	I/O L24N_6 VREF_6	I/O L20P_6	I/O L20N_6	VCCINT	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCINT
AD	I/O L19P_6	I/O L19N_6	GND	VCCO_6	VCCAUX	I/O L44P_6 ◆	I/O L44N_6 ◆	VCCO_6	I/O L17P_6 VREF_6	I/O L17N_6	I/O	I/O ◆	I/O L16P_5	I/O	I/O	I/O	I/O
AE	I/O L16P_6	I/O L16N_6	I/O L15P_6	I/O L15N_6	I/O L14P_6	I/O L14N_6	I/O L13P_6 VREF_6	I/O L13N_6	I/O L12P_6	GND	I/O L39P_5 ◆	I/O L12P_5	I/O L16N_5	I/O	I/O L23P_5	I/O	I/O L29P_5 VREF_5
AF	GND	I/O L11P_6	I/O L11N_6	I/O L10P_6	GND	I/O L09P_6	I/O L09N_6 VREF_6	I/O L12N_6	I/O ◆	I/O L07P_5	I/O L39N_5 ◆	I/O L12N_5	GND	I/O L19P_5 VREF_5	I/O L23N_5	GND	I/O L29N_5
AG	I/O L08P_6	I/O L08N_6	VCCO_6	I/O L10N_6	I/O L07P_6	I/O L07N_6	VCCO_6	M2	I/O	I/O L07N_5	VCCO_5	I/O	I/O L17P_5	I/O L19N_5	VCCO_5	VCCAUX	I/O L30P_5
AH	I/O	I/O	I/O L41P_6 ◆	I/O L41N_6 ◆	I/O L06P_6	I/O L06N_6	GND	VCCO_5	I/O L37P_5	I/O L08P_5	I/O L40P_5 ◆	I/O L13P_5	I/O L17N_5	I/O L20P_5	I/O L24P_5	I/O L27P_5	I/O L30N_5
AJ	I/O L05P_6	I/O L05N_6	I/O L04P_6	I/O L04N_6	VCCAUX	I/O	I/O L06P_5	IO VREF_5	I/O L37N_5	I/O L08N_5	I/O L40N_5 ◆	I/O L13N_5	VCCO_5	I/O L20N_5	I/O L24N_5	I/O L27N_5 VREF_5	I/O
AK	GND	I/O L03P_6	I/O L03N_6 VREF_6	M1	GND	VCCAUX	I/O L06N_5	I/O L35P_5	GND	I/O	VCCAUX	I/O L14P_5	GND	I/O	VCCAUX	GND	I/O L31P_5 D5
AL	I/O L02P_6	I/O L02N_6	VCCO_6	M0	IO VREF_5	I/O L04P_5	I/O L33P_5 ◆	I/O L35N_5	I/O L38P_5	I/O L09P_5	VCCO_5	I/O L14N_5	I/O L18P_5	I/O L21P_5	I/O L25P_5	VCCO_5	I/O L31N_5 D4
AM	I/O L01P_6 VRN_6	I/O L01N_6 VRP_6	GND	VCCO_5	I/O L03P_5	I/O L04N_5	I/O L33N_5 ◆	VCCO_5	I/O L38N_5	I/O L09N_5	GND	I/O	I/O L18N_5	I/O L21N_5	I/O L25N_5	I/O L28P_5 D7	I/O L32P_5 GCLK2
AN	GND	GND	I/O L01P_5 CS_B	I/O L02P_5	I/O L03N_5	I/O L05P_5	I/O L34P_5 ◆	I/O L36P_5	I/O	I/O L10P_5 VRN_5	I/O L11P_5	I/O L15P_5	VCCO_5	I/O L22P_5	I/O L26P_5	I/O L28N_5 D6	I/O L32N_5 GCLK3
AP	GND	GND	I/O L01N_5 RDWR_B	I/O L02N_5	GND	I/O L05N_5	I/O L34N_5 ◆	I/O L36N_5	GND	I/O L10N_5 VRP_5	I/O L11N_5 VREF_5	I/O L15N_5	GND	I/O L22N_5	I/O L26N_5	GND	IO VREF_5

Bank 6

Bank 5

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Bottom Left Corner of FG1156 Package (Top View)

Figure 59: FG1156 Package Footprint (Top View) Continued