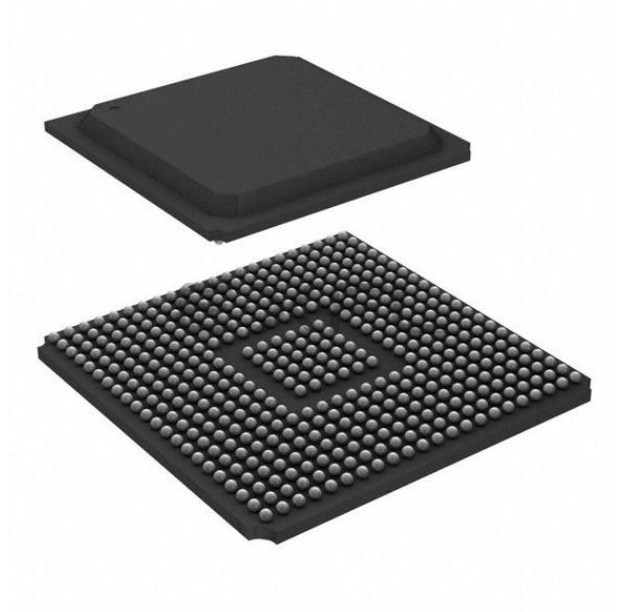


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1920
Number of Logic Elements/Cells	17280
Total RAM Bits	442368
Number of I/O	333
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1000-4fgg456c

Table 9: **Differential I/O Standards**

Signal Standard (IOSTANDARD)	V_{CCO} (Volts)		V_{REF} for Inputs (Volts)
	For Outputs	For Inputs	
LDT_25 (ULVDS_25)	2.5	–	–
LVDS_25	2.5	–	–
BLVDS_25	2.5	–	–
LVDSEXT_25	2.5	–	–
LVPECL_25	2.5	–	–
RSDS_25	2.5	–	–
DIFF_HSTL_II_18	1.8	–	–
DIFF_SSTL2_II	2.5	–	–

Notes:

1. See Table 10 for a listing of the differential DCI standards.

The need to supply V_{REF} and V_{CCO} imposes constraints on which standards can be used in the same bank. See The Organization of IOBs into Banks section for additional guidelines concerning the use of the V_{CCO} and V_{REF} lines.

Digitally Controlled Impedance (DCI)

When the round-trip delay of an output signal—i.e., from output to input and back again—exceeds rise and fall times, it is common practice to add termination resistors to the line carrying the signal. These resistors effectively match the impedance of a device's I/O to the characteristic impedance of the transmission line, thereby preventing reflections that adversely affect signal integrity. However, with the high I/O counts supported by modern devices, adding resistors requires significantly more components and board area. Furthermore, for some packages—e.g., ball grid arrays—it may not always be possible to place resistors close to pins.

DCI answers these concerns by providing two kinds of on-chip terminations: Parallel terminations make use of an integrated resistor network. Series terminations result from controlling the impedance of output drivers. DCI actively adjusts both parallel and series terminations to accurately match the characteristic impedance of the transmission line. This adjustment process compensates for differences in I/O impedance that can result from normal variation in the ambient temperature, the supply voltage and the manufacturing process. When the output driver turns off, the series termination, by definition, approaches a very high impedance; in contrast, parallel termination resistors remain at the targeted values.

DCI is available only for certain I/O standards, as listed in Table 10. DCI is selected by applying the appropriate I/O standard extensions to symbols or components. There are five basic ways to configure terminations, as shown in Table 11. The DCI I/O standard determines which of these terminations is put into effect.

HSTL_I_DCI-, HSTL_III_DCI-, and SSTL2_I_DCI-type outputs do not require the VRN and VRP reference resistors. Likewise, LVDCI-type inputs do not require the VRN and VRP reference resistors. In a bank without any DCI I/O or a bank containing non-DCI I/O and purely HSTL_I_DCI- or HSTL_III_DCI-type outputs, or SSTL2_I_DCI-type outputs or LVDCI-type inputs, the associated VRN and VRP pins can be used as general-purpose I/O pins.

The HSLVDCI (High-Speed LVDCI) standard is intended for bidirectional use. The driver is identical to LVDCI, while the input is identical to HSTL. By using a V_{REF}-referenced input, HSLVDCI allows greater input sensitivity at the receiver than when using a single-ended LVCMOS-type receiver.

In contrast, the 144-pin Thin Quad Flat Pack (TQ144) package and the 132-pin Chip-Scale Package (CP132) tie V_{CCO} together internally for the pair of banks on each side of the device. For example, the V_{CCO} Bank 0 and the V_{CCO} Bank 1 lines are tied together. The interconnected bank-pairs are 0/1, 2/3, 4/5, and 6/7. As a result, Spartan-3 devices in the CP132 and TQ144 packages support four independent V_{CCO} supplies.

Note: The CP132 package is discontinued. See http://www.xilinx.com/support/documentation /spartan-3_customer_notices.htm.

Spartan-3 FPGA Compatibility

Within the Spartan-3 family, all devices are pin-compatible by package. When the need for future logic resources outgrows the capacity of the Spartan-3 device in current use, a larger device in the same package can serve as a direct replacement. Larger devices may add extra V_{REF} and V_{CCO} lines to support a greater number of I/Os. In the larger device, more pins can convert from user I/Os to V_{REF} lines. Also, additional V_{CCO} lines are bonded out to pins that were “not connected” in the smaller device. Thus, it is important to plan for future upgrades at the time of the board’s initial design by laying out connections to the extra pins.

The Spartan-3 family is not pin-compatible with any previous Xilinx FPGA family or with other platforms among the Spartan-3 Generation FPGAs.

Rules Concerning Banks

When assigning I/Os to banks, it is important to follow the following V_{CCO} rules:

- Leave no V_{CCO} pins unconnected on the FPGA.
- Set all V_{CCO} lines associated with the (interconnected) bank to the same voltage level.
- The V_{CCO} levels used by all standards assigned to the I/Os of the (interconnected) bank(s) must agree. The Xilinx development software checks for this. Tables 8, 9, and 10 describe how different standards use the V_{CCO} supply.
- Only one of the following standards is allowed on outputs per bank: LVDS, LDT, LVDS_EXT, or RSDS. This restriction is for the eight banks in each device, even if the V_{CCO} levels are shared across banks, as in the CP132 and TQ144 packages.
- If none of the standards assigned to the I/Os of the (interconnected) bank(s) uses V_{CCO}, tie all associated V_{CCO} lines to 2.5V.
- In general, apply 2.5V to V_{CCO} Bank 4 from power-on to the end of configuration. Apply the same voltage to V_{CCO} Bank 5 during parallel configuration or a Readback operation. For information on how to program the FPGA using 3.3V signals and power, see the 3.3V-Tolerant Configuration Interface section.

If any of the standards assigned to the Inputs of the bank use V_{REF}, then observe the following additional rules:

- Connect *all* V_{REF} pins within the bank to the same voltage level.
- The V_{REF} levels used by all standards assigned to the Inputs of the bank must agree. The Xilinx development software checks for this. Tables 8 and 10 describe how different standards use the V_{REF} supply.

If none of the standards assigned to the Inputs of a bank use V_{REF} for biasing input switching thresholds, all associated V_{REF} pins function as User I/Os.

Exceptions to Banks Supporting I/O Standards

Bank 5 of any Spartan-3 device in a VQ100, CP132, or TQ144 package does not support DCI signal standards. In this case, bank 5 has neither VRN nor VRP pins.

Furthermore, banks 4 and 5 of any Spartan-3 device in a VQ100 package do not support signal standards using V_{REF} (see Table 8). In this case, the two banks do not have any V_{REF} pins.

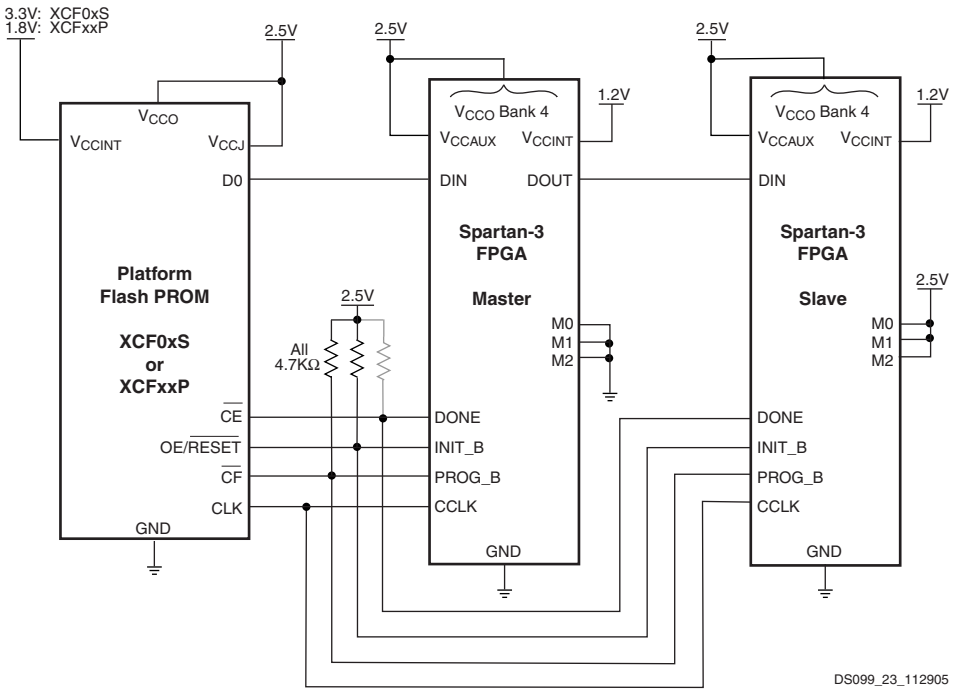
upper path), enter the slice and connect directly to the LUT. Once inside the slice, the lower 4-bit path passes through a function generator ‘F’ (or ‘G’) that performs logic operations. The function generator’s Data output, ‘D’, offers five possible paths:

- Exit the slice via line ‘X’ (or ‘Y’) and return to interconnect.
- Inside the slice, ‘X’ (or ‘Y’) serves as an input to the DXMUX (DYMUX) which feeds the data input, ‘D’, of the FFX (FFY) storage element. The ‘Q’ output of the storage element drives the line XQ (or YQ) which exits the slice.
- Control the CYMUXF (or CYMUXG) multiplexer on the carry chain.
- With the carry chain, serve as an input to the XORF (or XORG) exclusive-OR gate that performs arithmetic operations, producing a result on ‘X’ (or ‘Y’).
- Drive the multiplexer F5MUX to implement logic functions wider than four bits. The ‘D’ outputs of both the F-LUT and G-LUT serve as data inputs to this multiplexer.

In addition to the main logic paths described above, there are two bypass paths that enter the slice as BX and BY. Once inside the FPGA, BX in the bottom half of the slice (or BY in the top half) can take any of several possible branches:

- Bypass both the LUT and the storage element, then exit the slice as BXOUT (or BYOUT) and return to interconnect.
- Bypass the LUT, then pass through a storage element via the D input before exiting as XQ (or YQ).
- Control the wide function multiplexer F5MUX (or F6MUX).
- Via multiplexers, serve as an input to the carry chain.
- Drives the DI input of the LUT.
- BY can control the REV inputs of both the FFY and FFX storage elements.
- Finally, the DIG_MUX multiplexer can switch BY onto the DIG line, which exits the slice.

Other slice signals shown in Figure 12 are discussed in the sections that follow.



Notes:

1. There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.
2. For information on how to program the FPGA using 3.3V signals and power, see 3.3V-Tolerant Configuration Interface.

Figure 26: **Connection Diagram for Master and Slave Serial Configuration**

Slave Serial mode is selected by applying <111> to the mode pins (M0, M1, and M2). A pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

Master Serial Mode

In Master Serial mode, the FPGA drives CCLK pin, which behaves as a bidirectional I/O pin. The FPGA in the center of Figure 26 is set for Master Serial mode and connects to the serial configuration PROM and to the CCLK inputs of any slave FPGAs in a configuration daisy-chain. The master FPGA drives the configuration clock on the CCLK pin to the Xilinx Serial PROM, which, in response, provides bit-serial data to the FPGA's DIN input. The FPGA accepts this data on each rising CCLK edge. After the master FPGA finishes configuring, it passes data on its DOUT pin to the next FPGA device in a daisy-chain. The DOUT data appears after the falling CCLK clock edge.

The Master Serial mode interface is identical to Slave Serial except that an internal oscillator generates the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK, which always starts at a default frequency of 6 MHz. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

Slave Parallel Mode (SelectMAP)

The Parallel or SelectMAP modes support the fastest configuration. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data. An external source provides 8-bit-wide data, CCLK, an active-Low Chip Select (CS_B) signal and an active-Low Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the Slave Parallel mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, it is possible to use any of the Multipurpose pins (DIN/D0-D7, DOUT/BUSY, INIT_B, CS_B, and RDWR_B) as User I/Os. To do this, simply set the BitGen option *Persist* to *No* and assign the desired signals to multipurpose configuration pins using the Xilinx development software. Alternatively, it is possible to continue using the configuration port

Table 36: **DC Characteristics of User I/Os Using Single-Ended Standards**

Signal Standard (IOSTANDARD) and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
GTL		32	–	0.4	–
GTL_DCI		Note 3	Note 3		
GTLP		36	–	0.6	–
GTLP_DCI		Note 3	Note 3		
HSLVDCI_15		Note 3	Note 3	0.4	V_{CCO} – 0.4
HSLVDCI_18					
HSLVDCI_25					
HSLVDCI_33					
HSTL_I		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI		Note 3	Note 3		
HSTL_III		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI		Note 3	Note 3		
HSTL_I_18		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI_18		Note 3	Note 3		
HSTL_II_18		16	–16	0.4	V_{CCO} – 0.4
HSTL_II_DCI_18		Note 3	Note 3		
HSTL_III_18		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI_18		Note 3	Note 3		
LVCMOS12(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
LVCMOS15(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
LVDCI_15, LVDCI_DV2_15		Note 3	Note 3		
LVCMOS18(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
LVDCI_18, LVDCI_DV2_18		Note 3	Note 3		
LVCMOS25(4,5)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_25, LVDCI_DV2_25		Note 3	Note 3		

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS33	Slow	2 mA	6.38	7.34	ns
		4 mA	4.83	5.55	ns
		6 mA	4.01	4.61	ns
		8 mA	3.92	4.51	ns
		12 mA	2.91	3.35	ns
		16 mA	2.81	3.23	ns
		24 mA	2.49	2.86	ns
	Fast	2 mA	3.86	4.44	ns
		4 mA	1.87	2.15	ns
		6 mA	0.62	0.71	ns
		8 mA	0.61	0.70	ns
		12 mA	0.16	0.19	ns
		16 mA	0.14	0.16	ns
		24 mA	0.06	0.07	ns
LVDCI_33			0.28	0.32	ns
LVDCI_DV2_33			0.26	0.30	ns
LVTTL	Slow	2 mA	7.27	8.36	ns
		4 mA	4.94	5.69	ns
		6 mA	3.98	4.58	ns
		8 mA	3.98	4.58	ns
		12 mA	2.97	3.42	ns
		16 mA	2.84	3.26	ns
		24 mA	2.65	3.04	ns
	Fast	2 mA	4.32	4.97	ns
		4 mA	1.87	2.15	ns
		6 mA	1.27	1.47	ns
		8 mA	1.19	1.37	ns
		12 mA	0.42	0.48	ns
		16 mA	0.27	0.32	ns
		24 mA	0.16	0.18	ns

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 58 and Table 59) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 60 through Table 63) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 58 and Table 59.

Period jitter and cycle-cycle jitter are two (of many) different ways of characterizing clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the average clock period of all clock cycles in the collection of clock periods sampled (usually from 100,000 to more than a million samples for specification purposes). In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Delay-Locked Loop (DLL)

Table 58: **Recommended Operating Conditions for the DLL**

Symbol		Description	Frequency Mode/ F_{CLKIN} Range	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges								
F_{CLKIN}	CLKIN_FREQ_DLL_LF	Frequency for the CLKIN input	Low	18(2)	167(3)	18(2)	167(3)	MHz
	CLKIN_FREQ_DLL_HF		High	48	280(3)	48	280(3)(4)	MHz
Input Pulse Requirements								
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	$F_{CLKIN} \leq 100$ MHz	40%	60%	40%	60%	-
			$F_{CLKIN} > 100$ MHz	45%	55%	45%	55%	-
Input Clock Jitter Tolerance and Delay Path Variation(5)								
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	Low	–	±300	–	±300	ps
CLKIN_CYC_JITT_DLL_HF			High	–	±150	–	±150	ps
CLKIN_PER_JITT_DLL_LF		Period jitter at the CLKIN input	All	–	±1	–	±1	ns
CLKIN_PER_JITT_DLL_HF				–		–		
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input	All	–	±1	–	±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower F_{CLKIN} frequencies. See Table 60.
3. The CLKIN_DIVIDE_BY_2 attribute can be used to increase the effective input frequency range up to F_{BUFG}. When set to TRUE, CLKIN_DIVIDE_BY_2 divides the incoming clock frequency by two as it enters the DCM.
4. Industrial temperature range devices have additional requirements for continuous clocking, as specified in Table 64.
5. CLKIN input jitter beyond these limits may cause the DCM to lose lock. See UG331 for more details.

Date	Version	Description
05/25/07	2.2	Improved absolute maximum voltage specifications in Table 28, providing additional overshoot allowance. Improved XC3S50 HBM ESD to 2000V in Table 28. Based on extensive 90 nm production data, improved (reduced) the maximum quiescent current limits for the I_{CCINTQ} and I_{CCOQ} specifications in Table 34. Widened the recommended voltage range for the PCI standard and clarified the hysteresis footnote in Table 35. Noted restriction on combining differential outputs in Table 38. Updated footnote 1 in Table 64.
11/30/07	2.3	Updated 3.3V VCCO max from 3.45V to 3.465V in Table 32 and elsewhere. Reduced t_{ICCK} minimum from 0.50µs to 0.25µs in Table 65. Updated links to technical documentation.
06/25/08	2.4	Clarified dual marking. Added Mask and Fab Revisions. Added references to XAPP459 in Table 28 and Table 32. Removed absolute minimum and added footnote referring to timing analyzer for minimum delay values. Added HSLVDCI to Table 48 and Table 50. Updated t_{DICK} in Table 51 to match largest possible value in speed file. Updated formatting and links.
12/04/09	2.5	Updated notes 2 and 3 in Table 28. Removed silicon process specific information and revised notes in Table 30. Updated note 3 in Table 32. Updated note 3 in Table 34. Updated note 5 in Table 35. Updated V_{OL} max and V_{OH} min for SSTL2_II in Table 36. Updated note 5 in Table 36. Updated JTAG Waveforms in Figure 39. Updated V_{ICM} max for LVPECL_25 in Table 37. Updated RT and VT for LVDS_25_DCI in Table 48. Updated Simultaneously Switching Output Guidelines. Noted that the CP132 package is being discontinued in Table 49. Removed minimum values for T_{MULTCK} clock-to-output times in Table 54. Updated footnote 3 in Table 58. Removed minimum values for T_{MULT} propagation times in Table 55. Removed silicon process specific information and revised notes in Table 61. Updated Phase Shifter (PS).
10/29/12	3.0	Added Notice of Disclaimer. Per XCN07022, updated the discontinued FG1156 and FGG1156 package discussion throughout document. Per XCN08011, updated the discontinued CP132 and CPG132 package discussion throughout document. Revised description of V_{IN} in Table 32 and added note 7. Added note 4 to Table 33. This product is not recommended for new designs.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx website at the specified location in Table 83.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx website for each package.

Table 83: **Xilinx Package Mechanical Drawings**

Package	Web Link (URL)
VQ100 and VQG100	http://www.xilinx.com/support/documentation/package_specs/vq100.pdf
CP132 and CPG132(1)	http://www.xilinx.com/support/documentation/package_specs/cp132.pdf
TQ144 and TQG144	http://www.xilinx.com/support/documentation/package_specs/tq144.pdf
PQ208 and PQG208	http://www.xilinx.com/support/documentation/package_specs/pq208.pdf
FT256 and FTG256	http://www.xilinx.com/support/documentation/package_specs/ft256.pdf
FG320 and FGG320	http://www.xilinx.com/support/documentation/package_specs/fg320.pdf
FG456 and FGG456	http://www.xilinx.com/support/documentation/package_specs/fg456.pdf
FG676 and FGG676	http://www.xilinx.com/support/documentation/package_specs/fg676.pdf
FG900 and FGG900	http://www.xilinx.com/support/documentation/package_specs/fg900.pdf
FG1156 and FGG1156(1)	http://www.xilinx.com/support/documentation/package_specs/fg1156.pdf

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Power, Ground, and I/O by Package

Each package has three separate voltage supply inputs—VCCINT, VCCAUX, and VCCO—and a common ground return, GND. The numbers of pins dedicated to these functions varies by package, as shown in Table 84.

Table 84: **Power and Ground Supply Pins by Package**

Package	VCCINT	VCCAUX	VCCO	GND
VQ100	4	4	8	10
CP132(1)	4	4	12	12
TQ144	4	4	12	16
PQ208	4	8	12	28
FT256	8	8	24	32
FG320	12	8	28	40
FG456	12	8	40	52
FG676	20	16	64	76
FG900	32	24	80	120
FG1156(1)	40	32	104	184

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

A majority of package pins are user-defined I/O pins. However, the numbers and characteristics of these I/O depends on the device type and the package in which it is available, as shown in Table 85. The table shows the maximum number of single-ended I/O pins available, assuming that all I/O-, DUAL-, DCI-, VREF-, and GCLK-type pins are used as general-purpose I/O. Likewise, the table shows the maximum number of differential pin-pairs available on the package. Finally, the table shows how the total maximum user I/Os are distributed by pin type, including the number of unconnected—i.e., N.C.—pins on the device.

PQ208: 208-lead Plastic Quad Flat Pack

The 208-lead plastic quad flat package, PQ208, supports three different Spartan-3 devices, including the XC3S50, the XC3S200, and the XC3S400. The footprints for the XC3S200 and XC3S400 are identical, as shown in Table 93 and Figure 47. The XC3S50, however, has fewer I/O pins resulting in 17 unconnected pins on the PQ208 package, labeled as "N.C." In Table 93 and Figure 47, these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in Table 93 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S50 pinout and the pinout for the XC3S200 and XC3S400, then that difference is highlighted in Table 93. If the table entry is shaded grey, then there is an unconnected pin on the XC3S50 that maps to a user-I/O pin on the XC3S200 and XC3S400. If the table entry is shaded tan, then the unconnected pin on the XC3S50 maps to a VREF-type pin on the XC3S200 and XC3S400. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S50 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S50 device to an XC3S200 or XC3S400 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip

Pinout Table

Table 93: **PQ208 Package Pinout**

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
0	IO	IO	P189	I/O
0	IO	IO	P197	I/O
0	N.C. (◆)	IO/VREF_0	P200	VREF
0	IO/VREF_0	IO/VREF_0	P205	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	P204	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	P203	DCI
0	IO_L25N_0	IO_L25N_0	P199	I/O
0	IO_L25P_0	IO_L25P_0	P198	I/O
0	IO_L27N_0	IO_L27N_0	P196	I/O
0	IO_L27P_0	IO_L27P_0	P194	I/O
0	IO_L30N_0	IO_L30N_0	P191	I/O
0	IO_L30P_0	IO_L30P_0	P190	I/O
0	IO_L31N_0	IO_L31N_0	P187	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	P185	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	P184	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	P183	GCLK
0	VCCO_0	VCCO_0	P188	VCCO
0	VCCO_0	VCCO_0	P201	VCCO
1	IO	IO	P167	I/O
1	IO	IO	P175	I/O
1	IO	IO	P182	I/O
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	P162	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	P161	DCI

Table 93: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	P166	VREF
1	IO_L10P_1	IO_L10P_1	P165	I/O
1	IO_L27N_1	IO_L27N_1	P169	I/O
1	IO_L27P_1	IO_L27P_1	P168	I/O
1	IO_L28N_1	IO_L28N_1	P172	I/O
1	IO_L28P_1	IO_L28P_1	P171	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	P178	VREF
1	IO_L31P_1	IO_L31P_1	P176	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	P181	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	P180	GCLK
1	VCCO_1	VCCO_1	P164	VCCO
1	VCCO_1	VCCO_1	P177	VCCO
2	N.C. (◆)	IO/VREF_2	P154	VREF
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	P156	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	P155	DCI
2	IO_L19N_2	IO_L19N_2	P152	I/O
2	IO_L19P_2	IO_L19P_2	P150	I/O
2	IO_L20N_2	IO_L20N_2	P149	I/O
2	IO_L20P_2	IO_L20P_2	P148	I/O
2	IO_L21N_2	IO_L21N_2	P147	I/O
2	IO_L21P_2	IO_L21P_2	P146	I/O
2	IO_L22N_2	IO_L22N_2	P144	I/O
2	IO_L22P_2	IO_L22P_2	P143	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	P141	VREF
2	IO_L23P_2	IO_L23P_2	P140	I/O
2	IO_L24N_2	IO_L24N_2	P139	I/O
2	IO_L24P_2	IO_L24P_2	P138	I/O
2	N.C. (◆)	IO_L39N_2	P137	I/O
2	N.C. (◆)	IO_L39P_2	P135	I/O
2	IO_L40N_2	IO_L40N_2	P133	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	P132	VREF
2	VCCO_2	VCCO_2	P136	VCCO
2	VCCO_2	VCCO_2	P153	VCCO
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	P107	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	P106	DCI
3	N.C. (◆)	IO_L17N_3	P109	I/O
3	N.C. (◆)	IO_L17P_3/VREF_3	P108	VREF
3	IO_L19N_3	IO_L19N_3	P113	I/O
3	IO_L19P_3	IO_L19P_3	P111	I/O
3	IO_L20N_3	IO_L20N_3	P115	I/O

PQ208 Footprint

Left Half of Package (Top View)

XC3S50
(124 max. user I/O)

72 **I/O:** Unrestricted, general-purpose user I/O

16 **VREF:** User I/O or input voltage reference for bank

17 **N.C.:** Unconnected pins for XC3S50 (◆)

XC3S200, XC3S400
(141 max user I/O)

83 **I/O:** Unrestricted, general-purpose user I/O

22 **VREF:** User I/O or input voltage reference for bank

0 **N.C.:** No unconnected pins in this package

All devices

12 **DUAL:** Configuration pin, then possible user I/O

8 **GCLK:** User I/O or global clock buffer input

16 **DCI:** User I/O or reference resistor input for bank

7 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

4 **VCCINT:** Internal core voltage supply (+1.2V)

12 **VCCO:** Output voltage supply for bank

8 **VCCAUX:** Auxiliary voltage supply (+2.5V)

28 **GND:** Ground

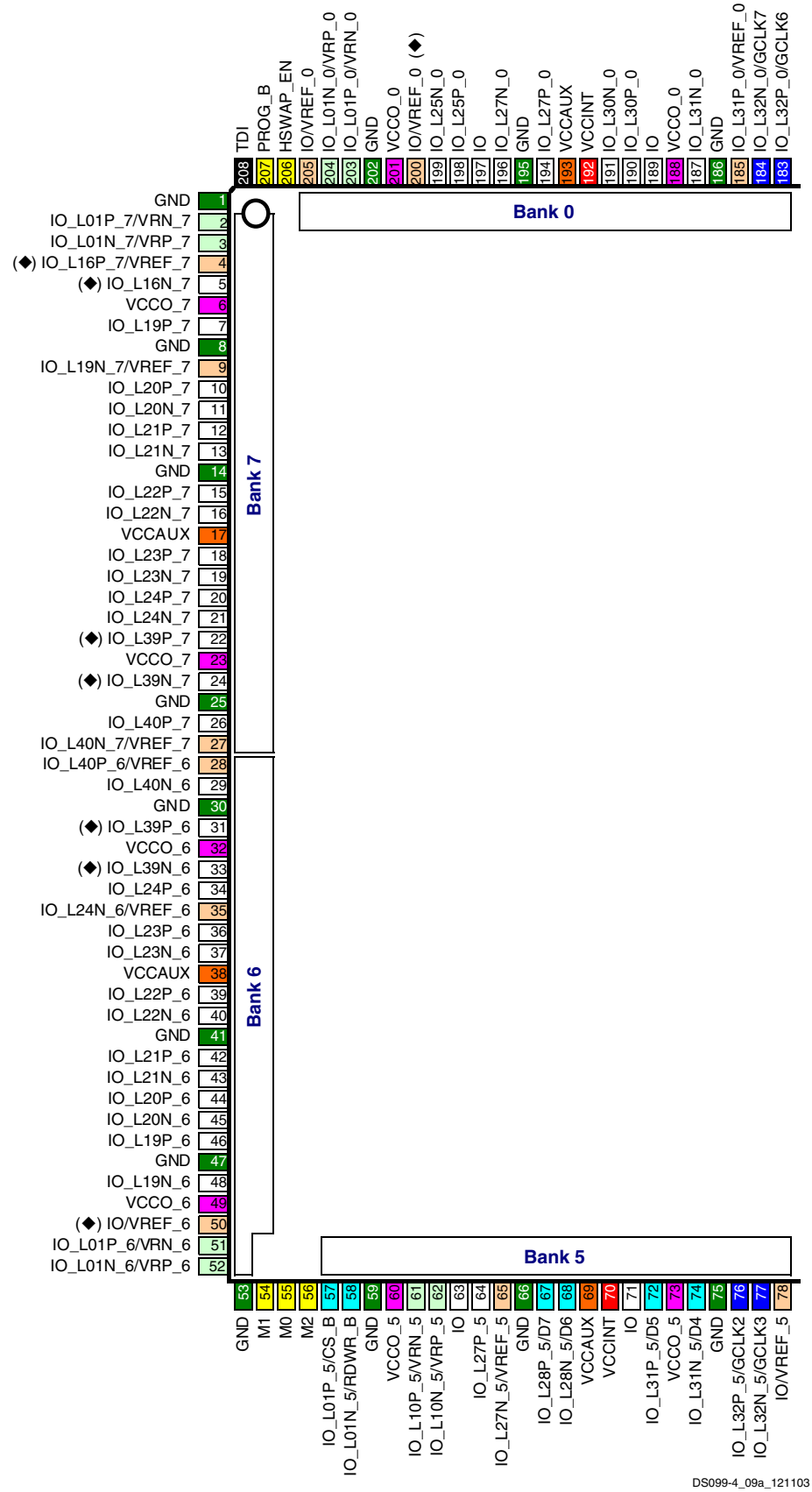


Figure 47: **PQ208 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

Right Half of FG456 Package (Top View)

	Bank 1										
	12	13	14	15	16	17	18	19	20	21	22	
A	I/O	I/O L30N_1	I/O L28N_1	I/O L25P_1	I/O L22N_1 ◆	VCCAUX	I/O L10N_1 VREF_1	I/O L06N_1 VREF_1	TMS	TCK	GND	A
B	I/O L32N_1 GCLK5	I/O L30P_1	I/O L28P_1	I/O L25N_1	I/O L22P_1 ◆	I/O L16N_1	I/O L10P_1	I/O L06P_1	I/O L01P_1 VRN_1	GND	TDO	B
C	I/O L32P_1 GCLK4	I/O L29N_1	GND	VCCO_1	I/O L19N_1 ◆	I/O L16P_1	I/O L09N_1	I/O L01N_1 VRP_1	I/O L01N_2 VRP_2	I/O L01P_2 VRN_2	I/O	C	
D	I/O L31N_1 VREF_1	I/O L29P_1	I/O L27N_1	I/O L24N_1	I/O L19P_1 ◆	I/O L15N_1	I/O L09P_1	I/O L16P_2	I/O L16N_2	I/O L17N_2	I/O L17P_2 VREF_2	D	
E	I/O L31P_1	IO VREF_1	I/O L27P_1	I/O L24P_1	I/O	I/O L15P_1	I/O L19N_2	I/O L20N_2	I/O L20P_2	I/O L21N_2	I/O L21P_2	E	
F	I/O	I/O	IO VREF_1 ◆	VCCO_1	I/O	I/O	I/O L19P_2	I/O L23N_2 VREF_2	I/O L24N_2	I/O L24P_2	VCCAUX	F	
G	VCCO_1	VCCO_1	VCCO_1	VCCINT	VCCINT	I/O L22N_2	I/O L22P_2	I/O L23P_2	I/O L26N_2 ◆	I/O L27N_2	I/O L27P_2	G	Bank 2
H					VCCINT	VCCO_2	I/O L28N_2 ◆	I/O L26P_2 ◆	VCCO_2	I/O L29N_2 ◆	I/O L29P_2 ◆	H	
J	GND	GND	GND		VCCO_2	I/O L28P_2 ◆	I/O L31N_2 ◆	I/O L31P_2 ◆	GND	I/O L32N_2 ◆	I/O L32P_2 ◆	J	
K	GND	GND	GND		VCCO_2	I/O L33N_2 ◆	I/O L33P_2 ◆	I/O L34N_2 VREF_2	I/O L34P_2	I/O L35N_2	I/O L35P_2	K	
L	GND	GND	GND		VCCO_2	I/O L38N_2	I/O L38P_2	I/O L39N_2	I/O L39P_2	I/O L40N_2	I/O L40P_2 VREF_2	L	
M	GND	GND	GND		VCCO_3	I/O L38P_3	I/O L38N_3	I/O L39P_3	I/O L39N_3	I/O L40P_3	I/O L40N_3 VREF_3	M	
N	GND	GND	GND		VCCO_3	I/O L33P_3 ◆	I/O L33N_3 ◆	I/O L34P_3 VREF_3	I/O L34N_3	I/O L35P_3	I/O L35N_3	N	
P	GND	GND	GND		VCCO_3	I/O L31P_3 ◆	I/O L31N_3 ◆	I/O L29N_3 ◆	GND	I/O L32P_3 ◆	I/O L32N_3 ◆	P	
R					VCCINT	VCCO_3	I/O L24N_3	I/O L29P_3 ◆	VCCO_3	I/O L28P_3 ◆	I/O L28N_3 ◆	R	
T	VCCO_4	VCCO_4	VCCO_4	VCCINT	VCCINT	I/O L22N_3	I/O L24P_3	I/O L26P_3 ◆	I/O L26N_3 ◆	I/O L27P_3	I/O L27N_3	T	Bank 3
U	I/O L30N_4 D2	I/O L28N_4	I/O L25N_4	VCCO_4	I/O	I/O	I/O L22P_3	I/O L20N_3	I/O L23P_3 VREF_3	I/O L23N_3	VCCAUX	U	
V	I/O L30P_4 D3	I/O L28P_4	I/O L25P_4	I/O L22N_4 VREF_4 ◆	I/O L16N_4	I/O L10N_4	IO VREF_4	I/O L17N_3	I/O L20P_3	I/O L21P_3	I/O L21N_3	V	
W	I/O L31N_4 INIT_B	I/O	I/O	I/O L22P_4 ◆	I/O L16P_4	I/O L10P_4	I/O L06N_4 VREF_4	I/O L17P_3 VREF_3	I/O L19P_3	I/O L19N_3	I/O L16N_3	W	
Y	I/O L31P_4 DOUT BUSY	I/O L29N_4	GND	VCCO_4	IO VREF_4	I/O L15N_4	I/O L06P_4	I/O L01P_3 VRN_3	I/O L01N_3 VRP_3	I/O	I/O L16P_3	Y	
AA	I/O L32N_4 GCLK1	I/O L29P_4	I/O L27N_4 DN D0	I/O L24N_4	I/O L19N_4 ◆	I/O L15P_4	I/O L09N_4	I/O L05N_4 ◆	I/O L01N_4 VRP_4	GND	CCLK	AA	
AB	I/O L32P_4 GCLK0	IO VREF_4	I/O L27P_4 D1	I/O L24P_4	I/O L19P_4 ◆	VCCAUX	I/O L09P_4	I/O L05P_4 ◆	I/O L01P_4 VRN_4	DONE	GND	AB	
		Bank 4											

DS099-4_11b_030503

Figure 52: FG456 Package Footprint (Top View) Continued

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	F6	DCI
7	IO_L02N_7	IO_L02N_7	IO_L02N_7	IO_L02N_7	IO_L02N_7	E3	I/O
7	IO_L02P_7	IO_L02P_7	IO_L02P_7	IO_L02P_7	IO_L02P_7	E4	I/O
7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	D1	VREF
7	IO_L03P_7	IO_L03P_7	IO_L03P_7	IO_L03P_7	IO_L03P_7	D2	I/O
7	N.C. (◆)	IO_L05N_7	IO_L05N_7	IO_L05N_7	IO_L05N_7	G6	I/O
7	N.C. (◆)	IO_L05P_7	IO_L05P_7	IO_L05P_7	IO_L05P_7	G7	I/O
7	N.C. (◆)	IO_L06N_7	IO_L06N_7	IO_L06N_7	IO_L06N_7	E1	I/O
7	N.C. (◆)	IO_L06P_7	IO_L06P_7	IO_L06P_7	IO_L06P_7	E2	I/O
7	N.C. (◆)	IO_L07N_7	IO_L07N_7	IO_L07N_7	IO_L07N_7	F3	I/O
7	N.C. (◆)	IO_L07P_7	IO_L07P_7	IO_L07P_7	IO_L07P_7	F4	I/O
7	N.C. (◆)	IO_L08N_7	IO_L08N_7	IO_L08N_7	IO_L08N_7	G4	I/O
7	N.C. (◆)	IO_L08P_7	IO_L08P_7	IO_L08P_7	IO_L08P_7	G5	I/O
7	N.C. (◆)	IO_L09N_7	IO_L09N_7	IO_L09N_7	IO_L09N_7	F1	I/O
7	N.C. (◆)	IO_L09P_7	IO_L09P_7	IO_L09P_7	IO_L09P_7	F2	I/O
7	N.C. (◆)	IO_L10N_7	IO_L10N_7	IO_L10N_7	IO_L10N_7	H6	I/O
7	N.C. (◆)	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	H7	VREF
7	IO_L14N_7	IO_L14N_7	IO_L14N_7	IO_L14N_7	IO_L14N_7	G1	I/O
7	IO_L14P_7	IO_L14P_7	IO_L14P_7	IO_L14P_7	IO_L14P_7	G2	I/O
7	IO_L16N_7	IO_L16N_7	IO_L16N_7	IO_L16N_7	IO_L16N_7	J6	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	H5	VREF
7	IO_L17N_7	IO_L17N_7	IO_L17N_7	IO_L17N_7	IO_L17N_7	H3	I/O
7	IO_L17P_7	IO_L17P_7	IO_L17P_7	IO_L17P_7	IO_L17P_7	H4	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	H1	VREF
7	IO_L19P_7	IO_L19P_7	IO_L19P_7	IO_L19P_7	IO_L19P_7	H2	I/O
7	IO_L20N_7	IO_L20N_7	IO_L20N_7	IO_L20N_7	IO_L20N_7	K7	I/O
7	IO_L20P_7	IO_L20P_7	IO_L20P_7	IO_L20P_7	IO_L20P_7	J7	I/O
7	IO_L21N_7	IO_L21N_7	IO_L21N_7	IO_L21N_7	IO_L21N_7	J4	I/O
7	IO_L21P_7	IO_L21P_7	IO_L21P_7	IO_L21P_7	IO_L21P_7	J5	I/O
7	IO_L22N_7	IO_L22N_7	IO_L22N_7	IO_L22N_7	IO_L22N_7	J2	I/O
7	IO_L22P_7	IO_L22P_7	IO_L22P_7	IO_L22P_7	IO_L22P_7	J3	I/O
7	IO_L23N_7	IO_L23N_7	IO_L23N_7	IO_L23N_7	IO_L23N_7	K5	I/O
7	IO_L23P_7	IO_L23P_7	IO_L23P_7	IO_L23P_7	IO_L23P_7	K6	I/O
7	IO_L24N_7	IO_L24N_7	IO_L24N_7	IO_L24N_7	IO_L24N_7	K3	I/O
7	IO_L24P_7	IO_L24P_7	IO_L24P_7	IO_L24P_7	IO_L24P_7	K4	I/O
7	IO_L26N_7	IO_L26N_7	IO_L26N_7	IO_L26N_7	IO_L26N_7	K1	I/O
7	IO_L26P_7	IO_L26P_7	IO_L26P_7	IO_L26P_7	IO_L26P_7	K2	I/O
7	IO_L27N_7	IO_L27N_7	IO_L27N_7	IO_L27N_7	IO_L27N_7	L7	I/O
7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	L8	VREF
7	IO_L28N_7	IO_L28N_7	IO_L28N_7	IO_L28N_7	IO_L28N_7	L5	I/O
7	IO_L28P_7	IO_L28P_7	IO_L28P_7	IO_L28P_7	IO_L28P_7	L6	I/O
7	IO_L29N_7	IO_L29N_7	IO_L29N_7	IO_L29N_7	IO_L29N_7	L1	I/O

FG900: 900-lead Fine-pitch Ball Grid Array

The 900-lead fine-pitch ball grid array package, FG900, supports three different Spartan-3 devices, including the XC3S2000, the XC3S4000, and the XC3S5000. The footprints for the XC3S4000 and XC3S5000 are identical, as shown in Table 107 and Figure 55. The XC3S2000, however, has fewer I/O pins which consequently results in 68 unconnected pins on the FG900 package, labeled as “N.C.” In Table 107 and Figure 55, these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in Table 107 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S2000 pinout and the pinout for the XC3S4000 and XC3S5000, then that difference is highlighted in Table 107. If the table entry is shaded, then there is an unconnected pin on the XC3S2000 that maps to a user-I/O pin on the XC3S4000 and XC3S5000.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 107: **FG900 Package Pinout**

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO	IO	E15	I/O
0	IO	IO	K15	I/O
0	IO	IO	D13	I/O
0	IO	IO	K13	I/O
0	IO	IO	G8	I/O
0	IO/VREF_0	IO/VREF_0	F9	VREF
0	IO/VREF_0	IO/VREF_0	C4	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L02N_0	IO_L02N_0	B5	I/O
0	IO_L02P_0	IO_L02P_0	A5	I/O
0	IO_L03N_0	IO_L03N_0	D5	I/O
0	IO_L03P_0	IO_L03P_0	E6	I/O
0	IO_L04N_0	IO_L04N_0	C6	I/O
0	IO_L04P_0	IO_L04P_0	B6	I/O
0	IO_L05N_0	IO_L05N_0	F6	I/O
0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	F7	VREF
0	IO_L06N_0	IO_L06N_0	D7	I/O
0	IO_L06P_0	IO_L06P_0	C7	I/O
0	IO_L07N_0	IO_L07N_0	F8	I/O
0	IO_L07P_0	IO_L07P_0	E8	I/O
0	IO_L08N_0	IO_L08N_0	D8	I/O
0	IO_L08P_0	IO_L08P_0	C8	I/O
0	IO_L09N_0	IO_L09N_0	B8	I/O
0	IO_L09P_0	IO_L09P_0	A8	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
5	IO_L07N_5	IO_L07N_5	AK8	I/O
5	IO_L07P_5	IO_L07P_5	AJ8	I/O
5	IO_L08N_5	IO_L08N_5	AC9	I/O
5	IO_L08P_5	IO_L08P_5	AB9	I/O
5	IO_L09N_5	IO_L09N_5	AG9	I/O
5	IO_L09P_5	IO_L09P_5	AF9	I/O
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	AK9	DCI
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	AJ9	DCI
5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	AE10	VREF
5	IO_L11P_5	IO_L11P_5	AE9	I/O
5	IO_L12N_5	IO_L12N_5	AJ10	I/O
5	IO_L12P_5	IO_L12P_5	AH10	I/O
5	IO_L13N_5	IO_L13N_5	AD11	I/O
5	IO_L13P_5	IO_L13P_5	AD10	I/O
5	IO_L14N_5	IO_L14N_5	AF11	I/O
5	IO_L14P_5	IO_L14P_5	AE11	I/O
5	IO_L15N_5	IO_L15N_5	AH11	I/O
5	IO_L15P_5	IO_L15P_5	AG11	I/O
5	IO_L16N_5	IO_L16N_5	AK11	I/O
5	IO_L16P_5	IO_L16P_5	AJ11	I/O
5	IO_L17N_5	IO_L17N_5	AB12	I/O
5	IO_L17P_5	IO_L17P_5	AC11	I/O
5	IO_L18N_5	IO_L18N_5	AD12	I/O
5	IO_L18P_5	IO_L18P_5	AC12	I/O
5	IO_L19N_5	IO_L19N_5	AF12	I/O
5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	AE12	VREF
5	IO_L20N_5	IO_L20N_5	AH12	I/O
5	IO_L20P_5	IO_L20P_5	AG12	I/O
5	IO_L21N_5	IO_L21N_5	AK12	I/O
5	IO_L21P_5	IO_L21P_5	AJ12	I/O
5	IO_L22N_5	IO_L22N_5	AA13	I/O
5	IO_L22P_5	IO_L22P_5	AA12	I/O
5	IO_L23N_5	IO_L23N_5	AC13	I/O
5	IO_L23P_5	IO_L23P_5	AB13	I/O
5	IO_L24N_5	IO_L24N_5	AG13	I/O
5	IO_L24P_5	IO_L24P_5	AF13	I/O
5	IO_L25N_5	IO_L25N_5	AK13	I/O
5	IO_L25P_5	IO_L25P_5	AJ13	I/O
5	IO_L26N_5	IO_L26N_5	AB14	I/O
5	IO_L26P_5	IO_L26P_5	AA14	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
7	VCCO_7	VCCO_7	N3	VCCO
7	VCCO_7	VCCO_7	G5	VCCO
7	VCCO_7	VCCO_7	J7	VCCO
7	VCCO_7	VCCO_7	N7	VCCO
7	VCCO_7	VCCO_7	L9	VCCO
7	VCCO_7	VCCO_7	M11	VCCO
7	VCCO_7	VCCO_7	N11	VCCO
7	VCCO_7	VCCO_7	P11	VCCO
N/A	GND	GND	A1	GND
N/A	GND	GND	B1	GND
N/A	GND	GND	F1	GND
N/A	GND	GND	K1	GND
N/A	GND	GND	P1	GND
N/A	GND	GND	U1	GND
N/A	GND	GND	AA1	GND
N/A	GND	GND	AE1	GND
N/A	GND	GND	AJ1	GND
N/A	GND	GND	AK1	GND
N/A	GND	GND	A2	GND
N/A	GND	GND	B2	GND
N/A	GND	GND	AJ2	GND
N/A	GND	GND	E5	GND
N/A	GND	GND	K5	GND
N/A	GND	GND	P5	GND
N/A	GND	GND	U5	GND
N/A	GND	GND	AA5	GND
N/A	GND	GND	AF5	GND
N/A	GND	GND	A6	GND
N/A	GND	GND	AK6	GND
N/A	GND	GND	K8	GND
N/A	GND	GND	P8	GND
N/A	GND	GND	U8	GND
N/A	GND	GND	AA8	GND
N/A	GND	GND	A10	GND
N/A	GND	GND	E10	GND
N/A	GND	GND	H10	GND
N/A	GND	GND	AC10	GND
N/A	GND	GND	AF10	GND
N/A	GND	GND	AK10	GND
N/A	GND	GND	R12	GND

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
2	IO_L19N_2	IO_L19N_2	M29	I/O
2	IO_L19P_2	IO_L19P_2	M30	I/O
2	IO_L20N_2	IO_L20N_2	M31	I/O
2	IO_L20P_2	IO_L20P_2	M32	I/O
2	IO_L21N_2	IO_L21N_2	M26	I/O
2	IO_L21P_2	IO_L21P_2	N25	I/O
2	IO_L22N_2	IO_L22N_2	N27	I/O
2	IO_L22P_2	IO_L22P_2	N28	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2VREF_2	N31	VREF
2	IO_L23P_2	IO_L23P_2	N32	I/O
2	IO_L24N_2	IO_L24N_2	N24	I/O
2	IO_L24P_2	IO_L24P_2	P24	I/O
2	IO_L26N_2	IO_L26N_2	P29	I/O
2	IO_L26P_2	IO_L26P_2	P30	I/O
2	IO_L27N_2	IO_L27N_2	P31	I/O
2	IO_L27P_2	IO_L27P_2	P32	I/O
2	IO_L28N_2	IO_L28N_2	P33	I/O
2	IO_L28P_2	IO_L28P_2	P34	I/O
2	IO_L29N_2	IO_L29N_2	R24	I/O
2	IO_L29P_2	IO_L29P_2	R25	I/O
2	IO_L30N_2	IO_L30N_2	R28	I/O
2	IO_L30P_2	IO_L30P_2	R29	I/O
2	IO_L31N_2	IO_L31N_2	R31	I/O
2	IO_L31P_2	IO_L31P_2	R32	I/O
2	IO_L32N_2	IO_L32N_2	R33	I/O
2	IO_L32P_2	IO_L32P_2	R34	I/O
2	IO_L33N_2	IO_L33N_2	R26	I/O
2	IO_L33P_2	IO_L33P_2	T25	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	T28	VREF
2	IO_L34P_2	IO_L34P_2	T29	I/O
2	IO_L35N_2	IO_L35N_2	T32	I/O
2	IO_L35P_2	IO_L35P_2	T33	I/O
2	IO_L37N_2	IO_L37N_2	U27	I/O
2	IO_L37P_2	IO_L37P_2	U28	I/O
2	IO_L38N_2	IO_L38N_2	U29	I/O
2	IO_L38P_2	IO_L38P_2	U30	I/O
2	IO_L39N_2	IO_L39N_2	U31	I/O
2	IO_L39P_2	IO_L39P_2	U32	I/O
2	IO_L40N_2	IO_L40N_2	U33	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	U34	VREF

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
6	IO_L16N_6	IO_L16N_6	AE2	I/O
6	IO_L16P_6	IO_L16P_6	AE1	I/O
6	IO_L17N_6	IO_L17N_6	AD10	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	AD9	VREF
6	IO_L19N_6	IO_L19N_6	AD2	I/O
6	IO_L19P_6	IO_L19P_6	AD1	I/O
6	IO_L20N_6	IO_L20N_6	AC11	I/O
6	IO_L20P_6	IO_L20P_6	AC10	I/O
6	IO_L21N_6	IO_L21N_6	AC8	I/O
6	IO_L21P_6	IO_L21P_6	AC7	I/O
6	IO_L22N_6	IO_L22N_6	AC6	I/O
6	IO_L22P_6	IO_L22P_6	AC5	I/O
6	IO_L23N_6	IO_L23N_6	AC2	I/O
6	IO_L23P_6	IO_L23P_6	AC1	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	AC9	VREF
6	IO_L24P_6	IO_L24P_6	AB10	I/O
6	IO_L25N_6	IO_L25N_6	AB8	I/O
6	IO_L25P_6	IO_L25P_6	AB7	I/O
6	IO_L26N_6	IO_L26N_6	AB4	I/O
6	IO_L26P_6	IO_L26P_6	AB3	I/O
6	IO_L27N_6	IO_L27N_6	AB11	I/O
6	IO_L27P_6	IO_L27P_6	AA11	I/O
6	IO_L28N_6	IO_L28N_6	AA8	I/O
6	IO_L28P_6	IO_L28P_6	AA7	I/O
6	IO_L29N_6	IO_L29N_6	AA6	I/O
6	IO_L29P_6	IO_L29P_6	AA5	I/O
6	IO_L30N_6	IO_L30N_6	AA4	I/O
6	IO_L30P_6	IO_L30P_6	AA3	I/O
6	IO_L31N_6	IO_L31N_6	AA2	I/O
6	IO_L31P_6	IO_L31P_6	AA1	I/O
6	IO_L32N_6	IO_L32N_6	Y11	I/O
6	IO_L32P_6	IO_L32P_6	Y10	I/O
6	IO_L33N_6	IO_L33N_6	Y4	I/O
6	IO_L33P_6	IO_L33P_6	Y3	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	Y2	VREF
6	IO_L34P_6	IO_L34P_6	Y1	I/O
6	IO_L35N_6	IO_L35N_6	Y9	I/O
6	IO_L35P_6	IO_L35P_6	W10	I/O
6	IO_L36N_6	IO_L36N_6	W7	I/O
6	IO_L36P_6	IO_L36P_6	W6	I/O

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
GND	GND	GND	GND	GND	VCCINT	I/O L51N_3 ◆	I/O	I/O	I/O L37P_3	I/O L37N_3	I/O L38P_3	I/O L38N_3	I/O L39P_3	I/O L39N_3	I/O L40P_3	I/O L40N_3 VREF_3	V
GND	GND	GND	GND	VCCINT	VCCO_3	I/O L51P_3 ◆	I/O L33N_3	GND	VCCAUX	I/O L34P_3 VREF_3	I/O L34N_3	GND	VCCO_3	I/O L35P_3	I/O L35N_3	GND	W
GND	GND	GND	GND	VCCINT	VCCO_3	I/O L50P_3	I/O L50N_3	I/O L33P_3	VCCO_3	I/O L30P_3	I/O L30N_3	VCCAUX	I/O L31P_3	I/O L31N_3	I/O L32P_3	I/O L32N_3	Y
GND	GND	GND	GND	VCCINT	VCCO_3	I/O L48N_3	I/O L49P_3 ◆	I/O L49N_3 ◆	I/O L26P_3	I/O L26N_3	I/O L27P_3	I/O L27N_3	I/O L28P_3	I/O L28N_3	I/O L29P_3	I/O L29N_3	AA
GND	VCCINT	VCCINT	VCCINT	VCCINT	VCCO_3	I/O L48P_3	I/O L24N_3	GND	I/O L46P_3	I/O L46N_3	VCCO_3	GND	I/O L47P_3	I/O L47N_3	VCCO_3	GND	AB
VCCINT	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCINT	I/O L20P_3	I/O L20N_3	I/O L24P_3	I/O L21P_3	I/O L21N_3	I/O L22P_3	I/O L22N_3	I/O L23P_3 VREF_3	I/O L23N_3	I/O L45P_3	I/O L45N_3	AC
I/O	I/O	I/O	I/O L18N_4	I/O	I/O L11N_4	DONE	I/O L17P_3 VREF_3	I/O L17N_3	VCCO_3	I/O L44P_3 ◆	I/O L44N_3 ◆	VCCAUX	VCCO_3	GND	I/O L19P_3	I/O L19N_3	AD
I/O	I/O	I/O L23N_4	I/O L18P_4	I/O	I/O L11P_4	I/O ◆	GND	I/O L12N_3	I/O L13P_3	I/O L13N_3 VREF_3	I/O L14P_3	I/O L14N_3	I/O L15P_3	I/O L15N_3	I/O L16P_3	I/O L16N_3	AE
I/O L29N_4	GND	I/O L23P_4	IO VREF_4	GND	I/O L12N_4	I/O	I/O L07N_4	I/O ◆	I/O L12P_3	I/O L09P_3 VREF_3	I/O L09N_3	GND	I/O L10N_3	I/O L11P_3	I/O L11N_3	GND	AF
I/O L29P_4	VCCAUX	VCCO_4	I/O L19N_4	I/O L16N_4	I/O L12P_4	VCCO_4	I/O L07P_4	I/O	I/O	VCCO_3	I/O L07P_3	I/O L07N_3	I/O L10P_3	VCCO_3	I/O L08P_3	I/O L08N_3	AG
I/O L30N_4 D2	I/O L27N_4 DIN D0	I/O L24N_4	I/O L19P_4	I/O L16P_4	IO VREF_4	I/O L39N_4 ◆	I/O L08N_4	I/O L05N_4	VCCO_4	GND	I/O L06P_3	I/O L06N_3	I/O L41P_3 ◆	I/O L41N_3 ◆	I/O	I/O	AH
I/O L30P_4 D3	I/O L27P_4 D1	I/O L24P_4	I/O L20N_4	VCCO_4	I/O L13N_4	I/O L39P_4 ◆	I/O L08P_4	I/O L05P_4	I/O	I/O L35N_4	I/O	VCCAUX	I/O L04P_3	I/O L04N_3	I/O L05P_3	I/O L05N_3	AJ
IO VREF_4	GND	VCCAUX	I/O L20P_4	GND	I/O L13P_4	VCCAUX	I/O	GND	I/O L38N_4	I/O L35P_4	VCCAUX	GND	N.C. ◆ ■	I/O L03P_3	I/O L03N_3	GND	AK
I/O L31N_4 INIT_B	VCCO_4	I/O L25N_4	I/O L21N_4	I/O L17N_4	I/O L14N_4	VCCO_4	I/O L09N_4	I/O L06N_4 VREF_4	I/O L38P_4	I/O L36N_4 ◆	I/O L33N_4	IO VREF_4	CCLK	VCCO_3	I/O L02P_3	I/O L02N_3 VREF_3	AL
I/O L31P_4 DOUT BUSY	I/O L28N_4	I/O L25P_4	I/O L21P_4	I/O L17P_4	I/O L14P_4	GND	I/O L09P_4	I/O L06P_4	VCCO_4	I/O L36P_4 ◆	I/O L33P_4	I/O L03N_4	VCCO_4	GND	I/O L01P_3 VRN_3	I/O L01N_3 VRP_3	AM
I/O L32N_4 GCLK1	I/O L28P_4	I/O L26N_4	I/O L22N_4 VREF_4	VCCO_4	I/O L15N_4	I/O L40N_4 ◆	I/O L10N_4	I/O	I/O L04N_4	I/O L37N_4 ◆	I/O L34N_4	I/O L03P_4	I/O L02N_4	I/O L01N_4 VRP_4	GND	GND	AN
I/O L32P_4 GCLK0	GND	I/O L26P_4 VREF_4	I/O L22P_4	GND	I/O L15P_4	I/O L40P_4 ◆	I/O L10P_4	GND	I/O L04P_4	I/O L37P_4 ◆	I/O L34P_4	GND	I/O L02P_4	I/O L01P_4 VRN_4	GND	GND	AP

Bank 3

Bank 4

DS099-4_14d_072903

Bottom Right Corner of FG1156 Package (Top View)

Figure 60: FG1156 Package Footprint (Top View) Continued