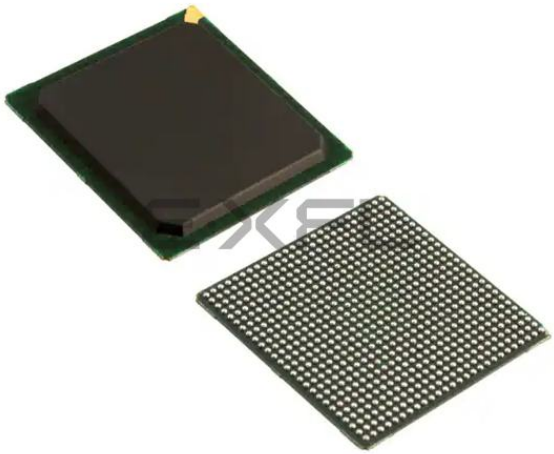

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 1920 |
| Number of Logic Elements/Cells | 17280 |
| Total RAM Bits | 442368 |
| Number of I/O | 391 |
| Number of Gates | 1000000 |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 676-BGA |
| Supplier Device Package | 676-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc3s1000-4fgg676c |

## ESD Protection

Clamp diodes protect all device pads against damage from Electro-Static Discharge (ESD) as well as excessive voltage transients. Each I/O has two clamp diodes: One diode extends P-to-N from the pad to $V_{CCO}$ and a second diode extends N-to-P from the pad to GND. During operation, these diodes are normally biased in the off state. These clamp diodes are always connected to the pad, regardless of the signal standard selected. The presence of diodes limits the ability of Spartan-3 FPGA I/Os to tolerate high signal voltages. The $V_{IN}$ absolute maximum rating in Table 28, page 58 specifies the voltage range that I/Os can tolerate.

## Slew Rate Control and Drive Strength

Two options, FAST and SLOW, control the output slew rate. The FAST option supports output switching at a high rate. The SLOW option reduces bus transients. These options are only available when using one of the LVCMOS or LVTTL standards, which also provide up to seven different levels of current drive strength: 2, 4, 6, 8, 12, 16, and 24 mA. Choosing the appropriate drive strength level is yet another means to minimize bus transients.

Table 7 shows the drive strengths that the LVCMOS and LVTTL standards support.

*Table 7:* **Programmable Output Drive Current**

| Signal Standard (IOSTANDARD) | Current Drive (mA) | | | | | | |
|---|---|---|---|---|---|---|---|
| | 2 | 4 | 6 | 8 | 12 | 16 | 24 |
| LVTTL | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| LVCMOS33 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| LVCMOS25 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| LVCMOS18 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | – |
| LVCMOS15 | ✓ | ✓ | ✓ | ✓ | ✓ | – | – |
| LVCMOS12 | ✓ | ✓ | ✓ | – | – | – | – |

## Boundary-Scan Capability

All Spartan-3 FPGA IOBs support boundary-scan testing compatible with IEEE 1149.1 standards. During boundary- scan operations such as EXTEST and HIGHZ the I/O pull-down resistor is active. For more information, see Boundary-Scan (JTAG) Mode, page 50, and refer to the “Using Boundary-Scan and BSDL Files” chapter in UG331.

## SelectIO Interface Signal Standards

The IOBs support 18 different single-ended signal standards, as listed in Table 8. Furthermore, the majority of IOBs can be used in specific pairs supporting any of eight differential signal standards, as shown in Table 9.

To define the SelectIO™ interface signaling standard in a design, set the IOSTANDARD attribute to the appropriate setting. Xilinx provides a variety of different methods for applying the IOSTANDARD for maximum flexibility. For a full description of different methods of applying attributes to control IOSTANDARD, refer to the “Using I/O Resources” chapter in UG331.

Together with placing the appropriate I/O symbol, two externally applied voltage levels, $V_{CCO}$ and $V_{REF}$, select the desired signal standard. The $V_{CCO}$ lines provide current to the output driver. The voltage on these lines determines the output voltage swing for all standards except GTL and GTLP.

All single-ended standards except the LVCMOS, LVTTL, and PCI varieties require a Reference Voltage ($V_{REF}$) to bias the input-switching threshold. Once a configuration data file is loaded into the FPGA that calls for the I/Os of a given bank to use such a signal standard, a few specifically reserved I/O pins on the same bank automatically convert to $V_{REF}$ inputs. When using one of the LVCMOS standards, these pins remain I/Os because the $V_{CCO}$ voltage biases the input-switching threshold, so there is no need for $V_{REF}$. Select the $V_{CCO}$ and $V_{REF}$ levels to suit the desired single-ended standard according to Table 8.

The DLL component has two clock inputs, CLKIN and CLKFB, as well as seven clock outputs, CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV as described in Table 16. The clock outputs drive simultaneously; however, the High Frequency mode only supports a subset of the outputs available in the Low Frequency mode. See DLL Frequency Modes, page 35. Signals that initialize and report the state of the DLL are discussed in The Status Logic Component, page 41.

*Table 16:* **DLL Signals**

| Signal | Direction | Description | Mode Support | |
|---|---|---|---|---|
| | | | Low Frequency | High Frequency |
| CLKIN | Input | Accepts original clock signal. | Yes | Yes |
| CLKFB | Input | Accepts either CLK0 or CLK2X as feed back signal. (Set CLK_FEEDBACK attribute accordingly). | Yes | Yes |
| CLK0 | Output | Generates clock signal with same frequency and phase as CLKIN. | Yes | Yes |
| CLK90 | Output | Generates clock signal with same frequency as CLKIN, only phase-shifted 90°. | Yes | No |
| CLK180 | Output | Generates clock signal with same frequency as CLKIN, only phase-shifted 180°. | Yes | Yes |
| CLK270 | Output | Generates clock signal with same frequency as CLKIN, only phase-shifted 270°. | Yes | No |
| CLK2X | Output | Generates clock signal with same phase as CLKIN, only twice the frequency. | Yes | No |
| CLK2X180 | Output | Generates clock signal with twice the frequency of CLKIN, phase-shifted 180° with respect to CLKIN. | Yes | No |
| CLKDV | Output | Divides the CLKIN frequency by CLKDV_DIVIDE value to generate lower frequency clock signal that is phase-aligned to CLKIN. | Yes | Yes |

The clock signal supplied to the CLKIN input serves as a reference waveform, with which the DLL seeks to align the feedback signal at the CLKFB input. When eliminating clock skew, the common approach to using the DLL is as follows: The CLK0 signal is passed through the clock distribution network to all the registers it synchronizes. These registers are either internal or external to the FPGA. After passing through the clock distribution network, the clock signal returns to the DLL via a feedback line called CLKFB. The control block inside the DLL measures the phase error between CLKFB and CLKIN. This phase error is a measure of the clock skew that the clock distribution network introduces. The control block activates the appropriate number of delay elements to cancel out the clock skew. Once the DLL has brought the CLK0 signal in phase with the CLKIN signal, it asserts the LOCKED output, indicating a “lock” on to the CLKIN signal.

### DLL Attributes and Related Functions

A number of different functional options can be set for the DLL component through the use of the attributes described in Table 17. Each attribute is described in detail in the sections that follow:

*Table 17:* **DLL Attributes**

| Attribute | Description | Values |
|---|---|---|
| CLK_FEEDBACK | Chooses either the CLK0 or CLK2X output to drive the CLKFB input | NONE, 1X, 2X |
| DLL_FREQUENCY_MODE | Chooses between High Frequency and Low Frequency modes | LOW, HIGH |
| CLKIN_DIVIDE_BY_2 | Halves the frequency of the CLKIN signal just as it enters the DCM | TRUE, FALSE |
| CLKDV_DIVIDE | Selects constant used to divide the CLKIN input frequency to generate the CLKDV output frequency | 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6.0, 6.5, 7.0, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16. |
| DUTY_CYCLE_CORRECTION | Enables 50% duty cycle correction for the CLK0, CLK90, CLK180, and CLK270 outputs | TRUE, FALSE |

### DLL Clock Input Connections

An external clock source enters the FPGA using a Global Clock Input Buffer (IBUFG), which directly accesses the global clock network or an Input Buffer (IBUF). Clock signals within the FPGA drive a global clock net using a Global Clock Multiplexer Buffer (BUFGMUX). The global clock net connects directly to the CLKIN input. The internal and external connections are shown in the [a] and [c] sections, respectively, of Figure 21. A differential clock (e.g., LVDS) can serve as an input to CLKIN.

### DLL Clock Output and Feedback Connections

As many as four of the nine DCM clock outputs can simultaneously drive the four BUFGMUX buffers on the same die edge (top or bottom). All DCM clock outputs can simultaneously drive general routing resources, including interconnect leading to OBUF buffers.

The feedback loop is essential for DLL operation and is established by driving the CLKFB input with either the CLK0 or the CLK2X signal so that any undesirable clock distribution delay is included in the loop. It is possible to use either of these two signals for synchronizing any of the seven DLL outputs: CLK0, CLK90, CLK180, CLK270, CLKDV, CLK2X, or CLK2X180. The value assigned to the CLK_FEEDBACK attribute must agree with the physical feedback connection: a value of 1X for the CLK0 case, 2X for the CLK2X case. If the DCM is used in an application that does not require the DLL—i.e., only the DFS is used—then there is no feedback loop so CLK_FEEDBACK is set to NONE.

CLK2X feedback is only supported on all mask revision ‘E’ and later devices (see Mask and Fab Revisions, page 58), on devices with the "GQ" fabrication code, and on all versions of the XC3S50 and XC3S1000.

There are two basic cases that determine how to connect the DLL clock outputs and feedback connections: on-chip synchronization and off-chip synchronization, which are illustrated in Figure 21.

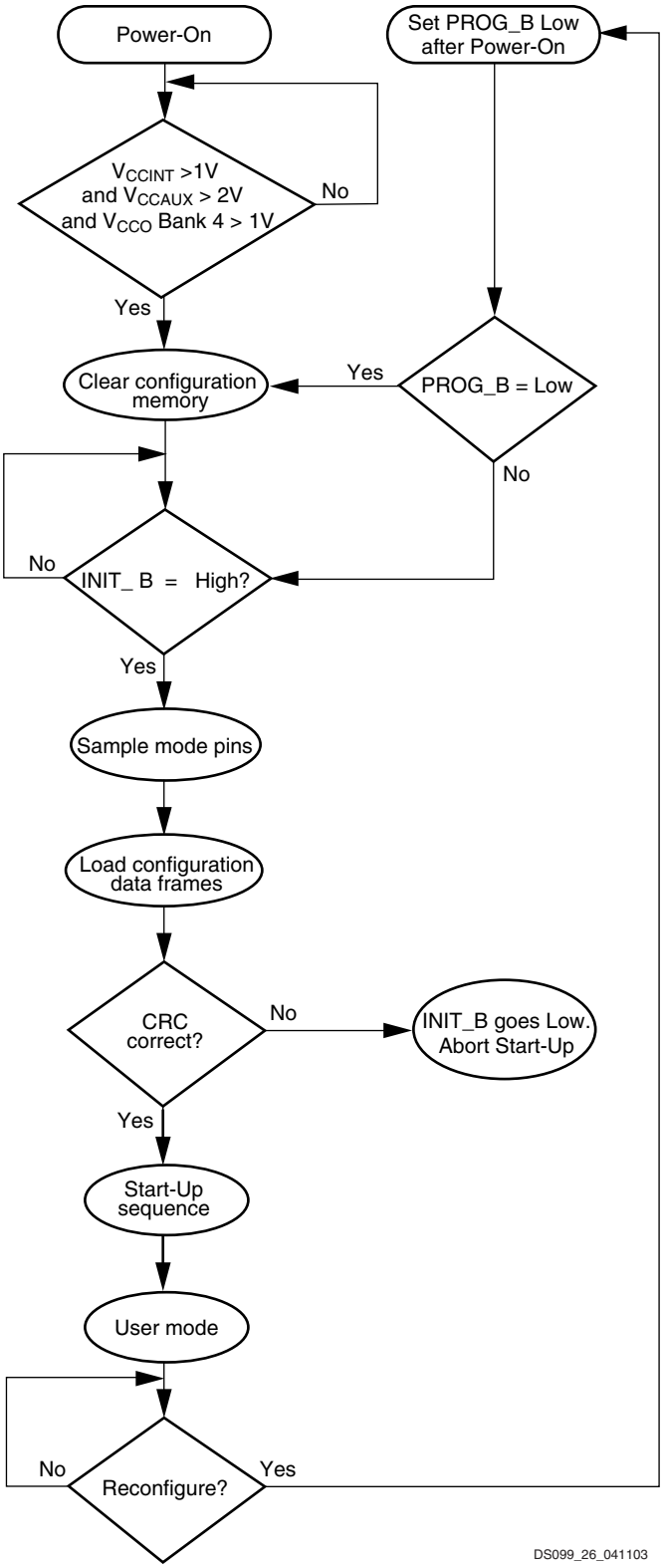


*Figure 29:* **Configuration Flow Diagram for the Serial and Parallel Modes**

## DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

- **Advance:** Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur. Use as estimates, not for production.
- **Preliminary:** Based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reported delays is greatly reduced compared to Advance data. Use as estimates, not for production.
- **Production:** These specifications are approved only after silicon has been characterized over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Parameter values are considered stable with no future changes expected.

  Production-quality systems must only use FPGA designs compiled with a Production status speed file. FPGA designs using a less mature speed file designation should only be used during system prototyping or preproduction qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **The following applies unless otherwise noted: The parameter values published in this module apply to all Spartan®-3 devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.** All parameters representing voltages are measured with respect to GND.

### Mask and Fab Revisions

Some specifications list different values for one or more mask or fab revisions, indicated by the device top marking (see Package Marking, page 5). The revision differences involve the power ramp rates, differential DC specifications, and DCM characteristics. The most recent revision (mask rev E and GQ fab/geometry code) is errata-free with improved specifications than earlier revisions.

Mask rev E with fab rev GQ has been shipping since 2005 (see XCN05009) and has been 100% of Xilinx Spartan-3 device shipments since 2006. SCD 0974 was provided to ensure the receipt of the rev E silicon, but it is no longer needed. Parts ordered under the SCD appended “0974” to the standard part number. For example, “XC3S50-4VQ100C” became “XC3S50-4VQ100C0974”.

*Table 28:* **Absolute Maximum Ratings**

| Symbol | Description | Conditions | | Min | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage relative to GND | | | –0.5 | 1.32 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND | | | –0.5 | 3.00 | V |
| $V_{CCO}$ | Output driver supply voltage relative to GND | | | –0.5 | 3.75 | V |
| $V_{REF}$ | Input reference voltage relative to GND | | | –0.5 | $V_{CCO}$ + 0.5 | V |
| $V_{IN}$ | Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND(2,4) | Driver in a high-impedance state | Commercial | –0.95 | 4.4 | V |
| | | | Industrial | –0.85 | 4.3 | |
| | Voltage applied to all Dedicated pins relative to GND(3) | | All temp. ranges | –0.5 | $V_{CCAUX}$ + 0.5 | V |

*Table 50:* **Recommended Number of Simultaneously Switching Outputs per $V_{CCO}$/GND Pair *(Cont'd)***

| Signal Standard (IOSTANDARD) | | | Package | | | | |
|---|---|---|---|---|---|---|---|
| | | | VQ100 | TQ144 | PQ208 | CP132 | FT256, FG320, FG456, FG676, FG900, FG1156 |
| LVCMOS33 | Slow | 2 | 34 | 24 | 24 | 52 | 76 |
| | | 4 | 17 | 14 | 14 | 26 | 46 |
| | | 6 | 17 | 11 | 11 | 26 | 27 |
| | | 8 | 10 | 10 | 10 | 13 | 20 |
| | | 12 | 9 | 9 | 9 | 13 | 13 |
| | | 16 | 8 | 8 | 8 | 8 | 10 |
| | | 24 | 8 | 8 | 8 | 8 | 9 |
| | Fast | 2 | 20 | 20 | 20 | 26 | 44 |
| | | 4 | 15 | 15 | 15 | 15 | 26 |
| | | 6 | 11 | 11 | 11 | 13 | 16 |
| | | 8 | 10 | 10 | 10 | 10 | 12 |
| | | 12 | 8 | 8 | 8 | 8 | 10 |
| | | 16 | 8 | 8 | 8 | 8 | 8 |
| | | 24 | 7 | 7 | 7 | 7 | 7 |
| LVDCI_33 | | | 10 | 10 | 10 | 10 | 10 |
| LVDCI_DV2_33 | | | 10 | 10 | 10 | 10 | 10 |
| HSLVDCI_33 | | | 10 | 10 | 10 | 10 | 10 |
| LVTTL | Slow | 2 | 34 | 25 | 25 | 52 | 60 |
| | | 4 | 17 | 16 | 16 | 26 | 41 |
| | | 6 | 17 | 15 | 15 | 26 | 29 |
| | | 8 | 12 | 12 | 12 | 13 | 22 |
| | | 12 | 10 | 10 | 10 | 13 | 13 |
| | | 16 | 10 | 10 | 10 | 10 | 11 |
| | | 24 | 8 | 8 | 8 | 8 | 9 |
| | Fast | 2 | 20 | 20 | 20 | 26 | 34 |
| | | 4 | 13 | 13 | 13 | 13 | 20 |
| | | 6 | 11 | 11 | 11 | 13 | 15 |
| | | 8 | 10 | 10 | 10 | 10 | 12 |
| | | 12 | 9 | 9 | 9 | 9 | 10 |
| | | 16 | 8 | 8 | 8 | 8 | 9 |
| | | 24 | 7 | 7 | 7 | 7 | 7 |

*Table 50:* **Recommended Number of Simultaneously Switching Outputs per $V_{CCO}$/GND Pair *(Cont'd)***

| Signal Standard (IOSTANDARD) | Package | | | | |
|---|---|---|---|---|---|
| | VQ100 | TQ144 | PQ208 | CP132 | FT256, FG320, FG456, FG676, FG900, FG1156 |
| PCI33_3 | 9 | 9 | 9 | 9 | 9 |
| SSTL18_I | 13 | 13 | 13 | 13 | 17 |
| SSTL18_I_DCI | 13 | 13 | 13 | 13 | 17 |
| SSTL18_II | 8 | 8 | 8 | 8 | 9 |
| SSTL2_I | 10 | 10 | 10 | 10 | 13 |
| SSTL2_I_DCI | 10 | 10 | 10 | 10 | 13 |
| SSTL2_II | 6 | 6 | 6 | 6 | 9 |
| SSTL2_II_DCI | 6 | 6 | 6 | 6 | 9 |
| **Differential Standards (Number of I/O Pairs or Channels)** | | | | | |
| LDT_25 (ULVDS_25) | 5 | 5 | 5 | 5 | 5 |
| LVDS_25 | 7 | 5 | 5 | 12 | 20 |
| BLVDS_25 | 2 | 1 | 1 | | 4 |
| LVDSEXT_25 | 5 | 5 | 5 | 5 | 5 |
| LVPECL_25 | 2 | 1 | 1 | | 4 |
| RSDS_25 | 7 | 5 | 5 | 12 | 20 |
| DIFF_HSTL_II_18 | 4 | 4 | 4 | 4 | 4 |
| DIFF_HSTL_II_18_DCI | 4 | 4 | 4 | 4 | 4 |
| DIFF_SSTL2_II | 3 | 3 | 3 | 3 | 4 |
| DIFF_SSTL2_II_DCI | 3 | 3 | 3 | 3 | 4 |

**Notes:**

1. The numbers in this table are recommendations that assume the FPGA is soldered on a printed circuit board using sound practices. This table assumes the following parasitic factors: combined PCB trace and land inductance per $V_{CCO}$ and GND pin of 1.0 nH, receiver capacitive load of 15 pF. Test limits are the $V_{IL}/V_{IH}$ voltage limits for the respective I/O standard.
2. Regarding the SSO numbers for all DCI standards, the $R_{REF}$ resistors connected to the VRN and VRP pins of the FPGA are 50W..
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: *Managing Ground Bounce in Large FPGAs* for information on how to perform weighted average SSO calculations.
4. Results are based on actual silicon testing using an FPGA soldered on a typical printed-circuit board.

*Table 61:* **Switching Characteristics for the DFS**

| Symbol | Description | Frequency Mode | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | -5 | | -4 | | |
| | | | | Min | Max | Min | Max | |
| **Output Frequency Ranges** | | | | | | | | |
| CLKOUT_FREQ_FX_LF | Frequency for the CLKFX and CLKFX180 outputs | Low | All | 18 | 210 | 18 | 210 | MHz |
| CLKOUT_FREQ_FX_HF | | High | All | 210 | 326(2) | 210 | 307(2) | MHz |
| **Output Clock Jitter** | | | | | | | | |
| CLKOUT_PER_JITT_FX | Period jitter at the CLKFX and CLKFX180 outputs | All | All | Note 3 | Note 3 | Note 3 | Note 3 | ps |
| **Duty Cycle**(4) | | | | | | | | |
| CLKOUT_DUTY_CYCLE_FX | Duty cycle precision for the CLKFX and CLKFX180 outputs | All | XC3S50 | – | ±100 | – | ±100 | ps |
| | | | XC3S200 | – | ±100 | – | ±100 | ps |
| | | | XC3S400 | – | ±250 | – | ±250 | ps |
| | | | XC3S1000 | – | ±400 | – | ±400 | ps |
| | | | XC3S1500 | – | ±400 | – | ±400 | ps |
| | | | XC3S2000 | – | ±400 | – | ±400 | ps |
| | | | XC3S4000 | – | ±400 | – | ±400 | ps |
| | | | XC3S5000 | – | ±400 | – | ±400 | ps |
| **Phase Alignment** | | | | | | | | |
| CLKOUT_PHASE | Phase offset between the DFS output and the CLK0 output | All | All | – | ±300 | – | ±300 | ps |
| **Lock Time** | | | | | | | | |
| LOCK_DLL_FX | When using the DFS in conjunction with the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. | All | All | – | 10.0 | – | 10.0 | ms |
| LOCK_FX | When using the DFS without the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. By asserting the LOCKED signal, the DFS indicates valid CLKFX and CLKFX180 signals. | All | All | – | 10.0 | – | 10.0 | ms |

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 32 and Table 60.
2. Mask revisions prior to the E mask revision have a CLKOUT_FREQ_FX_HF max of 280 MHz. See Mask and Fab Revisions, page 58.
3. Use the DCM Clocking Wizard in the ISE software for a Spartan-3 device specific number. Jitter number assumes 150 ps of input clock jitter.
4. The CLKFX and CLKFX180 outputs always approximate 50% duty cycles.
5. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) is in use.

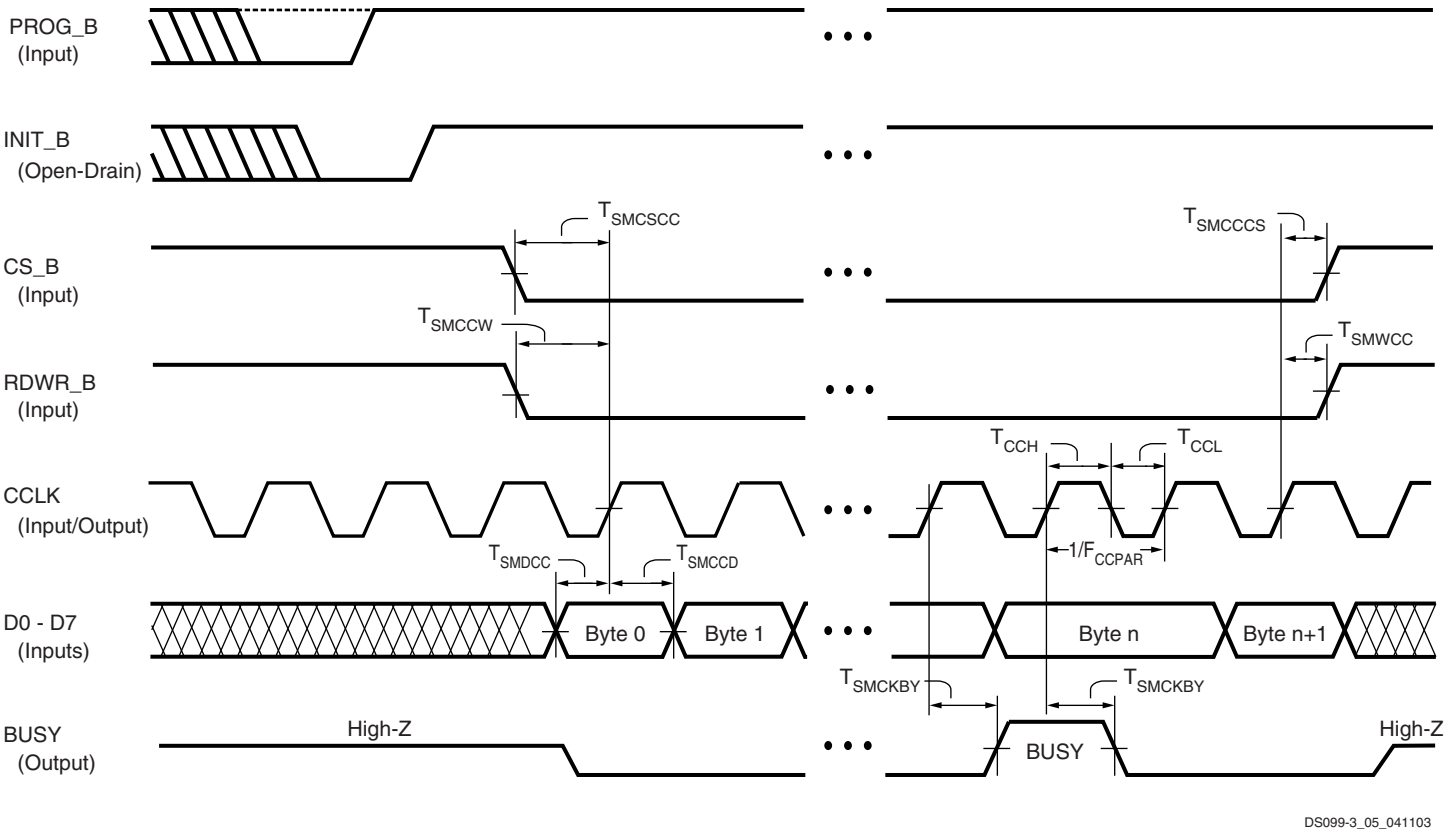


*Figure 38:* **Waveforms for Master and Slave Parallel Configuration**

*Table 67:* **Timing for the Master and Slave Parallel Configuration Modes**

| Symbol | Description | Slave/ Master | All Speed Grades | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| **Clock-to-Output Times** | | | | | |
| $T_{SMCKBY}$ | The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin | Slave | – | 12.0 | ns |
| **Setup Times** | | | | | |
| $T_{SMDCC}$ | The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin | Both | 10.0 | – | ns |
| $T_{SMCSCC}$ | The time from the setup of a logic level at the CS_B pin to the rising transition at the CCLK pin | | 10.0 | – | ns |
| $T_{SMCCW}$(3) | The time from the setup of a logic level at the RDWR_B pin to the rising transition at the CCLK pin | | 10.0 | – | ns |
| **Hold Times** | | | | | |
| $T_{SMCCD}$ | The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins | Both | 0 | – | ns |
| $T_{SMCCCS}$ | The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CS_B pin | | 0 | – | ns |
| $T_{SMWCC}$(3) | The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin | | 0 | – | ns |

Once the FPGA enters User mode after completing configuration, the DONE pin no longer drives the DONE pin Low. The bitstream generator option DonePin determines whether or not a pull-up resistor is present on the DONE pin to pull the pin to VCCAUX. If the pull-up resistor is eliminated, then the DONE pin must be pulled High using an external pull-up resistor or one of the FPGAs in the design must actively drive the DONE pin High via the DriveDone bitstream generator option.

The bitstream generator option DriveDone causes the FPGA to actively drive the DONE output High after configuration. This option should only be used in single-FPGA designs or on the last FPGA in a multi-FPGA daisy-chain.

By default, the bitstream generator software retains the pull-up resistor and does not actively drive the DONE pin as highlighted in Table 74, which shows the interaction of these bitstream options in single- and multi-FPGA designs.

*Table 74:* **DonePin and DriveDone Bitstream Option Interaction**

| DonePin | DriveDone | Single- or Multi-FPGA Design | Comments |
|---|---|---|---|
| Pullnone | No | Single | External pull-up resistor, with value between 330Ω to 3.3kΩ, required on DONE. |
| Pullnone | No | Multi | External pull-up resistor, with value between 330Ω to 3.3kΩ, required on common node connecting to all DONE pins. |
| Pullnone | Yes | Single | OK, no external requirements. |
| Pullnone | Yes | Multi | DriveDone on last device in daisy-chain only. No external requirements. |
| Pullup | No | Single | OK, but pull-up on DONE pin has slow rise time. May require 330Ω pull-up resistor for high CCLK frequencies. |
| Pullup | No | Multi | External pull-up resistor, with value between 330Ω to 3.3kΩ, required on common node connecting to all DONE pins. |
| Pullup | Yes | Single | OK, no external requirements. |
| Pullup | Yes | Multi | DriveDone on last device in daisy-chain only. No external requirements. |

### M2, M1, M0: Configuration Mode Selection

The M2, M1, and M0 inputs select the FPGA configuration mode, as described in Table 75. The logic levels applied to the mode pins are sampled on the rising edge of INIT_B.

*Table 75:* **Spartan-3 FPGA Mode Select Settings**

| Configuration Mode | M2 | M1 | M0 |
|---|---|---|---|
| Master Serial | 0 | 0 | 0 |
| Slave Serial | 1 | 1 | 1 |
| Master Parallel | 0 | 1 | 1 |
| Slave Parallel | 1 | 1 | 0 |
| JTAG | 1 | 0 | 1 |
| Reserved | 0 | 0 | 1 |
| Reserved | 0 | 1 | 0 |
| Reserved | 1 | 0 | 0 |
| After Configuration | X | X | X |

**Notes:**

1. X = don't care, either 0 or 1.

Before and during configuration, the mode pins have an internal pull-up resistor to VCCAUX, regardless of the HSWAP_EN pin. If the mode pins are unconnected, then the FPGA defaults to the Slave Serial configuration mode. After configuration successfully completes, any levels applied to these input are ignored. Furthermore, the bitstream generator options M0Pin, M1Pin, and M2Pin determines whether a pull-up resistor, pull-down resistor, or no resistor is present on its respective mode pin, M0, M1, or M2.

## Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3 FPGA is reported using either the XPower Estimator (XPE) or the XPower Analyzer integrated in the Xilinx ISE development software. Table 86 provides the thermal characteristics for the various Spartan-3 device/package offerings.

The junction-to-case thermal resistance ($\theta_{JC}$) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board ($\theta_{JB}$) value similarly reports the difference between the board and junction temperature. The junction-to-ambient ($\theta_{JA}$) value reports the temperature difference per watt between the ambient environment and the junction temperature. The $\theta_{JA}$ value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the $\theta_{JA}$ value in a system without a fan. The thermal resistance drops with increasing air flow.

*Table 86:* **Spartan-3 FPGA Package Thermal Characteristics**

| Package | Device | Junction-to-Case ($\theta_{JC}$) | Junction-to-Board ($\theta_{JB}$) | Junction-to-Ambient ($\theta_{JA}$) at Different Air Flows | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Still Air (0 LFM) | 250 LFM | 500 LFM | 750 LFM | |
| VQ(G)100 | XC3S50 | 12.0 | – | 46.2 | 38.4 | 35.8 | 34.9 | °C/Watt |
| | XC3S200 | 10.0 | – | 40.5 | 33.7 | 31.3 | 30.5 | °C/Watt |
| CP(G)132(1) | XC3S50 | 14.5 | 32.8 | 53.0 | 46.4 | 44.0 | 42.5 | °C/Watt |
| TQ(G)144 | XC3S50 | 7.6 | – | 41.0 | 31.9 | 27.2 | 25.6 | °C/Watt |
| | XC3S200 | 6.6 | – | 34.5 | 26.9 | 23.0 | 21.6 | °C/Watt |
| | XC3S400 | 6.1 | – | 32.8 | 25.5 | 21.8 | 20.4 | °C/Watt |
| PQ(G)208 | XC3S50 | 10.6 | – | 37.4 | 27.6 | 24.4 | 22.6 | °C/Watt |
| | XC3S200 | 8.6 | – | 36.2 | 26.7 | 23.6 | 21.9 | °C/Watt |
| | XC3S400 | 7.5 | – | 35.4 | 26.1 | 23.1 | 21.4 | °C/Watt |
| FT(G)256 | XC3S200 | 9.9 | 22.9 | 31.7 | 25.6 | 24.5 | 24.2 | °C/Watt |
| | XC3S400 | 7.9 | 19.0 | 28.4 | 22.8 | 21.5 | 21.0 | °C/Watt |
| | XC3S1000 | 5.6 | 14.7 | 24.8 | 19.2 | 18.0 | 17.5 | °C/Watt |
| FG(G)320 | XC3S400 | 8.9 | 13.9 | 24.4 | 19.0 | 17.8 | 17.0 | °C/Watt |
| | XC3S1000 | 7.8 | 11.8 | 22.3 | 17.0 | 15.8 | 15.0 | °C/Watt |
| | XC3S1500 | 6.7 | 9.8 | 20.3 | 15.18 | 13.8 | 13.1 | °C/Watt |
| FG(G)456 | XC3S400 | 8.4 | 13.6 | 20.8 | 15.1 | 13.9 | 13.4 | °C/Watt |
| | XC3S1000 | 6.4 | 10.6 | 19.3 | 13.4 | 12.3 | 11.7 | °C/Watt |
| | XC3S1500 | 4.9 | 8.3 | 18.3 | 12.4 | 11.2 | 10.7 | °C/Watt |
| | XC3S2000 | 3.7 | 6.5 | 17.7 | 11.7 | 10.5 | 10.0 | °C/Watt |
| FG(G)676 | XC3S1000 | 6.0 | 10.4 | 17.9 | 13.7 | 12.6 | 12.0 | °C/Watt |
| | XC3S1500 | 4.9 | 8.8 | 16.8 | 12.4 | 11.3 | 10.7 | °C/Watt |
| | XC3S2000 | 4.1 | 7.9 | 15.6 | 11.1 | 9.9 | 9.3 | °C/Watt |
| | XC3S4000 | 3.6 | 7.0 | 15.0 | 10.5 | 9.3 | 8.7 | °C/Watt |
| | XC3S5000 | 3.4 | 6.3 | 14.7 | 10.3 | 9.1 | 8.5 | °C/Watt |
| FG(G)900 | XC3S2000 | 3.7 | 7.0 | 14.3 | 10.3 | 9.3 | 8.8 | °C/Watt |
| | XC3S4000 | 3.3 | 6.4 | 13.6 | 9.7 | 8.7 | 8.2 | °C/Watt |
| | XC3S5000 | 2.9 | 5.9 | 13.1 | 9.2 | 8.1 | 7.6 | °C/Watt |

# CP132: 132-Ball Chip-Scale Package

**Note:** The CP132 and CPG132 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

The pinout and footprint for the XC3S50 in the 132-ball chip-scale package, CP132, appear in Table 89 and Figure 45.

All the package pins appear in Table 89 and are sorted by bank number, then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The CP132 footprint has eight I/O banks. However, the voltage supplies for the two I/O banks along an edge are connected together internally. Consequently, there are four output voltage supplies, labeled VCCO_TOP, VCCO_RIGHT, VCCO_BOTTOM, and VCCO_LEFT.

## Pinout Table

*Table 89:* **CP132 Package Pinout**

| Bank | XC3S50 Pin Name | CP132 Ball | Type |
|---|---|---|---|
| 0 | IO_L01N_0/VRP_0 | A3 | DCI |
| 0 | IO_L01P_0/VRN_0 | C4 | DCI |
| 0 | IO_L27N_0 | C5 | I/O |
| 0 | IO_L27P_0 | B5 | I/O |
| 0 | IO_L30N_0 | B6 | I/O |
| 0 | IO_L30P_0 | A6 | I/O |
| 0 | IO_L31N_0 | C7 | I/O |
| 0 | IO_L31P_0/VREF_0 | B7 | VREF |
| 0 | IO_L32N_0/GCLK7 | A7 | GCLK |
| 0 | IO_L32P_0/GCLK6 | C8 | GCLK |
| 1 | IO_L01N_1/VRP_1 | A13 | DCI |
| 1 | IO_L01P_1/VRN_1 | B13 | DCI |
| 1 | IO_L27N_1 | C11 | I/O |
| 1 | IO_L27P_1 | A12 | I/O |
| 1 | IO_L28N_1 | A11 | I/O |
| 1 | IO_L28P_1 | B11 | I/O |
| 1 | IO_L31N_1/VREF_1 | C9 | VREF |
| 1 | IO_L31P_1 | A10 | I/O |
| 1 | IO_L32N_1/GCLK5 | A8 | GCLK |
| 1 | IO_L32P_1/GCLK4 | A9 | GCLK |
| 2 | IO_L01N_2/VRP_2 | D12 | DCI |
| 2 | IO_L01P_2/VRN_2 | C14 | DCI |
| 2 | IO_L20N_2 | E12 | I/O |
| 2 | IO_L20P_2 | E13 | I/O |
| 2 | IO_L21N_2 | E14 | I/O |
| 2 | IO_L21P_2 | F12 | I/O |
| 2 | IO_L23N_2/VREF_2 | F13 | VREF |
| 2 | IO_L23P_2 | F14 | I/O |
| 2 | IO_L24N_2 | G12 | I/O |

*Table 93:* **PQ208 Package Pinout *(Cont'd)***

| Bank | XC3S50 Pin Name | XC3S200, XC3S400 Pin Names | PQ208 Pin Number | Type |
|---|---|---|---|---|
| 3 | IO_L20P_3 | IO_L20P_3 | P114 | I/O |
| 3 | IO_L21N_3 | IO_L21N_3 | P117 | I/O |
| 3 | IO_L21P_3 | IO_L21P_3 | P116 | I/O |
| 3 | IO_L22N_3 | IO_L22N_3 | P120 | I/O |
| 3 | IO_L22P_3 | IO_L22P_3 | P119 | I/O |
| 3 | IO_L23N_3 | IO_L23N_3 | P123 | I/O |
| 3 | IO_L23P_3/VREF_3 | IO_L23P_3/VREF_3 | P122 | VREF |
| 3 | IO_L24N_3 | IO_L24N_3 | P125 | I/O |
| 3 | IO_L24P_3 | IO_L24P_3 | P124 | I/O |
| 3 | N.C. (◆) | IO_L39N_3 | P128 | I/O |
| 3 | N.C. (◆) | IO_L39P_3 | P126 | I/O |
| 3 | IO_L40N_3/VREF_3 | IO_L40N_3/VREF_3 | P131 | VREF |
| 3 | IO_L40P_3 | IO_L40P_3 | P130 | I/O |
| 3 | VCCO_3 | VCCO_3 | P110 | VCCO |
| 3 | VCCO_3 | VCCO_3 | P127 | VCCO |
| 4 | IO | IO | P93 | I/O |
| 4 | N.C. (◆) | IO | P97 | I/O |
| 4 | IO/VREF_4 | IO/VREF_4 | P85 | VREF |
| 4 | N.C. (◆) | IO/VREF_4 | P96 | VREF |
| 4 | IO/VREF_4 | IO/VREF_4 | P102 | VREF |
| 4 | IO_L01N_4/VRP_4 | IO_L01N_4/VRP_4 | P101 | DCI |
| 4 | IO_L01P_4/VRN_4 | IO_L01P_4/VRN_4 | P100 | DCI |
| 4 | IO_L25N_4 | IO_L25N_4 | P95 | I/O |
| 4 | IO_L25P_4 | IO_L25P_4 | P94 | I/O |
| 4 | IO_L27N_4/DIN/D0 | IO_L27N_4/DIN/D0 | P92 | DUAL |
| 4 | IO_L27P_4/D1 | IO_L27P_4/D1 | P90 | DUAL |
| 4 | IO_L30N_4/D2 | IO_L30N_4/D2 | P87 | DUAL |
| 4 | IO_L30P_4/D3 | IO_L30P_4/D3 | P86 | DUAL |
| 4 | IO_L31N_4/INIT_B | IO_L31N_4/INIT_B | P83 | DUAL |
| 4 | IO_L31P_4/DOUT/BUSY | IO_L31P_4/DOUT/BUSY | P81 | DUAL |
| 4 | IO_L32N_4/GCLK1 | IO_L32N_4/GCLK1 | P80 | GCLK |
| 4 | IO_L32P_4/GCLK0 | IO_L32P_4/GCLK0 | P79 | GCLK |
| 4 | VCCO_4 | VCCO_4 | P84 | VCCO |
| 4 | VCCO_4 | VCCO_4 | P98 | VCCO |
| 5 | IO | IO | P63 | I/O |
| 5 | IO | IO | P71 | I/O |
| 5 | IO/VREF_5 | IO/VREF_5 | P78 | VREF |
| 5 | IO_L01N_5/RDWR_B | IO_L01N_5/RDWR_B | P58 | DUAL |
| 5 | IO_L01P_5/CS_B | IO_L01P_5/CS_B | P57 | DUAL |
| 5 | IO_L10N_5/VRP_5 | IO_L10N_5/VRP_5 | P62 | DCI |

*Table 98:* **FG320 Package Pinout *(Cont'd)***

| Bank | XC3S400, XC3S1000, XC3S1500 Pin Name | FG320 Pin Number | Type |
|---|---|---|---|
| 2 | IO_L20N_2 | E17 | I/O |
| 2 | IO_L20P_2 | E18 | I/O |
| 2 | IO_L21N_2 | F15 | I/O |
| 2 | IO_L21P_2 | E15 | I/O |
| 2 | IO_L22N_2 | F14 | I/O |
| 2 | IO_L22P_2 | G14 | I/O |
| 2 | IO_L23N_2/VREF_2 | G18 | VREF |
| 2 | IO_L23P_2 | F17 | I/O |
| 2 | IO_L24N_2 | G15 | I/O |
| 2 | IO_L24P_2 | G16 | I/O |
| 2 | IO_L27N_2 | H13 | I/O |
| 2 | IO_L27P_2 | H14 | I/O |
| 2 | IO_L34N_2/VREF_2 | H16 | VREF |
| 2 | IO_L34P_2 | H15 | I/O |
| 2 | IO_L35N_2 | H17 | I/O |
| 2 | IO_L35P_2 | H18 | I/O |
| 2 | IO_L39N_2 | J18 | I/O |
| 2 | IO_L39P_2 | J17 | I/O |
| 2 | IO_L40N_2 | J15 | I/O |
| 2 | IO_L40P_2/VREF_2 | J14 | VREF |
| 2 | VCCO_2 | F16 | VCCO |
| 2 | VCCO_2 | H12 | VCCO |
| 2 | VCCO_2 | J12 | VCCO |
| 3 | IO | K15 | I/O |
| 3 | IO_L01N_3/VRP_3 | T17 | DCI |
| 3 | IO_L01P_3/VRN_3 | T16 | DCI |
| 3 | IO_L16N_3 | T18 | I/O |
| 3 | IO_L16P_3 | U18 | I/O |
| 3 | IO_L17N_3 | P16 | I/O |
| 3 | IO_L17P_3/VREF_3 | R16 | VREF |
| 3 | IO_L19N_3 | R17 | I/O |
| 3 | IO_L19P_3 | R18 | I/O |
| 3 | IO_L20N_3 | P18 | I/O |
| 3 | IO_L20P_3 | P17 | I/O |
| 3 | IO_L21N_3 | P15 | I/O |
| 3 | IO_L21P_3 | N15 | I/O |
| 3 | IO_L22N_3 | M14 | I/O |
| 3 | IO_L22P_3 | N14 | I/O |
| 3 | IO_L23N_3 | M15 | I/O |
| 3 | IO_L23P_3/VREF_3 | M16 | VREF |

*Table 100:* **FG456 Package Pinout *(Cont'd)***

| Bank | 3S400 Pin Name | 3S1000, 3S1500, 3S2000 Pin Name | FG456 Pin Number | Type |
|---|---|---|---|---|
| 1 | IO_L15P_1 | IO_L15P_1 | E17 | I/O |
| 1 | IO_L16N_1 | IO_L16N_1 | B17 | I/O |
| 1 | IO_L16P_1 | IO_L16P_1 | C17 | I/O |
| 1 | N.C. (◆) | IO_L19N_1 | C16 | I/O |
| 1 | N.C. (◆) | IO_L19P_1 | D16 | I/O |
| 1 | N.C. (◆) | IO_L22N_1 | A16 | I/O |
| 1 | N.C. (◆) | IO_L22P_1 | B16 | I/O |
| 1 | IO_L24N_1 | IO_L24N_1 | D15 | I/O |
| 1 | IO_L24P_1 | IO_L24P_1 | E15 | I/O |
| 1 | IO_L25N_1 | IO_L25N_1 | B15 | I/O |
| 1 | IO_L25P_1 | IO_L25P_1 | A15 | I/O |
| 1 | IO_L27N_1 | IO_L27N_1 | D14 | I/O |
| 1 | IO_L27P_1 | IO_L27P_1 | E14 | I/O |
| 1 | IO_L28N_1 | IO_L28N_1 | A14 | I/O |
| 1 | IO_L28P_1 | IO_L28P_1 | B14 | I/O |
| 1 | IO_L29N_1 | IO_L29N_1 | C13 | I/O |
| 1 | IO_L29P_1 | IO_L29P_1 | D13 | I/O |
| 1 | IO_L30N_1 | IO_L30N_1 | A13 | I/O |
| 1 | IO_L30P_1 | IO_L30P_1 | B13 | I/O |
| 1 | IO_L31N_1/VREF_1 | IO_L31N_1/VREF_1 | D12 | VREF |
| 1 | IO_L31P_1 | IO_L31P_1 | E12 | I/O |
| 1 | IO_L32N_1/GCLK5 | IO_L32N_1/GCLK5 | B12 | GCLK |
| 1 | IO_L32P_1/GCLK4 | IO_L32P_1/GCLK4 | C12 | GCLK |
| 1 | VCCO_1 | VCCO_1 | C15 | VCCO |
| 1 | VCCO_1 | VCCO_1 | F15 | VCCO |
| 1 | VCCO_1 | VCCO_1 | G12 | VCCO |
| 1 | VCCO_1 | VCCO_1 | G13 | VCCO |
| 1 | VCCO_1 | VCCO_1 | G14 | VCCO |
| 2 | IO | IO | C22 | I/O |
| 2 | IO_L01N_2/VRP_2 | IO_L01N_2/VRP_2 | C20 | DCI |
| 2 | IO_L01P_2/VRN_2 | IO_L01P_2/VRN_2 | C21 | DCI |
| 2 | IO_L16N_2 | IO_L16N_2 | D20 | I/O |
| 2 | IO_L16P_2 | IO_L16P_2 | D19 | I/O |
| 2 | IO_L17N_2 | IO_L17N_2 | D21 | I/O |
| 2 | IO_L17P_2/VREF_2 | IO_L17P_2/VREF_2 | D22 | VREF |
| 2 | IO_L19N_2 | IO_L19N_2 | E18 | I/O |
| 2 | IO_L19P_2 | IO_L19P_2 | F18 | I/O |
| 2 | IO_L20N_2 | IO_L20N_2 | E19 | I/O |
| 2 | IO_L20P_2 | IO_L20P_2 | E20 | I/O |
| 2 | IO_L21N_2 | IO_L21N_2 | E21 | I/O |

*Table 103:* **FG676 Package Pinout *(Cont'd)***

| Bank | XC3S1000 Pin Name | XC3S1500 Pin Name | XC3S2000 Pin Name | XC3S4000 Pin Name | XC3S5000 Pin Name | FG676 Pin Number | Type |
|---|---|---|---|---|---|---|---|
| 6 | IO_L20N_6 | IO_L20N_6 | IO_L20N_6 | IO_L20N_6 | IO_L20N_6 | V7 | I/O |
| 6 | IO_L20P_6 | IO_L20P_6 | IO_L20P_6 | IO_L20P_6 | IO_L20P_6 | U7 | I/O |
| 6 | IO_L21N_6 | IO_L21N_6 | IO_L21N_6 | IO_L21N_6 | IO_L21N_6 | V5 | I/O |
| 6 | IO_L21P_6 | IO_L21P_6 | IO_L21P_6 | IO_L21P_6 | IO_L21P_6 | V4 | I/O |
| 6 | IO_L22N_6 | IO_L22N_6 | IO_L22N_6 | IO_L22N_6 | IO_L22N_6 | V3 | I/O |
| 6 | IO_L22P_6 | IO_L22P_6 | IO_L22P_6 | IO_L22P_6 | IO_L22P_6 | V2 | I/O |
| 6 | IO_L23N_6 | IO_L23N_6 | IO_L23N_6 | IO_L23N_6 | IO_L23N_6 | U6 | I/O |
| 6 | IO_L23P_6 | IO_L23P_6 | IO_L23P_6 | IO_L23P_6 | IO_L23P_6 | U5 | I/O |
| 6 | IO_L24N_6/VREF_6 | IO_L24N_6/VREF_6 | IO_L24N_6/VREF_6 | IO_L24N_6/VREF_6 | IO_L24N_6/VREF_6 | U4 | VREF |
| 6 | IO_L24P_6 | IO_L24P_6 | IO_L24P_6 | IO_L24P_6 | IO_L24P_6 | U3 | I/O |
| 6 | IO_L26N_6 | IO_L26N_6 | IO_L26N_6 | IO_L26N_6 | IO_L26N_6 | U2 | I/O |
| 6 | IO_L26P_6 | IO_L26P_6 | IO_L26P_6 | IO_L26P_6 | IO_L26P_6 | U1 | I/O |
| 6 | IO_L27N_6 | IO_L27N_6 | IO_L27N_6 | IO_L27N_6 | IO_L27N_6 | T8 | I/O |
| 6 | IO_L27P_6 | IO_L27P_6 | IO_L27P_6 | IO_L27P_6 | IO_L27P_6 | T7 | I/O |
| 6 | IO_L28N_6 | IO_L28N_6 | IO_L28N_6 | IO_L28N_6 | IO_L28N_6 | T6 | I/O |
| 6 | IO_L28P_6 | IO_L28P_6 | IO_L28P_6 | IO_L28P_6 | IO_L28P_6 | T5 | I/O |
| 6 | IO_L29N_6 | IO_L29N_6 | IO_L29N_6 | IO_L29N_6 | IO_L29N_6 | T2 | I/O |
| 6 | IO_L29P_6 | IO_L29P_6 | IO_L29P_6 | IO_L29P_6 | IO_L29P_6 | T1 | I/O |
| 6 | IO_L31N_6 | IO_L31N_6 | IO_L31N_6 | IO_L31N_6 | IO_L31N_6 | R8 | I/O |
| 6 | IO_L31P_6 | IO_L31P_6 | IO_L31P_6 | IO_L31P_6 | IO_L31P_6 | R7 | I/O |
| 6 | IO_L32N_6 | IO_L32N_6 | IO_L32N_6 | IO_L32N_6 | IO_L32N_6 | R6 | I/O |
| 6 | IO_L32P_6 | IO_L32P_6 | IO_L32P_6 | IO_L32P_6 | IO_L32P_6 | R5 | I/O |
| 6 | IO_L33N_6 | IO_L33N_6 | IO_L33N_6 | IO_L33N_6 | IO_L33N_6 | T4 | I/O |
| 6 | IO_L33P_6 | IO_L33P_6 | IO_L33P_6 | IO_L33P_6 | IO_L33P_6 | R3 | I/O |
| 6 | IO_L34N_6/VREF_6 | IO_L34N_6/VREF_6 | IO_L34N_6/VREF_6 | IO_L34N_6/VREF_6 | IO_L34N_6/VREF_6 | R2 | VREF |
| 6 | IO_L34P_6 | IO_L34P_6 | IO_L34P_6 | IO_L34P_6 | IO_L34P_6 | R1 | I/O |
| 6 | IO_L35N_6 | IO_L35N_6 | IO_L35N_6 | IO_L35N_6 | IO_L35N_6 | P8 | I/O |
| 6 | IO_L35P_6 | IO_L35P_6 | IO_L35P_6 | IO_L35P_6 | IO_L35P_6 | P7 | I/O |
| 6 | IO_L38N_6 | IO_L38N_6 | IO_L38N_6 | IO_L38N_6 | IO_L38N_6 | P6 | I/O |
| 6 | IO_L38P_6 | IO_L38P_6 | IO_L38P_6 | IO_L38P_6 | IO_L38P_6 | P5 | I/O |
| 6 | IO_L39N_6 | IO_L39N_6 | IO_L39N_6 | IO_L39N_6 | IO_L39N_6 | P4 | I/O |
| 6 | IO_L39P_6 | IO_L39P_6 | IO_L39P_6 | IO_L39P_6 | IO_L39P_6 | P3 | I/O |
| 6 | IO_L40N_6 | IO_L40N_6 | IO_L40N_6 | IO_L40N_6 | IO_L40N_6 | P2 | I/O |
| 6 | IO_L40P_6/VREF_6 | IO_L40P_6/VREF_6 | IO_L40P_6/VREF_6 | IO_L40P_6/VREF_6 | IO_L40P_6/VREF_6 | P1 | VREF |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | P9 | VCCO |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | P10 | VCCO |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | R9 | VCCO |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | T3 | VCCO |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | T9 | VCCO |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | U8 | VCCO |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | V8 | VCCO |
| 6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | VCCO_6 | Y3 | VCCO |
| 7 | IO_L01N_7/VRP_7 | IO_L01N_7/VRP_7 | IO_L01N_7/VRP_7 | IO_L01N_7/VRP_7 | IO_L01N_7/VRP_7 | F5 | DCI |

*Table 107:* **FG900 Package Pinout *(Cont'd)***

| Bank | XC3S2000 Pin Name | XC3S4000, XC3S5000 Pin Name | FG900 Pin Number | Type |
|---|---|---|---|---|
| 2 | VCCO_2 | VCCO_2 | J28 | VCCO |
| 2 | VCCO_2 | VCCO_2 | N28 | VCCO |
| 3 | IO | IO | AB25 | I/O |
| 3 | IO_L01N_3/VRP_3 | IO_L01N_3/VRP_3 | AH30 | DCI |
| 3 | IO_L01P_3/VRN_3 | IO_L01P_3/VRN_3 | AH29 | DCI |
| 3 | IO_L02N_3/VREF_3 | IO_L02N_3/VREF_3 | AG28 | VREF |
| 3 | IO_L02P_3 | IO_L02P_3 | AG27 | I/O |
| 3 | IO_L03N_3 | IO_L03N_3 | AG30 | I/O |
| 3 | IO_L03P_3 | IO_L03P_3 | AG29 | I/O |
| 3 | IO_L04N_3 | IO_L04N_3 | AF30 | I/O |
| 3 | IO_L04P_3 | IO_L04P_3 | AF29 | I/O |
| 3 | IO_L05N_3 | IO_L05N_3 | AE26 | I/O |
| 3 | IO_L05P_3 | IO_L05P_3 | AF27 | I/O |
| 3 | IO_L06N_3 | IO_L06N_3 | AE29 | I/O |
| 3 | IO_L06P_3 | IO_L06P_3 | AE28 | I/O |
| 3 | IO_L07N_3 | IO_L07N_3 | AD28 | I/O |
| 3 | IO_L07P_3 | IO_L07P_3 | AD27 | I/O |
| 3 | IO_L08N_3 | IO_L08N_3 | AD30 | I/O |
| 3 | IO_L08P_3 | IO_L08P_3 | AD29 | I/O |
| 3 | IO_L09N_3 | IO_L09N_3 | AC24 | I/O |
| 3 | IO_L09P_3/VREF_3 | IO_L09P_3/VREF_3 | AD25 | VREF |
| 3 | IO_L10N_3 | IO_L10N_3 | AC26 | I/O |
| 3 | IO_L10P_3 | IO_L10P_3 | AC25 | I/O |
| 3 | IO_L11N_3 | IO_L11N_3 | AC28 | I/O |
| 3 | IO_L11P_3 | IO_L11P_3 | AC27 | I/O |
| 3 | IO_L13N_3/VREF_3 | IO_L13N_3/VREF_3 | AC30 | VREF |
| 3 | IO_L13P_3 | IO_L13P_3 | AC29 | I/O |
| 3 | IO_L14N_3 | IO_L14N_3 | AB27 | I/O |
| 3 | IO_L14P_3 | IO_L14P_3 | AB26 | I/O |
| 3 | IO_L15N_3 | IO_L15N_3 | AB30 | I/O |
| 3 | IO_L15P_3 | IO_L15P_3 | AB29 | I/O |
| 3 | IO_L16N_3 | IO_L16N_3 | AA22 | I/O |
| 3 | IO_L16P_3 | IO_L16P_3 | AB23 | I/O |
| 3 | IO_L17N_3 | IO_L17N_3 | AA25 | I/O |
| 3 | IO_L17P_3/VREF_3 | IO_L17P_3/VREF_3 | AA24 | VREF |
| 3 | IO_L19N_3 | IO_L19N_3 | AA29 | I/O |
| 3 | IO_L19P_3 | IO_L19P_3 | AA28 | I/O |
| 3 | IO_L20N_3 | IO_L20N_3 | Y21 | I/O |
| 3 | IO_L20P_3 | IO_L20P_3 | AA21 | I/O |
| 3 | IO_L21N_3 | IO_L21N_3 | Y24 | I/O |

*Table 107:* **FG900 Package Pinout *(Cont'd)***

| Bank | XC3S2000 Pin Name | XC3S4000, XC3S5000 Pin Name | FG900 Pin Number | Type |
|---|---|---|---|---|
| 4 | IO_L31P_4/DOUT/BUSY | IO_L31P_4/DOUT/BUSY | AH16 | DUAL |
| 4 | IO_L32N_4/GCLK1 | IO_L32N_4/GCLK1 | AJ16 | GCLK |
| 4 | IO_L32P_4/GCLK0 | IO_L32P_4/GCLK0 | AK16 | GCLK |
| 4 | N.C. (◆) | IO_L33N_4 | AH25 | I/O |
| 4 | N.C. (◆) | IO_L33P_4 | AJ25 | I/O |
| 4 | N.C. (◆) | IO_L34N_4 | AE25 | I/O |
| 4 | N.C. (◆) | IO_L34P_4 | AE24 | I/O |
| 4 | N.C. (◆) | IO_L35N_4 | AG24 | I/O |
| 4 | N.C. (◆) | IO_L35P_4 | AH24 | I/O |
| 4 | N.C. (◆) | IO_L38N_4 | AJ24 | I/O |
| 4 | N.C. (◆) | IO_L38P_4 | AK24 | I/O |
| 4 | VCCO_4 | VCCO_4 | Y17 | VCCO |
| 4 | VCCO_4 | VCCO_4 | Y18 | VCCO |
| 4 | VCCO_4 | VCCO_4 | AD18 | VCCO |
| 4 | VCCO_4 | VCCO_4 | AH18 | VCCO |
| 4 | VCCO_4 | VCCO_4 | Y19 | VCCO |
| 4 | VCCO_4 | VCCO_4 | AB20 | VCCO |
| 4 | VCCO_4 | VCCO_4 | AD22 | VCCO |
| 4 | VCCO_4 | VCCO_4 | AH22 | VCCO |
| 4 | VCCO_4 | VCCO_4 | AF24 | VCCO |
| 4 | VCCO_4 | VCCO_4 | AH26 | VCCO |
| 5 | IO | IO | AE6 | I/O |
| 5 | IO | IO | AB10 | I/O |
| 5 | IO | IO | AA11 | I/O |
| 5 | IO | IO | AA15 | I/O |
| 5 | IO | IO | AE15 | I/O |
| 5 | IO/VREF_5 | IO/VREF_5 | AH4 | VREF |
| 5 | IO/VREF_5 | IO/VREF_5 | AK15 | VREF |
| 5 | IO_L01N_5/RDWR_B | IO_L01N_5/RDWR_B | AK4 | DUAL |
| 5 | IO_L01P_5/CS_B | IO_L01P_5/CS_B | AJ4 | DUAL |
| 5 | IO_L02N_5 | IO_L02N_5 | AK5 | I/O |
| 5 | IO_L02P_5 | IO_L02P_5 | AJ5 | I/O |
| 5 | IO_L03N_5 | IO_L03N_5 | AF6 | I/O |
| 5 | IO_L03P_5 | IO_L03P_5 | AG5 | I/O |
| 5 | IO_L04N_5 | IO_L04N_5 | AJ6 | I/O |
| 5 | IO_L04P_5 | IO_L04P_5 | AH6 | I/O |
| 5 | IO_L05N_5 | IO_L05N_5 | AE7 | I/O |
| 5 | IO_L05P_5 | IO_L05P_5 | AD7 | I/O |
| 5 | IO_L06N_5 | IO_L06N_5 | AH7 | I/O |
| 5 | IO_L06P_5 | IO_L06P_5 | AG7 | I/O |

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| 2 | IO_L19N_2 | IO_L19N_2 | M29 | I/O |
| 2 | IO_L19P_2 | IO_L19P_2 | M30 | I/O |
| 2 | IO_L20N_2 | IO_L20N_2 | M31 | I/O |
| 2 | IO_L20P_2 | IO_L20P_2 | M32 | I/O |
| 2 | IO_L21N_2 | IO_L21N_2 | M26 | I/O |
| 2 | IO_L21P_2 | IO_L21P_2 | N25 | I/O |
| 2 | IO_L22N_2 | IO_L22N_2 | N27 | I/O |
| 2 | IO_L22P_2 | IO_L22P_2 | N28 | I/O |
| 2 | IO_L23N_2/VREF_2 | IO_L23N_2VREF_2 | N31 | VREF |
| 2 | IO_L23P_2 | IO_L23P_2 | N32 | I/O |
| 2 | IO_L24N_2 | IO_L24N_2 | N24 | I/O |
| 2 | IO_L24P_2 | IO_L24P_2 | P24 | I/O |
| 2 | IO_L26N_2 | IO_L26N_2 | P29 | I/O |
| 2 | IO_L26P_2 | IO_L26P_2 | P30 | I/O |
| 2 | IO_L27N_2 | IO_L27N_2 | P31 | I/O |
| 2 | IO_L27P_2 | IO_L27P_2 | P32 | I/O |
| 2 | IO_L28N_2 | IO_L28N_2 | P33 | I/O |
| 2 | IO_L28P_2 | IO_L28P_2 | P34 | I/O |
| 2 | IO_L29N_2 | IO_L29N_2 | R24 | I/O |
| 2 | IO_L29P_2 | IO_L29P_2 | R25 | I/O |
| 2 | IO_L30N_2 | IO_L30N_2 | R28 | I/O |
| 2 | IO_L30P_2 | IO_L30P_2 | R29 | I/O |
| 2 | IO_L31N_2 | IO_L31N_2 | R31 | I/O |
| 2 | IO_L31P_2 | IO_L31P_2 | R32 | I/O |
| 2 | IO_L32N_2 | IO_L32N_2 | R33 | I/O |
| 2 | IO_L32P_2 | IO_L32P_2 | R34 | I/O |
| 2 | IO_L33N_2 | IO_L33N_2 | R26 | I/O |
| 2 | IO_L33P_2 | IO_L33P_2 | T25 | I/O |
| 2 | IO_L34N_2/VREF_2 | IO_L34N_2/VREF_2 | T28 | VREF |
| 2 | IO_L34P_2 | IO_L34P_2 | T29 | I/O |
| 2 | IO_L35N_2 | IO_L35N_2 | T32 | I/O |
| 2 | IO_L35P_2 | IO_L35P_2 | T33 | I/O |
| 2 | IO_L37N_2 | IO_L37N_2 | U27 | I/O |
| 2 | IO_L37P_2 | IO_L37P_2 | U28 | I/O |
| 2 | IO_L38N_2 | IO_L38N_2 | U29 | I/O |
| 2 | IO_L38P_2 | IO_L38P_2 | U30 | I/O |
| 2 | IO_L39N_2 | IO_L39N_2 | U31 | I/O |
| 2 | IO_L39P_2 | IO_L39P_2 | U32 | I/O |
| 2 | IO_L40N_2 | IO_L40N_2 | U33 | I/O |
| 2 | IO_L40P_2/VREF_2 | IO_L40P_2/VREF_2 | U34 | VREF |

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| 7 | IO_L01P_7/VRN_7 | IO_L01P_7/VRN_7 | C2 | DCI |
| 7 | IO_L02N_7 | IO_L02N_7 | D1 | I/O |
| 7 | IO_L02P_7 | IO_L02P_7 | D2 | I/O |
| 7 | IO_L03N_7/VREF_7 | IO_L03N_7/VREF_7 | E2 | VREF |
| 7 | IO_L03P_7 | IO_L03P_7 | E3 | I/O |
| 7 | IO_L04N_7 | IO_L04N_7 | F3 | I/O |
| 7 | IO_L04P_7 | IO_L04P_7 | F4 | I/O |
| 7 | IO_L05N_7 | IO_L05N_7 | F1 | I/O |
| 7 | IO_L05P_7 | IO_L05P_7 | F2 | I/O |
| 7 | IO_L06N_7 | IO_L06N_7 | G5 | I/O |
| 7 | IO_L06P_7 | IO_L06P_7 | G6 | I/O |
| 7 | IO_L07N_7 | IO_L07N_7 | H5 | I/O |
| 7 | IO_L07P_7 | IO_L07P_7 | H6 | I/O |
| 7 | IO_L08N_7 | IO_L08N_7 | H1 | I/O |
| 7 | IO_L08P_7 | IO_L08P_7 | H2 | I/O |
| 7 | IO_L09N_7 | IO_L09N_7 | J6 | I/O |
| 7 | IO_L09P_7 | IO_L09P_7 | J7 | I/O |
| 7 | IO_L10N_7 | IO_L10N_7 | J4 | I/O |
| 7 | IO_L10P_7/VREF_7 | IO_L10P_7/VREF_7 | H4 | VREF |
| 7 | IO_L11N_7 | IO_L11N_7 | J2 | I/O |
| 7 | IO_L11P_7 | IO_L11P_7 | J3 | I/O |
| 7 | IO_L12N_7 | IO_L12N_7 | K9 | I/O |
| 7 | IO_L12P_7 | IO_L12P_7 | J8 | I/O |
| 7 | IO_L13N_7 | IO_L13N_7 | K7 | I/O |
| 7 | IO_L13P_7 | IO_L13P_7 | K8 | I/O |
| 7 | IO_L14N_7 | IO_L14N_7 | K5 | I/O |
| 7 | IO_L14P_7 | IO_L14P_7 | K6 | I/O |
| 7 | IO_L15N_7 | IO_L15N_7 | K3 | I/O |
| 7 | IO_L15P_7 | IO_L15P_7 | K4 | I/O |
| 7 | IO_L16N_7 | IO_L16N_7 | K1 | I/O |
| 7 | IO_L16P_7/VREF_7 | IO_L16P_7/VREF_7 | K2 | VREF |
| 7 | IO_L17N_7 | IO_L17N_7 | L9 | I/O |
| 7 | IO_L17P_7 | IO_L17P_7 | L10 | I/O |
| 7 | IO_L19N_7/VREF_7 | IO_L19N_7/VREF_7 | L1 | VREF |
| 7 | IO_L19P_7 | IO_L19P_7 | L2 | I/O |
| 7 | IO_L20N_7 | IO_L20N_7 | M10 | I/O |
| 7 | IO_L20P_7 | IO_L20P_7 | M11 | I/O |
| 7 | IO_L21N_7 | IO_L21N_7 | M7 | I/O |
| 7 | IO_L21P_7 | IO_L21P_7 | M8 | I/O |
| 7 | IO_L22N_7 | IO_L22N_7 | M5 | I/O |