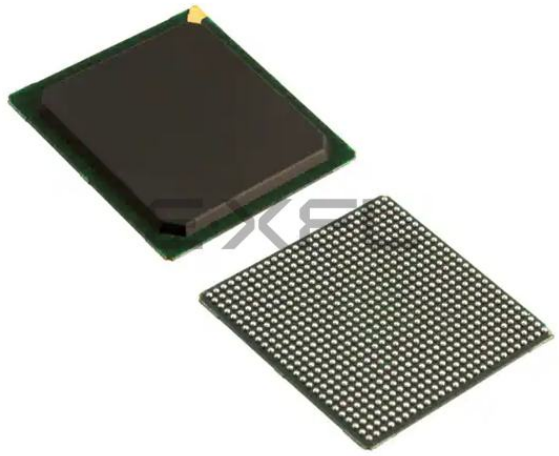
AMD Xilinx - XC3S1000-4FGG676I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1920
Number of Logic Elements/Cells	17280
Total RAM Bits	442368
Number of I/O	391
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1000-4fgg676i

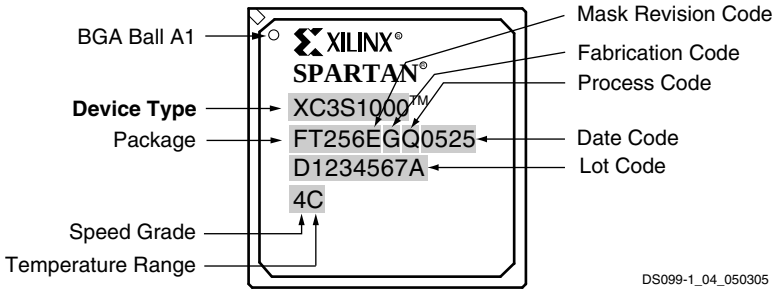


Figure 3: **Spartan-3 FPGA BGA Package Marking Example for Part Number XC3S1000-4FT256C**

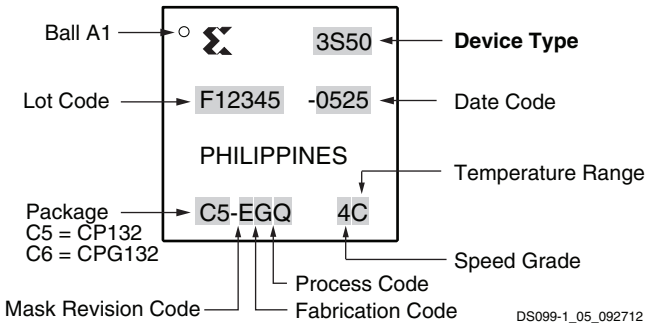


Figure 4: **Spartan-3 FPGA CP132 and CPG132 Package Marking Example for XC3S50-4CP132C**

Ordering Information

Spartan-3 FPGAs are available in both standard (Figure 5) and Pb-free (Figure 6) packaging options for all device/package combinations. The Pb-free packages include a special 'G' character in the ordering code.

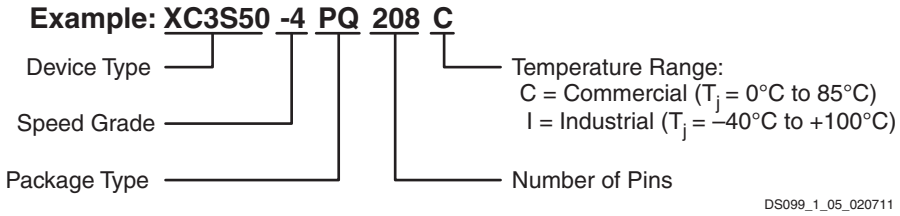


Figure 5: **Standard Packaging**

For additional information on Pb-free packaging, see XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

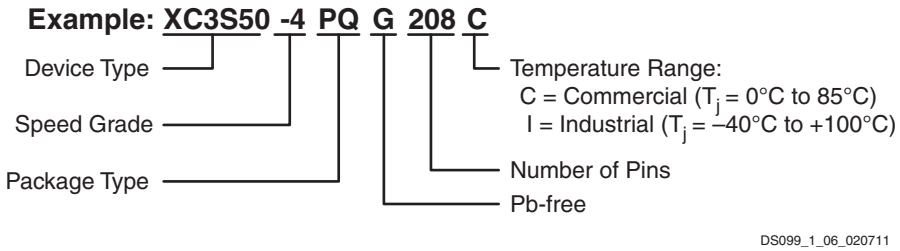


Figure 6: **Pb-Free Packaging**

ESD Protection

Clamp diodes protect all device pads against damage from Electro-Static Discharge (ESD) as well as excessive voltage transients. Each I/O has two clamp diodes: One diode extends P-to-N from the pad to V_{CCO} and a second diode extends N-to-P from the pad to GND. During operation, these diodes are normally biased in the off state. These clamp diodes are always connected to the pad, regardless of the signal standard selected. The presence of diodes limits the ability of Spartan-3 FPGA I/Os to tolerate high signal voltages. The V_{IN} absolute maximum rating in Table 28, page 58 specifies the voltage range that I/Os can tolerate.

Slew Rate Control and Drive Strength

Two options, FAST and SLOW, control the output slew rate. The FAST option supports output switching at a high rate. The SLOW option reduces bus transients. These options are only available when using one of the LVCMOS or LVTTL standards, which also provide up to seven different levels of current drive strength: 2, 4, 6, 8, 12, 16, and 24 mA. Choosing the appropriate drive strength level is yet another means to minimize bus transients.

Table 7 shows the drive strengths that the LVCMOS and LVTTL standards support.

Table 7: **Programmable Output Drive Current**

Signal Standard (IOSTANDARD)	Current Drive (mA)						
	2	4	6	8	12	16	24
LVTTL	✓	✓	✓	✓	✓	✓	✓
LVCMOS33	✓	✓	✓	✓	✓	✓	✓
LVCMOS25	✓	✓	✓	✓	✓	✓	✓
LVCMOS18	✓	✓	✓	✓	✓	✓	–
LVCMOS15	✓	✓	✓	✓	✓	–	–
LVCMOS12	✓	✓	✓	–	–	–	–

Boundary-Scan Capability

All Spartan-3 FPGA IOBs support boundary-scan testing compatible with IEEE 1149.1 standards. During boundary- scan operations such as EXTEST and HIGHZ the I/O pull-down resistor is active. For more information, see Boundary-Scan (JTAG) Mode, page 50, and refer to the “Using Boundary-Scan and BSDL Files” chapter in UG331.

SelectIO Interface Signal Standards

The IOBs support 18 different single-ended signal standards, as listed in Table 8. Furthermore, the majority of IOBs can be used in specific pairs supporting any of eight differential signal standards, as shown in Table 9.

To define the SelectIO™ interface signaling standard in a design, set the IOSTANDARD attribute to the appropriate setting. Xilinx provides a variety of different methods for applying the IOSTANDARD for maximum flexibility. For a full description of different methods of applying attributes to control IOSTANDARD, refer to the “Using I/O Resources” chapter in UG331.

Together with placing the appropriate I/O symbol, two externally applied voltage levels, V_{CCO} and V_{REF}, select the desired signal standard. The V_{CCO} lines provide current to the output driver. The voltage on these lines determines the output voltage swing for all standards except GTL and GTLP.

All single-ended standards except the LVCMOS, LVTTL, and PCI varieties require a Reference Voltage (V_{REF}) to bias the input-switching threshold. Once a configuration data file is loaded into the FPGA that calls for the I/Os of a given bank to use such a signal standard, a few specifically reserved I/O pins on the same bank automatically convert to V_{REF} inputs. When using one of the LVCMOS standards, these pins remain I/Os because the V_{CCO} voltage biases the input-switching threshold, so there is no need for V_{REF}. Select the V_{CCO} and V_{REF} levels to suit the desired single-ended standard according to Table 8.

The DCI feature operates independently for each of the device's eight banks. Each bank has an 'N' reference pin (VRN) and a 'P' reference pin, (VRP), to calibrate driver and termination resistance. Only when using a DCI standard on a given bank do these two pins function as VRN and VRP. When not using a DCI standard, the two pins function as user I/Os. As shown in Figure 9, add an external reference resistor to pull the VRN pin up to V_{CCO} and another reference resistor to pull the VRP pin down to GND. Also see Figure 42, page 116. Both resistors have the same value—commonly 50Ω—with one-percent tolerance, which is either the characteristic impedance of the line or twice that, depending on the DCI standard in use. Standards having a symbol name that contains the letters "DV2" use a reference resistor value that is twice the line impedance. DCI adjusts the output driver impedance to match the reference resistors' value or half that, according to the standard. DCI always adjusts the on-chip termination resistors to directly match the reference resistors' value.

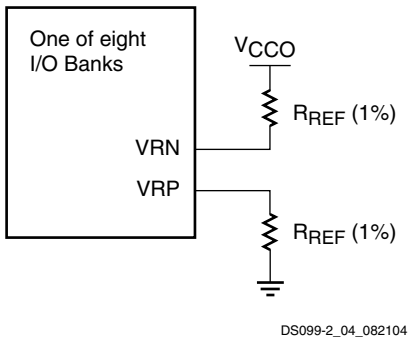


Figure 9: **Connection of Reference Resistors (R_{REF})**

The rules guiding the use of DCI standards on banks are as follows:

- No more than one DCI I/O standard with a Single Termination is allowed per bank.
- No more than one DCI I/O standard with a Split Termination is allowed per bank.
- Single Termination, Split Termination, Controlled- Impedance Driver, and Controlled-Impedance Driver with Half Impedance can co-exist in the same bank.

See also The Organization of IOBs into Banks, immediately below, and DCI: User I/O or Digitally Controlled Impedance Resistor Reference Input, page 115.

The Organization of IOBs into Banks

IOBs are allocated among eight banks, so that each side of the device has two banks, as shown in Figure 10. For all packages, each bank has independent V_{REF} lines. For example, V_{REF} Bank 3 lines are separate from the V_{REF} lines going to all other banks.

For the Very Thin Quad Flat Pack (VQ), Plastic Quad Flat Pack (PQ), Fine Pitch Thin Ball Grid Array (FT), and Fine Pitch Ball Grid Array (FG) packages, each bank has dedicated V_{CCO} lines. For example, the V_{CCO} Bank 7 lines are separate from the V_{CCO} lines going to all other banks. Thus, Spartan-3 devices in these packages support eight independent V_{CCO} supplies.

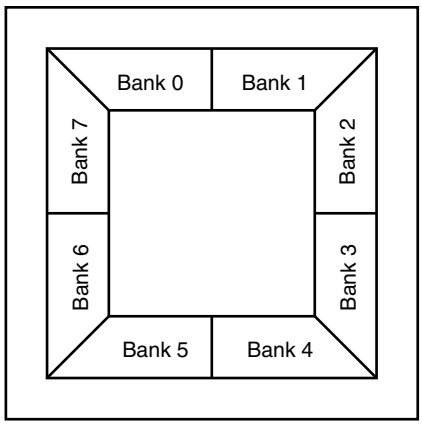
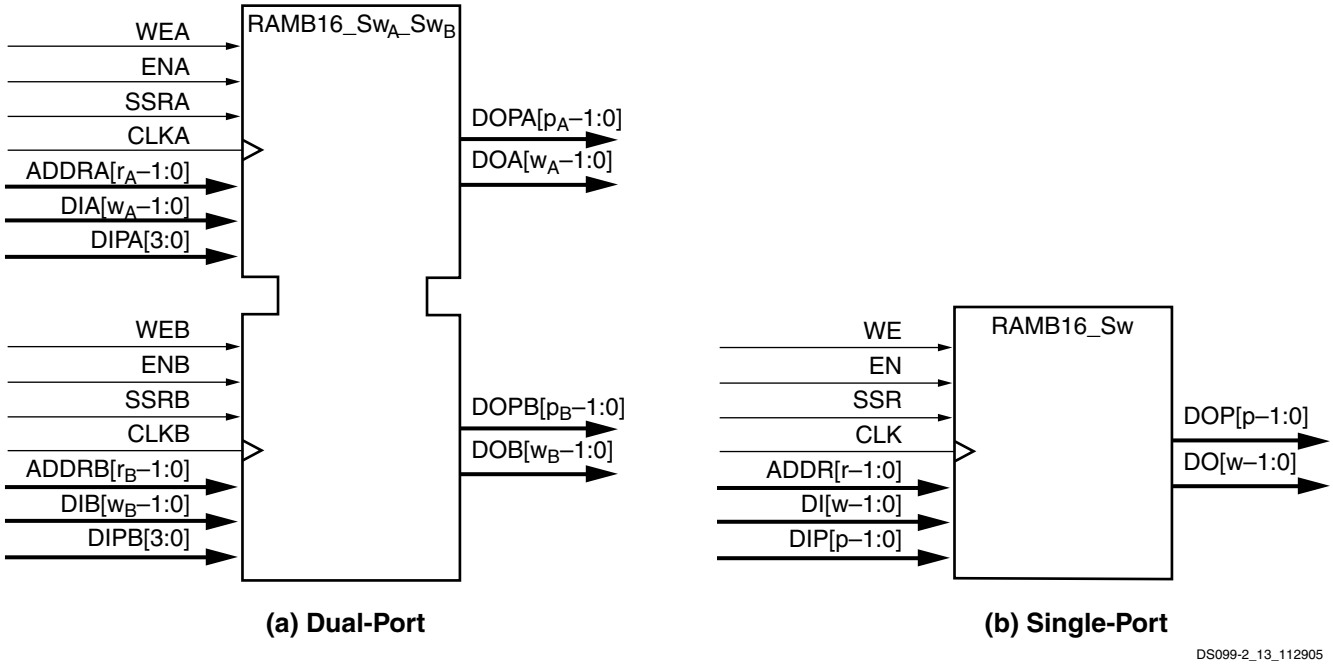


Figure 10: **Spartan-3 FPGA I/O Banks (Top View)**



Notes:

1. w_A and w_B are integers representing the total data path width (i.e., data bits plus parity bits) at ports A and B, respectively.
2. p_A and p_B are integers that indicate the number of data path lines serving as parity bits.
3. r_A and r_B are integers representing the address bus width at ports A and B, respectively.
4. The control signals CLK, WE, EN, and SSR on both ports have the option of inverted polarity.

Figure 14: **Block RAM Primitives**

Table 13: **Block RAM Port Signals**

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Address Bus	ADDRA	ADDRB	Input	The Address Bus selects a memory location for read or write operations. The width (w) of the port's associated data path determines the number of available address lines (r). Whenever a port is enabled (ENA or ENB = High), address transitions must meet the data sheet setup and hold times with respect to the port clock (CLKA or CLKB). This requirement must be met, even if the RAM read output is of no interest.
Data Input Bus	DIA	DIB	Input	Data at the DI input bus is written to the addressed memory location addressed on an enabled active CLK edge. It is possible to configure a port's total data path width (w) to be 1, 2, 4, 9, 18, or 36 bits. This selection applies to both the DI and DO paths of a given port. Each port is independent. For a port assigned a width (w), the number of addressable locations is 16,384/(w-p) where "p" is the number of parity bits. Each memory location has a width of "w" (including parity bits). See the DIP signal description for more information of parity.
Parity Data Input(s)	DIPA	DIPB	Input	Parity inputs represent additional bits included in the data input path to support error detection. The number of parity bits "p" included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 14.

Table 22: **Status Logic Signals**

Signal	Direction	Description
RST	Input	A High resets the entire DCM to its initial power-on state. Initializes the DLL taps for a delay of zero. Sets the LOCKED output Low. This input is asynchronous.
STATUS[7:0]	Output	The bit values on the STATUS bus provide information regarding the state of DLL and PS operation
LOCKED	Output	Indicates that the CLKIN and CLKFB signals are in phase by going High. The two signals are out-of-phase when Low.

Table 23: **DCM STATUS Bus**

Bit	Name	Description
0	Phase Shift Overflow	A value of 1 indicates a phase shift overflow when one of two conditions occurs: Incrementing (or decrementing) TPS beyond 255/256 of a CLKIN cycle. The DLL is producing its maximum possible phase shift (i.e., all delay taps are active).(1)
1	CLKIN Input Stopped Toggling	A value of 1 indicates that the CLKIN input signal is not toggling. A value of 0 indicates toggling. This bit functions only when the CLKFB input is connected.(2)
2	CLKFX/CLKFX180 Output Stopped Toggling	A value of 1 indicates that the CLKFX or CLKFX180 output signals are not toggling. A value of 0 indicates toggling. This bit functions only when using the Digital Frequency Synthesizer (DFS).
3:7	Reserved	–

Notes:

1. The DLL phase shift with all delay taps active is specified as the parameter FINE_SHIFT_RANGE.
2. If only the DFS clock outputs are used, but none of the DLL clock outputs, this bit will not go High when the CLKIN signal stops.

Table 24: **Status Attributes**

Attribute	Description	Values
STARTUP_WAIT	Delays transition from configuration to user mode until lock condition is achieved.	TRUE, FALSE

Stabilizing DCM Clocks Before User Mode

It is possible to delay the completion of device configuration until after the DLL has achieved a lock condition using the STARTUP_WAIT attribute described in Table 24. This option ensures that the FPGA does not enter user mode—i.e., begin functional operation—until all system clocks generated by the DCM are stable. In order to achieve the delay, it is necessary to set the attribute to TRUE as well as set the BitGen option LCK_cycle to one of the six cycles making up the Startup phase of configuration. The selected cycle defines the point at which configuration will halt until the LOCKED output goes High.

Global Clock Network

Spartan-3 devices have eight Global Clock inputs called GCLK0 - GCLK7. These inputs provide access to a low-capacitance, low-skew network that is well-suited to carrying high-frequency signals. The Spartan-3 FPGAs clock network is shown in Figure 23. GCLK0 through GCLK3 are located in the center of the bottom edge. GCLK4 through GCLK7 are located in the center of the top edge.

Eight Global Clock Multiplexers (also called BUFGMUX elements) are provided that accept signals from Global Clock inputs and route them to the internal clock network as well as DCMs. Four BUFGMUX elements are located in the center of the bottom edge, just above the GCLK0 - GCLK3 inputs. The remaining four BUFGMUX elements are located in the center of the top edge, just below the GCLK4 - GCLK7 inputs.

Pairs of BUFGMUX elements share global inputs, as shown in Figure 24. For example, the GCLK4 and GCLK5 inputs both potentially connect to BUFGMUX4 and BUFGMUX5 located in the upper right center. A differential clock input uses a pair of GCLK inputs to connect to a single BUFGMUX element.

Revision History

Date	Version No.	Description
04/11/03	1.0	Initial Xilinx release
05/19/03	1.1	Added Block RAM column, DCMs, and multipliers to XC3S50 descriptions.
07/11/03	1.2	Explained the configuration port *Persist* option in Slave Parallel Mode (SelectMAP) section. Updated Figure 8 and Double-Data-Rate Transmission section to indicate that DDR clocking for the XC3S50 is the same as that for all other Spartan-3 devices. Updated description of I/O voltage tolerance in ESD Protection section. In Table 10, changed input termination type for DCI version of the LVCMOS standard to *None*. Added additional flexibility for making DLL connections in Figure 21 and accompanying text. In the Configuration section, inserted an explanation of how to choose power supplies for the configuration interface, including guidelines for achieving 3.3V-tolerance.
08/24/04	1.3	Showed inversion of 3-state signal (Figure 7). Clarified description of pull-up and pull-down resistors (Table 6 and page 13). Added information on operating block RAM with multipliers to page 26. Corrected output buffer name in Figure 21. Corrected description of how DOUT is synchronized to CCLK (page 47).
08/19/05	1.4	Corrected description of WRITE_FIRST and READ_FIRST in Table 13. Added note regarding address setup and hold time requirements whenever a block RAM port is enabled (Table 13). Added information in the maximum length of a Configuration daisy-chain. Added reference to XAPP453 in 3.3V-Tolerant Configuration Interface section. Added information on the STATUS[2] DCM output (Table 23). Added information on CCLK behavior and termination recommendations to Configuration. Added Additional Configuration Details section. Added Powering Spartan-3 FPGAs section. Removed GSR from Figure 31 because its timing is not programmable.
04/03/06	2.0	Updated Figure 7. Updated Figure 14. Updated Table 10. Updated Figure 22. Corrected Platform Flash supply voltage name and value in Figure 26 and Figure 28. Added No Internal Charge Pumps or Free-Running Oscillators. Corrected a few minor typographical errors.
04/26/06	2.1	Added more information on the pull-up resistors that are active during configuration to Configuration. Added information to Boundary-Scan (JTAG) Mode about potential interactions when configuring via JTAG if the mode select pins are set for other than JTAG.
05/25/07	2.2	Added Spartan-3 FPGA Design Documentation. Noted SSTL2_I_DCI 25-Ohm driver in Table 10 and Table 11. Added note that pull-down is active during boundary scan tests.
11/30/07	2.3	Updated links to documentation on xilinx.com.
06/25/08	2.4	Added HSLVDCI to Table 10. Updated formatting and links.
12/04/09	2.5	Updated HSLVDCI description in Digitally Controlled Impedance (DCI). Updated the low-voltage differential signaling V_{CCO} values in Table 10. Noted that the CP132 package is being discontinued in The Organization of IOBs into Banks. Updated rule 4 in Rules Concerning Banks. Added software version requirement in The Fixed Phase Mode.
10/29/12	3.0	Added Notice of Disclaimer. Per XCN07022, updated the discontinued FG1156 and FGG1156 package discussion throughout document. Per XCN08011, updated the discontinued CP132 and CPG132 package discussion throughout document. This product is not recommended for new designs.

Switching Characteristics

All Spartan-3 devices are available in two speed grades: –4 and the higher performance –5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reported delays may still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Production-quality systems must use FPGA designs compiled using a Production status speed file. FPGAs designs using a less mature speed file designation may only be used during system prototyping or preproduction qualification. FPGA designs using Advance or Preliminary status speed files should never be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

Xilinx ISE Software Updates: http://www.xilinx.com/support/download/index.htm

All specified limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the following applies: Parameter values apply to all Spartan-3 devices. All parameters representing voltages are measured with respect to GND.

Selected timing parameters and their representative values are included below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3 FPGA v1.38 speed files are the original source for many but not all of the values. The v1.38 speed files are available in Xilinx Integrated Software Environment (ISE) software version 8.2i.

The speed grade designations for these files are shown in Table 39. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 39: **Spartan-3 FPGA Speed Grade Designations (ISE v8.2i or Later)**

Device	Advance	Preliminary	Production
XC3S50			-4, -5 (v1.37 and later)
XC3S200			
XC3S400			
XC3S1000			
XC3S1500			
XC3S2000			
XC3S4000			
XC3S5000			-4, -5 (v1.38 and later)

Simultaneously Switching Output Guidelines

This section provides guidelines for the maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins, of a given output signal standard, that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 49 and Table 50 provide the essential SSO guidelines. For each device/package combination, Table 49 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and will possibly not match the physical number of pairs. For each output signal standard and drive strength, Table 50 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The Table 50 guidelines are categorized by package style. Multiply the appropriate numbers from Table 49 and Table 50 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines may result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 49 x Table 50

The recommended maximum SSO values assume that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The number of SSOs allowed for quad-flat packages (VQ, TQ, PQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 49: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	VQ100	CP132 (1)(2)	TQ144 (1)	PQ208	FT256	FG320	FG456	FG676	FG900	FG1156 (2)
XC3S50	1	1.5	1.5	2	–	–	–	–	–	–
XC3S200	1	–	1.5	2	3	–	–	–	–	–
XC3S400	–	–	1.5	2	3	3	5	–	–	–
XC3S1000	–	–	–	–	3	3	5	5	–	–
XC3S1500	–	–	–	–	–	3	5	6	–	–
XC3S2000	–	–	–	–	–	–	5	6	9	–
XC3S4000	–	–	–	–	–	–	–	6	10	12
XC3S5000	–	–	–	–	–	–	–	6	10	12

Notes:

1. The V_{CCO} lines for the pair of banks on each side of the CP132 and TQ144 packages are internally tied together. Each pair of interconnected banks shares three V_{CCO}/GND pairs. Consequently, the per bank number is 1.5.
2. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.
3. The information in this table also applies to Pb-free packages.

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair**

Signal Standard (IOSTANDARD)			Package				
			VQ100	TQ144	PQ208	CP132	FT256, FG320, FG456, FG676, FG900, FG1156
Single-Ended Standards							
GTL			0	0	0	1	14
GTL_DCI			0	0	0	1	14
GTLP			0	0	0	1	19
GTLP_DCI			0	0	0	1	19
HSLVDCI_15			6	6	6	6	14
HSLVDCI_18			7	7	7	7	10
HSLVDCI_25			7	7	7	7	11
HSLVDCI_33			10	10	10	10	10
HSTL_I			11	11	11	11	17
HSTL_I_DCI			11	11	11	11	17
HSTL_III			7	7	7	7	7
HSTL_III_DCI			7	7	7	7	7
HSTL_I_18			13	13	13	13	17
HSTL_I_DCI_18			13	13	13	13	17
HSTL_II_18			9	9	9	9	9
HSTL_II_DCI_18			9	9	9	9	9
HSTL_III_18			8	8	8	8	8
HSTL_III_DCI_18			8	8	8	8	8
LVCMOS12	Slow	2	17	17	17	17	55
		4	13	13	13	13	32
		6	10	10	10	10	18
	Fast	2	12	12	12	12	31
		4	11	11	11	11	13
		6	9	9	9	9	9
LVCMOS15	Slow	2	16	12	12	19	55
		4	8	7	7	9	31
		6	7	7	7	9	18
		8	6	6	6	6	15
		12	5	5	5	5	10
	Fast	2	10	10	10	13	25
		4	6	7	7	7	16
		6	7	7	7	7	13
		8	6	6	6	6	11
		12	6	6	6	6	7

Table 56: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{BCKO}	When reading from the Block RAM, the time from the active transition at the CLK input to data appearing at the DOUT output	–	2.09	–	2.40	ns
Setup Times						
T_{BDCK}	Time from the setup of data at the DIN inputs to the active transition at the CLK input of the Block RAM	0.43	–	0.49	–	ns
Hold Times						
T_{BCKD}	Time from the active transition at the Block RAM's CLK input to the point where data is last held at the DIN inputs	0	–	0	–	ns
Clock Timing						
T_{BPWH}	Block RAM CLK signal High pulse width	1.19	∞	1.37	∞	ns
T_{BPWL}	Block RAM CLK signal Low pulse width	1.19	∞	1.37	∞	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. For minimums, use the values reported by the Xilinx timing analyzer.

Clock Distribution Switching Characteristics

Table 57: **Clock Distribution Switching Characteristics**

Description	Symbol	Maximum		Units
		Speed Grade		
		-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I-input to O-output delay	T_{GIO}	0.36	0.41	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0- and I1-inputs. Same as BUFGCE enable CE-input	T_{GSI}	0.53	0.60	ns

Notes:

1. For minimums, use the values reported by the Xilinx timing analyzer.

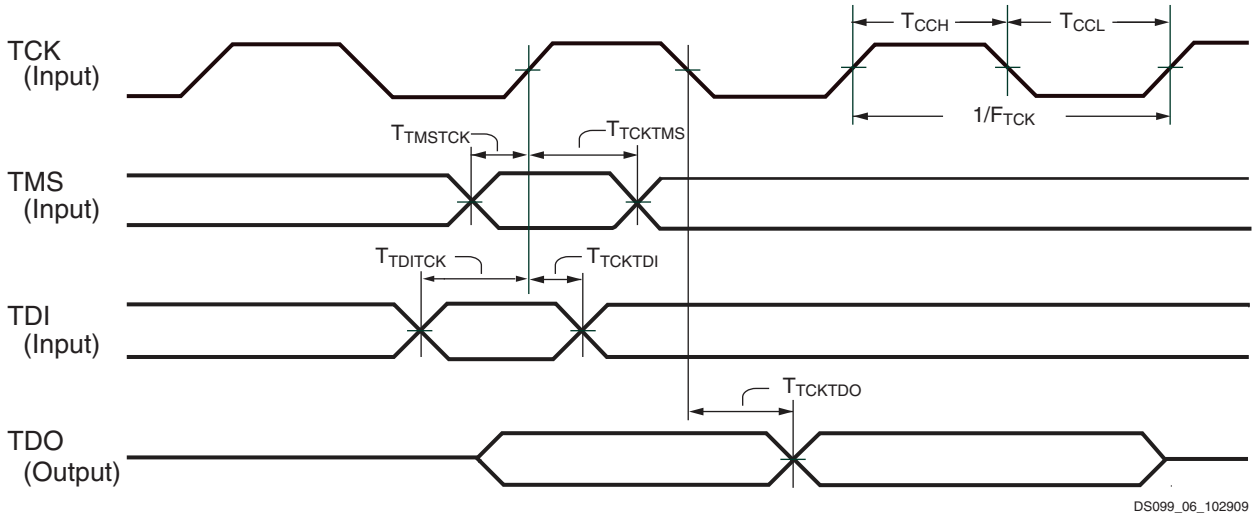


Figure 39: **JTAG Waveforms**

Table 68: **Timing for the JTAG Test Access Port**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin		1.0	11.0	ns
Setup Times					
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin		7.0	–	ns
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin		7.0	–	ns
Hold Times					
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin		0	–	ns
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin		0	–	ns
Clock Timing					
T_{TCKH}	TCK pin High pulse width		5	∞	ns
T_{TCKL}	TCK pin Low pulse width		5	∞	ns
F_{TCK}	Frequency of the TCK signal	JTAG Configuration	0	33	MHz
		Boundary-Scan	0	25	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.

Revision History

Date	Version	Description
04/11/03	1.0	Initial Xilinx release.
07/11/03	1.1	Extended Absolute Maximum Rating for junction temperature in Table 28. Added numbers for typical quiescent supply current (Table 34) and DLL timing.
02/06/04	1.2	Revised V_{IN} maximum rating (Table 28). Added power-on requirements (Table 30), leakage current number (Table 33), and differential output voltage levels (Table 38) for Rev. 0. Published new quiescent current numbers (Table 34). Updated pull-up and pull-down resistor strengths (Table 33). Added LVDCI_DV2 and LVPECL standards (Table 37 and Table 38). Changed CCLK setup time (Table 66 and Table 67).
03/04/04	1.3	Added timing numbers from v1.29 speed files as well as DCM timing (Table 58 through Table 63).
08/24/04	1.4	Added reference to errata documents on page 49. Clarified Absolute Maximum Ratings and added ESD information (Table 28). Explained V_{CCO} ramp time measurement (Table 30). Clarified I_L specification (Table 33). Updated quiescent current numbers and added information on power-on and surplus current (Table 34). Adjusted V_{REF} range for HSTL_III and HSTL_I_18 and changed V_{IH} min for LVCMOS12 (Table 35). Added note limiting V_{TT} range for SSTL2_II signal standards (Table 36). Calculated V_{OH} and V_{OL} levels for differential standards (Table 38). Updated Switching Characteristics with speed file v1.32 (Table 40 through Table 48 and Table 51 through Table 56). Corrected IOB test conditions (Table 41). Updated DCM timing with latest characterization data (Table 58 through Table 62). Improved DCM CLKIN pulse width specification (Table 58). Recommended use of Virtex-II FPGA Jitter calculator (Table 61). Improved DCM PSCLK pulse width specification (Table 62). Changed Phase Shifter lock time parameter (Table 63). Because the BitGen option Centered_x#_y# is not necessary for Variable Phase Shift mode, removed BitGen command table and referring text. Adjusted maximum CCLK frequency for the slave serial and parallel configuration modes (Table 66). Inverted CCLK waveform (Figure 37). Adjusted JTAG setup times (Table 68).
12/17/04	1.5	Updated timing parameters to match v1.35 speed file. Improved V_{CCO} ramp time specification (Table 30). Added a note limiting the rate of change of V_{CCAUX} (Table 32). Added typical quiescent current values for the XC3S2000, XC3S4000, and XC3S5000 (Table 34). Increased I_{OH} and I_{OL} for SSTL2-I and SSTL2-II standards (Table 36). Added SSO guidelines for the VQ, TQ, and PQ packages as well as edited SSO guidelines for the FT and FG packages (Table 50). Added maximum CCLK frequencies for configuration using compressed bitstreams (Table 66 and Table 67). Added specifications for the HSLVDCI standards (Table 35, Table 36, Table 44, Table 47, Table 48, and Table 50).
08/19/05	1.6	Updated timing parameters to match v1.37 speed file. All Spartan-3 FPGA part types, except XC3S5000, promoted to Production status. Removed V_{CCO} ramp rate restriction from all mask revision 'E' and later devices (Table 30). Added equivalent resistance values for internal pull-up and pull-down resistors (Table 33). Added worst-case quiescent current values for XC3S2000, XC3S4000, XC3S5000 (Table 34). Added industrial temperature range specification and improved typical quiescent current values (Table 34). Improved the DLL minimum clock input frequency specification from 24 MHz down to 18 MHz (Table 58). Improved the DFS minimum and maximum clock output frequency specifications (Table 60, Table 61). Added new miscellaneous DCM specifications (Table 64), primarily affecting Industrial temperature range applications. Updated Simultaneously Switching Output Guidelines and Table 50 for QFP packages. Added information on SSTL18_II I/O standard and timing to support DDR2 SDRAM interfaces. Added differential (or complementary single-ended) DIFF_HSTL_II_18 and DIFF_SSTL2_II I/O standards, including DCI terminated versions. Added electro-static discharge (ESD) data for the XC3S2000 and larger FPGAs (Table 28). Added link to Spartan-3 FPGA errata notices and how to receive automatic notifications of data sheet or errata changes.
04/03/06	2.0	Upgraded Module 3, removing Preliminary status. Moved XC3S5000 to Production status in Table 39. Finalized I/O timing on XC3S5000 for v1.38 speed files. Added minimum timing values for various logic and I/O paths. Corrected labels for R_{PU} and R_{PD} and updated R_{PD} conditions for in Table 33. Added final mask revision 'E' specifications for LVDS_25, RSDS_25, LVDSEXT_25 differential outputs to Table 38. Added BLVDS termination requirements to Figure 34. Improved recommended Simultaneous Switching Outputs (SSOs) limits in Table 50 for quad-flat packaged based on silicon testing using devices soldered on a printed circuit board. Updated Note 2 in Table 63. Updated Note 6 in Table 30. Added INIT_B minimum pulse width specification, T_{INIT}, to Table 65.
04/26/06	2.1	Updated document links.

Table 71: **Dual-Purpose Pins Used in Master or Slave Serial Mode**

Pin Name	Direction	Description
DIN	Input	**Serial Data Input:** During the Master or Slave Serial configuration modes, DIN is the serial configuration data input, and all data is synchronized to the rising CCLK edge. After configuration, this pin is available as a user I/O. This signal is located in Bank 4 and its output voltage determined by VCCO_4. The BitGen option ***Persist*** permits this pin to retain its configuration function in the User mode.
DOUT	Output	**Serial Data Output:** In a multi-FPGA design where all the FPGAs use serial mode, connect the DOUT output of one FPGA—in either Master or Slave Serial mode—to the DIN input of the next FPGA—in Slave Serial mode—so that configuration data passes from one to the next, in daisy-chain fashion. This "daisy chain" permits sequential configuration of multiple FPGAs. This signal is located in Bank 4 and its output voltage determined by VCCO_4. The BitGen option ***Persist*** permits this pin to retain its configuration function in the User mode.
INIT_B	Bidirectional (open-drain)	**Initializing Configuration Memory/Configuration Error:** Just after power is applied, the FPGA produces a Low-to-High transition on this pin indicating that initialization (*i.e.*, clearing) of the configuration memory has finished. Before entering the User mode, this pin functions as an open-drain output, which requires a pull-up resistor in order to produce a High logic level. In a multi-FPGA design, tie (wire AND) the INIT_B pins from all FPGAs together so that the common node transitions High only after all of the FPGAs have been successfully initialized. Externally holding this pin Low beyond the initialization phase delays the start of configuration. This action stalls the FPGA at the configuration step just before the mode select pins are sampled. During configuration, the FPGA indicates the occurrence of a data (i.e., CRC) error by asserting INIT_B Low. This signal is located in Bank 4 and its output voltage determined by VCCO_4. The BitGen option ***Persist*** permits this pin to retain its configuration function in the User mode.

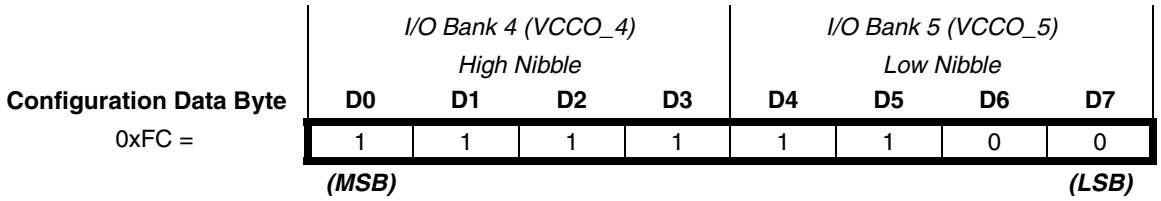


Figure 41: **Configuration Data Byte Mapping to D0-D7 Bits**

Parallel Configuration Modes (SelectMAP)

This section describes the dual-purpose configuration pins used during the Master and Slave Parallel configuration modes, sometimes also called the SelectMAP modes. In both Master and Slave Parallel configuration modes, D0-D7 form the byte-wide configuration data input. See Table 75 for Mode Select pin settings required for Parallel modes.

As shown in Figure 41, D0 is the most-significant bit while D7 is the least-significant bit. Bits D0-D3 form the high nibble of the byte and bits D4-D7 form the low nibble.

In the Parallel configuration modes, both the VCCO_4 and VCCO_5 voltage supplies are required and must both equal the voltage of the attached configuration device, typically either 2.5V or 3.3V.

Assert Low both the chip-select pin, CS_B, and the read/write control pin, RDWR_B, to write the configuration data byte presented on the D0-D7 pins to the FPGA on a rising-edge of the configuration clock, CCLK. The order of CS_B and RDWR_B does not matter, although RDWR_B must be asserted throughout the configuration process. If RDWR_B is de-asserted during configuration, the FPGA aborts the configuration operation.

After configuration, these pins are available as general-purpose user I/O. However, the SelectMAP configuration interface is optionally available for debugging and dynamic reconfiguration. To use these SelectMAP pins after configuration, set the Persist bitstream generation option.

The Readback debugging option, for example, requires the Persist bitstream generation option. During Readback mode, assert CS_B Low, along with RDWR_B High, to read a configuration data byte from the FPGA to the D0-D7 bus on a rising CCLK edge. During Readback mode, D0-D7 are output pins.

In all the cases, the configuration data and control signals are synchronized to the rising edge of the CCLK clock signal.

Package Overview

Table 81 shows the 10 low-cost, space-saving production package styles for the Spartan-3 family. Each package style is available as a standard and an environmentally-friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "VQ100" package becomes "VQG100" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 83.

Not all Spartan-3 device densities are available in all packages. However, for a specific package there is a common footprint that supports the various devices available in that package. See the footprint diagrams that follow.

Table 81: **Spartan-3 Family Package Options**

Package	Leads	Type	Maximum I/O	Pitch (mm)	Footprint (mm)	Height (mm)
VQ100 / VQG100	100	Very-thin Quad Flat Pack	63	0.5	16 x 16	1.20
CP132 / CPG132(1)	132	Chip-Scale Package	89	0.5	8 x 8	1.10
TQ144 / TQG144	144	Thin Quad Flat Pack	97	0.5	22 x 22	1.60
PQ208 / PQG208	208	Quad Flat Pack	141	0.5	30.6 x 30.6	4.10
FT256 / FTG256	256	Fine-pitch, Thin Ball Grid Array	173	1.0	17 x 17	1.55
FG320 / FGG320	320	Fine-pitch Ball Grid Array	221	1.0	19 x 19	2.00
FG456 / FGG456	456	Fine-pitch Ball Grid Array	333	1.0	23 x 23	2.60
FG676 / FGG676	676	Fine-pitch Ball Grid Array	489	1.0	27 x 27	2.60
FG900 / FGG900	900	Fine-pitch Ball Grid Array	633	1.0	31 x 31	2.60
FG1156 / FGG1156(1)	1156	Fine-pitch Ball Grid Array	784	1.0	35 x 35	2.60

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Selecting the Right Package Option

Spartan-3 FPGAs are available in both quad-flat pack (QFP) and ball grid array (BGA) packaging options. While QFP packaging offers the lowest absolute cost, the BGA packages are superior in almost every other aspect, as summarized in Table 82. Consequently, Xilinx recommends using BGA packaging whenever possible.

Table 82: **Comparing Spartan-3 Device Packaging Options**

Characteristic	Quad Flat-Pack (QFP)	Ball Grid Array (BGA)
Maximum User I/O	141	633
Packing Density (Logic/Area)	Good	Better
Signal Integrity	Fair	Better
Simultaneous Switching Output (SSO) Support	Limited	Better
Thermal Dissipation	Fair	Better
Minimum Printed Circuit Board (PCB) Layers	4	6
Hand Assembly/Rework	Possible	Very Difficult

Table 91: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
2	IO_L23N_2/VREF_2	P98	VREF
2	IO_L23P_2	P97	I/O
2	IO_L24N_2	P96	I/O
2	IO_L24P_2	P95	I/O
2	IO_L40N_2	P93	I/O
2	IO_L40P_2/VREF_2	P92	VREF
3	IO	P76	I/O
3	IO_L01N_3/VRP_3	P74	DCI
3	IO_L01P_3/VRN_3	P73	DCI
3	IO_L20N_3	P78	I/O
3	IO_L20P_3	P77	I/O
3	IO_L21N_3	P80	I/O
3	IO_L21P_3	P79	I/O
3	IO_L22N_3	P83	I/O
3	IO_L22P_3	P82	I/O
3	IO_L23N_3	P85	I/O
3	IO_L23P_3/VREF_3	P84	VREF
3	IO_L24N_3	P87	I/O
3	IO_L24P_3	P86	I/O
3	IO_L40N_3/VREF_3	P90	VREF
3	IO_L40P_3	P89	I/O
4	IO/VREF_4	P70	VREF
4	IO_L01N_4/VRP_4	P69	DCI
4	IO_L01P_4/VRN_4	P68	DCI
4	IO_L27N_4/DIN/D0	P65	DUAL
4	IO_L27P_4/D1	P63	DUAL
4	IO_L30N_4/D2	P60	DUAL
4	IO_L30P_4/D3	P59	DUAL
4	IO_L31N_4/INIT_B	P58	DUAL
4	IO_L31P_4/DOUT/BUSY	P57	DUAL
4	IO_L32N_4/GCLK1	P56	GCLK
4	IO_L32P_4/GCLK0	P55	GCLK
5	IO/VREF_5	P44	VREF
5	IO_L01N_5/RDWR_B	P41	DUAL
5	IO_L01P_5/CS_B	P40	DUAL
5	IO_L28N_5/D6	P47	DUAL
5	IO_L28P_5/D7	P46	DUAL
5	IO_L31N_5/D4	P51	DUAL
5	IO_L31P_5/D5	P50	DUAL
5	IO_L32N_5/GCLK3	P53	GCLK

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
4	IO_L31P_4/ DOUT/BUSY	V10	DUAL
4	IO_L32N_4/GCLK1	N10	GCLK
4	IO_L32P_4/GCLK0	P10	GCLK
4	VCCO_4	M10	VCCO
4	VCCO_4	M11	VCCO
4	VCCO_4	T13	VCCO
4	VCCO_4	U11	VCCO
5	IO	N8	I/O
5	IO	P8	I/O
5	IO	U6	I/O
5	IO/VREF_5	R9	VREF
5	IO_L01N_5/RDWR_B	V3	DUAL
5	IO_L01P_5/CS_B	V2	DUAL
5	IO_L06N_5	T5	I/O
5	IO_L06P_5	T4	I/O
5	IO_L10N_5/VRP_5	V4	DCI
5	IO_L10P_5/VRN_5	U4	DCI
5	IO_L15N_5	R6	I/O
5	IO_L15P_5	R5	I/O
5	IO_L16N_5	V5	I/O
5	IO_L16P_5	U5	I/O
5	IO_L27N_5/VREF_5	P6	VREF
5	IO_L27P_5	P7	I/O
5	IO_L28N_5/D6	R7	DUAL
5	IO_L28P_5/D7	T7	DUAL
5	IO_L29N_5	V8	I/O
5	IO_L29P_5/VREF_5	V7	VREF
5	IO_L30N_5	R8	I/O
5	IO_L30P_5	T8	I/O
5	IO_L31N_5/D4	U9	DUAL
5	IO_L31P_5/D5	V9	DUAL
5	IO_L32N_5/GCLK3	N9	GCLK
5	IO_L32P_5/GCLK2	P9	GCLK
5	VCCO_5	M8	VCCO
5	VCCO_5	M9	VCCO
5	VCCO_5	T6	VCCO
5	VCCO_5	U8	VCCO
6	IO	K6	I/O
6	IO_L01N_6/VRP_6	T3	DCI

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
3	IO_L16P_3	IO_L16P_3	Y22	I/O
3	IO_L17N_3	IO_L17N_3	V19	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	W19	VREF
3	IO_L19N_3	IO_L19N_3	W21	I/O
3	IO_L19P_3	IO_L19P_3	W20	I/O
3	IO_L20N_3	IO_L20N_3	U19	I/O
3	IO_L20P_3	IO_L20P_3	V20	I/O
3	IO_L21N_3	IO_L21N_3	V22	I/O
3	IO_L21P_3	IO_L21P_3	V21	I/O
3	IO_L22N_3	IO_L22N_3	T17	I/O
3	IO_L22P_3	IO_L22P_3	U18	I/O
3	IO_L23N_3	IO_L23N_3	U21	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	U20	VREF
3	IO_L24N_3	IO_L24N_3	R18	I/O
3	IO_L24P_3	IO_L24P_3	T18	I/O
3	N.C. (◆)	IO_L26N_3	T20	I/O
3	N.C. (◆)	IO_L26P_3	T19	I/O
3	IO_L27N_3	IO_L27N_3	T22	I/O
3	IO_L27P_3	IO_L27P_3	T21	I/O
3	N.C. (◆)	IO_L28N_3	R22	I/O
3	N.C. (◆)	IO_L28P_3	R21	I/O
3	N.C. (◆)	IO_L29N_3	P19	I/O
3	N.C. (◆)	IO_L29P_3	R19	I/O
3	N.C. (◆)	IO_L31N_3	P18	I/O
3	N.C. (◆)	IO_L31P_3	P17	I/O
3	N.C. (◆)	IO_L32N_3	P22	I/O
3	N.C. (◆)	IO_L32P_3	P21	I/O
3	N.C. (◆)	IO_L33N_3	N18	I/O
3	N.C. (◆)	IO_L33P_3	N17	I/O
3	IO_L34N_3	IO_L34N_3	N20	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	N19	VREF
3	IO_L35N_3	IO_L35N_3	N22	I/O
3	IO_L35P_3	IO_L35P_3	N21	I/O
3	IO_L38N_3	IO_L38N_3	M18	I/O
3	IO_L38P_3	IO_L38P_3	M17	I/O
3	IO_L39N_3	IO_L39N_3	M20	I/O
3	IO_L39P_3	IO_L39P_3	M19	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	M22	VREF
3	IO_L40P_3	IO_L40P_3	M21	I/O
3	VCCO_3	VCCO_3	M16	VCCO

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
6	IO_L16N_6	IO_L16N_6	AE2	I/O
6	IO_L16P_6	IO_L16P_6	AE1	I/O
6	IO_L17N_6	IO_L17N_6	AD10	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	AD9	VREF
6	IO_L19N_6	IO_L19N_6	AD2	I/O
6	IO_L19P_6	IO_L19P_6	AD1	I/O
6	IO_L20N_6	IO_L20N_6	AC11	I/O
6	IO_L20P_6	IO_L20P_6	AC10	I/O
6	IO_L21N_6	IO_L21N_6	AC8	I/O
6	IO_L21P_6	IO_L21P_6	AC7	I/O
6	IO_L22N_6	IO_L22N_6	AC6	I/O
6	IO_L22P_6	IO_L22P_6	AC5	I/O
6	IO_L23N_6	IO_L23N_6	AC2	I/O
6	IO_L23P_6	IO_L23P_6	AC1	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	AC9	VREF
6	IO_L24P_6	IO_L24P_6	AB10	I/O
6	IO_L25N_6	IO_L25N_6	AB8	I/O
6	IO_L25P_6	IO_L25P_6	AB7	I/O
6	IO_L26N_6	IO_L26N_6	AB4	I/O
6	IO_L26P_6	IO_L26P_6	AB3	I/O
6	IO_L27N_6	IO_L27N_6	AB11	I/O
6	IO_L27P_6	IO_L27P_6	AA11	I/O
6	IO_L28N_6	IO_L28N_6	AA8	I/O
6	IO_L28P_6	IO_L28P_6	AA7	I/O
6	IO_L29N_6	IO_L29N_6	AA6	I/O
6	IO_L29P_6	IO_L29P_6	AA5	I/O
6	IO_L30N_6	IO_L30N_6	AA4	I/O
6	IO_L30P_6	IO_L30P_6	AA3	I/O
6	IO_L31N_6	IO_L31N_6	AA2	I/O
6	IO_L31P_6	IO_L31P_6	AA1	I/O
6	IO_L32N_6	IO_L32N_6	Y11	I/O
6	IO_L32P_6	IO_L32P_6	Y10	I/O
6	IO_L33N_6	IO_L33N_6	Y4	I/O
6	IO_L33P_6	IO_L33P_6	Y3	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	Y2	VREF
6	IO_L34P_6	IO_L34P_6	Y1	I/O
6	IO_L35N_6	IO_L35N_6	Y9	I/O
6	IO_L35P_6	IO_L35P_6	W10	I/O
6	IO_L36N_6	IO_L36N_6	W7	I/O
6	IO_L36P_6	IO_L36P_6	W6	I/O

User I/Os by Bank

Note: The FG(G)1156 package is discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Table 111 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S4000 in the FG1156 package. Similarly, Table 112 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S5000 in the FG1156 package.

Table 111: **User I/Os Per Bank for XC3S4000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	90	79	0	2	7	2
	1	90	79	0	2	7	2
Right	2	88	80	0	2	6	0
	3	88	79	0	2	7	0
Bottom	4	90	73	6	2	7	2
	5	90	73	6	2	7	2
Left	6	88	79	0	2	7	0
	7	88	79	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

Table 112: **User I/Os Per Bank for XC3S5000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	100	89	0	2	7	2
	1	100	89	0	2	7	2
Right	2	96	87	0	2	7	0
	3	96	87	0	2	7	0
Bottom	4	100	83	6	2	7	2
	5	100	83	6	2	7	2
Left	6	96	87	0	2	7	0
	7	96	87	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
GND	GND	GND	GND	GND	VCCINT	I/O L51N_3 ◆	I/O	I/O	I/O L37P_3	I/O L37N_3	I/O L38P_3	I/O L38N_3	I/O L39P_3	I/O L39N_3	I/O L40P_3	I/O L40N_3 VREF_3	V
GND	GND	GND	GND	VCCINT	VCCO_3	I/O L51P_3 ◆	I/O L33N_3	GND	VCCAUX	I/O L34P_3 VREF_3	I/O L34N_3	GND	VCCO_3	I/O L35P_3	I/O L35N_3	GND	W
GND	GND	GND	GND	VCCINT	VCCO_3	I/O L50P_3	I/O L50N_3	I/O L33P_3	VCCO_3	I/O L30P_3	I/O L30N_3	VCCAUX	I/O L31P_3	I/O L31N_3	I/O L32P_3	I/O L32N_3	Y
GND	GND	GND	GND	VCCINT	VCCO_3	I/O L48N_3	I/O L49P_3 ◆	I/O L49N_3 ◆	I/O L26P_3	I/O L26N_3	I/O L27P_3	I/O L27N_3	I/O L28P_3	I/O L28N_3	I/O L29P_3	I/O L29N_3	AA
GND	VCCINT	VCCINT	VCCINT	VCCINT	VCCO_3	I/O L48P_3	I/O L24N_3	GND	I/O L46P_3	I/O L46N_3	VCCO_3	GND	I/O L47P_3	I/O L47N_3	VCCO_3	GND	AB
VCCINT	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCINT	I/O L20P_3	I/O L20N_3	I/O L24P_3	I/O L21P_3	I/O L21N_3	I/O L22P_3	I/O L22N_3	I/O L23P_3 VREF_3	I/O L23N_3	I/O L45P_3	I/O L45N_3	AC
I/O	I/O	I/O	I/O L18N_4	I/O	I/O L11N_4	DONE	I/O L17P_3 VREF_3	I/O L17N_3	VCCO_3	I/O L44P_3 ◆	I/O L44N_3 ◆	VCCAUX	VCCO_3	GND	I/O L19P_3	I/O L19N_3	AD
I/O	I/O	I/O L23N_4	I/O L18P_4	I/O	I/O L11P_4	I/O ◆	GND	I/O L12N_3	I/O L13P_3	I/O L13N_3 VREF_3	I/O L14P_3	I/O L14N_3	I/O L15P_3	I/O L15N_3	I/O L16P_3	I/O L16N_3	AE
I/O L29N_4	GND	I/O L23P_4	IO VREF_4	GND	I/O L12N_4	I/O	I/O L07N_4	I/O ◆	I/O L12P_3	I/O L09P_3 VREF_3	I/O L09N_3	GND	I/O L10N_3	I/O L11P_3	I/O L11N_3	GND	AF
I/O L29P_4	VCCAUX	VCCO_4	I/O L19N_4	I/O L16N_4	I/O L12P_4	VCCO_4	I/O L07P_4	I/O	I/O	VCCO_3	I/O L07P_3	I/O L07N_3	I/O L10P_3	VCCO_3	I/O L08P_3	I/O L08N_3	AG
I/O L30N_4 D2	I/O L27N_4 DIN D0	I/O L24N_4	I/O L19P_4	I/O L16P_4	IO VREF_4	I/O L39N_4 ◆	I/O L08N_4	I/O L05N_4	VCCO_4	GND	I/O L06P_3	I/O L06N_3	I/O L41P_3 ◆	I/O L41N_3 ◆	I/O	I/O	AH
I/O L30P_4 D3	I/O L27P_4 D1	I/O L24P_4	I/O L20N_4	VCCO_4	I/O L13N_4	I/O L39P_4 ◆	I/O L08P_4	I/O L05P_4	I/O	I/O L35N_4	I/O	VCCAUX	I/O L04P_3	I/O L04N_3	I/O L05P_3	I/O L05N_3	AJ
IO VREF_4	GND	VCCAUX	I/O L20P_4	GND	I/O L13P_4	VCCAUX	I/O	GND	I/O L38N_4	I/O L35P_4	VCCAUX	GND	N.C. ◆ ■	I/O L03P_3	I/O L03N_3	GND	AK
I/O L31N_4 INIT_B	VCCO_4	I/O L25N_4	I/O L21N_4	I/O L17N_4	I/O L14N_4	VCCO_4	I/O L09N_4	I/O L06N_4 VREF_4	I/O L38P_4	I/O L36N_4 ◆	I/O L33N_4	IO VREF_4	CCLK	VCCO_3	I/O L02P_3	I/O L02N_3 VREF_3	AL
I/O L31P_4 DOUT BUSY	I/O L28N_4	I/O L25P_4	I/O L21P_4	I/O L17P_4	I/O L14P_4	GND	I/O L09P_4	I/O L06P_4	VCCO_4	I/O L36P_4 ◆	I/O L33P_4	I/O L03N_4	VCCO_4	GND	I/O L01P_3 VRN_3	I/O L01N_3 VRP_3	AM
I/O L32N_4 GCLK1	I/O L28P_4	I/O L26N_4	I/O L22N_4 VREF_4	VCCO_4	I/O L15N_4	I/O L40N_4 ◆	I/O L10N_4	I/O	I/O L04N_4	I/O L37N_4 ◆	I/O L34N_4	I/O L03P_4	I/O L02N_4	I/O L01N_4 VRP_4	GND	GND	AN
I/O L32P_4 GCLK0	GND	I/O L26P_4 VREF_4	I/O L22P_4	GND	I/O L15P_4	I/O L40P_4 ◆	I/O L10P_4	GND	I/O L04P_4	I/O L37P_4 ◆	I/O L34P_4	GND	I/O L02P_4	I/O L01P_4 VRN_4	GND	GND	AP

Bank 3

Bank 4

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Bottom Right Corner of FG1156 Package (Top View)

Figure 60: FG1156 Package Footprint (Top View) Continued