# AMD Xilinx - XC3S1000-4FTG256I Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 1920 |
| Number of Logic Elements/Cells | 17280 |
| Total RAM Bits | 442368 |
| Number of I/O | 173 |
| Number of Gates | 1000000 |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FTBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc3s1000-4ftg256i |

*Table 4:* **Example Ordering Information**

| Device | Speed Grade | | Package Type/Number of Pins | | Temperature Range ($T_j$) | |
|---|---|---|---|---|---|---|
| XC3S50 | -4 | Standard Performance | VQ(G)100 | 100-pin Very Thin Quad Flat Pack (VQFP) | C | Commercial (0°C to 85°C) |
| XC3S200 | -5 | High Performance(1) | CP(G)132(2) | 132-pin Chip-Scale Package (CSP) | I | Industrial (–40°C to 100°C) |
| XC3S400 | | | TQ(G)144 | 144-pin Thin Quad Flat Pack (TQFP) | | |
| XC3S1000 | | | PQ(G)208 | 208-pin Plastic Quad Flat Pack (PQFP) | | |
| XC3S1500 | | | FT(G)256 | 256-ball Fine-Pitch Thin Ball Grid Array (FTBGA) | | |
| XC3S2000 | | | FG(G)320 | 320-ball Fine-Pitch Ball Grid Array (FBGA) | | |
| XC3S4000 | | | FG(G)456 | 456-ball Fine-Pitch Ball Grid Array (FBGA) | | |
| XC3S5000 | | | FG(G)676 | 676-ball Fine-Pitch Ball Grid Array (FBGA) | | |
| | | | FG(G)900 | 900-ball Fine-Pitch Ball Grid Array (FBGA) | | |
| | | | FG(G)1156(2) | 1156-ball Fine-Pitch Ball Grid Array (FBGA) | | |

**Notes:**

1. The -5 speed grade is exclusively available in the Commercial temperature range.
2. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

## Revision History

| Date | Version | Description |
|---|---|---|
| 04/11/03 | 1.0 | Initial Xilinx release. |
| 04/24/03 | 1.1 | Updated block RAM, DCM, and multiplier counts for the XC3S50. |
| 12/24/03 | 1.2 | Added the FG320 package. |
| 07/13/04 | 1.3 | Added information on Pb-free packaging options. |
| 01/17/05 | 1.4 | Referenced Spartan-3 XA Automotive FPGA families in Table 1. Added XC3S50CP132, XC3S2000FG456, XC3S4000FG676 options to Table 3. Updated Package Marking to show mask revision code, fabrication facility code, and process technology code. |
| 08/19/05 | 1.5 | Added package markings for BGA packages (Figure 3) and CP132/CPG132 packages (Figure 4). Added differential (complementary single-ended) HSTL and SSTL I/O standards. |
| 04/03/06 | 2.0 | Increased number of supported single-ended and differential I/O standards. |
| 04/26/06 | 2.1 | Updated document links. |
| 05/25/07 | 2.2 | Updated Package Marking to allow for dual-marking. |
| 11/30/07 | 2.3 | Added XC3S5000 FG(G)676 to Table 3. Noted that FG(G)1156 package is being discontinued and updated max I/O count. |
| 06/25/08 | 2.4 | Updated max I/O counts based on FG1156 discontinuation. Clarified dual mark in Package Marking. Updated formatting and links. |
| 12/04/09 | 2.5 | CP132 and CPG132 packages are being discontinued. Added link to Spartan-3 FPGA customer notices. Updated Table 3 with package footprint dimensions. |
| 10/29/12 | 3.0 | Added Notice of Disclaimer section. Per XCN07022, updated the discontinued FG1156 and FGG1156 package discussion throughout document. Per XCN08011, updated the discontinued CP132 and CPG132 package discussion throughout document. Although the package is discontinued, updated the marking on Figure 4. This product is not recommended for new designs. |

According to Figure 7, the clock line OTCLK1 connects the CK inputs of the upper registers on the output and three-state paths. Similarly, OTCLK2 connects the CK inputs for the lower registers on the output and three-state paths. The upper and lower registers on the input path have independent clock lines: ICLK1 and ICLK2. The enable line OCE connects the CE inputs of the upper and lower registers on the output path. Similarly, TCE connects the CE inputs for the register pair on the three-state path and ICE does the same for the register pair on the input path. The Set/Reset (SR) line entering the IOB is common to all six registers, as is the Reverse (REV) line.

Each storage element supports numerous options in addition to the control over signal polarity described in the IOB Overview section. These are described in Table 6.

*Table 6:* **Storage Element Options**

| Option Switch | Function | Specificity |
|---|---|---|
| FF/Latch | Chooses between an edge-sensitive flip-flop or a level-sensitive latch | Independent for each storage element. |
| SYNC/ASYNC | Determines whether SR is synchronous or asynchronous | Independent for each storage element. |
| SRHIGH/SRLOW | Determines whether SR acts as a Set, which forces the storage element to a logic “1" (SRHIGH) or a Reset, which forces a logic “0” (SRLOW). | Independent for each storage element, except when using FDDR. In the latter case, the selection for the upper element (OFF1 or TFF2) applies to both elements. |
| INIT1/INIT0 | In the event of a Global Set/Reset, after configuration or upon activation of the GSR net, this switch decides whether to set or reset a storage element. By default, choosing SRLOW also selects INIT0; choosing SRHIGH also selects INIT1. | Independent for each storage element, except when using FDDR. In the latter case, selecting INIT0 for one element applies to both elements (even though INIT1 is selected for the other). |

## Double-Data-Rate Transmission

Double-Data-Rate (DDR) transmission describes the technique of synchronizing signals to both the rising and falling edges of the clock signal. Spartan-3 devices use register-pairs in all three IOB paths to perform DDR operations.

The pair of storage elements on the IOB’s Output path (OFF1 and OFF2), used as registers, combine with a special multiplexer to form a DDR D-type flip-flop (FDDR). This primitive permits DDR transmission where output data bits are synchronized to both the rising and falling edges of a clock. It is possible to access this function by placing either an FDDRRSE or an FDDRCPE component or symbol into the design. DDR operation requires two clock signals (50% duty cycle), one the inverted form of the other. These signals trigger the two registers in alternating fashion, as shown in Figure 8. Commonly, the Digital Clock Manager (DCM) generates the two clock signals by mirroring an incoming signal, then shifting it 180 degrees. This approach ensures minimal skew between the two signals.

The storage-element-pair on the Three-State path (TFF1 and TFF2) can also be combined with a local multiplexer to form an FDDR primitive. This permits synchronizing the output enable to both the rising and falling edges of a clock. This DDR operation is realized in the same way as for the output path.

The storage-element-pair on the input path (IFF1 and IFF2) allows an I/O to receive a DDR signal. An incoming DDR clock signal triggers one register and the inverted clock signal triggers the other register. In this way, the registers take turns capturing bits of the incoming DDR data signal.

*Table 9:* **Differential I/O Standards**

| Signal Standard (IOSTANDARD) | $V_{CCO}$ (Volts) | | $V_{REF}$ for Inputs (Volts) |
|---|---|---|---|
| | For Outputs | For Inputs | |
| LDT_25 (ULVDS_25) | 2.5 | – | – |
| LVDS_25 | 2.5 | – | – |
| BLVDS_25 | 2.5 | – | – |
| LVDSEXT_25 | 2.5 | – | – |
| LVPECL_25 | 2.5 | – | – |
| RSDS_25 | 2.5 | – | – |
| DIFF_HSTL_II_18 | 1.8 | – | – |
| DIFF_SSTL2_II | 2.5 | – | – |

**Notes:**

1. See Table 10 for a listing of the differential DCI standards.

The need to supply $V_{REF}$ and $V_{CCO}$ imposes constraints on which standards can be used in the same bank. See The Organization of IOBs into Banks section for additional guidelines concerning the use of the $V_{CCO}$ and $V_{REF}$ lines.

## Digitally Controlled Impedance (DCI)

When the round-trip delay of an output signal—i.e., from output to input and back again—exceeds rise and fall times, it is common practice to add termination resistors to the line carrying the signal. These resistors effectively match the impedance of a device's I/O to the characteristic impedance of the transmission line, thereby preventing reflections that adversely affect signal integrity. However, with the high I/O counts supported by modern devices, adding resistors requires significantly more components and board area. Furthermore, for some packages—e.g., ball grid arrays—it may not always be possible to place resistors close to pins.

DCI answers these concerns by providing two kinds of on-chip terminations: Parallel terminations make use of an integrated resistor network. Series terminations result from controlling the impedance of output drivers. DCI actively adjusts both parallel and series terminations to accurately match the characteristic impedance of the transmission line. This adjustment process compensates for differences in I/O impedance that can result from normal variation in the ambient temperature, the supply voltage and the manufacturing process. When the output driver turns off, the series termination, by definition, approaches a very high impedance; in contrast, parallel termination resistors remain at the targeted values.

DCI is available only for certain I/O standards, as listed in Table 10. DCI is selected by applying the appropriate I/O standard extensions to symbols or components. There are five basic ways to configure terminations, as shown in Table 11. The DCI I/O standard determines which of these terminations is put into effect.

HSTL_I_DCI-, HSTL_III_DCI-, and SSTL2_I_DCI-type outputs do not require the VRN and VRP reference resistors. Likewise, LVDCI-type inputs do not require the VRN and VRP reference resistors. In a bank without any DCI I/O or a bank containing non-DCI I/O and purely HSTL_I_DCI- or HSTL_III_DCI-type outputs, or SSTL2_I_DCI-type outputs or LVDCI-type inputs, the associated VRN and VRP pins can be used as general-purpose I/O pins.

The HSLVDCI (High-Speed LVDCI) standard is intended for bidirectional use. The driver is identical to LVDCI, while the input is identical to HSTL. By using a $V_{REF}$-referenced input, HSLVDCI allows greater input sensitivity at the receiver than when using a single-ended LVCMOS-type receiver.

*Table 10:* **DCI I/O Standards**

| Category of Signal Standard | Signal Standard (IOSTANDARD) | $V_{CCO}$ (V) | | $V_{REF}$ for Inputs (V) | Termination Type | |
|---|---|---|---|---|---|---|
| | | For Outputs | For Inputs | | At Output | At Input |
| **Single-Ended** | | | | | | |
| Gunning Transceiver Logic | GTL_DCI | 1.2 | 1.2 | 0.8 | Single | Single |
| | GTLP_DCI | 1.5 | 1.5 | 1.0 | | |
| High-Speed Transceiver Logic | HSTL_I_DCI | 1.5 | 1.5 | 0.75 | None | Split |
| | HSTL_III_DCI | 1.5 | 1.5 | 0.9 | None | Single |
| | HSTL_I_DCI_18 | 1.8 | 1.8 | 0.9 | None | Split |
| | HSTL_II_DCI_18<br>DIFF_HSTL_II_18_DCI | 1.8 | 1.8 | 0.9 | Split | |
| | HSTL_III_DCI_18 | 1.8 | 1.8 | 1.1 | None | Single |
| Low-Voltage CMOS | LVDCI_15 | 1.5 | 1.5 | – | Controlled impedance driver | None |
| | LVDCI_18 | 1.8 | 1.8 | – | | |
| | LVDCI_25 | 2.5 | 2.5 | – | | |
| | LVDCI_33[2] | 3.3 | 3.3 | – | | |
| | LVDCI_DV2_15 | 1.5 | 1.5 | – | Controlled driver with half-impedance | |
| | LVDCI_DV2_18 | 1.8 | 1.8 | – | | |
| | LVDCI_DV2_25 | 2.5 | 2.5 | – | | |
| | LVDCI_DV2_33 | 3.3 | 3.3 | – | | |
| Hybrid HSTL Input and LVCMOS Output | HSLVDCI_15 | 1.5 | 1.5 | 0.75 | Controlled impedance driver | None |
| | HSLVDCI_18 | 1.8 | 1.8 | 0.9 | | |
| | HSLVDCI_25 | 2.5 | 2.5 | 1.25 | | |
| | HSLVDCI_33 | 3.3 | 3.3 | 1.65 | | |
| Stub Series Terminated Logic[3] | SSTL18_I_DCI | 1.8 | 1.8 | 0.9 | 25Ω driver | Split |
| | SSTL2_I_DCI | 2.5 | 2.5 | 1.25 | 25Ω driver | |
| | SSTL2_II_DCI<br>DIFF_SSTL2_II_DCI | 2.5 | 2.5 | 1.25 | Split with 25Ω driver | |
| **Differential** | | | | | | |
| Low-Voltage Differential Signaling | LVDS_25_DCI | N/A | 2.5 | – | None | Split on each line of pair |
| | LVDSEXT_25_DCI | N/A | 2.5 | – | | |

**Notes:**

1. DCI signal standards are not supported in Bank 5 of any Spartan-3 FPGA packaged in a VQ100, CP132, or TQ144 package.
2. Equivalent to LVTTL DCI.
3. The SSTL18_II signal standard does not have a DCI equivalent.

upper path), enter the slice and connect directly to the LUT. Once inside the slice, the lower 4-bit path passes through a function generator ‘F’ (or ‘G’) that performs logic operations. The function generator’s Data output, ‘D’, offers five possible paths:

- Exit the slice via line ‘X’ (or ‘Y’) and return to interconnect.
- Inside the slice, ‘X’ (or ‘Y’) serves as an input to the DXMUX (DYMUX) which feeds the data input, ‘D’, of the FFX (FFY) storage element. The ‘Q’ output of the storage element drives the line XQ (or YQ) which exits the slice.
- Control the CYMUXF (or CYMUXG) multiplexer on the carry chain.
- With the carry chain, serve as an input to the XORF (or XORG) exclusive-OR gate that performs arithmetic operations, producing a result on ‘X’ (or ‘Y’).
- Drive the multiplexer F5MUX to implement logic functions wider than four bits. The ‘D’ outputs of both the F-LUT and G-LUT serve as data inputs to this multiplexer.

In addition to the main logic paths described above, there are two bypass paths that enter the slice as BX and BY. Once inside the FPGA, BX in the bottom half of the slice (or BY in the top half) can take any of several possible branches:

- Bypass both the LUT and the storage element, then exit the slice as BXOUT (or BYOUT) and return to interconnect.
- Bypass the LUT, then pass through a storage element via the D input before exiting as XQ (or YQ).
- Control the wide function multiplexer F5MUX (or F6MUX).
- Via multiplexers, serve as an input to the carry chain.
- Drives the DI input of the LUT.
- BY can control the REV inputs of both the FFY and FFX storage elements.
- Finally, the DIG_MUX multiplexer can switch BY onto the DIG line, which exits the slice.

Other slice signals shown in Figure 12 are discussed in the sections that follow.

### Coarse Phase Shift Outputs of the DLL Component

In addition to CLK0 for zero-phase alignment to the CLKIN signal, the DLL also provides the CLK90, CLK180 and CLK270 outputs for 90°, 180° and 270° phase-shifted signals, respectively. These signals are described in Table 16, page 33. Their relative timing in the Low Frequency Mode is shown in Figure 22, page 37. The CLK90, CLK180 and CLK270 outputs are not available when operating in the High Frequency mode. (See the description of the DLL_FREQUENCY_MODE attribute in Table 17, page 33.) For control in finer increments than 90°, see Phase Shifter (PS), page 39.

### Basic Frequency Synthesis Outputs of the DLL Component

The DLL component provides basic options for frequency multiplication and division in addition to the more flexible synthesis capability of the DFS component, described in a later section. These operations result in output clock signals with frequencies that are either a fraction (for division) or a multiple (for multiplication) of the incoming clock frequency. The CLK2X output produces an in-phase signal that is twice the frequency of CLKIN. The CLK2X180 output also doubles the frequency, but is 180° out-of-phase with respect to CLKIN. The CLKDIV output generates a clock frequency that is a predetermined fraction of the CLKIN frequency. The CLKDV_DIVIDE attribute determines the factor used to divide the CLKIN frequency. The attribute can be set to various values as described in Table 17. The basic frequency synthesis outputs are described in Table 16. Their relative timing in the Low Frequency Mode is shown in Figure 22.

The CLK2X and CLK2X180 outputs are not available when operating in the High Frequency mode. See the description of the DLL_FREQUENCY_MODE attribute in Table 18.

### Duty Cycle Correction of DLL Clock Outputs

The CLK2X(1), CLK2X180, and CLKDV(2) output signals ordinarily exhibit a 50% duty cycle—even if the incoming CLKIN signal has a different duty cycle. A 50% duty cycle means that the High and Low times of each clock cycle are equal. The DUTY_CYCLE_CORRECTION attribute determines whether or not duty cycle correction is applied to the CLK0, CLK90, CLK180 and CLK270 outputs. If DUTY_CYCLE_CORRECTION is set to TRUE, then the duty cycle of these four outputs is corrected to 50%. If DUTY_CYCLE_CORRECTION is set to FALSE, then these outputs exhibit the same duty cycle as the CLKIN signal. Figure 22 compares the characteristics of the DLL's output signals to those of the CLKIN signal.

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1. The CLK2X output generates a 25% duty cycle clock at the same frequency as the CLKIN signal until the DLL has achieved lock.
2. The duty cycle of the CLKDV outputs may differ somewhat from 50% (i.e., the signal will be High for less than 50% of the period) when the CLKDV_DIVIDE attribute is set to a non-integer value *and* the DLL is operating in the High Frequency mode.

*Table 20:* **PS Attributes**

| Attribute | Description | Values |
|---|---|---|
| CLKOUT_PHASE_SHIFT | Disables PS component or chooses between Fixed Phase and Variable Phase modes. | NONE, FIXED, VARIABLE |
| PHASE_SHIFT | Determines size and direction of initial fine phase shift. | Integers from –255 to +255(1) |

**Notes:**

1. The practical range of values will be less when $T_{CLKIN}$ > FINE_SHIFT_RANGE in the Fixed Phase mode, also when $T_{CLKIN}$ > (FINE_SHIFT_RANGE)/2 in the Variable Phase mode. the FINE_SHIFT_RANGE represents the sum total delay of all taps.

## The Variable Phase Mode

The "Variable Phase" mode dynamically adjusts the fine phase shift over time using three inputs to the PS component, namely PSEN, PSCLK and PSINCDEC, as defined in Table 21.

After device configuration, the PS component initially determines $T_{PS}$ by evaluating Equation (4) for the value assigned to the PHASE_SHIFT attribute. Then to dynamically adjust that phase shift, use the three PS inputs to increase or decrease the fine phase shift.

PSINCDEC is synchronized to the PSCLK clock signal, which is enabled by asserting PSEN. It is possible to drive the PSCLK input with the CLKIN signal or any other clock signal. A request for phase adjustment is entered as follows: For each PSCLK cycle that PSINCDEC is High, the PS component adds 1/256 of a CLKIN cycle to $T_{PS}$. Similarly, for each enabled PSCLK cycle that PSINCDEC is Low, the PS component subtracts 1/256 of a CLKIN cycle from $T_{PS}$. The phase adjustment may require as many as 100 CLKIN cycles plus three PSCLK cycles to take effect, at which point the output PSDONE goes High for one PSCLK cycle. This pulse indicates that the PS component has finished the present adjustment and is now ready for the next request. Asserting the Reset (RST) input, returns $T_{PS}$ to its original shift time, as determined by the PHASE_SHIFT attribute value. The set of waveforms in section [c] of Figure 23, page 41 illustrates the relationship between CLKFB and CLKIN in the Variable Phase mode.

*Table 21:* **Signals for Variable Phase Mode**

| Signal | Direction | Description |
|---|---|---|
| PSEN(1) | Input | Enables PSCLK for variable phase adjustment. |
| PSCLK(1) | Input | Clock to synchronize phase shift adjustment. |
| PSINCDEC(1) | Input | Chooses between increment and decrement for phase adjustment. It is synchronized to the PSCLK signal. |
| PSDONE | Output | Goes High to indicate that present phase adjustment is complete and PS component is ready for next phase adjustment request. It is synchronized to the PSCLK signal. |

**Notes:**

1. It is possible to program this input for either a true or inverted polarity

## Revision History

| Date | Version No. | Description |
|---|---|---|
| 04/11/03 | 1.0 | Initial Xilinx release |
| 05/19/03 | 1.1 | Added Block RAM column, DCMs, and multipliers to XC3S50 descriptions. |
| 07/11/03 | 1.2 | Explained the configuration port *Persist* option in Slave Parallel Mode (SelectMAP) section. Updated Figure 8 and Double-Data-Rate Transmission section to indicate that DDR clocking for the XC3S50 is the same as that for all other Spartan-3 devices. Updated description of I/O voltage tolerance in ESD Protection section. In Table 10, changed input termination type for DCI version of the LVCMOS standard to *None*. Added additional flexibility for making DLL connections in Figure 21 and accompanying text. In the Configuration section, inserted an explanation of how to choose power supplies for the configuration interface, including guidelines for achieving 3.3V-tolerance. |
| 08/24/04 | 1.3 | Showed inversion of 3-state signal (Figure 7). Clarified description of pull-up and pull-down resistors (Table 6 and page 13). Added information on operating block RAM with multipliers to page 26. Corrected output buffer name in Figure 21. Corrected description of how DOUT is synchronized to CCLK (page 47). |
| 08/19/05 | 1.4 | Corrected description of WRITE_FIRST and READ_FIRST in Table 13. Added note regarding address setup and hold time requirements whenever a block RAM port is enabled (Table 13). Added information in the maximum length of a Configuration daisy-chain. Added reference to XAPP453 in 3.3V-Tolerant Configuration Interface section. Added information on the STATUS[2] DCM output (Table 23). Added information on CCLK behavior and termination recommendations to Configuration. Added Additional Configuration Details section. Added Powering Spartan-3 FPGAs section. Removed GSR from Figure 31 because its timing is not programmable. |
| 04/03/06 | 2.0 | Updated Figure 7. Updated Figure 14. Updated Table 10. Updated Figure 22. Corrected Platform Flash supply voltage name and value in Figure 26 and Figure 28. Added No Internal Charge Pumps or Free-Running Oscillators. Corrected a few minor typographical errors. |
| 04/26/06 | 2.1 | Added more information on the pull-up resistors that are active during configuration to Configuration. Added information to Boundary-Scan (JTAG) Mode about potential interactions when configuring via JTAG if the mode select pins are set for other than JTAG. |
| 05/25/07 | 2.2 | Added Spartan-3 FPGA Design Documentation. Noted SSTL2_I_DCI 25-Ohm driver in Table 10 and Table 11. Added note that pull-down is active during boundary scan tests. |
| 11/30/07 | 2.3 | Updated links to documentation on xilinx.com. |
| 06/25/08 | 2.4 | Added HSLVDCI to Table 10. Updated formatting and links. |
| 12/04/09 | 2.5 | Updated HSLVDCI description in Digitally Controlled Impedance (DCI). Updated the low-voltage differential signaling $V_{CCO}$ values in Table 10. Noted that the CP132 package is being discontinued in The Organization of IOBs into Banks. Updated rule 4 in Rules Concerning Banks. Added software version requirement in The Fixed Phase Mode. |
| 10/29/12 | 3.0 | Added Notice of Disclaimer. Per XCN07022, updated the discontinued FG1156 and FGG1156 package discussion throughout document. Per XCN08011, updated the discontinued CP132 and CPG132 package discussion throughout document. This product is not recommended for new designs. |

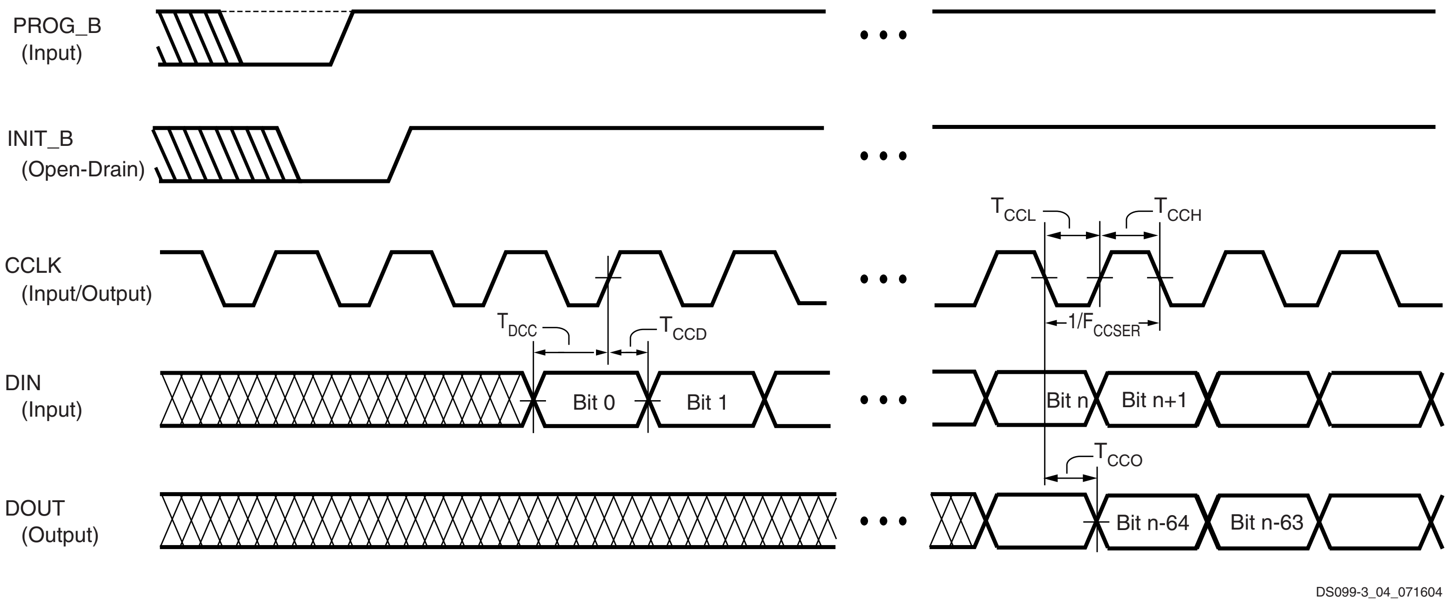


*Figure 37:* **Waveforms for Master and Slave Serial Configuration**

*Table 66:* **Timing for the Master and Slave Serial Configuration Modes**

| Symbol | Description | | Slave/ Master | All Speed Grades | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| **Clock-to-Output Times** | | | | | | |
| $T_{CCO}$ | The time from the falling transition on the CCLK pin to data appearing at the DOUT pin | | Both | 1.5 | 12.0 | ns |
| **Setup Times** | | | | | | |
| $T_{DCC}$ | The time from the setup of data at the DIN pin to the rising transition at the CCLK pin | | Both | 10.0 | – | ns |
| **Hold Times** | | | | | | |
| $T_{CCD}$ | The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin | | Both | 0 | – | ns |
| **Clock Timing** | | | | | | |
| $T_{CCH}$ | CCLK input pin High pulse width | | Slave | 5.0 | ∞ | ns |
| $T_{CCL}$ | CCLK input pin Low pulse width | | | 5.0 | ∞ | ns |
| $F_{CCSER}$ | Frequency of the clock signal at the CCLK input pin | No bitstream compression | | 0 | 66[2] | MHz |
| | | With bitstream compression | | 0 | 20 | MHz |
| | | During STARTUP phase | | 0 | 50 | MHz |
| $\Delta F_{CCSER}$ | Variation from the CCLK output frequency set using the ConfigRate BitGen option | | Master | –50% | +50% | – |

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

All VCCAUX inputs must be connected together and to the +2.5V voltage supply. Furthermore, there must be sufficient supply decoupling to guarantee problem-free operation, as described in XAPP623.

Because VCCAUX connects to the DCMs and the DCMs are sensitive to voltage changes, be sure that the VCCAUX supply and the ground return paths are designed for low noise and low voltage drop, especially that caused by a large number of simultaneous switching I/Os.

### GND Type: Ground

All GND pins must be connected and have a low resistance path back to the various VCCO, VCCINT, and VCCAUX supplies.

## Pin Behavior During Configuration

Table 79 shows how various pins behave during the FPGA configuration process. The actual behavior depends on the values applied to the M2, M1, and M0 mode select pins and the HSWAP_EN pin. The mode select pins determine which of the DUAL type pins are active during configuration. In JTAG configuration mode, none of the DUAL-type pins are used for configuration and all behave as user-I/O pins.

All DUAL-type pins not actively used during configuration and all I/O-type, DCI-type, VREF-type, GCLK-type pins are high impedance (floating, three-stated, Hi-Z) during the configuration process. These pins are indicated in Table 79 as shaded table entries or cells. These pins have a pull-up resistor to their associated VCCO if the HSWAP_EN pin is Low. When HSWAP_EN is High, these pull-up resistors are disabled during configuration.

Some pins always have an active pull-up resistor during configuration, regardless of the value applied to the HSWAP_EN pin. After configuration, these pull-up resistors are controlled by Bitstream Options.

- All the dedicated CONFIG-type configuration pins (CCLK, PROG_B, DONE, M2, M1, M0, and HSWAP_EN) have a pull-up resistor to VCCAUX.
- All JTAG-type pins (TCK, TDI, TMS, TDO) have a pull-up resistor to VCCAUX.
- The INIT_B DUAL-purpose pin has a pull-up resistor to VCCO_4 or VCCO_BOTTOM, depending on package style.

After configuration completes, some pins have optional behavior controlled by the configuration bitstream loaded into the part. For example, via the bitstream, all unused I/O pins can be collectively configured as input pins with either a pull-up resistor, a pull-down resistor, or be left in a high-impedance state.

*Table 79:* **Pin Behavior After Power-Up, During Configuration**

| Pin Name | Configuration Mode Settings <M2:M1:M0> | | | | | Bitstream Configuration Option |
|---|---|---|---|---|---|---|
| | Serial Modes | | SelectMap Parallel Modes | | JTAG Mode <1:0:1> | |
| | Master <0:0:0> | Slave <1:1:1> | Master <0:1:1> | Slave <1:1:0> | | |
| **I/O: General-purpose I/O pins** | | | | | | |
| IO | ▨ | ▨ | ▨ | ▨ | ▨ | UnusedPin |
| IO_Lxxy_# | ▨ | ▨ | ▨ | ▨ | ▨ | UnusedPin |
| **DUAL: Dual-purpose configuration pins** | | | | | | |
| IO_Lxxy_#/ DIN/D0 | DIN (I) | DIN (I) | D0 (I/O) | D0 (I/O) | ▨ | Persist UnusedPin |
| IO_Lxxy_#/ D1 | ▨ | ▨ | D1 (I/O) | D1 (I/O) | ▨ | Persist UnusedPin |
| IO_Lxxy_#/ D2 | ▨ | ▨ | D2 (I/O) | D2 (I/O) | ▨ | Persist UnusedPin |
| IO_Lxxy_#/ D3 | ▨ | ▨ | D3 (I/O) | D3 (I/O) | ▨ | Persist UnusedPin |
| IO_Lxxy_#/ D4 | ▨ | ▨ | D4 (I/O) | D4 (I/O) | ▨ | Persist UnusedPin |

*Table 91:* **TQ144 Package Pinout *(Cont'd)***

| Bank | XC3S50, XC3S200, XC3S400 Pin Name | TQ144 Pin Number | Type |
|---|---|---|---|
| 2 | IO_L23N_2/VREF_2 | P98 | VREF |
| 2 | IO_L23P_2 | P97 | I/O |
| 2 | IO_L24N_2 | P96 | I/O |
| 2 | IO_L24P_2 | P95 | I/O |
| 2 | IO_L40N_2 | P93 | I/O |
| 2 | IO_L40P_2/VREF_2 | P92 | VREF |
| 3 | IO | P76 | I/O |
| 3 | IO_L01N_3/VRP_3 | P74 | DCI |
| 3 | IO_L01P_3/VRN_3 | P73 | DCI |
| 3 | IO_L20N_3 | P78 | I/O |
| 3 | IO_L20P_3 | P77 | I/O |
| 3 | IO_L21N_3 | P80 | I/O |
| 3 | IO_L21P_3 | P79 | I/O |
| 3 | IO_L22N_3 | P83 | I/O |
| 3 | IO_L22P_3 | P82 | I/O |
| 3 | IO_L23N_3 | P85 | I/O |
| 3 | IO_L23P_3/VREF_3 | P84 | VREF |
| 3 | IO_L24N_3 | P87 | I/O |
| 3 | IO_L24P_3 | P86 | I/O |
| 3 | IO_L40N_3/VREF_3 | P90 | VREF |
| 3 | IO_L40P_3 | P89 | I/O |
| 4 | IO/VREF_4 | P70 | VREF |
| 4 | IO_L01N_4/VRP_4 | P69 | DCI |
| 4 | IO_L01P_4/VRN_4 | P68 | DCI |
| 4 | IO_L27N_4/DIN/D0 | P65 | DUAL |
| 4 | IO_L27P_4/D1 | P63 | DUAL |
| 4 | IO_L30N_4/D2 | P60 | DUAL |
| 4 | IO_L30P_4/D3 | P59 | DUAL |
| 4 | IO_L31N_4/INIT_B | P58 | DUAL |
| 4 | IO_L31P_4/DOUT/BUSY | P57 | DUAL |
| 4 | IO_L32N_4/GCLK1 | P56 | GCLK |
| 4 | IO_L32P_4/GCLK0 | P55 | GCLK |
| 5 | IO/VREF_5 | P44 | VREF |
| 5 | IO_L01N_5/RDWR_B | P41 | DUAL |
| 5 | IO_L01P_5/CS_B | P40 | DUAL |
| 5 | IO_L28N_5/D6 | P47 | DUAL |
| 5 | IO_L28P_5/D7 | P46 | DUAL |
| 5 | IO_L31N_5/D4 | P51 | DUAL |
| 5 | IO_L31P_5/D5 | P50 | DUAL |
| 5 | IO_L32N_5/GCLK3 | P53 | GCLK |

*Table 103:* **FG676 Package Pinout *(Cont'd)***

| Bank | XC3S1000 Pin Name | XC3S1500 Pin Name | XC3S2000 Pin Name | XC3S4000 Pin Name | XC3S5000 Pin Name | FG676 Pin Number | Type |
|---|---|---|---|---|---|---|---|
| N/A | GND | GND | GND | GND | GND | R16 | GND |
| N/A | GND | GND | GND | GND | GND | R17 | GND |
| N/A | GND | GND | GND | GND | GND | R23 | GND |
| N/A | GND | GND | GND | GND | GND | T10 | GND |
| N/A | GND | GND | GND | GND | GND | T11 | GND |
| N/A | GND | GND | GND | GND | GND | T12 | GND |
| N/A | GND | GND | GND | GND | GND | T13 | GND |
| N/A | GND | GND | GND | GND | GND | T14 | GND |
| N/A | GND | GND | GND | GND | GND | T15 | GND |
| N/A | GND | GND | GND | GND | GND | T16 | GND |
| N/A | GND | GND | GND | GND | GND | T17 | GND |
| N/A | GND | GND | GND | GND | GND | U11 | GND |
| N/A | GND | GND | GND | GND | GND | U12 | GND |
| N/A | GND | GND | GND | GND | GND | U15 | GND |
| N/A | GND | GND | GND | GND | GND | U16 | GND |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | A2 | VCCAUX |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | A9 | VCCAUX |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | A18 | VCCAUX |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | A25 | VCCAUX |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | AE1 | VCCAUX |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | AE26 | VCCAUX |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | AF2 | VCCAUX |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | AF9 | VCCAUX |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | AF18 | VCCAUX |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | AF25 | VCCAUX |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | B1 | VCCAUX |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | B26 | VCCAUX |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | J1 | VCCAUX |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | J26 | VCCAUX |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | V1 | VCCAUX |
| N/A | VCCAUX | VCCAUX | VCCAUX | VCCAUX | VCCAUX | V26 | VCCAUX |
| N/A | VCCINT | VCCINT | VCCINT | VCCINT | VCCINT | H8 | VCCINT |
| N/A | VCCINT | VCCINT | VCCINT | VCCINT | VCCINT | H19 | VCCINT |
| N/A | VCCINT | VCCINT | VCCINT | VCCINT | VCCINT | J9 | VCCINT |
| N/A | VCCINT | VCCINT | VCCINT | VCCINT | VCCINT | J10 | VCCINT |
| N/A | VCCINT | VCCINT | VCCINT | VCCINT | VCCINT | J17 | VCCINT |
| N/A | VCCINT | VCCINT | VCCINT | VCCINT | VCCINT | J18 | VCCINT |
| N/A | VCCINT | VCCINT | VCCINT | VCCINT | VCCINT | K9 | VCCINT |
| N/A | VCCINT | VCCINT | VCCINT | VCCINT | VCCINT | K10 | VCCINT |
| N/A | VCCINT | VCCINT | VCCINT | VCCINT | VCCINT | K17 | VCCINT |
| N/A | VCCINT | VCCINT | VCCINT | VCCINT | VCCINT | K18 | VCCINT |
| N/A | VCCINT | VCCINT | VCCINT | VCCINT | VCCINT | U9 | VCCINT |
| N/A | VCCINT | VCCINT | VCCINT | VCCINT | VCCINT | U10 | VCCINT |

*Table 107:* **FG900 Package Pinout *(Cont'd)***

| Bank | XC3S2000 Pin Name | XC3S4000, XC3S5000 Pin Name | FG900 Pin Number | Type |
|---|---|---|---|---|
| 2 | IO_L04N_2 | IO_L04N_2 | E29 | I/O |
| 2 | IO_L04P_2 | IO_L04P_2 | E30 | I/O |
| 2 | IO_L05N_2 | IO_L05N_2 | F28 | I/O |
| 2 | IO_L05P_2 | IO_L05P_2 | F29 | I/O |
| 2 | IO_L06N_2 | IO_L06N_2 | G27 | I/O |
| 2 | IO_L06P_2 | IO_L06P_2 | G28 | I/O |
| 2 | IO_L07N_2 | IO_L07N_2 | G29 | I/O |
| 2 | IO_L07P_2 | IO_L07P_2 | G30 | I/O |
| 2 | IO_L08N_2 | IO_L08N_2 | G25 | I/O |
| 2 | IO_L08P_2 | IO_L08P_2 | H24 | I/O |
| 2 | IO_L09N_2/VREF_2 | IO_L09N_2/VREF_2 | H25 | VREF |
| 2 | IO_L09P_2 | IO_L09P_2 | H26 | I/O |
| 2 | IO_L10N_2 | IO_L10N_2 | H27 | I/O |
| 2 | IO_L10P_2 | IO_L10P_2 | H28 | I/O |
| 2 | IO_L12N_2 | IO_L12N_2 | H29 | I/O |
| 2 | IO_L12P_2 | IO_L12P_2 | H30 | I/O |
| 2 | IO_L13N_2 | IO_L13N_2 | J26 | I/O |
| 2 | IO_L13P_2/VREF_2 | IO_L13P_2/VREF_2 | J27 | VREF |
| 2 | IO_L14N_2 | IO_L14N_2 | J29 | I/O |
| 2 | IO_L14P_2 | IO_L14P_2 | J30 | I/O |
| 2 | IO_L15N_2 | IO_L15N_2 | J23 | I/O |
| 2 | IO_L15P_2 | IO_L15P_2 | K22 | I/O |
| 2 | IO_L16N_2 | IO_L16N_2 | K24 | I/O |
| 2 | IO_L16P_2 | IO_L16P_2 | K25 | I/O |
| 2 | IO_L19N_2 | IO_L19N_2 | L25 | I/O |
| 2 | IO_L19P_2 | IO_L19P_2 | L26 | I/O |
| 2 | IO_L20N_2 | IO_L20N_2 | L27 | I/O |
| 2 | IO_L20P_2 | IO_L20P_2 | L28 | I/O |
| 2 | IO_L21N_2 | IO_L21N_2 | L29 | I/O |
| 2 | IO_L21P_2 | IO_L21P_2 | L30 | I/O |
| 2 | IO_L22N_2 | IO_L22N_2 | M22 | I/O |
| 2 | IO_L22P_2 | IO_L22P_2 | M23 | I/O |
| 2 | IO_L23N_2/VREF_2 | IO_L23N_2/VREF_2 | M24 | VREF |
| 2 | IO_L23P_2 | IO_L23P_2 | M25 | I/O |
| 2 | IO_L24N_2 | IO_L24N_2 | M27 | I/O |
| 2 | IO_L24P_2 | IO_L24P_2 | M28 | I/O |
| 2 | IO_L26N_2 | IO_L26N_2 | M21 | I/O |
| 2 | IO_L26P_2 | IO_L26P_2 | N21 | I/O |
| 2 | IO_L27N_2 | IO_L27N_2 | N22 | I/O |
| 2 | IO_L27P_2 | IO_L27P_2 | N23 | I/O |

*Table 107:* **FG900 Package Pinout *(Cont'd)***

| Bank | XC3S2000 Pin Name | XC3S4000, XC3S5000 Pin Name | FG900 Pin Number | Type |
|---|---|---|---|---|
| 2 | VCCO_2 | VCCO_2 | J28 | VCCO |
| 2 | VCCO_2 | VCCO_2 | N28 | VCCO |
| 3 | IO | IO | AB25 | I/O |
| 3 | IO_L01N_3/VRP_3 | IO_L01N_3/VRP_3 | AH30 | DCI |
| 3 | IO_L01P_3/VRN_3 | IO_L01P_3/VRN_3 | AH29 | DCI |
| 3 | IO_L02N_3/VREF_3 | IO_L02N_3/VREF_3 | AG28 | VREF |
| 3 | IO_L02P_3 | IO_L02P_3 | AG27 | I/O |
| 3 | IO_L03N_3 | IO_L03N_3 | AG30 | I/O |
| 3 | IO_L03P_3 | IO_L03P_3 | AG29 | I/O |
| 3 | IO_L04N_3 | IO_L04N_3 | AF30 | I/O |
| 3 | IO_L04P_3 | IO_L04P_3 | AF29 | I/O |
| 3 | IO_L05N_3 | IO_L05N_3 | AE26 | I/O |
| 3 | IO_L05P_3 | IO_L05P_3 | AF27 | I/O |
| 3 | IO_L06N_3 | IO_L06N_3 | AE29 | I/O |
| 3 | IO_L06P_3 | IO_L06P_3 | AE28 | I/O |
| 3 | IO_L07N_3 | IO_L07N_3 | AD28 | I/O |
| 3 | IO_L07P_3 | IO_L07P_3 | AD27 | I/O |
| 3 | IO_L08N_3 | IO_L08N_3 | AD30 | I/O |
| 3 | IO_L08P_3 | IO_L08P_3 | AD29 | I/O |
| 3 | IO_L09N_3 | IO_L09N_3 | AC24 | I/O |
| 3 | IO_L09P_3/VREF_3 | IO_L09P_3/VREF_3 | AD25 | VREF |
| 3 | IO_L10N_3 | IO_L10N_3 | AC26 | I/O |
| 3 | IO_L10P_3 | IO_L10P_3 | AC25 | I/O |
| 3 | IO_L11N_3 | IO_L11N_3 | AC28 | I/O |
| 3 | IO_L11P_3 | IO_L11P_3 | AC27 | I/O |
| 3 | IO_L13N_3/VREF_3 | IO_L13N_3/VREF_3 | AC30 | VREF |
| 3 | IO_L13P_3 | IO_L13P_3 | AC29 | I/O |
| 3 | IO_L14N_3 | IO_L14N_3 | AB27 | I/O |
| 3 | IO_L14P_3 | IO_L14P_3 | AB26 | I/O |
| 3 | IO_L15N_3 | IO_L15N_3 | AB30 | I/O |
| 3 | IO_L15P_3 | IO_L15P_3 | AB29 | I/O |
| 3 | IO_L16N_3 | IO_L16N_3 | AA22 | I/O |
| 3 | IO_L16P_3 | IO_L16P_3 | AB23 | I/O |
| 3 | IO_L17N_3 | IO_L17N_3 | AA25 | I/O |
| 3 | IO_L17P_3/VREF_3 | IO_L17P_3/VREF_3 | AA24 | VREF |
| 3 | IO_L19N_3 | IO_L19N_3 | AA29 | I/O |
| 3 | IO_L19P_3 | IO_L19P_3 | AA28 | I/O |
| 3 | IO_L20N_3 | IO_L20N_3 | Y21 | I/O |
| 3 | IO_L20P_3 | IO_L20P_3 | AA21 | I/O |
| 3 | IO_L21N_3 | IO_L21N_3 | Y24 | I/O |

*Table 107:* **FG900 Package Pinout *(Cont'd)***

| Bank | XC3S2000 Pin Name | XC3S4000, XC3S5000 Pin Name | FG900 Pin Number | Type |
|---|---|---|---|---|
| N/A | GND | GND | K30 | GND |
| N/A | GND | GND | P30 | GND |
| N/A | GND | GND | U30 | GND |
| N/A | GND | GND | AA30 | GND |
| N/A | GND | GND | AE30 | GND |
| N/A | GND | GND | AJ30 | GND |
| N/A | GND | GND | AK30 | GND |
| N/A | GND | GND | AK2 | GND |
| N/A | VCCAUX | VCCAUX | F4 | VCCAUX |
| N/A | VCCAUX | VCCAUX | K4 | VCCAUX |
| N/A | VCCAUX | VCCAUX | P4 | VCCAUX |
| N/A | VCCAUX | VCCAUX | U4 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AA4 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AE4 | VCCAUX |
| N/A | VCCAUX | VCCAUX | D6 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AG6 | VCCAUX |
| N/A | VCCAUX | VCCAUX | D10 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AG10 | VCCAUX |
| N/A | VCCAUX | VCCAUX | D14 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AG14 | VCCAUX |
| N/A | VCCAUX | VCCAUX | D17 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AG17 | VCCAUX |
| N/A | VCCAUX | VCCAUX | D21 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AG21 | VCCAUX |
| N/A | VCCAUX | VCCAUX | D25 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AG25 | VCCAUX |
| N/A | VCCAUX | VCCAUX | F27 | VCCAUX |
| N/A | VCCAUX | VCCAUX | K27 | VCCAUX |
| N/A | VCCAUX | VCCAUX | P27 | VCCAUX |
| N/A | VCCAUX | VCCAUX | U27 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AA27 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AE27 | VCCAUX |
| N/A | VCCINT | VCCINT | L11 | VCCINT |
| N/A | VCCINT | VCCINT | R11 | VCCINT |
| N/A | VCCINT | VCCINT | T11 | VCCINT |
| N/A | VCCINT | VCCINT | Y11 | VCCINT |
| N/A | VCCINT | VCCINT | M12 | VCCINT |
| N/A | VCCINT | VCCINT | N12 | VCCINT |
| N/A | VCCINT | VCCINT | P12 | VCCINT |
| N/A | VCCINT | VCCINT | U12 | VCCINT |

*Table 107:* **FG900 Package Pinout *(Cont'd)***

| Bank | XC3S2000 Pin Name | XC3S4000, XC3S5000 Pin Name | FG900 Pin Number | Type |
|---|---|---|---|---|
| N/A | VCCINT | VCCINT | V12 | VCCINT |
| N/A | VCCINT | VCCINT | W12 | VCCINT |
| N/A | VCCINT | VCCINT | M13 | VCCINT |
| N/A | VCCINT | VCCINT | W13 | VCCINT |
| N/A | VCCINT | VCCINT | M14 | VCCINT |
| N/A | VCCINT | VCCINT | W14 | VCCINT |
| N/A | VCCINT | VCCINT | L15 | VCCINT |
| N/A | VCCINT | VCCINT | Y15 | VCCINT |
| N/A | VCCINT | VCCINT | L16 | VCCINT |
| N/A | VCCINT | VCCINT | Y16 | VCCINT |
| N/A | VCCINT | VCCINT | M17 | VCCINT |
| N/A | VCCINT | VCCINT | W17 | VCCINT |
| N/A | VCCINT | VCCINT | M18 | VCCINT |
| N/A | VCCINT | VCCINT | W18 | VCCINT |
| N/A | VCCINT | VCCINT | M19 | VCCINT |
| N/A | VCCINT | VCCINT | N19 | VCCINT |
| N/A | VCCINT | VCCINT | P19 | VCCINT |
| N/A | VCCINT | VCCINT | U19 | VCCINT |
| N/A | VCCINT | VCCINT | V19 | VCCINT |
| N/A | VCCINT | VCCINT | W19 | VCCINT |
| N/A | VCCINT | VCCINT | L20 | VCCINT |
| N/A | VCCINT | VCCINT | R20 | VCCINT |
| N/A | VCCINT | VCCINT | T20 | VCCINT |
| N/A | VCCINT | VCCINT | Y20 | VCCINT |
| VCCAUX | CCLK | CCLK | AH28 | CONFIG |
| VCCAUX | DONE | DONE | AJ28 | CONFIG |
| VCCAUX | HSWAP_EN | HSWAP_EN | A3 | CONFIG |
| VCCAUX | M0 | M0 | AJ3 | CONFIG |
| VCCAUX | M1 | M1 | AH3 | CONFIG |
| VCCAUX | M2 | M2 | AK3 | CONFIG |
| VCCAUX | PROG_B | PROG_B | B3 | CONFIG |
| VCCAUX | TCK | TCK | B28 | JTAG |
| VCCAUX | TDI | TDI | C3 | JTAG |
| VCCAUX | TDO | TDO | C28 | JTAG |
| VCCAUX | TMS | TMS | A28 | JTAG |

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| 0 | IO_L23P_0 | IO_L23P_0 | J15 | I/O |
| 0 | IO_L24N_0 | IO_L24N_0 | G15 | I/O |
| 0 | IO_L24P_0 | IO_L24P_0 | F15 | I/O |
| 0 | IO_L25N_0 | IO_L25N_0 | D15 | I/O |
| 0 | IO_L25P_0 | IO_L25P_0 | C15 | I/O |
| 0 | IO_L26N_0 | IO_L26N_0 | B15 | I/O |
| 0 | IO_L26P_0/VREF_0 | IO_L26P_0/VREF_0 | A15 | VREF |
| 0 | IO_L27N_0 | IO_L27N_0 | G16 | I/O |
| 0 | IO_L27P_0 | IO_L27P_0 | F16 | I/O |
| 0 | IO_L28N_0 | IO_L28N_0 | C16 | I/O |
| 0 | IO_L28P_0 | IO_L28P_0 | B16 | I/O |
| 0 | IO_L29N_0 | IO_L29N_0 | J17 | I/O |
| 0 | IO_L29P_0 | IO_L29P_0 | H17 | I/O |
| 0 | IO_L30N_0 | IO_L30N_0 | G17 | I/O |
| 0 | IO_L30P_0 | IO_L30P_0 | F17 | I/O |
| 0 | IO_L31N_0 | IO_L31N_0 | D17 | I/O |
| 0 | IO_L31P_0/VREF_0 | IO_L31P_0/VREF_0 | C17 | VREF |
| 0 | IO_L32N_0/GCLK7 | IO_L32N_0/GCLK7 | B17 | GCLK |
| 0 | IO_L32P_0/GCLK6 | IO_L32P_0/GCLK6 | A17 | GCLK |
| 0 | N.C. (◆) | IO_L33N_0 | D7 | I/O |
| 0 | N.C. (◆) | IO_L33P_0 | C7 | I/O |
| 0 | N.C. (◆) | IO_L34N_0 | B7 | I/O |
| 0 | N.C. (◆) | IO_L34P_0 | A7 | I/O |
| 0 | IO_L35N_0 | IO_L35N_0 | E8 | I/O |
| 0 | IO_L35P_0 | IO_L35P_0 | D8 | I/O |
| 0 | IO_L36N_0 | IO_L36N_0 | B8 | I/O |
| 0 | IO_L36P_0 | IO_L36P_0 | A8 | I/O |
| 0 | IO_L37N_0 | IO_L37N_0 | D10 | I/O |
| 0 | IO_L37P_0 | IO_L37P_0 | C10 | I/O |
| 0 | IO_L38N_0 | IO_L38N_0 | B10 | I/O |
| 0 | IO_L38P_0 | IO_L38P_0 | A10 | I/O |
| 0 | N.C. (◆) | IO_L39N_0 | G11 | I/O |
| 0 | N.C. (◆) | IO_L39P_0 | F11 | I/O |
| 0 | N.C. (◆) | IO_L40N_0 | B11 | I/O |
| 0 | N.C. (◆) | IO_L40P_0 | A11 | I/O |
| 0 | VCCO_0 | VCCO_0 | B13 | VCCO |
| 0 | VCCO_0 | VCCO_0 | C4 | VCCO |
| 0 | VCCO_0 | VCCO_0 | C8 | VCCO |
| 0 | VCCO_0 | VCCO_0 | D11 | VCCO |
| 0 | VCCO_0 | VCCO_0 | D16 | VCCO |

*Table 110:* **FG1156 Package Pinout** ***(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| 5 | IO_L04P_5 | IO_L04P_5 | AL6 | I/O |
| 5 | IO_L05N_5 | IO_L05N_5 | AP6 | I/O |
| 5 | IO_L05P_5 | IO_L05P_5 | AN6 | I/O |
| 5 | IO_L06N_5 | IO_L06N_5 | AK7 | I/O |
| 5 | IO_L06P_5 | IO_L06P_5 | AJ7 | I/O |
| 5 | IO_L07N_5 | IO_L07N_5 | AG10 | I/O |
| 5 | IO_L07P_5 | IO_L07P_5 | AF10 | I/O |
| 5 | IO_L08N_5 | IO_L08N_5 | AJ10 | I/O |
| 5 | IO_L08P_5 | IO_L08P_5 | AH10 | I/O |
| 5 | IO_L09N_5 | IO_L09N_5 | AM10 | I/O |
| 5 | IO_L09P_5 | IO_L09P_5 | AL10 | I/O |
| 5 | IO_L10N_5/VRP_5 | IO_L10N_5/VRP_5 | AP10 | DCI |
| 5 | IO_L10P_5/VRN_5 | IO_L10P_5/VRN_5 | AN10 | DCI |
| 5 | IO_L11N_5/VREF_5 | IO_L11N_5/VREF_5 | AP11 | VREF |
| 5 | IO_L11P_5 | IO_L11P_5 | AN11 | I/O |
| 5 | IO_L12N_5 | IO_L12N_5 | AF12 | I/O |
| 5 | IO_L12P_5 | IO_L12P_5 | AE12 | I/O |
| 5 | IO_L13N_5 | IO_L13N_5 | AJ12 | I/O |
| 5 | IO_L13P_5 | IO_L13P_5 | AH12 | I/O |
| 5 | IO_L14N_5 | IO_L14N_5 | AL12 | I/O |
| 5 | IO_L14P_5 | IO_L14P_5 | AK12 | I/O |
| 5 | IO_L15N_5 | IO_L15N_5 | AP12 | I/O |
| 5 | IO_L15P_5 | IO_L15P_5 | AN12 | I/O |
| 5 | IO_L16N_5 | IO_L16N_5 | AE13 | I/O |
| 5 | IO_L16P_5 | IO_L16P_5 | AD13 | I/O |
| 5 | IO_L17N_5 | IO_L17N_5 | AH13 | I/O |
| 5 | IO_L17P_5 | IO_L17P_5 | AG13 | I/O |
| 5 | IO_L18N_5 | IO_L18N_5 | AM13 | I/O |
| 5 | IO_L18P_5 | IO_L18P_5 | AL13 | I/O |
| 5 | IO_L19N_5 | IO_L19N_5 | AG14 | I/O |
| 5 | IO_L19P_5/VREF_5 | IO_L19P_5/VREF_5 | AF14 | VREF |
| 5 | IO_L20N_5 | IO_L20N_5 | AJ14 | I/O |
| 5 | IO_L20P_5 | IO_L20P_5 | AH14 | I/O |
| 5 | IO_L21N_5 | IO_L21N_5 | AM14 | I/O |
| 5 | IO_L21P_5 | IO_L21P_5 | AL14 | I/O |
| 5 | IO_L22N_5 | IO_L22N_5 | AP14 | I/O |
| 5 | IO_L22P_5 | IO_L22P_5 | AN14 | I/O |
| 5 | IO_L23N_5 | IO_L23N_5 | AF15 | I/O |
| 5 | IO_L23P_5 | IO_L23P_5 | AE15 | I/O |
| 5 | IO_L24N_5 | IO_L24N_5 | AJ15 | I/O |

## FG1156 Footprint

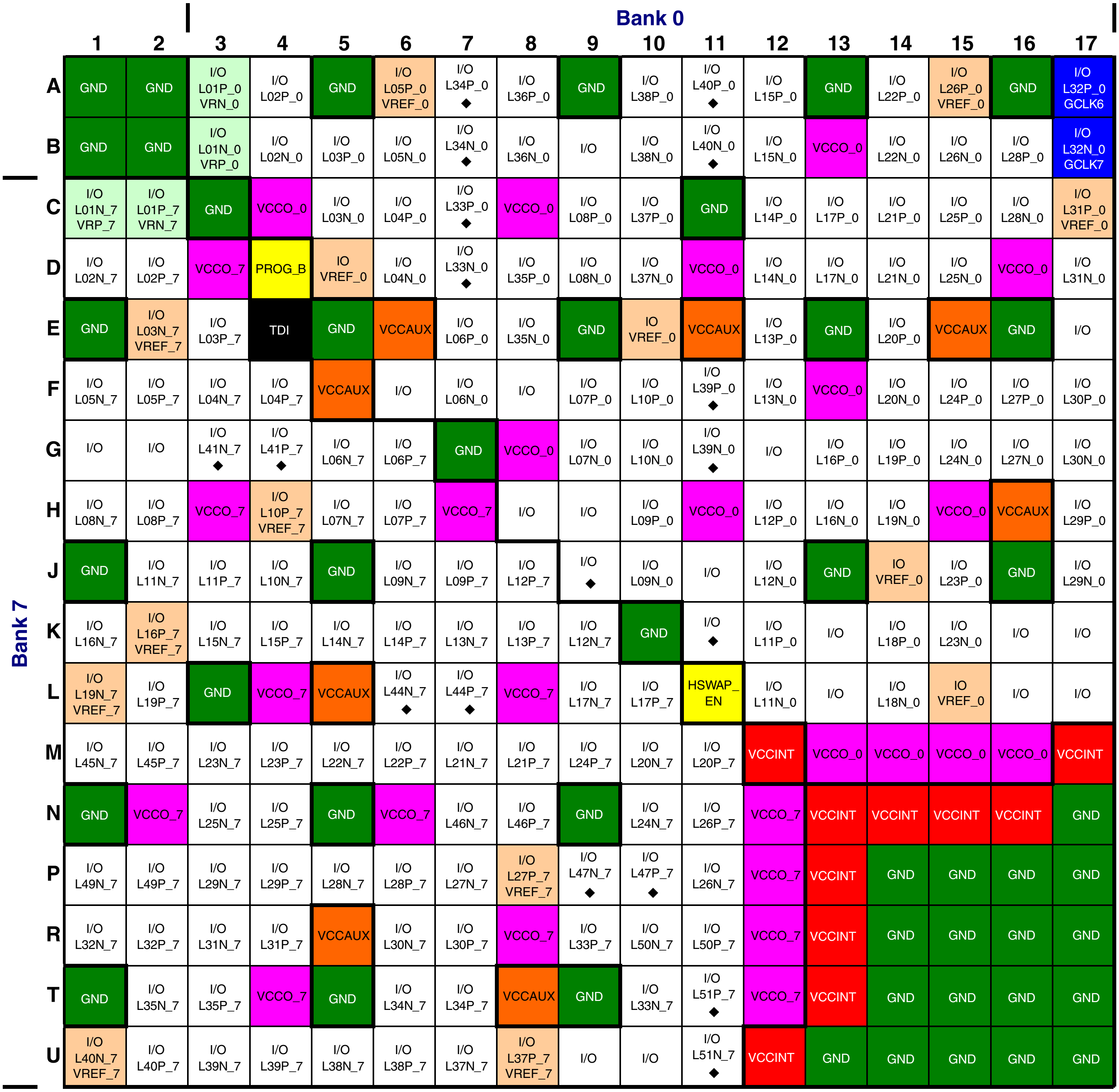
### *Top Left Corner of FG1156 Package (Top View)*

**XC3S4000**
**(712 max. user I/O)**

| | | | | | |
|---|---|---|---|---|---|
| 621 | **I/O:** Unrestricted, general-purpose user I/O | 55 | **VREF:** User I/O or input voltage reference for bank | 73 | **N.C.:** Unconnected pins for XC3S4000 (◆) |

**XC3S5000**
**(784 max. user I/O)**

| | | | | | |
|---|---|---|---|---|---|
| 692 | **I/O:** Unrestricted, general-purpose user I/O | 56 | **VREF:** User I/O or input voltage reference for bank | 1 | **N.C.:** Unconnected pins for XC3S5000 (■) |



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | GND | I/O L01P_0 VRN_0 | I/O L02P_0 | GND | I/O L05P_0 VREF_0 | I/O L34P_0 ◆ | I/O L36P_0 | GND | I/O L38P_0 | I/O L40P_0 ◆ | I/O L15P_0 | GND | I/O L22P_0 | I/O L26P_0 VREF_0 | GND | I/O L32P_0 GCLK6 |
| B | GND | GND | I/O L01N_0 VRP_0 | I/O L02N_0 | I/O L03P_0 | I/O L05N_0 | I/O L34N_0 ◆ | I/O L36N_0 | I/O | I/O L38N_0 | I/O L40N_0 ◆ | I/O L15N_0 | VCCO_0 | I/O L22N_0 | I/O L26N_0 | I/O L28P_0 | I/O L32N_0 GCLK7 |
| C | I/O L01N_7 VRP_7 | I/O L01P_7 VRN_7 | GND | VCCO_0 | I/O L03N_0 | I/O L04P_0 | I/O L33P_0 ◆ | VCCO_0 | I/O L08P_0 | I/O L37P_0 | GND | I/O L14P_0 | I/O L17P_0 | I/O L21P_0 | I/O L25P_0 | I/O L28N_0 | I/O L31P_0 VREF_0 |
| D | I/O L02N_7 | I/O L02P_7 | VCCO_7 | PROG_B | IO VREF_0 | I/O L04N_0 | I/O L33N_0 ◆ | I/O L35P_0 | I/O L08N_0 | I/O L37N_0 | VCCO_0 | I/O L14N_0 | I/O L17N_0 | I/O L21N_0 | I/O L25N_0 | VCCO_0 | I/O L31N_0 |
| E | GND | I/O L03N_7 VREF_7 | I/O L03P_7 | TDI | GND | VCCAUX | I/O L06P_0 | I/O L35N_0 | GND | IO VREF_0 | VCCAUX | I/O L13P_0 | GND | I/O L20P_0 | VCCAUX | GND | I/O |
| F | I/O L05N_7 | I/O L05P_7 | I/O L04N_7 | I/O L04P_7 | VCCAUX | I/O | I/O L06N_0 | I/O | I/O L07P_0 | I/O L10P_0 | I/O L39P_0 ◆ | I/O L13N_0 | VCCO_0 | I/O L20N_0 | I/O L24P_0 | I/O L27P_0 | I/O L30P_0 |
| G | I/O | I/O | I/O L41N_7 ◆ | I/O L41P_7 ◆ | I/O L06N_7 | I/O L06P_7 | GND | VCCO_0 | I/O L07N_0 | I/O L10N_0 | I/O L39N_0 ◆ | I/O | I/O L16P_0 | I/O L19P_0 | I/O L24N_0 | I/O L27N_0 | I/O L30N_0 |
| H | I/O L08N_7 | I/O L08P_7 | VCCO_7 | I/O L10P_7 VREF_7 | I/O L07N_7 | I/O L07P_7 | VCCO_7 | I/O | I/O | I/O L09P_0 | VCCO_0 | I/O L12P_0 | I/O L16N_0 | I/O L19N_0 | VCCO_0 | VCCAUX | I/O L29P_0 |
| J | GND | I/O L11N_7 | I/O L11P_7 | I/O L10N_7 | GND | I/O L09N_7 | I/O L09P_7 | I/O L12P_7 | I/O ◆ | I/O L09N_0 | I/O | I/O L12N_0 | GND | IO VREF_0 | I/O L23P_0 | GND | I/O L29N_0 |
| K | I/O L16N_7 | I/O L16P_7 VREF_7 | I/O L15N_7 | I/O L15P_7 | I/O L14N_7 | I/O L14P_7 | I/O L13N_7 | I/O L13P_7 | I/O L12N_7 | GND | I/O ◆ | I/O L11P_0 | I/O | I/O L18P_0 | I/O L23N_0 | I/O | I/O |
| L | I/O L19N_7 VREF_7 | I/O L19P_7 | GND | VCCO_7 | VCCAUX | I/O L44N_7 ◆ | I/O L44P_7 ◆ | VCCO_7 | I/O L17N_7 | I/O L17P_7 | HSWAP_EN | I/O L11N_0 | I/O | I/O L18N_0 | IO VREF_0 | I/O | I/O |
| M | I/O L45N_7 | I/O L45P_7 | I/O L23N_7 | I/O L23P_7 | I/O L22N_7 | I/O L22P_7 | I/O L21N_7 | I/O L21P_7 | I/O L24P_7 | I/O L20N_7 | I/O L20P_7 | VCCINT | VCCO_0 | VCCO_0 | VCCO_0 | VCCO_0 | VCCINT |
| N | GND | VCCO_7 | I/O L25N_7 | I/O L25P_7 | GND | VCCO_7 | I/O L46N_7 | I/O L46P_7 | GND | I/O L24N_7 | I/O L26P_7 | VCCO_7 | VCCINT | VCCINT | VCCINT | VCCINT | GND |
| P | I/O L49N_7 | I/O L49P_7 | I/O L29N_7 | I/O L29P_7 | I/O L28N_7 | I/O L28P_7 | I/O L27N_7 | I/O L27P_7 VREF_7 | I/O L47N_7 ◆ | I/O L47P_7 ◆ | I/O L26N_7 | VCCO_7 | VCCINT | GND | GND | GND | GND |
| R | I/O L32N_7 | I/O L32P_7 | I/O L31N_7 | I/O L31P_7 | VCCAUX | I/O L30N_7 | I/O L30P_7 | VCCO_7 | I/O L33P_7 | I/O L50N_7 | I/O L50P_7 | VCCO_7 | VCCINT | GND | GND | GND | GND |
| T | GND | I/O L35N_7 | I/O L35P_7 | VCCO_7 | GND | I/O L34N_7 | I/O L34P_7 | VCCAUX | GND | I/O L33N_7 | I/O L51P_7 ◆ | VCCO_7 | VCCINT | GND | GND | GND | GND |
| U | I/O L40N_7 VREF_7 | I/O L40P_7 | I/O L39N_7 | I/O L39P_7 | I/O L38N_7 | I/O L38P_7 | I/O L37N_7 | I/O L37P_7 VREF_7 | I/O | I/O | I/O L51N_7 ◆ | VCCINT | GND | GND | GND | GND | GND |

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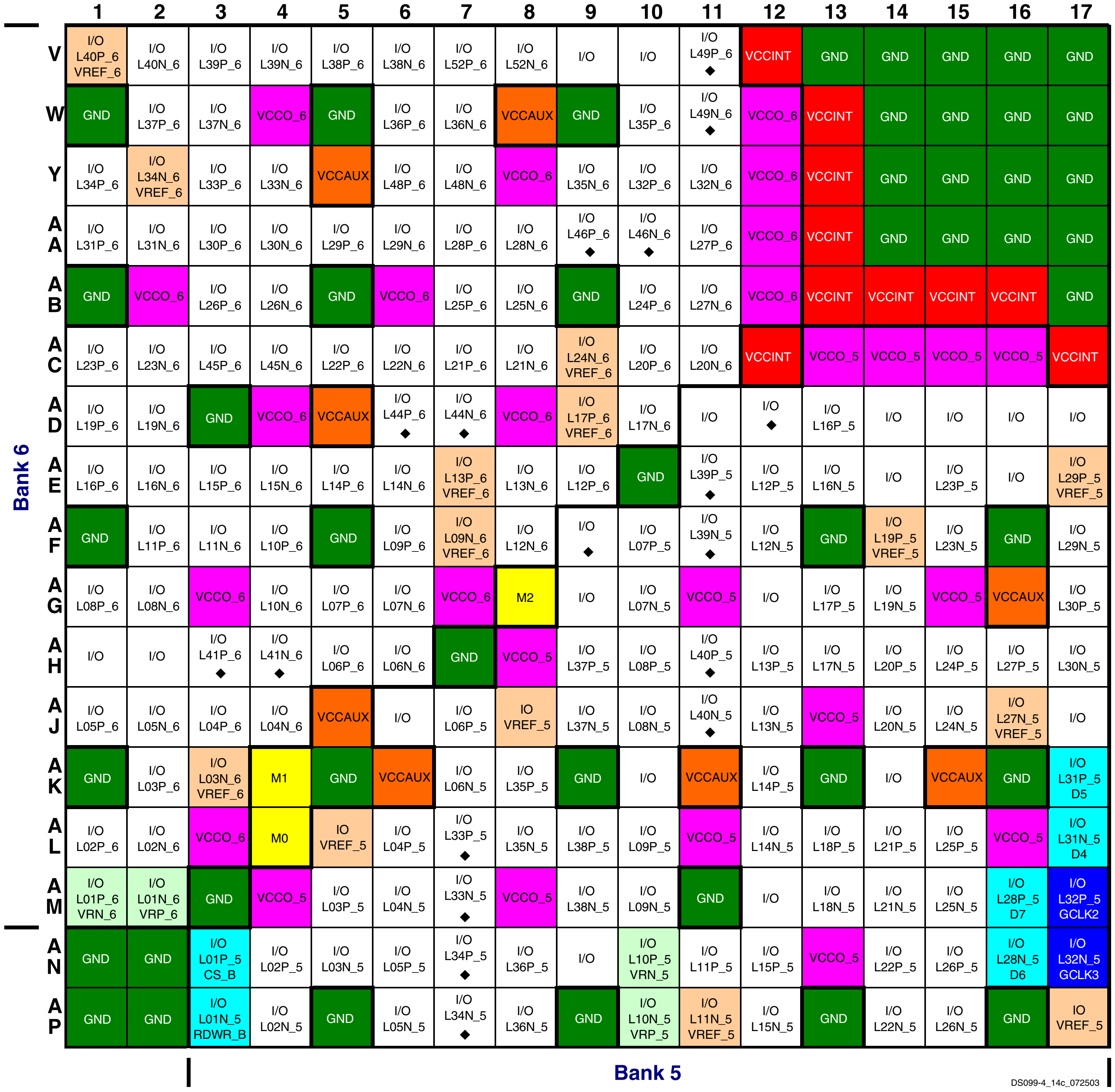
*Figure 57:* **FG1156 Package Footprint (Top View)**



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| V | I/O L40P_6 VREF_6 | I/O L40N_6 | I/O L39P_6 | I/O L39N_6 | I/O L38P_6 | I/O L38N_6 | I/O L52P_6 | I/O L52N_6 | I/O | I/O | I/O L49P_6 ◆ | VCCINT | GND | GND | GND | GND | GND |
| W | GND | I/O L37P_6 | I/O L37N_6 | VCCO_6 | GND | I/O L36P_6 | I/O L36N_6 | VCCAUX | GND | I/O L35P_6 | I/O L49N_6 ◆ | VCCO_6 | VCCINT | GND | GND | GND | GND |
| Y | I/O L34P_6 | I/O L34N_6 VREF_6 | I/O L33P_6 | I/O L33N_6 | VCCAUX | I/O L48P_6 | I/O L48N_6 | VCCO_6 | I/O L35N_6 | I/O L32P_6 | I/O L32N_6 | VCCO_6 | VCCINT | GND | GND | GND | GND |
| AA | I/O L31P_6 | I/O L31N_6 | I/O L30P_6 | I/O L30N_6 | I/O L29P_6 | I/O L29N_6 | I/O L28P_6 | I/O L28N_6 | I/O L46P_6 ◆ | I/O L46N_6 ◆ | I/O L27P_6 | VCCO_6 | VCCINT | GND | GND | GND | GND |
| AB | GND | VCCO_6 | I/O L26P_6 | I/O L26N_6 | GND | VCCO_6 | I/O L25P_6 | I/O L25N_6 | GND | I/O L24P_6 | I/O L27N_6 | VCCO_6 | VCCINT | VCCINT | VCCINT | VCCINT | GND |
| AC | I/O L23P_6 | I/O L23N_6 | I/O L45P_6 | I/O L45N_6 | I/O L22P_6 | I/O L22N_6 | I/O L21P_6 | I/O L21N_6 | I/O L24N_6 VREF_6 | I/O L20P_6 | I/O L20N_6 | VCCINT | VCCO_5 | VCCO_5 | VCCO_5 | VCCO_5 | VCCINT |
| AD | I/O L19P_6 | I/O L19N_6 | GND | VCCO_6 | VCCAUX | I/O L44P_6 ◆ | I/O L44N_6 ◆ | VCCO_6 | I/O L17P_6 VREF_6 | I/O L17N_6 | I/O | I/O ◆ | I/O L16P_5 | I/O | I/O | I/O | I/O |
| AE | I/O L16P_6 | I/O L16N_6 | I/O L15P_6 | I/O L15N_6 | I/O L14P_6 | I/O L14N_6 | I/O L13P_6 VREF_6 | I/O L13N_6 | I/O L12P_6 | GND | I/O L39P_5 ◆ | I/O L12P_5 | I/O L16N_5 | I/O | I/O L23P_5 | I/O | I/O L29P_5 VREF_5 |
| AF | GND | I/O L11P_6 | I/O L11N_6 | I/O L10P_6 | GND | I/O L09P_6 | I/O L09N_6 VREF_6 | I/O L12N_6 | I/O ◆ | I/O L07P_5 | I/O L39N_5 ◆ | I/O L12N_5 | GND | I/O L19P_5 VREF_5 | I/O L23N_5 | GND | I/O L29N_5 |
| AG | I/O L08P_6 | I/O L08N_6 | VCCO_6 | I/O L10N_6 | I/O L07P_6 | I/O L07N_6 | VCCO_6 | M2 | I/O | I/O L07N_5 | VCCO_5 | I/O | I/O L17P_5 | I/O L19N_5 | VCCO_5 | VCCAUX | I/O L30P_5 |
| AH | I/O | I/O | I/O L41P_6 ◆ | I/O L41N_6 ◆ | I/O L06P_6 | I/O L06N_6 | GND | VCCO_5 | I/O L37P_5 | I/O L08P_5 | I/O L40P_5 ◆ | I/O L13P_5 | I/O L17N_5 | I/O L20P_5 | I/O L24P_5 | I/O L27P_5 | I/O L30N_5 |
| AJ | I/O L05P_6 | I/O L05N_6 | I/O L04P_6 | I/O L04N_6 | VCCAUX | I/O | I/O L06P_5 | IO VREF_5 | I/O L37N_5 | I/O L08N_5 | I/O L40N_5 ◆ | I/O L13N_5 | VCCO_5 | I/O L20N_5 | I/O L24N_5 | I/O L27N_5 VREF_5 | I/O |
| AK | GND | I/O L03P_6 | I/O L03N_6 VREF_6 | M1 | GND | VCCAUX | I/O L06N_5 | I/O L35P_5 | GND | I/O | VCCAUX | I/O L14P_5 | GND | I/O | VCCAUX | GND | I/O L31P_5 D5 |
| AL | I/O L02P_6 | I/O L02N_6 | VCCO_6 | M0 | IO VREF_5 | I/O L04P_5 | I/O L33P_5 ◆ | I/O L35N_5 | I/O L38P_5 | I/O L09P_5 | VCCO_5 | I/O L14N_5 | I/O L18P_5 | I/O L21P_5 | I/O L25P_5 | VCCO_5 | I/O L31N_5 D4 |
| AM | I/O L01P_6 VRN_6 | I/O L01N_6 VRP_6 | GND | VCCO_5 | I/O L03P_5 | I/O L04N_5 | I/O L33N_5 ◆ | VCCO_5 | I/O L38N_5 | I/O L09N_5 | GND | I/O | I/O L18N_5 | I/O L21N_5 | I/O L25N_5 | I/O L28P_5 D7 | I/O L32P_5 GCLK2 |
| AN | GND | GND | I/O L01P_5 CS_B | I/O L02P_5 | I/O L03N_5 | I/O L05P_5 | I/O L34P_5 ◆ | I/O L36P_5 | I/O | I/O L10P_5 VRN_5 | I/O L11P_5 | I/O L15P_5 | VCCO_5 | I/O L22P_5 | I/O L26P_5 | I/O L28N_5 D6 | I/O L32N_5 GCLK3 |
| AP | GND | GND | I/O L01N_5 RDWR_B | I/O L02N_5 | GND | I/O L05N_5 | I/O L34N_5 ◆ | I/O L36N_5 | GND | I/O L10N_5 VRP_5 | I/O L11N_5 VREF_5 | I/O L15N_5 | GND | I/O L22N_5 | I/O L26N_5 | GND | IO VREF_5 |

***Bottom Left Corner of FG1156 Package (Top View)***

Figure 59: FG1156 Package Footprint (Top View) Continued