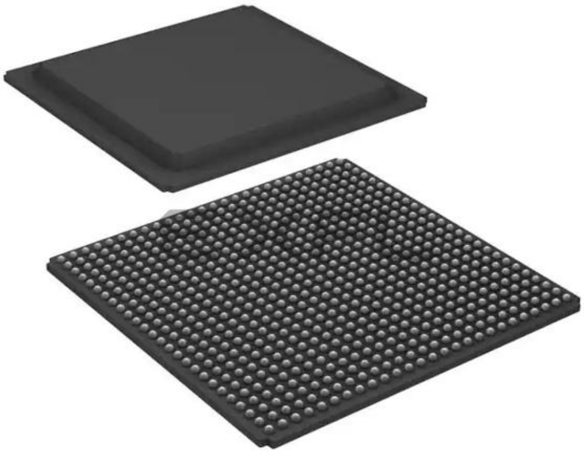

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

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Details	
Product Status	Active
Number of LABs/CLBs	1920
Number of Logic Elements/Cells	17280
Total RAM Bits	442368
Number of I/O	391
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1000-5fg676c

IOBs

For additional information, refer to the chapter entitled "Using I/O Resources" in UG331: *Spartan-3 Generation FPGA User Guide*.

IOB Overview

The Input/Output Block (IOB) provides a programmable, bidirectional interface between an I/O pin and the FPGA's internal logic.

A simplified diagram of the IOB's internal structure appears in Figure 7. There are three main signal paths within the IOB: the output path, input path, and 3-state path. Each path has its own pair of storage elements that can act as either registers or latches. For more information, see the Storage Element Functions section. The three main signal paths are as follows:

- The input path carries data from the pad, which is bonded to a package pin, through an optional programmable delay element directly to the I line. There are alternate routes through a pair of storage elements to the IQ1 and IQ2 lines. The IOB outputs I, IQ1, and IQ2 all lead to the FPGA's internal logic. The delay element can be set to ensure a hold time of zero.
- The output path, starting with the O1 and O2 lines, carries data from the FPGA's internal logic through a multiplexer and then a three-state driver to the IOB pad. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.
- The 3-state path determines when the output driver is high impedance. The T1 and T2 lines carry data from the FPGA's internal logic through a multiplexer to the output driver. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements. When the T1 or T2 lines are asserted High, the output driver is high-impedance (floating, hi-Z). The output driver is active-Low enabled.
- All signal paths entering the IOB, including those associated with the storage elements, have an inverter option. Any inverter placed on these paths is automatically absorbed into the IOB.

Storage Element Functions

There are three pairs of storage elements in each IOB, one pair for each of the three paths. It is possible to configure each of these storage elements as an edge-triggered D-type flip-flop (FD) or a level-sensitive latch (LD).

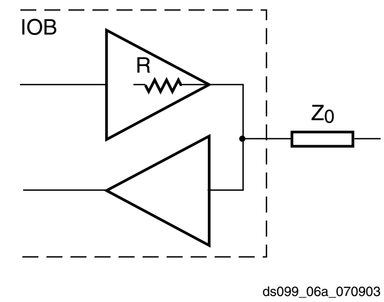
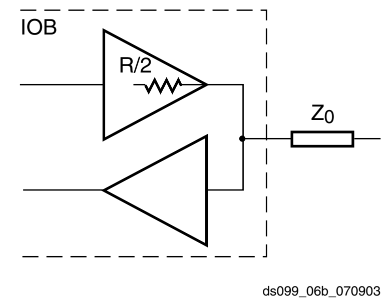
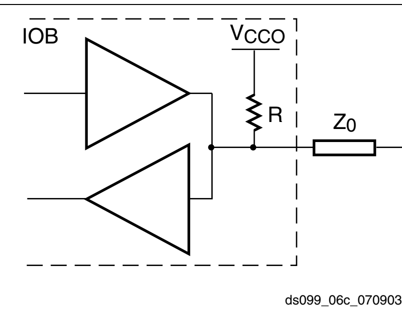
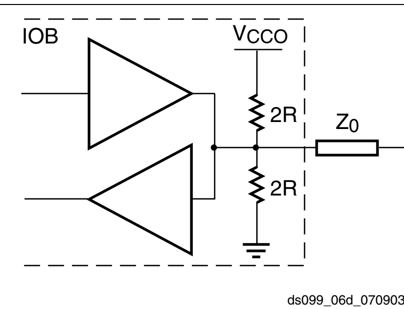
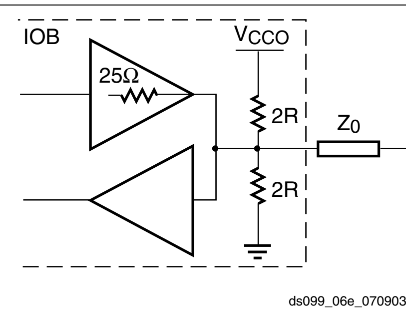
The storage-element-pair on either the Output path or the Three-State path can be used together with a special multiplexer to produce Double-Data-Rate (DDR) transmission. This is accomplished by taking data synchronized to the clock signal's rising edge and converting them to bits synchronized on both the rising and the falling edge. The combination of two registers and a multiplexer is referred to as a Double-Data-Rate D-type flip-flop (FDDR). See Double-Data-Rate Transmission, page 12 for more information.

The signal paths associated with the storage element are described in Table 5.

Table 5: **Storage Element Signal Description**

Storage Element Signal	Description	Function
D	Data input	Data at this input is stored on the active edge of CK enabled by CE. For latch operation when the input is enabled, data passes directly to the output Q.
Q	Data output	The data on this output reflects the state of the storage element. For operation as a latch in transparent mode, Q will mirror the data at D.
CK	Clock input	A signal's active edge on this input with CE asserted, loads data into the storage element.
CE	Clock Enable input	When asserted, this input enables CK. If not connected, CE defaults to the asserted state.
SR	Set/Reset	Forces storage element into the state specified by the SRHIGH/SRLOW attributes. The SYNC/ASYNC attribute setting determines if the SR input is synchronized to the clock or not.
REV	Reverse	Used together with SR. Forces storage element into the state opposite from what SR does.

Table 11: **DCI Terminations**

Termination	Schematic[(1)]	Signal Standards (IOSTANDARD)
Controlled impedance output driver		LVDCI_15 LVDCI_18 LVDCI_25 LVDCI_33 HSLVDCI_15 HSLVDCI_18 HSLVDCI_25 HSLVDCI_33
Controlled output driver with half impedance		LVDCI_DV2_15 LVDCI_DV2_18 LVDCI_DV2_25 LVDCI_DV2_33
Single resistor		GTL_DCI GTLP_DCI HSTL_III_DCI[(2)] HSTL_III_DCI_18[(2)]
Split resistors		HSTL_I_DCI[(2)] HSTL_I_DCI_18[(2)] HSTL_II_DCI_18 DIFF_HSTL_II_18_DCI DIFF_SSTL2_II_DCI LVDS_25_DCI LVDSEXT_25_DCI
Split resistors with output driver impedance fixed to 25Ω		SSTL18_I_DCI[(3)] SSTL2_I_DCI[(3)] SSTL2_II_DCI

Notes:

1. The value of R is equivalent to the characteristic impedance of the line connected to the I/O. It is also equal to half the value of RREF for the DV2 standards and RREF for all other DCI standards.
2. For DCI using HSTL Classes I and III, terminations only go into effect at inputs (not at outputs).
3. For DCI using SSTL Class I, the split termination only goes into effect at inputs (not at outputs).

Table 13: **Block RAM Port Signals *(Cont'd)***

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Data Output Bus	DOA	DOB	Output	Basic data access occurs whenever WE is inactive. The DO outputs mirror the data stored in the addressed memory location. Data access with WE asserted is also possible if one of the following two attributes is chosen: WRITE_FIRST and READ_FIRST. WRITE_FIRST simultaneously presents the new input data on the DO output port and writes the data to the address RAM location. READ_FIRST presents the previously stored RAM data on the DO output port while writing new data to RAM. A third attribute, NO_CHANGE, latches the DO outputs upon the assertion of WE. It is possible to configure a port's total data path width (w) to be 1, 2, 4, 9, 18, or 36 bits. This selection applies to both the DI and DO paths. See the DI signal description.
Parity Data Output(s)	DOPA	DOPB	Output	Parity inputs represent additional bits included in the data input path to support error detection. The number of parity bits "p" included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 14.
Write Enable	WEA	WEB	Input	When asserted together with EN, this input enables the writing of data to the RAM. In this case, the data access attributes WRITE_FIRST, READ_FIRST or NO_CHANGE determines if and how data is updated on the DO outputs. See the DO signal description. When WE is inactive with EN asserted, read operations are still possible. In this case, a transparent latch passes data from the addressed memory location to the DO outputs.
Clock Enable	ENA	ENB	Input	When asserted, this input enables the CLK signal to synchronize Block RAM functions as follows: the writing of data to the DI inputs (when WE is also asserted), the updating of data at the DO outputs as well as the setting/resetting of the DO output latches. When de-asserted, the above functions are disabled.
Set/Reset	SSRA	SSRB	Input	When asserted, this pin forces the DO output latch to the value that the SRVAL attribute is set to. A Set/Reset operation on one port has no effect on the other ports functioning, nor does it disturb the memory's data contents. It is synchronized to the CLK signal.
Clock	CLKA	CLKB	Input	This input accepts the clock signal to which read and write operations are synchronized. All associated port inputs are required to meet setup times with respect to the clock signal's active edge. The data output bus responds after a clock-to-out delay referenced to the clock signal's active edge.

Port Aspect Ratios

On a given port, it is possible to select a number of different possible widths ($w - p$) for the DI/DO buses as shown in Table 14. These two buses always have the same width. This data bus width selection is independent for each port. If the data bus width of Port A differs from that of Port B, the Block RAM automatically performs a bus-matching function. When data are written to a port with a narrow bus, then read from a port with a wide bus, the latter port will effectively combine "narrow" words to form "wide" words. Similarly, when data are written into a port with a wide bus, then read from a port with a narrow bus, the latter port will divide "wide" words to form "narrow" words. When the data bus width is eight bits or greater, extra parity bits become available. The width of the total data path (w) is the sum of the DI/DO bus width and any parity bits (p).

The width selection made for the DI/DO bus determines the number of address lines according to the relationship expressed below:

$$r = 14 - [\log(w-p)/\log(2)] \qquad \textit{Equation 1}$$

In turn, the number of address lines delimits the total number (n) of addressable locations or depth according to the following equation:

$$n = 2^r \qquad \textit{Equation 2}$$

The product of w and n yields the total block RAM capacity. Equation 1 and Equation 2 show that as the data bus width increases, the number of address lines along with the number of addressable memory locations decreases. Using the permissible DI/DO bus widths as inputs to these equations provides the bus width and memory capacity measures shown in Table 14.

Table 14: **Port Aspect Ratios for Port A or B**

DI/DO Bus Width (w – p Bits)	DIP/DOP Bus Width (p Bits)	Total Data Path Width (w Bits)	ADDR Bus Width (r Bits)	No. of Addressable Locations (n)	Block RAM Capacity (Bits)
1	0	1	14	16,384	16,384
2	0	2	13	8,192	16,384
4	0	4	12	4,096	16,384
8	1	9	11	2,048	18,432
16	2	18	10	1,024	18,432
32	4	36	9	512	18,432

Block RAM Data Operations

Writing data to and accessing data from the block RAM are synchronous operations that take place independently on each of the two ports.

The waveforms for the write operation are shown in the top half of the Figure 15, Figure 16, and Figure 17. When the WE and EN signals enable the active edge of CLK, data at the DI input bus is written to the block RAM location addressed by the ADDR lines.

There are a number of different conditions under which data can be accessed at the DO outputs. Basic data access always occurs when the WE input is inactive. Under this condition, data stored in the memory location addressed by the ADDR lines passes through a transparent output latch to the DO outputs. The timing for basic data access is shown in the portions of Figure 15, Figure 16, and Figure 17 during which WE is Low.

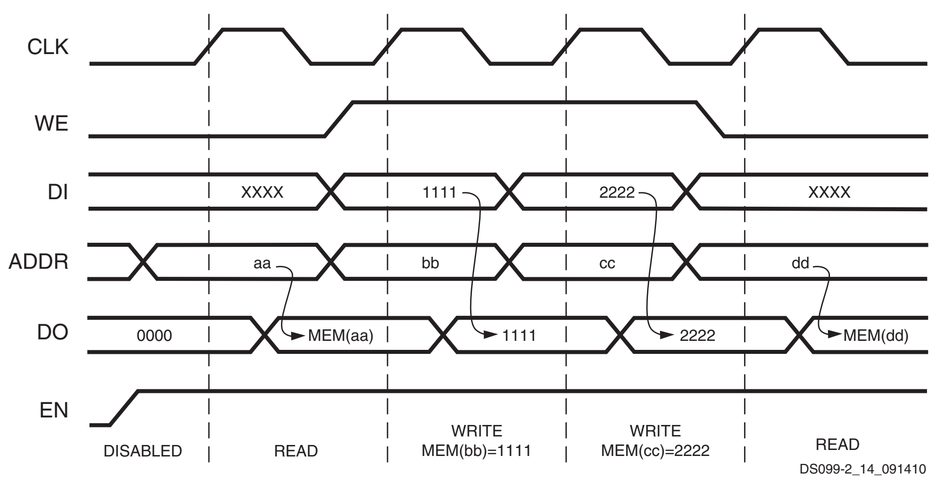


Figure 15: **Waveforms of Block RAM Data Operations with WRITE_FIRST Selected**

Data can also be accessed on the DO outputs when asserting the WE input. This is accomplished using two different attributes:

Choosing the WRITE_FIRST attribute, data is written to the addressed memory location on an enabled active CLK edge and is also passed to the DO outputs. WRITE_FIRST timing is shown in the portion of Figure 15 during which WE is High.

Choosing the READ_FIRST attribute, data already stored in the addressed location pass to the DO outputs before that location is overwritten with new data from the DI inputs on an enabled active CLK edge. READ_FIRST timing is shown in the portion of Figure 16 during which WE is High.

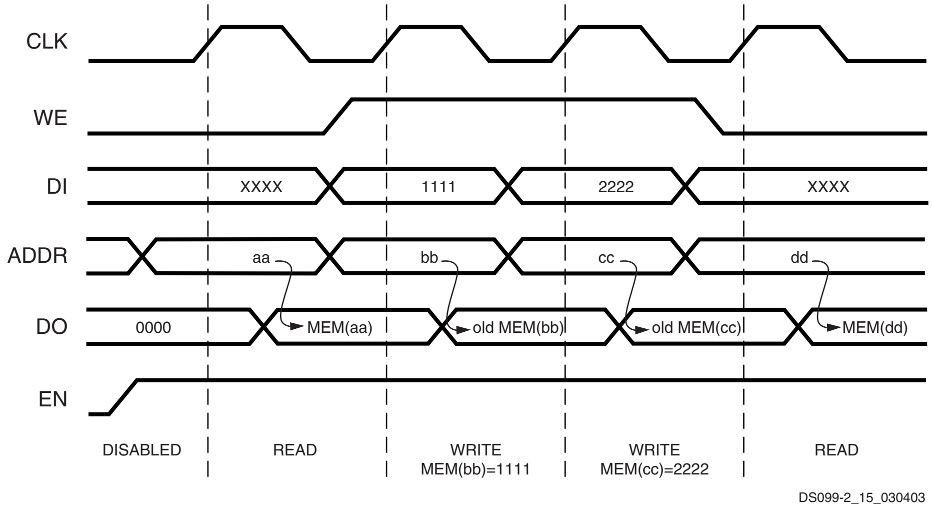


Figure 16: **Waveforms of Block RAM Data Operations with READ_FIRST Selected**

Choosing a third attribute called NO_CHANGE puts the DO outputs in a latched state when asserting WE. Under this condition, the DO outputs will retain the data driven just before WE was asserted. NO_CHANGE timing is shown in the portion of Figure 17 during which WE is High.

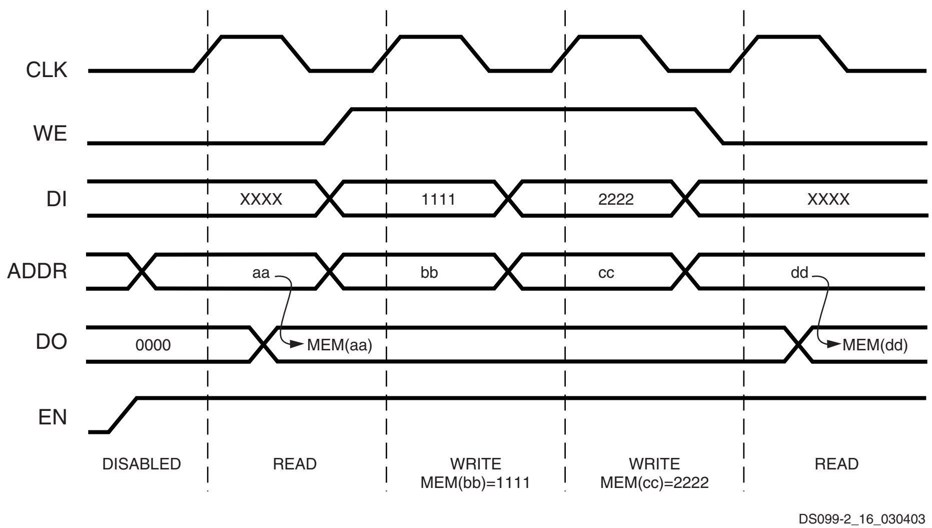


Figure 17: **Waveforms of Block RAM Data Operations with NO_CHANGE Selected**

Dedicated Multipliers

All Spartan-3 devices provide embedded multipliers that accept two 18-bit words as inputs to produce a 36-bit product. This section provides an introduction to multipliers. For further details, refer to the chapter entitled “Using Embedded Multipliers” in UG331.

The input buses to the multiplier accept data in two’s-complement form (either 18-bit signed or 17-bit unsigned). One such multiplier is matched to each block RAM on the die. The close physical proximity of the two ensures efficient data handling. Cascading multipliers permits multiplicands more than three in number as well as wider than 18-bits. The multiplier is placed in a design using one of two primitives: an asynchronous version called MULT18X18 and a version with a register called MULT18X18S, as shown in Figure 18. The signals for these primitives are defined in Table 15.

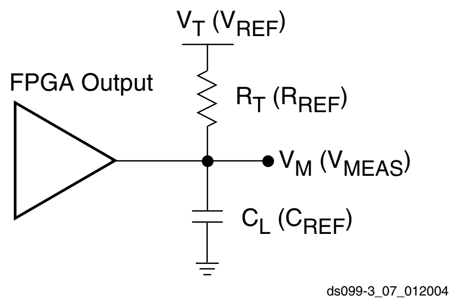
The CORE Generator system produces multipliers based on these primitives that can be configured to suit a wide range of requirements.

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 48 presents the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 35. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (e.g., LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 35: **Output Test Setup**

Table 48: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended						
GTL	0.8	V_{REF} – 0.2	V_{REF} + 0.2	25	1.2	V_{REF}
GTL_DCI				50	1.2	
GTLP	1.0	V_{REF} – 0.2	V_{REF} + 0.2	25	1.5	V_{REF}
GTLP_DCI				50	1.5	
HSLVDCI_15	0.9	V_{REF} – 0.5	V_{REF} + 0.5	1M	0	0.75
HSLVDCI_18						0.90
HSLVDCI_25						1.25
HSLVDCI_33						1.65
HSTL_I	0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_I_DCI						
HSTL_III	0.90	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_III_DCI						
HSTL_I_18	0.90	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_I_DCI_18						
HSTL_II_18	0.90	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_DCI_18						

CP132: 132-Ball Chip-Scale Package

Note: The CP132 and CPG132 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

The pinout and footprint for the XC3S50 in the 132-ball chip-scale package, CP132, appear in Table 89 and Figure 45.

All the package pins appear in Table 89 and are sorted by bank number, then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The CP132 footprint has eight I/O banks. However, the voltage supplies for the two I/O banks along an edge are connected together internally. Consequently, there are four output voltage supplies, labeled VCCO_TOP, VCCO_RIGHT, VCCO_BOTTOM, and VCCO_LEFT.

Pinout Table

Table 89: **CP132 Package Pinout**

Bank	XC3S50 Pin Name	CP132 Ball	Type
0	IO_L01N_0/VRP_0	A3	DCI
0	IO_L01P_0/VRN_0	C4	DCI
0	IO_L27N_0	C5	I/O
0	IO_L27P_0	B5	I/O
0	IO_L30N_0	B6	I/O
0	IO_L30P_0	A6	I/O
0	IO_L31N_0	C7	I/O
0	IO_L31P_0/VREF_0	B7	VREF
0	IO_L32N_0/GCLK7	A7	GCLK
0	IO_L32P_0/GCLK6	C8	GCLK
1	IO_L01N_1/VRP_1	A13	DCI
1	IO_L01P_1/VRN_1	B13	DCI
1	IO_L27N_1	C11	I/O
1	IO_L27P_1	A12	I/O
1	IO_L28N_1	A11	I/O
1	IO_L28P_1	B11	I/O
1	IO_L31N_1/VREF_1	C9	VREF
1	IO_L31P_1	A10	I/O
1	IO_L32N_1/GCLK5	A8	GCLK
1	IO_L32P_1/GCLK4	A9	GCLK
2	IO_L01N_2/VRP_2	D12	DCI
2	IO_L01P_2/VRN_2	C14	DCI
2	IO_L20N_2	E12	I/O
2	IO_L20P_2	E13	I/O
2	IO_L21N_2	E14	I/O
2	IO_L21P_2	F12	I/O
2	IO_L23N_2/VREF_2	F13	VREF
2	IO_L23P_2	F14	I/O
2	IO_L24N_2	G12	I/O

TQ144 Footprint

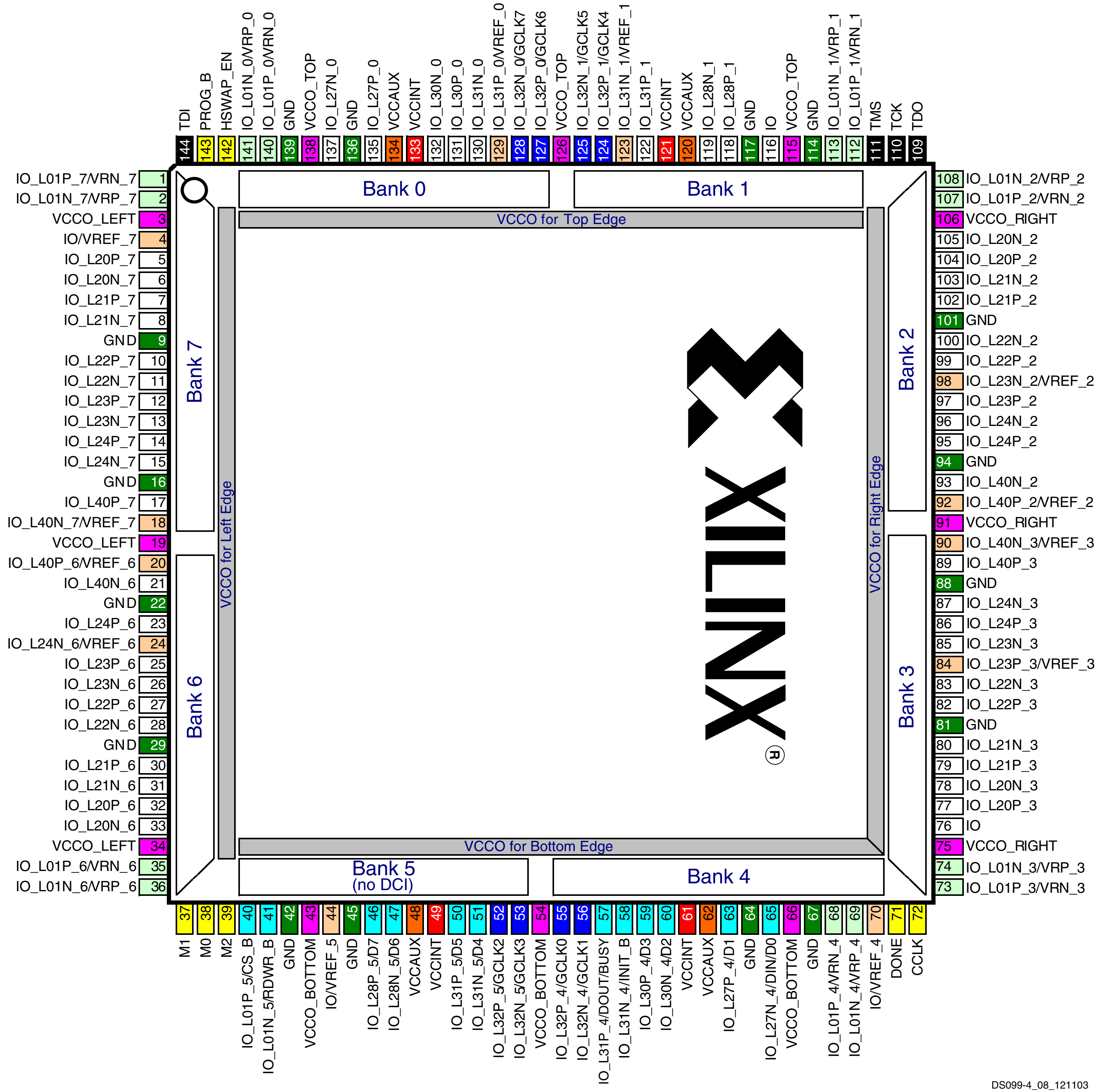


Figure 46: **TQ144 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

51	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	12	**VREF:** User I/O or input voltage reference for bank
14	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input	12	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	16	**GND:** Ground	4	**VCCAUX:** Auxiliary voltage supply (+2.5V)

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
1	IO_L10N_1/VREF_1	A13	VREF
1	IO_L10P_1	B13	I/O
1	IO_L27N_1	B12	I/O
1	IO_L27P_1	C12	I/O
1	IO_L28N_1	D11	I/O
1	IO_L28P_1	E11	I/O
1	IO_L29N_1	B11	I/O
1	IO_L29P_1	C11	I/O
1	IO_L30N_1	D10	I/O
1	IO_L30P_1	E10	I/O
1	IO_L31N_1/VREF_1	A10	VREF
1	IO_L31P_1	B10	I/O
1	IO_L32N_1/GCLK5	C9	GCLK
1	IO_L32P_1/GCLK4	D9	GCLK
1	VCCO_1	E9	VCCO
1	VCCO_1	F9	VCCO
1	VCCO_1	F10	VCCO
2	IO	G16	I/O
2	IO_L01N_2/VRP_2	B16	DCI
2	IO_L01P_2/VRN_2	C16	DCI
2	IO_L16N_2	C15	I/O
2	IO_L16P_2	D14	I/O
2	IO_L17N_2	D15	I/O
2	IO_L17P_2/VREF_2	D16	VREF
2	IO_L19N_2	E13	I/O
2	IO_L19P_2	E14	I/O
2	IO_L20N_2	E15	I/O
2	IO_L20P_2	E16	I/O
2	IO_L21N_2	F12	I/O
2	IO_L21P_2	F13	I/O
2	IO_L22N_2	F14	I/O
2	IO_L22P_2	F15	I/O
2	IO_L23N_2/VREF_2	G12	VREF
2	IO_L23P_2	G13	I/O
2	IO_L24N_2	G14	I/O
2	IO_L24P_2	G15	I/O
2	IO_L39N_2	H13	I/O
2	IO_L39P_2	H14	I/O
2	IO_L40N_2	H15	I/O
2	IO_L40P_2/VREF_2	H16	VREF

User I/Os by Bank

Table 97 indicates how the available user-I/O pins are distributed between the eight I/O banks on the FT256 package.

Table 97: **User I/Os Per Bank in FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	20	13	0	2	3	2
	1	20	13	0	2	3	2
Right	2	23	18	0	2	3	0
	3	23	18	0	2	3	0
Bottom	4	21	8	6	2	3	2
	5	20	7	6	2	3	2
Left	6	23	18	0	2	3	0
	7	23	18	0	2	3	0

FG320: 320-lead Fine-pitch Ball Grid Array

The 320-lead fine-pitch ball grid array package, FG320, supports three different Spartan-3 devices, including the XC3S400, the XC3S1000, and the XC3S1500. The footprint for all three devices is identical, as shown in Table 98 and Figure 50.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

All the package pins appear in Table 98 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 98: **FG320 Package Pinout**

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
0	IO	D9	I/O
0	IO	E7	I/O
0	IO/VREF_0	B3	VREF
0	IO/VREF_0	D6	VREF
0	IO_L01N_0/VRP_0	A2	DCI
0	IO_L01P_0/VRN_0	A3	DCI
0	IO_L09N_0	B4	I/O
0	IO_L09P_0	C4	I/O
0	IO_L10N_0	C5	I/O
0	IO_L10P_0	D5	I/O
0	IO_L15N_0	A4	I/O
0	IO_L15P_0	A5	I/O
0	IO_L25N_0	B5	I/O
0	IO_L25P_0	B6	I/O
0	IO_L27N_0	C7	I/O
0	IO_L27P_0	D7	I/O
0	IO_L28N_0	C8	I/O
0	IO_L28P_0	D8	I/O
0	IO_L29N_0	E8	I/O
0	IO_L29P_0	F8	I/O
0	IO_L30N_0	A7	I/O
0	IO_L30P_0	A8	I/O
0	IO_L31N_0	B9	I/O
0	IO_L31P_0/VREF_0	A9	VREF
0	IO_L32N_0/GCLK7	E9	GCLK
0	IO_L32P_0/GCLK6	F9	GCLK
0	VCCO_0	B8	VCCO
0	VCCO_0	C6	VCCO
0	VCCO_0	G8	VCCO

FG320 Footprint

Bank 0 (columns 2–9) | Bank 1 (columns 10–17)
Bank 7 (rows A–J, left) | Bank 6 (rows K–V, left)
Bank 2 (rows A–J, right) | Bank 3 (rows K–V, right)
Bank 5 (columns 2–9, bottom) | Bank 4 (columns 10–17, bottom)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	GND	I/O L01N_0 VRP_0	I/O L01P_0 VRN_0	I/O L15N_0	I/O L15P_0	GND	I/O L30N_0	I/O L30P_0	I/O L31P_0 VREF_0	I/O L31N_1 VREF_1	I/O	I/O VREF_1	GND	I/O L16N_1	I/O L10N_1 VREF_1	I/O L01N_1 VRP_1	I/O L01P_1 VRN_1	GND
B	I/O L16P_7 VREF_7	GND	I/O VREF_0	I/O L09N_0	I/O L25N_0	I/O L25P_0	VCCAUX	VCCO_0	I/O L31N_0	I/O L31P_1	VCCO_1	VCCAUX	I/O	I/O L16P_1	I/O L10P_1	TMS	GND	I/O L16N_2
C	I/O L16N_7	I/O L01P_7 VRN_7	I/O L01N_7 VRP_7	I/O L09P_0	I/O L10N_0	VCCO_0	I/O L27N_0	I/O L28N_0	GND	GND	I/O L30N_1	I/O L28N_1	VCCO_1	I/O L15N_1	I/O L15P_1	I/O L01N_2 VRP_2	I/O L01P_2 VRN_2	I/O L16P_2
D	I/O L17N_7	I/O L17P_7	I/O L19P_7	TDI	I/O L10P_0	I/O VREF_0	I/O L27P_0	I/O L28P_0	I/O	I/O	I/O L30P_1	I/O L28P_1	I/O L24P_1	I/O L24N_1	TDO	I/O L19N_2	I/O L17N_2	I/O L17P_2 VREF_2
E	I/O L20P_7	I/O L20N_7	I/O L19N_7 VREF_7	I/O L21N_7	PROG_B	HSWAP_EN	I/O	I/O L29N_0	I/O L32N_0 GCLK7	I/O L32N_1 GCLK5	I/O L29P_1	I/O L27P_1	I/O L27N_1	TCK	I/O L21P_2	I/O L19P_2	I/O L20N_2	I/O L20P_2
F	GND	I/O L23P_7	VCCO_7	I/O L21P_7	I/O L22P_7	VCCINT	VCCINT	I/O L29P_0	I/O L32P_0 GCLK6	I/O L32P_1 GCLK4	I/O L29N_1	VCCINT	VCCINT	I/O L22N_2	I/O L21N_2	VCCO_2	I/O L23P_2	GND
G	I/O L23N_7	VCCAUX	I/O L24P_7	I/O L24N_7	I/O L22N_7	VCCINT	GND	VCCO_0	VCCO_0	VCCO_1	VCCO_1	GND	VCCINT	I/O L22P_2	I/O L24N_2	I/O L24P_2	VCCAUX	I/O L23N_2 VREF_2
H	I/O L35N_7	I/O L35P_7	I/O L34P_7	I/O L34N_7	I/O L27N_7	I/O L27P_7 VREF_7	VCCO_7	GND	GND	GND	GND	VCCO_2	I/O L27N_2	I/O L27P_2	I/O L34P_2	I/O L34N_2 VREF_2	I/O L35N_2	I/O L35P_2
J	I/O L39N_7	I/O L39P_7	GND	I/O L40P_7	I/O L40N_7 VREF_7	I/O	VCCO_7	GND			GND	VCCO_2	I/O	I/O L40P_2 VREF_2	I/O L40N_2	GND	I/O L39P_2	I/O L39N_2
K	I/O L40N_6	I/O L40P_6 VREF_6	GND	I/O L39P_6	I/O L39N_6	I/O	VCCO_6	GND			GND	VCCO_3	I/O L39N_3	I/O L39P_3	I/O	GND	I/O L40N_3 VREF_3	I/O L40P_3
L	I/O L35P_6	I/O L35N_6	I/O L34N_6 VREF_6	I/O L34P_6	I/O L27P_6	I/O L27N_6	VCCO_6	GND	GND	GND	GND	VCCO_3	I/O L27P_3	I/O L27N_3	I/O L34N_3	I/O L34P_3 VREF_3	I/O L35P_3	I/O L35N_3
M	I/O L24P_6	VCCAUX	I/O L23N_6	I/O L23P_6	I/O L22P_6	VCCINT	GND	VCCO_5	VCCO_5	VCCO_4	VCCO_4	GND	VCCINT	I/O L22N_3	I/O L23N_3	I/O L23P_3 VREF_3	VCCAUX	I/O L24N_3
N	GND	I/O L24N_6 VREF_6	VCCO_6	I/O L21N_6	I/O L22N_6	VCCINT	VCCINT	I/O	I/O L32N_5 GCLK3	I/O L32N_4 GCLK1	I/O L30N_4 D2	VCCINT	VCCINT	I/O L22P_3	I/O L21P_3	VCCO_3	I/O L24P_3	GND
P	I/O L20P_6	I/O L20N_6	I/O L19P_6	I/O L21P_6	M0	I/O L27N_5 VREF_5	I/O L27P_5	I/O	I/O L32P_5 GCLK2	I/O L32P_4 GCLK0	I/O L30P_4 D3	I/O	I/O L25P_4	I/O L06N_4 VREF_4	I/O L21N_3	I/O L17N_3	I/O L20P_3	I/O L20N_3
R	I/O L17P_6 VREF_6	I/O L17N_6	I/O L19N_6	M2	I/O L15P_5	I/O L15N_5	I/O L28N_5 D6	I/O L30N_5	I/O VREF_5	I/O VREF_4	I/O L29N_4	I/O L27P_4 D1	I/O L25N_4	I/O L06P_4	DONE	I/O L17P_3 VREF_3	I/O L19N_3	I/O L19P_3
T	I/O L16P_6	I/O L01P_6 VRN_6	I/O L01N_6 VRP_6	I/O L06P_5	I/O L06N_5	VCCO_5	I/O L28P_5 D7	I/O L30P_5	GND	GND	I/O L29P_4	I/O L27N_4 DIN D0	VCCO_4	I/O L10N_4	CCLK	I/O L01P_3 VRN_3	I/O L01N_3 VRP_3	I/O L16N_3
U	I/O L16N_6	GND	M1	I/O L10P_5 VRN_5	I/O L16P_5	I/O	VCCAUX	VCCO_5	I/O L31N_5 D4	I/O L31N_4 INIT_B	VCCO_4	VCCAUX	I/O VREF_4	I/O L10P_4	I/O L09N_4	I/O L01N_4 VRP_4	GND	I/O L16P_3
V	GND	I/O L01P_5 CS_B	I/O L01N_5 RDWR_B	I/O L10N_5 VRP_5	I/O L16N_5	GND	I/O L29P_5 VREF_5	I/O L29N_5	I/O L31P_5 D5	I/O L31P_4 DOUT BUSY	I/O L28P_4	I/O L28N_4	GND	I/O	I/O L09P_4	I/O L01P_4 VRN_4	I/O VREF_4	GND

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Figure 50: **FG320 Package Footprint (Top View)**

156	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	29	**VREF:** User I/O or input voltage reference for bank
16	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input	28	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	12	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	40	**GND:** Ground	8	**VCCAUX:** Auxiliary voltage supply (+2.5V)

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
1	IO_L15P_1	IO_L15P_1	E17	I/O
1	IO_L16N_1	IO_L16N_1	B17	I/O
1	IO_L16P_1	IO_L16P_1	C17	I/O
1	N.C. (◆)	IO_L19N_1	C16	I/O
1	N.C. (◆)	IO_L19P_1	D16	I/O
1	N.C. (◆)	IO_L22N_1	A16	I/O
1	N.C. (◆)	IO_L22P_1	B16	I/O
1	IO_L24N_1	IO_L24N_1	D15	I/O
1	IO_L24P_1	IO_L24P_1	E15	I/O
1	IO_L25N_1	IO_L25N_1	B15	I/O
1	IO_L25P_1	IO_L25P_1	A15	I/O
1	IO_L27N_1	IO_L27N_1	D14	I/O
1	IO_L27P_1	IO_L27P_1	E14	I/O
1	IO_L28N_1	IO_L28N_1	A14	I/O
1	IO_L28P_1	IO_L28P_1	B14	I/O
1	IO_L29N_1	IO_L29N_1	C13	I/O
1	IO_L29P_1	IO_L29P_1	D13	I/O
1	IO_L30N_1	IO_L30N_1	A13	I/O
1	IO_L30P_1	IO_L30P_1	B13	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D12	VREF
1	IO_L31P_1	IO_L31P_1	E12	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B12	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C12	GCLK
1	VCCO_1	VCCO_1	C15	VCCO
1	VCCO_1	VCCO_1	F15	VCCO
1	VCCO_1	VCCO_1	G12	VCCO
1	VCCO_1	VCCO_1	G13	VCCO
1	VCCO_1	VCCO_1	G14	VCCO
2	IO	IO	C22	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C20	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C21	DCI
2	IO_L16N_2	IO_L16N_2	D20	I/O
2	IO_L16P_2	IO_L16P_2	D19	I/O
2	IO_L17N_2	IO_L17N_2	D21	I/O
2	IO_L17P_2/VREF_2	IO_L17P_2/VREF_2	D22	VREF
2	IO_L19N_2	IO_L19N_2	E18	I/O
2	IO_L19P_2	IO_L19P_2	F18	I/O
2	IO_L20N_2	IO_L20N_2	E19	I/O
2	IO_L20P_2	IO_L20P_2	E20	I/O
2	IO_L21N_2	IO_L21N_2	E21	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
3	IO_L19N_3	IO_L19N_3	IO_L19N_3	IO_L19N_3	IO_L19N_3	W26	I/O
3	IO_L19P_3	IO_L19P_3	IO_L19P_3	IO_L19P_3	IO_L19P_3	W25	I/O
3	IO_L20N_3	IO_L20N_3	IO_L20N_3	IO_L20N_3	IO_L20N_3	U20	I/O
3	IO_L20P_3	IO_L20P_3	IO_L20P_3	IO_L20P_3	IO_L20P_3	V20	I/O
3	IO_L21N_3	IO_L21N_3	IO_L21N_3	IO_L21N_3	IO_L21N_3	V23	I/O
3	IO_L21P_3	IO_L21P_3	IO_L21P_3	IO_L21P_3	IO_L21P_3	V22	I/O
3	IO_L22N_3	IO_L22N_3	IO_L22N_3	IO_L22N_3	IO_L22N_3	V25	I/O
3	IO_L22P_3	IO_L22P_3	IO_L22P_3	IO_L22P_3	IO_L22P_3	V24	I/O
3	IO_L23N_3	IO_L23N_3	IO_L23N_3	IO_L23N_3	IO_L23N_3	U22	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	U21	VREF
3	IO_L24N_3	IO_L24N_3	IO_L24N_3	IO_L24N_3	IO_L24N_3	U24	I/O
3	IO_L24P_3	IO_L24P_3	IO_L24P_3	IO_L24P_3	IO_L24P_3	U23	I/O
3	IO_L26N_3	IO_L26N_3	IO_L26N_3	IO_L26N_3	IO_L26N_3	U26	I/O
3	IO_L26P_3	IO_L26P_3	IO_L26P_3	IO_L26P_3	IO_L26P_3	U25	I/O
3	IO_L27N_3	IO_L27N_3	IO_L27N_3	IO_L27N_3	IO_L27N_3	T20	I/O
3	IO_L27P_3	IO_L27P_3	IO_L27P_3	IO_L27P_3	IO_L27P_3	T19	I/O
3	IO_L28N_3	IO_L28N_3	IO_L28N_3	IO_L28N_3	IO_L28N_3	T22	I/O
3	IO_L28P_3	IO_L28P_3	IO_L28P_3	IO_L28P_3	IO_L28P_3	T21	I/O
3	IO_L29N_3	IO_L29N_3	IO_L29N_3	IO_L29N_3	IO_L29N_3	T26	I/O
3	IO_L29P_3	IO_L29P_3	IO_L29P_3	IO_L29P_3	IO_L29P_3	T25	I/O
3	IO_L31N_3	IO_L31N_3	IO_L31N_3	IO_L31N_3	IO_L31N_3	R20	I/O
3	IO_L31P_3	IO_L31P_3	IO_L31P_3	IO_L31P_3	IO_L31P_3	R19	I/O
3	IO_L32N_3	IO_L32N_3	IO_L32N_3	IO_L32N_3	IO_L32N_3	R22	I/O
3	IO_L32P_3	IO_L32P_3	IO_L32P_3	IO_L32P_3	IO_L32P_3	R21	I/O
3	IO_L33N_3	IO_L33N_3	IO_L33N_3	IO_L33N_3	IO_L33N_3	R24	I/O
3	IO_L33P_3	IO_L33P_3	IO_L33P_3	IO_L33P_3	IO_L33P_3	T23	I/O
3	IO_L34N_3	IO_L34N_3	IO_L34N_3	IO_L34N_3	IO_L34N_3	R26	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	R25	VREF
3	IO_L35N_3	IO_L35N_3	IO_L35N_3	IO_L35N_3	IO_L35N_3	P20	I/O
3	IO_L35P_3	IO_L35P_3	IO_L35P_3	IO_L35P_3	IO_L35P_3	P19	I/O
3	IO_L38N_3	IO_L38N_3	IO_L38N_3	IO_L38N_3	IO_L38N_3	P22	I/O
3	IO_L38P_3	IO_L38P_3	IO_L38P_3	IO_L38P_3	IO_L38P_3	P21	I/O
3	IO_L39N_3	IO_L39N_3	IO_L39N_3	IO_L39N_3	IO_L39N_3	P24	I/O
3	IO_L39P_3	IO_L39P_3	IO_L39P_3	IO_L39P_3	IO_L39P_3	P23	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	P26	VREF
3	IO_L40P_3	IO_L40P_3	IO_L40P_3	IO_L40P_3	IO_L40P_3	P25	I/O
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	P17	VCCO
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	P18	VCCO
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	R18	VCCO
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	T18	VCCO
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	T24	VCCO
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	U19	VCCO
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	V19	VCCO

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	F6	DCI
7	IO_L02N_7	IO_L02N_7	IO_L02N_7	IO_L02N_7	IO_L02N_7	E3	I/O
7	IO_L02P_7	IO_L02P_7	IO_L02P_7	IO_L02P_7	IO_L02P_7	E4	I/O
7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	D1	VREF
7	IO_L03P_7	IO_L03P_7	IO_L03P_7	IO_L03P_7	IO_L03P_7	D2	I/O
7	N.C. (◆)	IO_L05N_7	IO_L05N_7	IO_L05N_7	IO_L05N_7	G6	I/O
7	N.C. (◆)	IO_L05P_7	IO_L05P_7	IO_L05P_7	IO_L05P_7	G7	I/O
7	N.C. (◆)	IO_L06N_7	IO_L06N_7	IO_L06N_7	IO_L06N_7	E1	I/O
7	N.C. (◆)	IO_L06P_7	IO_L06P_7	IO_L06P_7	IO_L06P_7	E2	I/O
7	N.C. (◆)	IO_L07N_7	IO_L07N_7	IO_L07N_7	IO_L07N_7	F3	I/O
7	N.C. (◆)	IO_L07P_7	IO_L07P_7	IO_L07P_7	IO_L07P_7	F4	I/O
7	N.C. (◆)	IO_L08N_7	IO_L08N_7	IO_L08N_7	IO_L08N_7	G4	I/O
7	N.C. (◆)	IO_L08P_7	IO_L08P_7	IO_L08P_7	IO_L08P_7	G5	I/O
7	N.C. (◆)	IO_L09N_7	IO_L09N_7	IO_L09N_7	IO_L09N_7	F1	I/O
7	N.C. (◆)	IO_L09P_7	IO_L09P_7	IO_L09P_7	IO_L09P_7	F2	I/O
7	N.C. (◆)	IO_L10N_7	IO_L10N_7	IO_L10N_7	IO_L10N_7	H6	I/O
7	N.C. (◆)	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	H7	VREF
7	IO_L14N_7	IO_L14N_7	IO_L14N_7	IO_L14N_7	IO_L14N_7	G1	I/O
7	IO_L14P_7	IO_L14P_7	IO_L14P_7	IO_L14P_7	IO_L14P_7	G2	I/O
7	IO_L16N_7	IO_L16N_7	IO_L16N_7	IO_L16N_7	IO_L16N_7	J6	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	H5	VREF
7	IO_L17N_7	IO_L17N_7	IO_L17N_7	IO_L17N_7	IO_L17N_7	H3	I/O
7	IO_L17P_7	IO_L17P_7	IO_L17P_7	IO_L17P_7	IO_L17P_7	H4	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	H1	VREF
7	IO_L19P_7	IO_L19P_7	IO_L19P_7	IO_L19P_7	IO_L19P_7	H2	I/O
7	IO_L20N_7	IO_L20N_7	IO_L20N_7	IO_L20N_7	IO_L20N_7	K7	I/O
7	IO_L20P_7	IO_L20P_7	IO_L20P_7	IO_L20P_7	IO_L20P_7	J7	I/O
7	IO_L21N_7	IO_L21N_7	IO_L21N_7	IO_L21N_7	IO_L21N_7	J4	I/O
7	IO_L21P_7	IO_L21P_7	IO_L21P_7	IO_L21P_7	IO_L21P_7	J5	I/O
7	IO_L22N_7	IO_L22N_7	IO_L22N_7	IO_L22N_7	IO_L22N_7	J2	I/O
7	IO_L22P_7	IO_L22P_7	IO_L22P_7	IO_L22P_7	IO_L22P_7	J3	I/O
7	IO_L23N_7	IO_L23N_7	IO_L23N_7	IO_L23N_7	IO_L23N_7	K5	I/O
7	IO_L23P_7	IO_L23P_7	IO_L23P_7	IO_L23P_7	IO_L23P_7	K6	I/O
7	IO_L24N_7	IO_L24N_7	IO_L24N_7	IO_L24N_7	IO_L24N_7	K3	I/O
7	IO_L24P_7	IO_L24P_7	IO_L24P_7	IO_L24P_7	IO_L24P_7	K4	I/O
7	IO_L26N_7	IO_L26N_7	IO_L26N_7	IO_L26N_7	IO_L26N_7	K1	I/O
7	IO_L26P_7	IO_L26P_7	IO_L26P_7	IO_L26P_7	IO_L26P_7	K2	I/O
7	IO_L27N_7	IO_L27N_7	IO_L27N_7	IO_L27N_7	IO_L27N_7	L7	I/O
7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	L8	VREF
7	IO_L28N_7	IO_L28N_7	IO_L28N_7	IO_L28N_7	IO_L28N_7	L5	I/O
7	IO_L28P_7	IO_L28P_7	IO_L28P_7	IO_L28P_7	IO_L28P_7	L6	I/O
7	IO_L29N_7	IO_L29N_7	IO_L29N_7	IO_L29N_7	IO_L29N_7	L1	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	U17	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	U18	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V9	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V10	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V17	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V18	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	W8	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	W19	VCCINT
VCC AUX	CCLK	CCLK	CCLK	CCLK	CCLK	AD26	CONFIG
VCC AUX	DONE	DONE	DONE	DONE	DONE	AC24	CONFIG
VCC AUX	HSWAP_EN	HSWAP_EN	HSWAP_EN	HSWAP_EN	HSWAP_EN	C2	CONFIG
VCC AUX	M0	M0	M0	M0	M0	AE3	CONFIG
VCC AUX	M1	M1	M1	M1	M1	AC3	CONFIG
VCC AUX	M2	M2	M2	M2	M2	AF3	CONFIG
VCC AUX	PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	D3	CONFIG
VCC AUX	TCK	TCK	TCK	TCK	TCK	B24	JTAG
VCC AUX	TDI	TDI	TDI	TDI	TDI	C1	JTAG
VCC AUX	TDO	TDO	TDO	TDO	TDO	D24	JTAG
VCC AUX	TMS	TMS	TMS	TMS	TMS	A24	JTAG

Notes:
1. XC3S1500 balls D25 and F25 are not VREF pins although they are designated as such. If a design uses an IOSTANDARD requiring VREF in bank 2 then apply the workaround in Answer Record 20519.
2. XC3S4000 is pin compatible with XC3S2000 but uses alternate differential pair labeling on six package balls (H20, H21, H22, H23, H24, J21).
3. XC3S5000 is pin compatible with XC3S4000 but uses alternate differential pair functionality on fifteen package balls (A3, A8, B8, B18, C4, C8, C18, D8, D18, E8, E18, H23, H24, AB9, and AC9).

FG676 Footprint

Left Half of Package (Top View)

XC3S1000 (391 max. user I/O)

- 315 — **I/O:** Unrestricted, general-purpose user I/O
- 40 — **VREF:** User I/O or input voltage reference for bank
- 98 — **N.C.:** Unconnected pins for XC3S1000 (◆)

XC3S1500 (487 max user I/O)

- 403 — **I/O:** Unrestricted, general-purpose user I/O
- 48 — **VREF:** User I/O or input voltage reference for bank
- 2 — **N.C.:** Unconnected pins for XC3S1500 (■)

XC3S2000, XC3S4000, XC3S5000 (489 max user I/O)

- 405 — **I/O:** Unrestricted, general-purpose user I/O
- 48 — **VREF:** User I/O or input voltage reference for bank
- 0 — **N.C.:** No unconnected pins

All devices

- 12 — **DUAL:** Configuration pin, then possible user I/O
- 8 — **GCLK:** User I/O or global clock buffer input
- 16 — **DCI:** User I/O or reference resistor input for bank
- 7 — **CONFIG:** Dedicated configuration pins
- 4 — **JTAG:** Dedicated JTAG port pins
- 20 — **VCCINT:** Internal core voltage supply (+1.2V)
- 64 — **VCCO:** Output voltage supply for bank
- 16 — **VCCAUX:** Auxiliary voltage supply (+2.5V)
- 76 — **GND:** Ground

Bank 0 (top, columns 3–13); Bank 7 (left, rows A–N); Bank 6 (left, rows P–AF); Bank 5 (bottom, columns 4–13)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	VCCAUX	I/O	I/O L05P_0 VREF_0	I/O	I/O	I/O L10P_0	I/O L15P_0	VCCAUX	I/O L23P_0 ◆	I/O L26P_0 VREF_0 ◆	I/O L29P_0	I/O L32P_0 GCLK6
B	VCCAUX	GND	I/O VREF_0	I/O L05N_0	I/O L06P_0	I/O L08P_0	I/O L10N_0	I/O L15N_0	I/O L18P_0 ◆	I/O L23N_0 ◆	I/O L26N_0 ◆	I/O L29N_0	I/O L32N_0 GCLK7
C	TDI	HSWAP_EN	GND	I/O	I/O L06N_0	I/O L08N_0	VCCO_0	I/O ◆	I/O L18N_0 ◆	I/O L22P_0	VCCO_0	I/O	I/O L31P_0 VREF_0
D	I/O L03N_7 VREF_7	I/O L03P_7	PROG_B	GND	I/O L01P_0 VRN_0	I/O L07P_0	I/O L09P_0	I/O L12P_0 ◆	I/O L17P_0 ◆	I/O L22N_0	I/O L25P_0	GND	I/O L31N_0
E	I/O L06N_7 ◆	I/O L06P_7 ◆	I/O L02N_7	I/O L02P_7	I/O L01N_0 VRP_0	I/O L07N_0	I/O L09N_0	I/O L12N_0 ◆	I/O L17N_0 ◆	I/O L19P_0	I/O L25N_0	I/O L28P_0	I/O
F	I/O L09N_7 ◆	I/O L09P_7 ◆	I/O L07N_7 ◆	I/O L07P_7 ◆	I/O L01N_7 VRP_7	I/O L01P_7 VRN_7	I/O VREF_0	I/O L11P_0 ◆	I/O L16P_0	I/O L19N_0	I/O L24P_0	I/O L28N_0	I/O L30P_0
G	I/O L14N_7	I/O L14P_7	VCCO_7	I/O L08N_7 ◆	I/O L08P_7 ◆	I/O L05N_7 ◆	I/O L05P_7 ◆	I/O L11N_0 ◆	I/O L16N_0	I/O VREF_0	I/O L24N_0	I/O L27N_0	I/O L30N_0
H	I/O L19N_7 VREF_7	I/O L19P_7	I/O L17N_7	I/O L17P_7	I/O L16P_7 VREF_7	I/O L10N_7 ◆	I/O L10P_7 VREF_7 ◆	VCCINT	VCCO_0	VCCO_0	I/O	I/O	I/O L27P_0
J	VCCAUX	I/O L22N_7	I/O L22P_7	I/O L21N_7	I/O L21P_7	I/O L16N_7	I/O L20P_7	VCCO_7	VCCINT	VCCINT	VCCO_0	VCCO_0	VCCO_0
K	I/O L26N_7	I/O L26P_7	I/O L24N_7	I/O L24P_7	I/O L23N_7	I/O L23P_7	I/O L20N_7	VCCO_7	VCCINT	VCCINT	GND	GND	VCCO_0
L	I/O L29N_7	I/O L29P_7	VCCO_7	I/O L33P_7	I/O L28N_7	I/O L28P_7	I/O L27N_7	I/O L27P_7 VREF_7	VCCO_7	GND	GND	GND	GND
M	I/O L34N_7	I/O L34P_7	I/O L33N_7	GND	I/O L32P_7	I/O L32N_7	I/O L31N_7	I/O L31P_7	VCCO_7	GND	GND	GND	GND
N	I/O L40N_7 VREF_7	I/O L40P_7	I/O L39N_7	I/O L39P_7	I/O L38N_7	I/O L38P_7	I/O L35N_7	I/O L35P_7	VCCO_7	VCCO_7	GND	GND	GND
P	I/O L40P_6 VREF_6	I/O L40N_6	I/O L39P_6	I/O L39N_6	I/O L38P_6	I/O L38N_6	I/O L35P_6	I/O L35N_6	VCCO_6	VCCO_6	GND	GND	GND
R	I/O L34P_6	I/O L34N_6 VREF_6	I/O L33P_6	GND	I/O L32P_6	I/O L32N_6	I/O L31P_6	I/O L31N_6	VCCO_6	GND	GND	GND	GND
T	I/O L29P_6	I/O L29N_6	VCCO_6	I/O L33N_6	I/O L28P_6	I/O L28N_6	I/O L27P_6	I/O L27N_6	VCCO_6	GND	GND	GND	GND
U	I/O L26P_6	I/O L26N_6	I/O L24P_6	I/O L24N_6 VREF_6	I/O L23P_6	I/O L23N_6	I/O L20P_6	VCCO_6	VCCINT	VCCINT	GND	GND	VCCO_5
V	VCCAUX	I/O L22P_6	I/O L22N_6	I/O L21P_6	I/O L21N_6	I/O L16N_6	I/O L20N_6	VCCO_6	VCCINT	VCCINT	VCCO_5	VCCO_5	VCCO_5
W	I/O L19P_6	I/O L19N_6	I/O L17P_6 VREF_6	I/O L17N_6	I/O L16P_6	I/O L14P_6	I/O L14N_6	VCCINT	VCCO_5	VCCO_5	I/O L24P_5	I/O L27P_5	I/O L30P_5
Y	I/O L10P_6 ◆	I/O L10N_6 ◆	VCCO_6	I/O L08P_6 ◆	I/O L08N_6 ◆	I/O L06P_6 ◆	I/O L06N_6 ◆	I/O	I/O L16P_5	I/O L19P_5 VREF_5	I/O L24N_5	I/O L27N_5 VREF_5	I/O L30N_5
AA	I/O L09P_6 ◆	I/O L09N_6 VREF_6 ◆	I/O L07P_6 ◆	I/O L07N_6 ◆	I/O ◆■	I/O L05P_5	I/O	I/O L11P_5 ◆	I/O L16N_5	I/O L19N_5	I/O L25P_5	I/O L28P_5 D7	I/O
AB	I/O L05P_6 ◆	I/O L05N_6 ◆	I/O L02P_6	I/O L02N_6	I/O L01P_5 CS_B	I/O L05N_5	I/O L09P_5	I/O L11N_5 VREF_5 ◆	I/O	I/O L22P_5	I/O L25N_5	I/O L28N_5 D6	I/O L31P_5 D5
AC	I/O L03P_6	I/O L03N_6 VREF_6	M1	GND	I/O L01N_5 RDWR_B	I/O L07P_5	I/O L09N_5	I/O L12P_5 ◆	I/O ◆	I/O L22N_5	I/O	GND	I/O L31N_5 D4
AD	I/O L01P_6 VRN_6	I/O L01N_6 VRP_6	GND	I/O L04P_5	I/O L06P_5	I/O L07N_5	VCCO_5	I/O L12N_5 ◆	I/O L18P_5 ◆	I/O	VCCO_5	I/O	I/O L32P_5 GCLK2
AE	VCCAUX	GND	M0	I/O L04N_5	I/O L06N_5	I/O L08P_5	I/O L10P_5 VRN_5	I/O L15P_5	I/O L18N_5 ◆	I/O L23P_5 ◆	I/O L26P_5 ◆	I/O L29P_5 VREF_5	I/O L32N_5 GCLK3
AF	GND	VCCAUX	M2	I/O	I/O VREF_5	I/O L08N_5	I/O L10N_5 VRP_5	I/O L15N_5	VCCAUX	I/O L23N_5 ◆	I/O L26N_5 ◆	I/O L29N_5	I/O VREF_5

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Figure 53: **FG676 Package Footprint (Top View)**

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	IO_L28N_2	IO_L28N_2	M26	I/O
2	IO_L28P_2	IO_L28P_2	N25	I/O
2	IO_L29N_2	IO_L29N_2	N26	I/O
2	IO_L29P_2	IO_L29P_2	N27	I/O
2	IO_L31N_2	IO_L31N_2	N29	I/O
2	IO_L31P_2	IO_L31P_2	N30	I/O
2	IO_L32N_2	IO_L32N_2	P21	I/O
2	IO_L32P_2	IO_L32P_2	P22	I/O
2	IO_L33N_2	IO_L33N_2	P24	I/O
2	IO_L33P_2	IO_L33P_2	P25	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	P28	VREF
2	IO_L34P_2	IO_L34P_2	P29	I/O
2	IO_L35N_2	IO_L35N_2	R21	I/O
2	IO_L35P_2	IO_L35P_2	R22	I/O
2	IO_L37N_2	IO_L37N_2	R23	I/O
2	IO_L37P_2	IO_L37P_2	R24	I/O
2	IO_L38N_2	IO_L38N_2	R25	I/O
2	IO_L38P_2	IO_L38P_2	R26	I/O
2	IO_L39N_2	IO_L39N_2	R27	I/O
2	IO_L39P_2	IO_L39P_2	R28	I/O
2	IO_L40N_2	IO_L40N_2	R29	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	R30	VREF
2	N.C. (◆)	IO_L41N_2	E27	I/O
2	N.C. (◆)	IO_L41P_2	F26	I/O
2	N.C. (◆)	IO_L45N_2	K28	I/O
2	N.C. (◆)	IO_L45P_2	K29	I/O
2	N.C. (◆)	IO_L46N_2	K21	I/O
2	N.C. (◆)	IO_L46P_2	L21	I/O
2	N.C. (◆)	IO_L47N_2	L23	I/O
2	N.C. (◆)	IO_L47P_2	L24	I/O
2	N.C. (◆)	IO_L50N_2	M29	I/O
2	N.C. (◆)	IO_L50P_2	M30	I/O
2	VCCO_2	VCCO_2	M20	VCCO
2	VCCO_2	VCCO_2	N20	VCCO
2	VCCO_2	VCCO_2	P20	VCCO
2	VCCO_2	VCCO_2	L22	VCCO
2	VCCO_2	VCCO_2	J24	VCCO
2	VCCO_2	VCCO_2	N24	VCCO
2	VCCO_2	VCCO_2	G26	VCCO
2	VCCO_2	VCCO_2	E28	VCCO

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
6	IO_L16N_6	IO_L16N_6	AE2	I/O
6	IO_L16P_6	IO_L16P_6	AE1	I/O
6	IO_L17N_6	IO_L17N_6	AD10	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	AD9	VREF
6	IO_L19N_6	IO_L19N_6	AD2	I/O
6	IO_L19P_6	IO_L19P_6	AD1	I/O
6	IO_L20N_6	IO_L20N_6	AC11	I/O
6	IO_L20P_6	IO_L20P_6	AC10	I/O
6	IO_L21N_6	IO_L21N_6	AC8	I/O
6	IO_L21P_6	IO_L21P_6	AC7	I/O
6	IO_L22N_6	IO_L22N_6	AC6	I/O
6	IO_L22P_6	IO_L22P_6	AC5	I/O
6	IO_L23N_6	IO_L23N_6	AC2	I/O
6	IO_L23P_6	IO_L23P_6	AC1	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	AC9	VREF
6	IO_L24P_6	IO_L24P_6	AB10	I/O
6	IO_L25N_6	IO_L25N_6	AB8	I/O
6	IO_L25P_6	IO_L25P_6	AB7	I/O
6	IO_L26N_6	IO_L26N_6	AB4	I/O
6	IO_L26P_6	IO_L26P_6	AB3	I/O
6	IO_L27N_6	IO_L27N_6	AB11	I/O
6	IO_L27P_6	IO_L27P_6	AA11	I/O
6	IO_L28N_6	IO_L28N_6	AA8	I/O
6	IO_L28P_6	IO_L28P_6	AA7	I/O
6	IO_L29N_6	IO_L29N_6	AA6	I/O
6	IO_L29P_6	IO_L29P_6	AA5	I/O
6	IO_L30N_6	IO_L30N_6	AA4	I/O
6	IO_L30P_6	IO_L30P_6	AA3	I/O
6	IO_L31N_6	IO_L31N_6	AA2	I/O
6	IO_L31P_6	IO_L31P_6	AA1	I/O
6	IO_L32N_6	IO_L32N_6	Y11	I/O
6	IO_L32P_6	IO_L32P_6	Y10	I/O
6	IO_L33N_6	IO_L33N_6	Y4	I/O
6	IO_L33P_6	IO_L33P_6	Y3	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	Y2	VREF
6	IO_L34P_6	IO_L34P_6	Y1	I/O
6	IO_L35N_6	IO_L35N_6	Y9	I/O
6	IO_L35P_6	IO_L35P_6	W10	I/O
6	IO_L36N_6	IO_L36N_6	W7	I/O
6	IO_L36P_6	IO_L36P_6	W6	I/O

User I/Os by Bank

Note: The FG(G)1156 package is discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Table 111 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S4000 in the FG1156 package. Similarly, Table 112 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S5000 in the FG1156 package.

Table 111: **User I/Os Per Bank for XC3S4000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	90	79	0	2	7	2
	1	90	79	0	2	7	2
Right	2	88	80	0	2	6	0
	3	88	79	0	2	7	0
Bottom	4	90	73	6	2	7	2
	5	90	73	6	2	7	2
Left	6	88	79	0	2	7	0
	7	88	79	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

Table 112: **User I/Os Per Bank for XC3S5000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	100	89	0	2	7	2
	1	100	89	0	2	7	2
Right	2	96	87	0	2	7	0
	3	96	87	0	2	7	0
Bottom	4	100	83	6	2	7	2
	5	100	83	6	2	7	2
Left	6	96	87	0	2	7	0
	7	96	87	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.