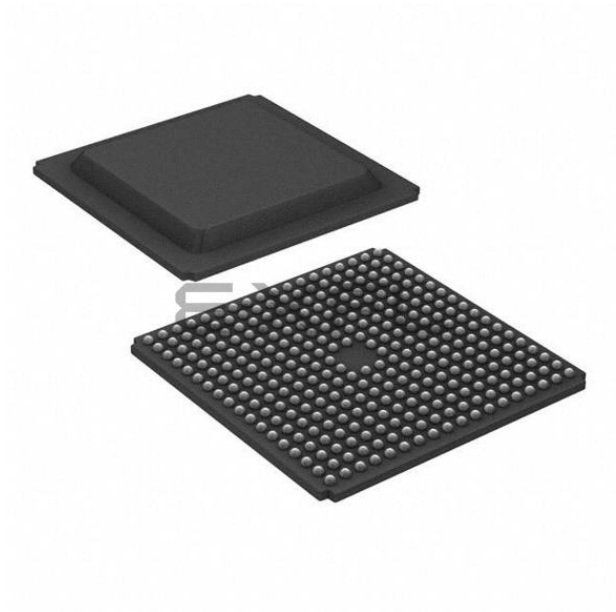
AMD Xilinx - XC3S1000-5FGG320C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1920
Number of Logic Elements/Cells	17280
Total RAM Bits	442368
Number of I/O	221
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1000-5fgg320c

ESD Protection

Clamp diodes protect all device pads against damage from Electro-Static Discharge (ESD) as well as excessive voltage transients. Each I/O has two clamp diodes: One diode extends P-to-N from the pad to V_{CCO} and a second diode extends N-to-P from the pad to GND. During operation, these diodes are normally biased in the off state. These clamp diodes are always connected to the pad, regardless of the signal standard selected. The presence of diodes limits the ability of Spartan-3 FPGA I/Os to tolerate high signal voltages. The V_{IN} absolute maximum rating in Table 28, page 58 specifies the voltage range that I/Os can tolerate.

Slew Rate Control and Drive Strength

Two options, FAST and SLOW, control the output slew rate. The FAST option supports output switching at a high rate. The SLOW option reduces bus transients. These options are only available when using one of the LVCMOS or LVTTL standards, which also provide up to seven different levels of current drive strength: 2, 4, 6, 8, 12, 16, and 24 mA. Choosing the appropriate drive strength level is yet another means to minimize bus transients.

Table 7 shows the drive strengths that the LVCMOS and LVTTL standards support.

Table 7: **Programmable Output Drive Current**

Signal Standard (IOSTANDARD)	Current Drive (mA)						
	2	4	6	8	12	16	24
LVTTL	✓	✓	✓	✓	✓	✓	✓
LVCMOS33	✓	✓	✓	✓	✓	✓	✓
LVCMOS25	✓	✓	✓	✓	✓	✓	✓
LVCMOS18	✓	✓	✓	✓	✓	✓	–
LVCMOS15	✓	✓	✓	✓	✓	–	–
LVCMOS12	✓	✓	✓	–	–	–	–

Boundary-Scan Capability

All Spartan-3 FPGA IOBs support boundary-scan testing compatible with IEEE 1149.1 standards. During boundary- scan operations such as EXTEST and HIGHZ the I/O pull-down resistor is active. For more information, see Boundary-Scan (JTAG) Mode, page 50, and refer to the “Using Boundary-Scan and BSDL Files” chapter in UG331.

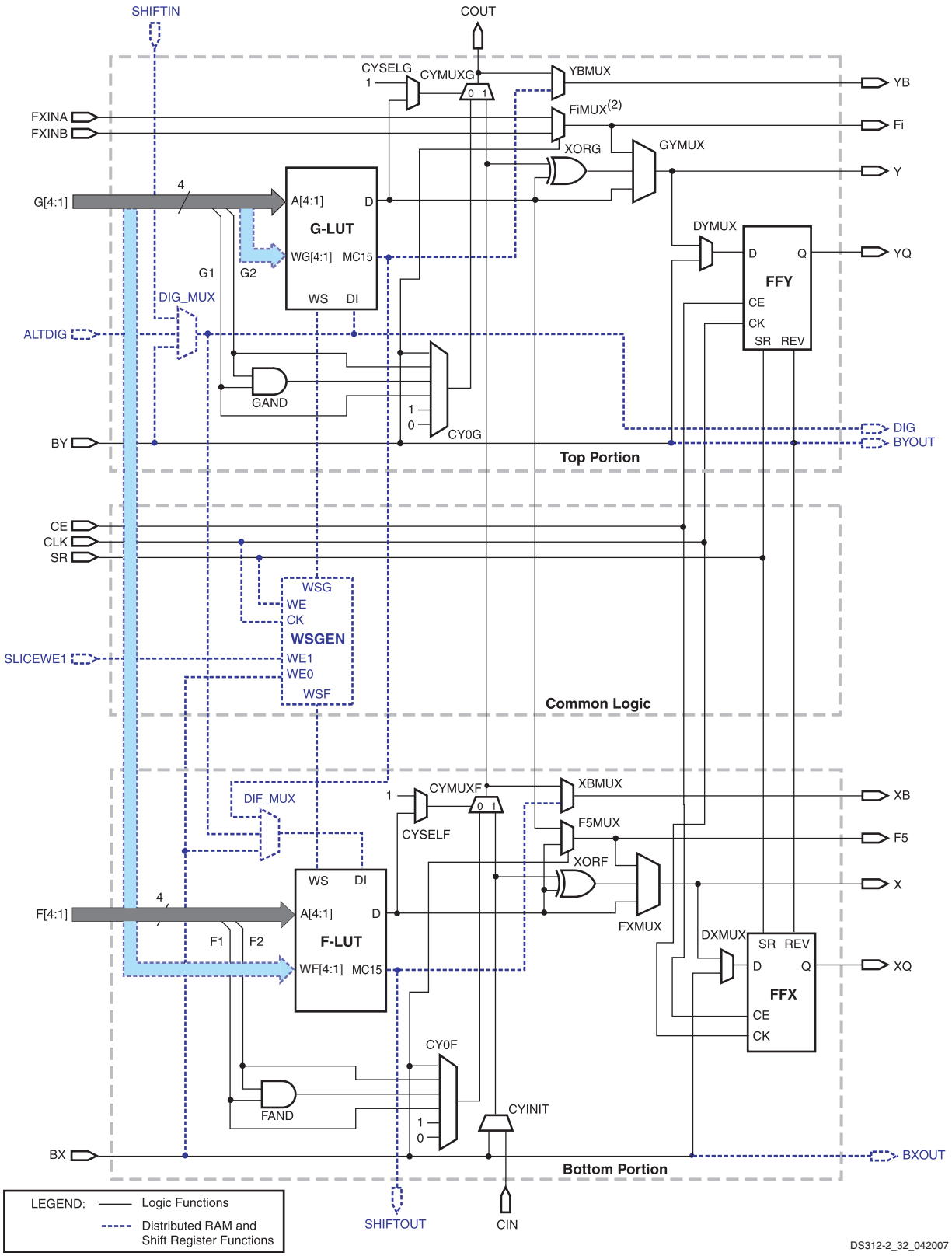
SelectIO Interface Signal Standards

The IOBs support 18 different single-ended signal standards, as listed in Table 8. Furthermore, the majority of IOBs can be used in specific pairs supporting any of eight differential signal standards, as shown in Table 9.

To define the SelectIO™ interface signaling standard in a design, set the IOSTANDARD attribute to the appropriate setting. Xilinx provides a variety of different methods for applying the IOSTANDARD for maximum flexibility. For a full description of different methods of applying attributes to control IOSTANDARD, refer to the “Using I/O Resources” chapter in UG331.

Together with placing the appropriate I/O symbol, two externally applied voltage levels, V_{CCO} and V_{REF}, select the desired signal standard. The V_{CCO} lines provide current to the output driver. The voltage on these lines determines the output voltage swing for all standards except GTL and GTLP.

All single-ended standards except the LVCMOS, LVTTL, and PCI varieties require a Reference Voltage (V_{REF}) to bias the input-switching threshold. Once a configuration data file is loaded into the FPGA that calls for the I/Os of a given bank to use such a signal standard, a few specifically reserved I/O pins on the same bank automatically convert to V_{REF} inputs. When using one of the LVCMOS standards, these pins remain I/Os because the V_{CCO} voltage biases the input-switching threshold, so there is no need for V_{REF}. Select the V_{CCO} and V_{REF} levels to suit the desired single-ended standard according to Table 8.



Notes:

1. Options to invert signal polarity as well as other options that enable lines for various functions are not shown.
2. The index i can be 6, 7, or 8, depending on the slice. In this position, the upper right-hand slice has an F8MUX, and the upper left-hand slice has an F7MUX. The lower right-hand and left-hand slices both have an F6MUX.

Figure 12: **Simplified Diagram of the Left-Hand SLICEM**

- **Phase Shifting:** The DCM provides the ability to shift the phase of all its output clock signals with respect to its input clock signal.

The DCM has four functional components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), the Phase Shifter (PS), and the Status Logic. Each component has its associated signals, as shown in Figure 19.

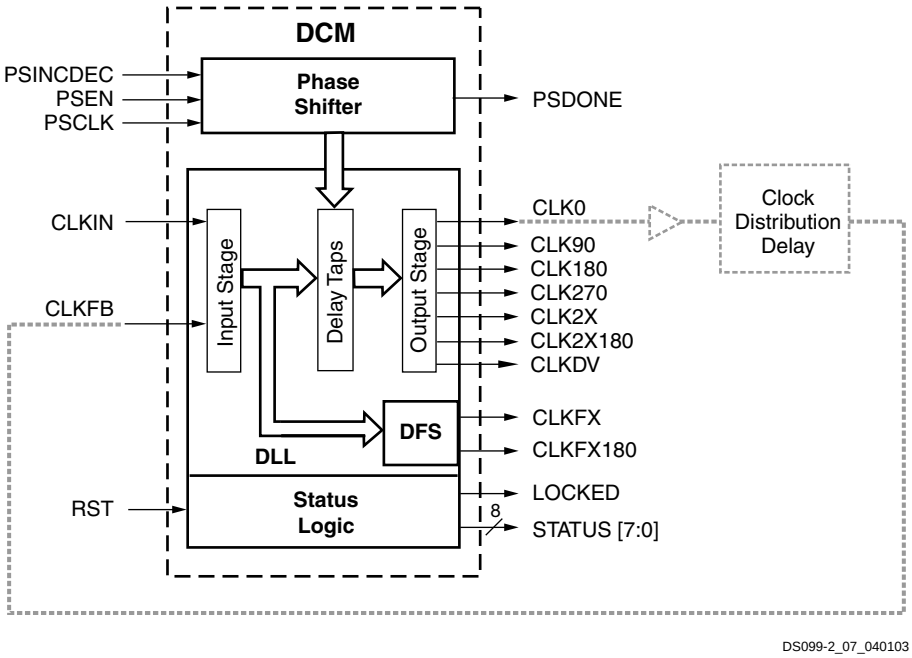


Figure 19: **DCM Functional Blocks and Associated Signals**

Delay-Locked Loop (DLL)

The most basic function of the DLL component is to eliminate clock skew. The main signal path of the DLL consists of an input stage, followed by a series of discrete delay elements or *taps,* which in turn leads to an output stage. This path together with logic for phase detection and control forms a system complete with feedback as shown in Figure 20.

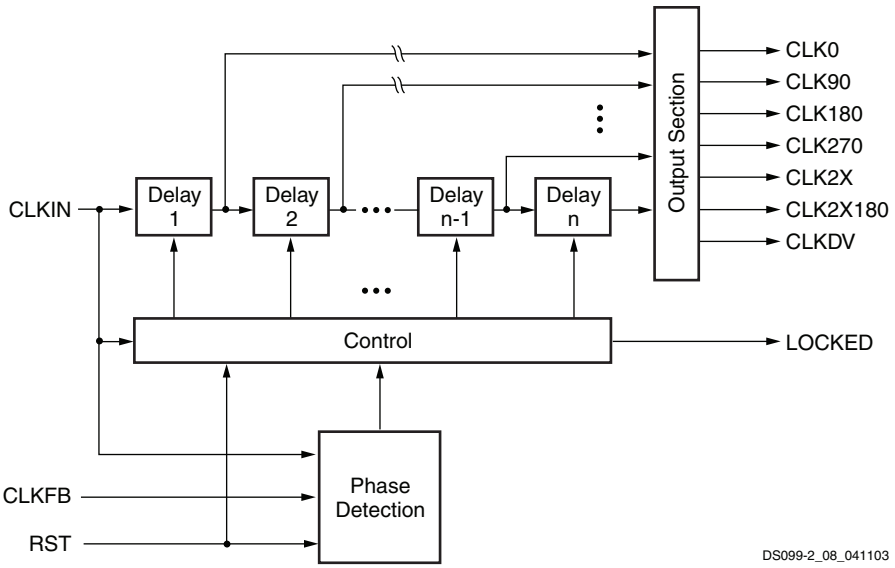


Figure 20: **Simplified Functional Diagram of DLL**

Interconnect

Interconnect (or routing) passes signals among the various functional elements of Spartan-3 devices. There are four kinds of interconnect: Long lines, Hex lines, Double lines, and Direct lines.

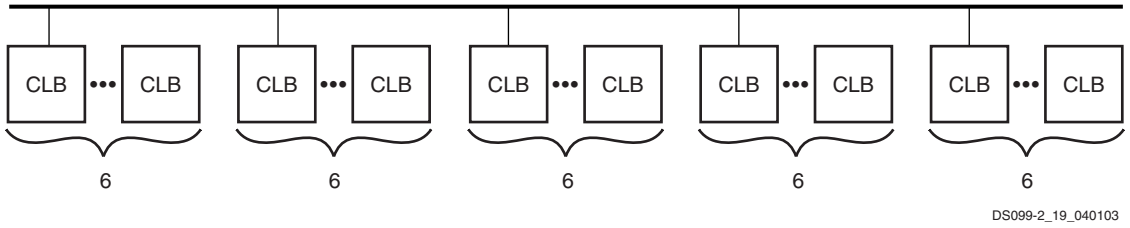
Long lines connect to one out of every six CLBs (see section [a] of Figure 25). Because of their low capacitance, these lines are well-suited for carrying high-frequency signals with minimal loading effects (e.g. skew). If all eight Global Clock Inputs are already committed and there remain additional clock signals to be assigned, Long lines serve as a good alternative.

Hex lines connect one out of every three CLBs (see section [b] of Figure 25). These lines fall between Long lines and Double lines in terms of capability: Hex lines approach the high-frequency characteristics of Long lines at the same time, offering greater connectivity.

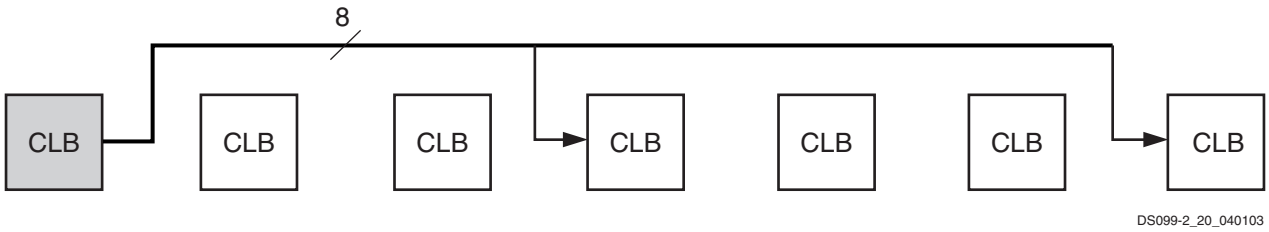
Double lines connect to every other CLB (see section [c] of Figure 25). Compared to the types of lines already discussed, Double lines provide a higher degree of flexibility when making connections.

Direct lines afford any CLB direct access to neighboring CLBs (see section [d] of Figure 25). These lines are most often used to conduct a signal from a "source" CLB to a Double, Hex, or Long line and then from the longer interconnect back to a Direct line accessing a "destination" CLB.

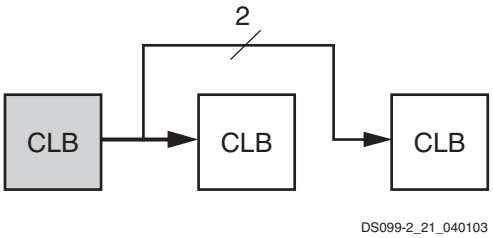
For more details, refer to the "*Using Interconnect*" chapter in UG331.



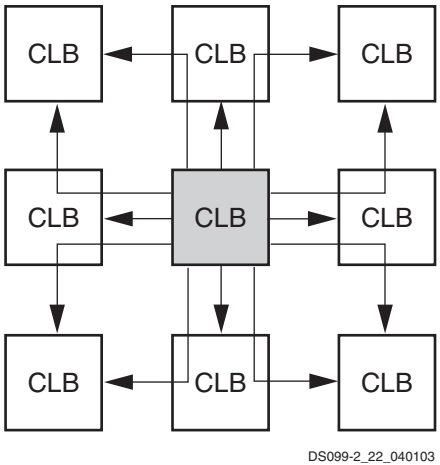
(a) Long Lines



(b) Hex Lines



(c) Double Lines



(d) Direct Lines

Figure 25: **Types of Interconnect**

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DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

- **Advance:** Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur. Use as estimates, not for production.
- **Preliminary:** Based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reported delays is greatly reduced compared to Advance data. Use as estimates, not for production.
- **Production:** These specifications are approved only after silicon has been characterized over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Parameter values are considered stable with no future changes expected.

  Production-quality systems must only use FPGA designs compiled with a Production status speed file. FPGA designs using a less mature speed file designation should only be used during system prototyping or preproduction qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **The following applies unless otherwise noted: The parameter values published in this module apply to all Spartan®-3 devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.** All parameters representing voltages are measured with respect to GND.

Mask and Fab Revisions

Some specifications list different values for one or more mask or fab revisions, indicated by the device top marking (see Package Marking, page 5). The revision differences involve the power ramp rates, differential DC specifications, and DCM characteristics. The most recent revision (mask rev E and GQ fab/geometry code) is errata-free with improved specifications than earlier revisions.

Mask rev E with fab rev GQ has been shipping since 2005 (see XCN05009) and has been 100% of Xilinx Spartan-3 device shipments since 2006. SCD 0974 was provided to ensure the receipt of the rev E silicon, but it is no longer needed. Parts ordered under the SCD appended “0974” to the standard part number. For example, “XC3S50-4VQ100C” became “XC3S50-4VQ100C0974”.

Table 28: **Absolute Maximum Ratings**

Symbol	Description	Conditions		Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND			–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage relative to GND			–0.5	3.00	V
V_{CCO}	Output driver supply voltage relative to GND			–0.5	3.75	V
V_{REF}	Input reference voltage relative to GND			–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND(2,4)	Driver in a high-impedance state	Commercial	–0.95	4.4	V
			Industrial	–0.85	4.3	
	Voltage applied to all Dedicated pins relative to GND(3)		All temp. ranges	–0.5	V_{CCAUX} + 0.5	V

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS33	Slow	2 mA	6.38	7.34	ns
		4 mA	4.83	5.55	ns
		6 mA	4.01	4.61	ns
		8 mA	3.92	4.51	ns
		12 mA	2.91	3.35	ns
		16 mA	2.81	3.23	ns
		24 mA	2.49	2.86	ns
	Fast	2 mA	3.86	4.44	ns
		4 mA	1.87	2.15	ns
		6 mA	0.62	0.71	ns
		8 mA	0.61	0.70	ns
		12 mA	0.16	0.19	ns
		16 mA	0.14	0.16	ns
		24 mA	0.06	0.07	ns
LVDCI_33			0.28	0.32	ns
LVDCI_DV2_33			0.26	0.30	ns
LVTTL	Slow	2 mA	7.27	8.36	ns
		4 mA	4.94	5.69	ns
		6 mA	3.98	4.58	ns
		8 mA	3.98	4.58	ns
		12 mA	2.97	3.42	ns
		16 mA	2.84	3.26	ns
		24 mA	2.65	3.04	ns
	Fast	2 mA	4.32	4.97	ns
		4 mA	1.87	2.15	ns
		6 mA	1.27	1.47	ns
		8 mA	1.19	1.37	ns
		12 mA	0.42	0.48	ns
		16 mA	0.27	0.32	ns
		24 mA	0.16	0.18	ns

Table 71: **Dual-Purpose Pins Used in Master or Slave Serial Mode**

Pin Name	Direction	Description
DIN	Input	**Serial Data Input:** During the Master or Slave Serial configuration modes, DIN is the serial configuration data input, and all data is synchronized to the rising CCLK edge. After configuration, this pin is available as a user I/O. This signal is located in Bank 4 and its output voltage determined by VCCO_4. The BitGen option ***Persist*** permits this pin to retain its configuration function in the User mode.
DOUT	Output	**Serial Data Output:** In a multi-FPGA design where all the FPGAs use serial mode, connect the DOUT output of one FPGA—in either Master or Slave Serial mode—to the DIN input of the next FPGA—in Slave Serial mode—so that configuration data passes from one to the next, in daisy-chain fashion. This "daisy chain" permits sequential configuration of multiple FPGAs. This signal is located in Bank 4 and its output voltage determined by VCCO_4. The BitGen option ***Persist*** permits this pin to retain its configuration function in the User mode.
INIT_B	Bidirectional (open-drain)	**Initializing Configuration Memory/Configuration Error:** Just after power is applied, the FPGA produces a Low-to-High transition on this pin indicating that initialization (*i.e.*, clearing) of the configuration memory has finished. Before entering the User mode, this pin functions as an open-drain output, which requires a pull-up resistor in order to produce a High logic level. In a multi-FPGA design, tie (wire AND) the INIT_B pins from all FPGAs together so that the common node transitions High only after all of the FPGAs have been successfully initialized. Externally holding this pin Low beyond the initialization phase delays the start of configuration. This action stalls the FPGA at the configuration step just before the mode select pins are sampled. During configuration, the FPGA indicates the occurrence of a data (i.e., CRC) error by asserting INIT_B Low. This signal is located in Bank 4 and its output voltage determined by VCCO_4. The BitGen option ***Persist*** permits this pin to retain its configuration function in the User mode.

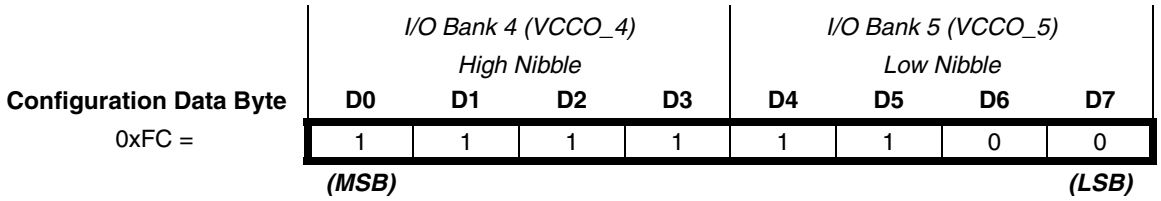

Figure 41: **Configuration Data Byte Mapping to D0-D7 Bits**

Parallel Configuration Modes (SelectMAP)

This section describes the dual-purpose configuration pins used during the Master and Slave Parallel configuration modes, sometimes also called the SelectMAP modes. In both Master and Slave Parallel configuration modes, D0-D7 form the byte-wide configuration data input. See Table 75 for Mode Select pin settings required for Parallel modes.

As shown in Figure 41, D0 is the most-significant bit while D7 is the least-significant bit. Bits D0-D3 form the high nibble of the byte and bits D4-D7 form the low nibble.

In the Parallel configuration modes, both the VCCO_4 and VCCO_5 voltage supplies are required and must both equal the voltage of the attached configuration device, typically either 2.5V or 3.3V.

Assert Low both the chip-select pin, CS_B, and the read/write control pin, RDWR_B, to write the configuration data byte presented on the D0-D7 pins to the FPGA on a rising-edge of the configuration clock, CCLK. The order of CS_B and RDWR_B does not matter, although RDWR_B must be asserted throughout the configuration process. If RDWR_B is de-asserted during configuration, the FPGA aborts the configuration operation.

After configuration, these pins are available as general-purpose user I/O. However, the SelectMAP configuration interface is optionally available for debugging and dynamic reconfiguration. To use these SelectMAP pins after configuration, set the Persist bitstream generation option.

The Readback debugging option, for example, requires the Persist bitstream generation option. During Readback mode, assert CS_B Low, along with RDWR_B High, to read a configuration data byte from the FPGA to the D0-D7 bus on a rising CCLK edge. During Readback mode, D0-D7 are output pins.

In all the cases, the configuration data and control signals are synchronized to the rising edge of the CCLK clock signal.

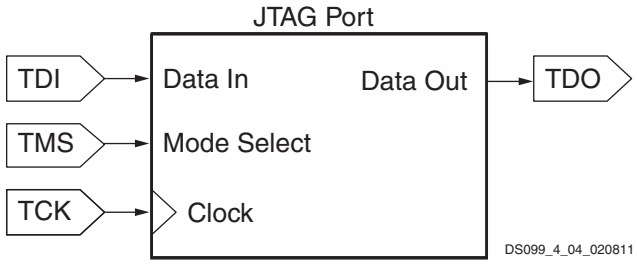

Figure 43: **JTAG Port**

IDCODE Register

Spartan-3 FPGAs contain a 32-bit identification register called the IDCODE register, as defined in the IEEE 1149.1 JTAG standard. The fixed value electrically identifies the manufacture (Xilinx) and the type of device being addressed over a JTAG chain. This register allows the JTAG host to identify the device being tested or programmed via JTAG. See Table 78.

Using JTAG Port After Configuration

The JTAG port is always active and available before, during, and after FPGA configuration. Add the BSCAN_SPARTAN3 primitive to the design to create user-defined JTAG instructions and JTAG chains to communicate with internal logic.

Furthermore, the contents of the User ID register within the JTAG port can be specified as a Bitstream Generation option. By default, the 32-bit User ID register contains `0xFFFFFFFF`.

Table 78: **Spartan-3 JTAG IDCODE Register Values (hexadecimal)**

Part Number	IDCODE Register
XC3S50	0x0140C093
XC3S200	0x01414093
XC3S400	0x0141C093
XC3S1000	0x01428093
XC3S1500	0x01434093
XC3S2000	0x01440093
XC3S4000	0x01448093
XC3S5000	0x01450093

Precautions When Using the JTAG Port in 3.3V Environments

The JTAG port is powered by the +2.5V VCCAUX power supply. When connecting to a 3.3V interface, the JTAG input pins must be current-limited using a series resistor. Similarly, the TDO pin is a CMOS output powered from +2.5V. The TDO output can directly drive a 3.3V input but with reduced noise immunity. See 3.3V-Tolerant Configuration Interface, page 47. See also XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional details.

The following interface precautions are recommended when connecting the JTAG port to a 3.3V interface.

- Avoid actively driving the JTAG input signals High with 3.3V signal levels. If required in the application, use series current-limiting resistors to keep the current below 10 mA per pin.
- If possible, drive the FPGA JTAG inputs with drivers that can be placed in high-impedance (Hi-Z) after using the JTAG port. Alternatively, drive the FPGA JTAG inputs with open-drain outputs, which only drive Low. In both cases, pull-up resistors are required. The FPGA JTAG pins have pull-up resistors to VCCAUX before configuration and optional pull-up resistors after configuration, controlled by Bitstream Options, page 125.

Table 89: **CP132 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	CP132 Ball	Type
2	IO_L24P_2	G13	I/O
2	IO_L40N_2	G14	I/O
2	IO_L40P_2/VREF_2	H12	VREF
3	IO_L01N_3/VRP_3	N13	DCI
3	IO_L01P_3/VRN_3	N14	DCI
3	IO_L20N_3	L12	I/O
3	IO_L20P_3	M14	I/O
3	IO_L22N_3	L14	I/O
3	IO_L22P_3	L13	I/O
3	IO_L23N_3	K13	I/O
3	IO_L23P_3/VREF_3	K12	VREF
3	IO_L24N_3	J12	I/O
3	IO_L24P_3	K14	I/O
3	IO_L40N_3/VREF_3	H14	VREF
3	IO_L40P_3	J13	I/O
4	IO/VREF_4	N12	VREF
4	IO_L01N_4/VRP_4	P12	DCI
4	IO_L01P_4/VRN_4	M11	DCI
4	IO_L27N_4/DIN/D0	M10	DUAL
4	IO_L27P_4/D1	N10	DUAL
4	IO_L30N_4/D2	N9	DUAL
4	IO_L30P_4/D3	P9	DUAL
4	IO_L31N_4/INIT_B	M8	DUAL
4	IO_L31P_4/DOUT/BUSY	N8	DUAL
4	IO_L32N_4/GCLK1	P8	GCLK
4	IO_L32P_4/GCLK0	M7	GCLK
5	IO_L01N_5/RDWR_B	P2	DUAL
5	IO_L01P_5/CS_B	N2	DUAL
5	IO_L27N_5/VREF_5	M4	VREF
5	IO_L27P_5	P3	I/O
5	IO_L28N_5/D6	P4	DUAL
5	IO_L28P_5/D7	N4	DUAL
5	IO_L31N_5/D4	M6	DUAL
5	IO_L31P_5/D5	P5	DUAL
5	IO_L32N_5/GCLK3	P7	GCLK
5	IO_L32P_5/GCLK2	P6	GCLK
6	IO_L01N_6/VRP_6	L3	DCI
6	IO_L01P_6/VRN_6	M1	DCI
6	IO_L20N_6	K3	I/O
6	IO_L20P_6	K2	I/O

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
N/A	GND	T16	GND
N/A	VCCAUX	A6	VCCAUX
N/A	VCCAUX	A11	VCCAUX
N/A	VCCAUX	F1	VCCAUX
N/A	VCCAUX	F16	VCCAUX
N/A	VCCAUX	L1	VCCAUX
N/A	VCCAUX	L16	VCCAUX
N/A	VCCAUX	T6	VCCAUX
N/A	VCCAUX	T11	VCCAUX
N/A	VCCINT	D4	VCCINT
N/A	VCCINT	D13	VCCINT
N/A	VCCINT	E5	VCCINT
N/A	VCCINT	E12	VCCINT
N/A	VCCINT	M5	VCCINT
N/A	VCCINT	M12	VCCINT
N/A	VCCINT	N4	VCCINT
N/A	VCCINT	N13	VCCINT
VCCAUX	CCLK	T15	CONFIG
VCCAUX	DONE	R14	CONFIG
VCCAUX	HSWAP_EN	C4	CONFIG
VCCAUX	M0	P3	CONFIG
VCCAUX	M1	T2	CONFIG
VCCAUX	M2	P4	CONFIG
VCCAUX	PROG_B	B3	CONFIG
VCCAUX	TCK	C14	JTAG
VCCAUX	TDI	A2	JTAG
VCCAUX	TDO	A15	JTAG
VCCAUX	TMS	C13	JTAG

FG320: 320-lead Fine-pitch Ball Grid Array

The 320-lead fine-pitch ball grid array package, FG320, supports three different Spartan-3 devices, including the XC3S400, the XC3S1000, and the XC3S1500. The footprint for all three devices is identical, as shown in Table 98 and Figure 50.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

All the package pins appear in Table 98 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 98: **FG320 Package Pinout**

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
0	IO	D9	I/O
0	IO	E7	I/O
0	IO/VREF_0	B3	VREF
0	IO/VREF_0	D6	VREF
0	IO_L01N_0/VRP_0	A2	DCI
0	IO_L01P_0/VRN_0	A3	DCI
0	IO_L09N_0	B4	I/O
0	IO_L09P_0	C4	I/O
0	IO_L10N_0	C5	I/O
0	IO_L10P_0	D5	I/O
0	IO_L15N_0	A4	I/O
0	IO_L15P_0	A5	I/O
0	IO_L25N_0	B5	I/O
0	IO_L25P_0	B6	I/O
0	IO_L27N_0	C7	I/O
0	IO_L27P_0	D7	I/O
0	IO_L28N_0	C8	I/O
0	IO_L28P_0	D8	I/O
0	IO_L29N_0	E8	I/O
0	IO_L29P_0	F8	I/O
0	IO_L30N_0	A7	I/O
0	IO_L30P_0	A8	I/O
0	IO_L31N_0	B9	I/O
0	IO_L31P_0/VREF_0	A9	VREF
0	IO_L32N_0/GCLK7	E9	GCLK
0	IO_L32P_0/GCLK6	F9	GCLK
0	VCCO_0	B8	VCCO
0	VCCO_0	C6	VCCO
0	VCCO_0	G8	VCCO

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
3	IO_L24N_3	M18	I/O
3	IO_L24P_3	N17	I/O
3	IO_L27N_3	L14	I/O
3	IO_L27P_3	L13	I/O
3	IO_L34N_3	L15	I/O
3	IO_L34P_3/VREF_3	L16	VREF
3	IO_L35N_3	L18	I/O
3	IO_L35P_3	L17	I/O
3	IO_L39N_3	K13	I/O
3	IO_L39P_3	K14	I/O
3	IO_L40N_3/VREF_3	K17	VREF
3	IO_L40P_3	K18	I/O
3	VCCO_3	K12	VCCO
3	VCCO_3	L12	VCCO
3	VCCO_3	N16	VCCO
4	IO	P12	I/O
4	IO	V14	I/O
4	IO/VREF_4	R10	VREF
4	IO/VREF_4	U13	VREF
4	IO/VREF_4	V17	VREF
4	IO_L01N_4/VRP_4	U16	DCI
4	IO_L01P_4/VRN_4	V16	DCI
4	IO_L06N_4/VREF_4	P14	VREF
4	IO_L06P_4	R14	I/O
4	IO_L09N_4	U15	I/O
4	IO_L09P_4	V15	I/O
4	IO_L10N_4	T14	I/O
4	IO_L10P_4	U14	I/O
4	IO_L25N_4	R13	I/O
4	IO_L25P_4	P13	I/O
4	IO_L27N_4/DIN/D0	T12	DUAL
4	IO_L27P_4/D1	R12	DUAL
4	IO_L28N_4	V12	I/O
4	IO_L28P_4	V11	I/O
4	IO_L29N_4	R11	I/O
4	IO_L29P_4	T11	I/O
4	IO_L30N_4/D2	N11	DUAL
4	IO_L30P_4/D3	P11	DUAL
4	IO_L31N_4/INIT_B	U10	DUAL

User I/Os by Bank

Table 101 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S400 in the FG456 package. Similarly, Table 102 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1000, XC3S1500, and XC3S2000 in the FG456 package.

Table 101: **User I/Os Per Bank for XC3S400 in FG456 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	35	27	0	2	4	2
	1	35	27	0	2	4	2
Right	2	31	25	0	2	4	0
	3	31	25	0	2	4	0
Bottom	4	35	21	6	2	4	2
	5	35	21	6	2	4	2
Left	6	31	25	0	2	4	0
	7	31	25	0	2	4	0

Table 102: **User I/Os Per Bank for XC3S1000, XC3S1500, and XC3S2000 in FG456 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	40	31	0	2	5	2
	1	40	31	0	2	5	2
Right	2	43	37	0	2	4	0
	3	43	37	0	2	4	0
Bottom	4	41	26	6	2	5	2
	5	40	25	6	2	5	2
Left	6	43	37	0	2	4	0
	7	43	37	0	2	4	0

Right Half of FG456 Package (Top View)

	Bank 1										
	12	13	14	15	16	17	18	19	20	21	22	
A	I/O	I/O L30N_1	I/O L28N_1	I/O L25P_1	I/O L22N_1 ◆	VCCAUX	I/O L10N_1 VREF_1	I/O L06N_1 VREF_1	TMS	TCK	GND	A
B	I/O L32N_1 GCLK5	I/O L30P_1	I/O L28P_1	I/O L25N_1	I/O L22P_1 ◆	I/O L16N_1	I/O L10P_1	I/O L06P_1	I/O L01P_1 VRN_1	GND	TDO	B
C	I/O L32P_1 GCLK4	I/O L29N_1	GND	VCCO_1	I/O L19N_1 ◆	I/O L16P_1	I/O L09N_1	I/O L01N_1 VRP_1	I/O L01N_2 VRP_2	I/O L01P_2 VRN_2	I/O	C	
D	I/O L31N_1 VREF_1	I/O L29P_1	I/O L27N_1	I/O L24N_1	I/O L19P_1 ◆	I/O L15N_1	I/O L09P_1	I/O L16P_2	I/O L16N_2	I/O L17N_2	I/O L17P_2 VREF_2	D	
E	I/O L31P_1	IO VREF_1	I/O L27P_1	I/O L24P_1	I/O	I/O L15P_1	I/O L19N_2	I/O L20N_2	I/O L20P_2	I/O L21N_2	I/O L21P_2	E	
F	I/O	I/O	IO VREF_1 ◆	VCCO_1	I/O	I/O	I/O L19P_2	I/O L23N_2 VREF_2	I/O L24N_2	I/O L24P_2	VCCAUX	F	
G	VCCO_1	VCCO_1	VCCO_1	VCCINT	VCCINT	I/O L22N_2	I/O L22P_2	I/O L23P_2	I/O L26N_2 ◆	I/O L27N_2	I/O L27P_2	G	Bank 2
H					VCCINT	VCCO_2	I/O L28N_2 ◆	I/O L26P_2 ◆	VCCO_2	I/O L29N_2 ◆	I/O L29P_2 ◆	H	
J	GND	GND	GND		VCCO_2	I/O L28P_2 ◆	I/O L31N_2 ◆	I/O L31P_2 ◆	GND	I/O L32N_2 ◆	I/O L32P_2 ◆	J	
K	GND	GND	GND		VCCO_2	I/O L33N_2 ◆	I/O L33P_2 ◆	I/O L34N_2 VREF_2	I/O L34P_2	I/O L35N_2	I/O L35P_2	K	
L	GND	GND	GND		VCCO_2	I/O L38N_2	I/O L38P_2	I/O L39N_2	I/O L39P_2	I/O L40N_2	I/O L40P_2 VREF_2	L	
M	GND	GND	GND		VCCO_3	I/O L38P_3	I/O L38N_3	I/O L39P_3	I/O L39N_3	I/O L40P_3	I/O L40N_3 VREF_3	M	
N	GND	GND	GND		VCCO_3	I/O L33P_3 ◆	I/O L33N_3 ◆	I/O L34P_3 VREF_3	I/O L34N_3	I/O L35P_3	I/O L35N_3	N	
P	GND	GND	GND		VCCO_3	I/O L31P_3 ◆	I/O L31N_3 ◆	I/O L29N_3 ◆	GND	I/O L32P_3 ◆	I/O L32N_3 ◆	P	
R					VCCINT	VCCO_3	I/O L24N_3	I/O L29P_3 ◆	VCCO_3	I/O L28P_3 ◆	I/O L28N_3 ◆	R	
T	VCCO_4	VCCO_4	VCCO_4	VCCINT	VCCINT	I/O L22N_3	I/O L24P_3	I/O L26P_3 ◆	I/O L26N_3 ◆	I/O L27P_3	I/O L27N_3	T	Bank 3
U	I/O L30N_4 D2	I/O L28N_4	I/O L25N_4	VCCO_4	I/O	I/O	I/O L22P_3	I/O L20N_3	I/O L23P_3 VREF_3	I/O L23N_3	VCCAUX	U	
V	I/O L30P_4 D3	I/O L28P_4	I/O L25P_4	I/O L22N_4 VREF_4 ◆	I/O L16N_4	I/O L10N_4	IO VREF_4	I/O L17N_3	I/O L20P_3	I/O L21P_3	I/O L21N_3	V	
W	I/O L31N_4 INIT_B	I/O	I/O	I/O L22P_4 ◆	I/O L16P_4	I/O L10P_4	I/O L06N_4 VREF_4	I/O L17P_3 VREF_3	I/O L19P_3	I/O L19N_3	I/O L16N_3	W	
Y	I/O L31P_4 DOUT BUSY	I/O L29N_4	GND	VCCO_4	IO VREF_4	I/O L15N_4	I/O L06P_4	I/O L01P_3 VRN_3	I/O L01N_3 VRP_3	I/O	I/O L16P_3	Y	
AA	I/O L32N_4 GCLK1	I/O L29P_4	I/O L27N_4 DN D0	I/O L24N_4	I/O L19N_4 ◆	I/O L15P_4	I/O L09N_4	I/O L05N_4 ◆	I/O L01N_4 VRP_4	GND	CCLK	AA	
AB	I/O L32P_4 GCLK0	IO VREF_4	I/O L27P_4 D1	I/O L24P_4	I/O L19P_4 ◆	VCCAUX	I/O L09P_4	I/O L05P_4 ◆	I/O L01P_4 VRN_4	DONE	GND	AB	
		Bank 4											

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Figure 52: FG456 Package Footprint (Top View) Continued

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
7	VCCO_7	VCCO_7	N3	VCCO
7	VCCO_7	VCCO_7	G5	VCCO
7	VCCO_7	VCCO_7	J7	VCCO
7	VCCO_7	VCCO_7	N7	VCCO
7	VCCO_7	VCCO_7	L9	VCCO
7	VCCO_7	VCCO_7	M11	VCCO
7	VCCO_7	VCCO_7	N11	VCCO
7	VCCO_7	VCCO_7	P11	VCCO
N/A	GND	GND	A1	GND
N/A	GND	GND	B1	GND
N/A	GND	GND	F1	GND
N/A	GND	GND	K1	GND
N/A	GND	GND	P1	GND
N/A	GND	GND	U1	GND
N/A	GND	GND	AA1	GND
N/A	GND	GND	AE1	GND
N/A	GND	GND	AJ1	GND
N/A	GND	GND	AK1	GND
N/A	GND	GND	A2	GND
N/A	GND	GND	B2	GND
N/A	GND	GND	AJ2	GND
N/A	GND	GND	E5	GND
N/A	GND	GND	K5	GND
N/A	GND	GND	P5	GND
N/A	GND	GND	U5	GND
N/A	GND	GND	AA5	GND
N/A	GND	GND	AF5	GND
N/A	GND	GND	A6	GND
N/A	GND	GND	AK6	GND
N/A	GND	GND	K8	GND
N/A	GND	GND	P8	GND
N/A	GND	GND	U8	GND
N/A	GND	GND	AA8	GND
N/A	GND	GND	A10	GND
N/A	GND	GND	E10	GND
N/A	GND	GND	H10	GND
N/A	GND	GND	AC10	GND
N/A	GND	GND	AF10	GND
N/A	GND	GND	AK10	GND
N/A	GND	GND	R12	GND

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L03P_3	IO_L03P_3	AK32	I/O
3	IO_L04N_3	IO_L04N_3	AJ32	I/O
3	IO_L04P_3	IO_L04P_3	AJ31	I/O
3	IO_L05N_3	IO_L05N_3	AJ34	I/O
3	IO_L05P_3	IO_L05P_3	AJ33	I/O
3	IO_L06N_3	IO_L06N_3	AH30	I/O
3	IO_L06P_3	IO_L06P_3	AH29	I/O
3	IO_L07N_3	IO_L07N_3	AG30	I/O
3	IO_L07P_3	IO_L07P_3	AG29	I/O
3	IO_L08N_3	IO_L08N_3	AG34	I/O
3	IO_L08P_3	IO_L08P_3	AG33	I/O
3	IO_L09N_3	IO_L09N_3	AF29	I/O
3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	AF28	VREF
3	IO_L10N_3	IO_L10N_3	AF31	I/O
3	IO_L10P_3	IO_L10P_3	AG31	I/O
3	IO_L11N_3	IO_L11N_3	AF33	I/O
3	IO_L11P_3	IO_L11P_3	AF32	I/O
3	IO_L12N_3	IO_L12N_3	AE26	I/O
3	IO_L12P_3	IO_L12P_3	AF27	I/O
3	IO_L13N_3/VREF_3	IO_L13N_3/VREF_3	AE28	VREF
3	IO_L13P_3	IO_L13P_3	AE27	I/O
3	IO_L14N_3	IO_L14N_3	AE30	I/O
3	IO_L14P_3	IO_L14P_3	AE29	I/O
3	IO_L15N_3	IO_L15N_3	AE32	I/O
3	IO_L15P_3	IO_L15P_3	AE31	I/O
3	IO_L16N_3	IO_L16N_3	AE34	I/O
3	IO_L16P_3	IO_L16P_3	AE33	I/O
3	IO_L17N_3	IO_L17N_3	AD26	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	AD25	VREF
3	IO_L19N_3	IO_L19N_3	AD34	I/O
3	IO_L19P_3	IO_L19P_3	AD33	I/O
3	IO_L20N_3	IO_L20N_3	AC25	I/O
3	IO_L20P_3	IO_L20P_3	AC24	I/O
3	IO_L21N_3	IO_L21N_3	AC28	I/O
3	IO_L21P_3	IO_L21P_3	AC27	I/O
3	IO_L22N_3	IO_L22N_3	AC30	I/O
3	IO_L22P_3	IO_L22P_3	AC29	I/O
3	IO_L23N_3	IO_L23N_3	AC32	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	AC31	VREF
3	IO_L24N_3	IO_L24N_3	AB25	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
4	VCCO_4	VCCO_4	AC19	VCCO
4	VCCO_4	VCCO_4	AC20	VCCO
4	VCCO_4	VCCO_4	AC21	VCCO
4	VCCO_4	VCCO_4	AC22	VCCO
4	VCCO_4	VCCO_4	AG20	VCCO
4	VCCO_4	VCCO_4	AG24	VCCO
4	VCCO_4	VCCO_4	AH27	VCCO
4	VCCO_4	VCCO_4	AJ22	VCCO
4	VCCO_4	VCCO_4	AL19	VCCO
4	VCCO_4	VCCO_4	AL24	VCCO
4	VCCO_4	VCCO_4	AM27	VCCO
4	VCCO_4	VCCO_4	AM31	VCCO
4	VCCO_4	VCCO_4	AN22	VCCO
5	IO	IO	AD11	I/O
5	N.C. (◆)	IO	AD12	I/O
5	IO	IO	AD14	I/O
5	IO	IO	AD15	I/O
5	IO	IO	AD16	I/O
5	IO	IO	AD17	I/O
5	IO	IO	AE14	I/O
5	IO	IO	AE16	I/O
5	N.C. (◆)	IO	AF9	I/O
5	IO	IO	AG9	I/O
5	IO	IO	AG12	I/O
5	IO	IO	AJ6	I/O
5	IO	IO	AJ17	I/O
5	IO	IO	AK10	I/O
5	IO	IO	AK14	I/O
5	IO	IO	AM12	I/O
5	IO	IO	AN9	I/O
5	IO/VREF_5	IO/VREF_5	AJ8	VREF
5	IO/VREF_5	IO/VREF_5	AL5	VREF
5	IO/VREF_5	IO/VREF_5	AP17	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	AP3	DUAL
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AN3	DUAL
5	IO_L02N_5	IO_L02N_5	AP4	I/O
5	IO_L02P_5	IO_L02P_5	AN4	I/O
5	IO_L03N_5	IO_L03N_5	AN5	I/O
5	IO_L03P_5	IO_L03P_5	AM5	I/O
5	IO_L04N_5	IO_L04N_5	AM6	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	GND	GND	AA18	GND
N/A	GND	GND	AA19	GND
N/A	GND	GND	AA20	GND
N/A	GND	GND	AA21	GND
N/A	GND	GND	AB1	GND
N/A	GND	GND	AB17	GND
N/A	GND	GND	AB18	GND
N/A	GND	GND	AB26	GND
N/A	GND	GND	AB30	GND
N/A	GND	GND	AB34	GND
N/A	GND	GND	AB5	GND
N/A	GND	GND	AB9	GND
N/A	GND	GND	AD3	GND
N/A	GND	GND	AD32	GND
N/A	GND	GND	AE10	GND
N/A	GND	GND	AE25	GND
N/A	GND	GND	AF1	GND
N/A	GND	GND	AF13	GND
N/A	GND	GND	AF16	GND
N/A	GND	GND	AF19	GND
N/A	GND	GND	AF22	GND
N/A	GND	GND	AF30	GND
N/A	GND	GND	AF34	GND
N/A	GND	GND	AF5	GND
N/A	GND	GND	AH28	GND
N/A	GND	GND	AH7	GND
N/A	GND	GND	AK1	GND
N/A	GND	GND	AK13	GND
N/A	GND	GND	AK16	GND
N/A	GND	GND	AK19	GND
N/A	GND	GND	AK22	GND
N/A	GND	GND	AK26	GND
N/A	GND	GND	AK30	GND
N/A	GND	GND	AK34	GND
N/A	GND	GND	AK5	GND
N/A	GND	GND	AK9	GND
N/A	GND	GND	AM11	GND
N/A	GND	GND	AM24	GND
N/A	GND	GND	AM3	GND
N/A	GND	GND	AM32	GND

User I/Os by Bank

Note: The FG(G)1156 package is discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Table 111 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S4000 in the FG1156 package. Similarly, Table 112 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S5000 in the FG1156 package.

Table 111: **User I/Os Per Bank for XC3S4000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	90	79	0	2	7	2
	1	90	79	0	2	7	2
Right	2	88	80	0	2	6	0
	3	88	79	0	2	7	0
Bottom	4	90	73	6	2	7	2
	5	90	73	6	2	7	2
Left	6	88	79	0	2	7	0
	7	88	79	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

Table 112: **User I/Os Per Bank for XC3S5000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	100	89	0	2	7	2
	1	100	89	0	2	7	2
Right	2	96	87	0	2	7	0
	3	96	87	0	2	7	0
Bottom	4	100	83	6	2	7	2
	5	100	83	6	2	7	2
Left	6	96	87	0	2	7	0
	7	96	87	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.