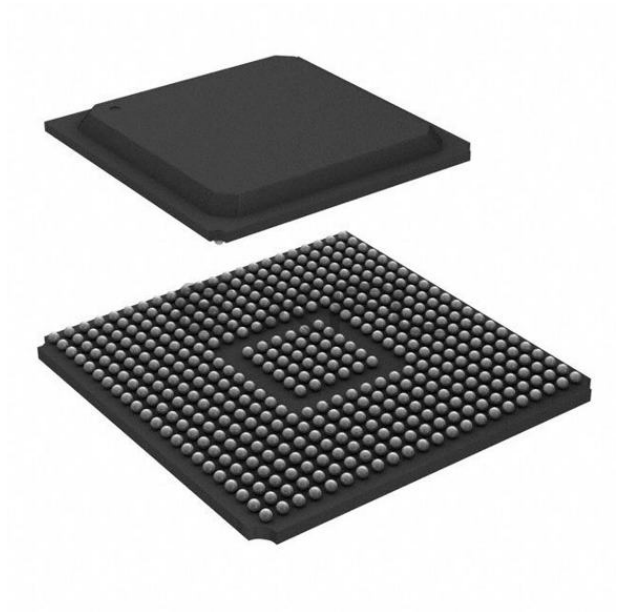
# AMD Xilinx - XC3S1000-5FGG456C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 1920 |
| Number of Logic Elements/Cells | 17280 |
| Total RAM Bits | 442368 |
| Number of I/O | 333 |
| Number of Gates | 1000000 |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 456-BBGA |
| Supplier Device Package | 456-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc3s1000-5fgg456c |

power, the configuration data is written to the FPGA using any of five different modes: Master Parallel, Slave Parallel, Master Serial, Slave Serial, and Boundary Scan (JTAG). The Master and Slave Parallel modes use an 8-bit-wide SelectMAP port.

The recommended memory for storing the configuration data is the low-cost Xilinx Platform Flash PROM family, which includes the XCF00S PROMs for serial configuration and the higher density XCF00P PROMs for parallel or serial configuration.

## I/O Capabilities

The SelectIO feature of Spartan-3 devices supports eighteen single-ended standards and eight differential standards as listed in Table 2. Many standards support the DCI feature, which uses integrated terminations to eliminate unwanted signal reflections.

*Table 2:* **Signal Standards Supported by the Spartan-3 Family**

| Standard Category | Description | $V_{CCO}$ (V) | Class | Symbol (IOSTANDARD) | DCI Option |
|---|---|---|---|---|---|
| **Single-Ended** | | | | | |
| GTL | Gunning Transceiver Logic | N/A | Terminated | GTL | Yes |
| | | | Plus | GTLP | Yes |
| HSTL | High-Speed Transceiver Logic | 1.5 | I | HSTL_I | Yes |
| | | | III | HSTL_III | Yes |
| | | 1.8 | I | HSTL_I_18 | Yes |
| | | | II | HSTL_II_18 | Yes |
| | | | III | HSTL_III_18 | Yes |
| LVCMOS | Low-Voltage CMOS | 1.2 | N/A | LVCMOS12 | No |
| | | 1.5 | N/A | LVCMOS15 | Yes |
| | | 1.8 | N/A | LVCMOS18 | Yes |
| | | 2.5 | N/A | LVCMOS25 | Yes |
| | | 3.3 | N/A | LVCMOS33 | Yes |
| LVTTL | Low-Voltage Transistor-Transistor Logic | 3.3 | N/A | LVTTL | No |
| PCI | Peripheral Component Interconnect | 3.0 | 33 MHz(1) | PCI33_3 | No |
| SSTL | Stub Series Terminated Logic | 1.8 | N/A (±6.7 mA) | SSTL18_I | Yes |
| | | | N/A (±13.4 mA) | SSTL18_II | No |
| | | 2.5 | I | SSTL2_I | Yes |
| | | | II | SSTL2_II | Yes |
| **Differential** | | | | | |
| LDT (ULVDS) | Lightning Data Transport (HyperTransport™) Logic | 2.5 | N/A | LDT_25 | No |
| LVDS | Low-Voltage Differential Signaling | | Standard | LVDS_25 | Yes |
| | | | Bus | BLVDS_25 | No |
| | | | Extended Mode | LVDSEXT_25 | Yes |
| LVPECL | Low-Voltage Positive Emitter-Coupled Logic | 2.5 | N/A | LVPECL_25 | No |
| RSDS | Reduced-Swing Differential Signaling | 2.5 | N/A | RSDS_25 | No |
| HSTL | Differential High-Speed Transceiver Logic | 1.8 | II | DIFF_HSTL_II_18 | Yes |
| SSTL | Differential Stub Series Terminated Logic | 2.5 | II | DIFF_SSTL2_II | Yes |

**Notes:**

1. 66 MHz PCI is not supported by the Xilinx IP core although PCI66_3 is an available I/O standard.

According to Figure 7, the clock line OTCLK1 connects the CK inputs of the upper registers on the output and three-state paths. Similarly, OTCLK2 connects the CK inputs for the lower registers on the output and three-state paths. The upper and lower registers on the input path have independent clock lines: ICLK1 and ICLK2. The enable line OCE connects the CE inputs of the upper and lower registers on the output path. Similarly, TCE connects the CE inputs for the register pair on the three-state path and ICE does the same for the register pair on the input path. The Set/Reset (SR) line entering the IOB is common to all six registers, as is the Reverse (REV) line.

Each storage element supports numerous options in addition to the control over signal polarity described in the IOB Overview section. These are described in Table 6.

*Table 6:* **Storage Element Options**

| Option Switch | Function | Specificity |
|---|---|---|
| FF/Latch | Chooses between an edge-sensitive flip-flop or a level-sensitive latch | Independent for each storage element. |
| SYNC/ASYNC | Determines whether SR is synchronous or asynchronous | Independent for each storage element. |
| SRHIGH/SRLOW | Determines whether SR acts as a Set, which forces the storage element to a logic “1" (SRHIGH) or a Reset, which forces a logic “0” (SRLOW). | Independent for each storage element, except when using FDDR. In the latter case, the selection for the upper element (OFF1 or TFF2) applies to both elements. |
| INIT1/INIT0 | In the event of a Global Set/Reset, after configuration or upon activation of the GSR net, this switch decides whether to set or reset a storage element. By default, choosing SRLOW also selects INIT0; choosing SRHIGH also selects INIT1. | Independent for each storage element, except when using FDDR. In the latter case, selecting INIT0 for one element applies to both elements (even though INIT1 is selected for the other). |

## Double-Data-Rate Transmission

Double-Data-Rate (DDR) transmission describes the technique of synchronizing signals to both the rising and falling edges of the clock signal. Spartan-3 devices use register-pairs in all three IOB paths to perform DDR operations.

The pair of storage elements on the IOB’s Output path (OFF1 and OFF2), used as registers, combine with a special multiplexer to form a DDR D-type flip-flop (FDDR). This primitive permits DDR transmission where output data bits are synchronized to both the rising and falling edges of a clock. It is possible to access this function by placing either an FDDRRSE or an FDDRCPE component or symbol into the design. DDR operation requires two clock signals (50% duty cycle), one the inverted form of the other. These signals trigger the two registers in alternating fashion, as shown in Figure 8. Commonly, the Digital Clock Manager (DCM) generates the two clock signals by mirroring an incoming signal, then shifting it 180 degrees. This approach ensures minimal skew between the two signals.

The storage-element-pair on the Three-State path (TFF1 and TFF2) can also be combined with a local multiplexer to form an FDDR primitive. This permits synchronizing the output enable to both the rising and falling edges of a clock. This DDR operation is realized in the same way as for the output path.

The storage-element-pair on the input path (IFF1 and IFF2) allows an I/O to receive a DDR signal. An incoming DDR clock signal triggers one register and the inverted clock signal triggers the other register. In this way, the registers take turns capturing bits of the incoming DDR data signal.