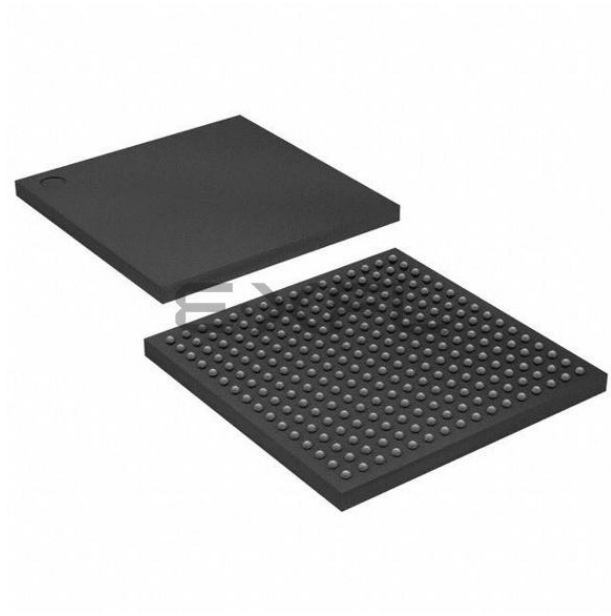
AMD Xilinx - XC3S1000-5FTG256C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1920
Number of Logic Elements/Cells	17280
Total RAM Bits	442368
Number of I/O	173
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1000-5ftg256c

Supply Voltages for the IOBs

Three different supplies power the IOBs:

- The V_{CCO} supplies, one for each of the FPGA's I/O banks, power the output drivers, except when using the GTL and GTLP signal standards. The voltage on the V_{CCO} pins determines the voltage swing of the output signal.
- V_{CCINT} is the main power supply for the FPGA's internal logic.
- The V_{CCAUX} is an auxiliary source of power, primarily to optimize the performance of various FPGA functions such as I/O switching.

The I/Os During Power-On, Configuration, and User Mode

With no power applied to the FPGA, all I/Os are in a high-impedance state. The V_{CCINT} (1.2V), V_{CCAUX} (2.5V), and V_{CCO} supplies may be applied in any order. Before power-on can finish, V_{CCINT}, V_{CCO} Bank 4, and V_{CCAUX} must have reached their respective minimum recommended operating levels (see Table 29, page 59). At this time, all I/O drivers also will be in a high-impedance state. V_{CCO} Bank 4, V_{CCINT}, and V_{CCAUX} serve as inputs to the internal Power-On Reset circuit (POR).

A Low level applied to the HSWAP_EN input enables pull-up resistors on User I/Os from power-on throughout configuration. A High level on HSWAP_EN disables the pull-up resistors, allowing the I/Os to float. If the HSWAP_EN pin is floating, then an internal pull-up resistor pulls HSWAP_EN High. As soon as power is applied, the FPGA begins initializing its configuration memory. At the same time, the FPGA internally asserts the Global Set-Reset (GSR), which asynchronously resets all IOB storage elements to a Low state.

Upon the completion of initialization, INIT_B goes High, sampling the M0, M1, and M2 inputs to determine the configuration mode. At this point, the configuration data is loaded into the FPGA. The I/O drivers remain in a high-impedance state (with or without pull-up resistors, as determined by the HSWAP_EN input) throughout configuration.

The Global Three State (GTS) net is released during Start-Up, marking the end of configuration and the beginning of design operation in the User mode. At this point, those I/Os to which signals have been assigned go active while all unused I/Os remain in a high-impedance state. The release of the GSR net, also part of Start-up, leaves the IOB registers in a Low state by default, unless the loaded design reverses the polarity of their respective RS inputs.

In User mode, all internal pull-up resistors on the I/Os are disabled and HSWAP_EN becomes a "don't care" input. If it is desirable to have pull-up or pull-down resistors on I/Os carrying signals, the appropriate symbol—e.g., PULLUP, PULLDOWN—must be placed at the appropriate pads in the design. The Bitstream Generator (Bitgen) option UnusedPin available in the Xilinx development software determines whether unused I/Os collectively have pull-up resistors, pull-down resistors, or no resistors in User mode.

CLB Overview

For more details on the CLBs, refer to the chapter entitled "Using Configurable Logic Blocks" in UG331.

The Configurable Logic Blocks (CLBs) constitute the main logic resource for implementing synchronous as well as combinatorial circuits. Each CLB comprises four interconnected slices, as shown in Figure 11. These slices are grouped in pairs. Each pair is organized as a column with an independent carry chain.

The nomenclature that the FPGA Editor—part of the Xilinx development software—uses to designate slices is as follows: The letter 'X' followed by a number identifies columns of slices. The 'X' number counts up in sequence from the left side of the die to the right. The letter 'Y' followed by a number identifies the position of each slice in a pair as well as indicating the CLB row. The 'Y' number counts slices starting from the bottom of the die according to the sequence: 0, 1, 0, 1 (the first CLB row); 2, 3, 2, 3 (the second CLB row); etc. Figure 11 shows the CLB located in the lower left-hand corner of the die. Slices X0Y0 and X0Y1 make up the column-pair on the left where as slices X1Y0 and X1Y1 make up the column-pair on the right. For each CLB, the term "left-hand" (or SLICEM) indicates the pair of slices labeled with an even 'X' number, such as X0, and the term "right-hand" (or SLICEL) designates the pair of slices with an odd 'X' number, e.g., X1.

Configuration

Spartan-3 devices are configured by loading application specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are "Dedicated" to one function only, while others, indicated by the term "Dual-Purpose", can be re-used as general-purpose User I/Os once configuration is complete.

Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M0, M1, and M2 are Dedicated pins. The mode pin settings are shown in Table 26.

Table 26: **Spartan-3 FPGAs Configuration Mode Pin Settings**

Configuration Mode(1)	M0	M1	M2	Synchronizing Clock	Data Width	Serial DOUT(2)
Master Serial	0	0	0	CCLK Output	1	Yes
Slave Serial	1	1	1	CCLK Input	1	Yes
Master Parallel	1	1	0	CCLK Output	8	No
Slave Parallel	0	1	1	CCLK Input	8	No
JTAG	1	0	1	TCK Input	1	No

Notes:

1. The voltage levels on the M0, M1, and M2 pins select the configuration mode.
2. The daisy chain is possible only in the Serial modes when DOUT is used.

The HSWAP_EN input pin defines whether the I/O pins that are not actively used during configuration have pull-up resistors during configuration. By default, HSWAP_EN is tied High (via an internal pull-up resistor if left floating) which shuts off the pull-up resistors on the user I/O pins during configuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration. The Dedicated configuration pins (CCLK, DONE, PROG_B, M2, M1, M0, HSWAP_EN) and the JTAG pins (TDI, TMS, TCK, and TDO) always have a pull-up resistor to VCCAUX during configuration, regardless of the value on the HSWAP_EN pin. Similarly, the dual-purpose INIT_B pin has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM, depending on the package style.

Depending on the chosen configuration mode, the FPGA either generates a CCLK output, or CCLK is an input accepting an externally generated clock.

A persist option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected then the configuration pins with the exception of CCLK, PROG_B, and DONE can be used as user I/O in normal operation. The persist option does not apply to the boundary-scan related pins. The persist feature is valuable in applications that readback configuration data after entering the User mode.

Table 27 lists the total number of bits required to configure each FPGA as well as the PROMs suitable for storing those bits. See DS123: *Platform Flash In-System Programmable Configuration PROMs* data sheet for more information.

Table 27: **Spartan-3 FPGA Configuration Data**

Device	File Sizes	Xilinx Platform Flash PROM	
		Serial Configuration	Parallel Configuration
XC3S50	439,264	XCF01S	XCF08P
XC3S200	1,047,616	XCF01S	XCF08P
XC3S400	1,699,136	XCF02S	XCF08P
XC3S1000	3,223,488	XCF04S	XCF08P
XC3S1500	5,214,784	XCF08P	XCF08P
XC3S2000	7,673,024	XCF08P	XCF08P
XC3S4000	11,316,864	XCF16P	XCF16P
XC3S5000	13,271,936	XCF16P	XCF16P

The maximum bitstream length that Spartan-3 FPGAs support in serial daisy-chains is 4,294,967,264 bits (4 Gbits), roughly equivalent to a daisy-chain with 323 XC3S5000 FPGAs. This is a limit only for serial daisy-chains where configuration data is passed via the FPGA's DOUT pin. There is no such limit for JTAG chains.

Table 45: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max[3]	Max[3]	
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OTCLK input to data appearing at the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.46	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.94	2.23	ns
T_{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin		XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	XC3S200 XC3S400	2.10	2.41	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	2.77	3.18	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) net to setting/resetting data at the Output pin		All	8.07	9.28	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 47.
3. For minimums, use the values reported by the Xilinx timing analyzer.

Table 48: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
HSTL_III_DCI_18							
LVCMOS12		-	0	1.2	1M	0	0.6
LVCMOS15		-	0	1.5	1M	0	0.75
LVDCI_15							
LVDCI_DV2_15							
HSLVDCI_15							
LVCMOS18		-	0	1.8	1M	0	0.9
LVDCI_18							
LVDCI_DV2_18							
HSLVDCI_18							
LVCMOS25		-	0	2.5	1M	0	1.25
LVDCI_25							
LVDCI_DV2_25							
HSLVDCI_25							
LVCMOS33		-	0	3.3	1M	0	1.65
LVDCI_33							
LVDCI_DV2_33							
HSLVDCI_33							
LVTTL		-	0	3.3	1M	0	1.4
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_I_DCI							
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_I_DCI							
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL2_II_DCI					50	1.25	
Differential							
LDT_25 (ULVDS_25)		-	V_{ICM} – 0.125	V_{ICM} + 0.125	60	0.6	V_{ICM}
LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_25_DCI					N/A	N/A	
BLVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
LVDSEXT_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDSEXT_25_DCI					N/A	N/A	
LVPECL_25		-	V_{ICM} – 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25		-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
DIFF_HSTL_II_18		-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.8	V_{ICM}
DIFF_HSTL_II_18_DCI							

Spartan-3 FPGA Family: Pinout Descriptions

DS099 (v3.0) October 29, 2012 **Product Specification**

Introduction

This data sheet module describes the various pins on a Spartan®-3 FPGA and how they connect to the supported component packages.

- The Pin Types section categorizes all of the FPGA pins by their function type.
- The Pin Definitions section provides a top-level description for each pin on the device.
- The Detailed, Functional Pin Descriptions section offers significantly more detail about each pin, especially for the dual- or special-function pins used during device configuration.
- Some pins have associated behavior that is controlled by settings in the configuration bitstream. These options are described in the Bitstream Options section.
- The Package Overview section describes the various packaging options available for Spartan-3 FPGAs. Detailed pin list tables and footprint diagrams are provided for each package solution.

Pin Descriptions

Pin Types

A majority of the pins on a Spartan-3 FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3 device packages, as outlined in Table 69. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 69: **Types of Pins on Spartan-3 FPGAs**

Pin Type/ Color Code	Description	Pin Name
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO, IO_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. There are 12 dual-purpose configuration pins on every package. The INIT_B pin has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM during configuration.	IO_Lxxy_#/DIN/D0, IO_Lxxy_#/D1, IO_Lxxy_#/D2, IO_Lxxy_#/D3, IO_Lxxy_#/D4, IO_Lxxy_#/D5, IO_Lxxy_#/D6, IO_Lxxy_#/D7, IO_Lxxy_#/CS_B, IO_Lxxy_#/RDWR_B, IO_Lxxy_#/BUSY/DOUT, IO_Lxxy_#/INIT_B
CONFIG	Dedicated configuration pin. Not available as a user-I/O pin. Every package has seven dedicated configuration pins. These pins are powered by VCCAUX and have a dedicated internal pull-up resistor to VCCAUX during configuration.	CCLK, DONE, M2, M1, M0, PROG_B, HSWAP_EN
JTAG	Dedicated JTAG pin. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX and have a dedicated internal pull-up resistor to VCCAUX during configuration.	TDI, TMS, TCK, TDO
DCI	Dual-purpose pin that is either a user-I/O pin or used to calibrate output buffer impedance for a specific bank using Digital Controlled Impedance (DCI). There are two DCI pins per I/O bank.	IO/VRN_# IO_Lxxy_#/VRN_# IO/VRP_# IO_Lxxy_#/VRP_#

Table 72: **Dual-Purpose Configuration Pins for Parallel (SelectMAP) Configuration Modes *(Cont'd)***

<table>
<tr><th>Pin Name</th><th>Direction</th><th>Description</th></tr>
<tr><td>BUSY</td><td>Output</td><td>Configuration Data Rate Control for Parallel Mode:
In the Slave and Master Parallel modes, BUSY throttles the rate at which configuration data is loaded. BUSY is only necessary if CCLK operates at greater than 50 MHz. Ignore BUSY for frequencies of 50 MHz and below.
When BUSY is Low, the FPGA accepts the next configuration data byte on the next rising CCLK edge for which CS_B and RDWR_B are Low. When BUSY is High, the FPGA ignores the next configuration data byte. The next configuration data value must be held or reloaded until the next rising CCLK edge when BUSY is Low. When CS_B is High, BUSY is in a high impedance state.
<table><tr><th>BUSY</th><th>Function</th></tr><tr><td>0</td><td>The FPGA is ready to accept the next configuration data byte.</td></tr><tr><td>1</td><td>The FPGA is busy processing the current configuration data byte and is not ready to accept the next byte.</td></tr><tr><td>Hi-Z</td><td>If CS_B is High, then BUSY is high impedance.</td></tr></table>This signal is located in Bank 4 and its output voltage is determined by VCCO_4. The BitGen option Persist permits this pin to retain its configuration function in the User mode.</td></tr>
<tr><td>INIT_B</td><td>Bidirectional (open-drain)</td><td>Initializing Configuration Memory/Configuration Error (active-Low):
See description under Serial Configuration Modes, page 112.</td></tr>
</table>

JTAG Configuration Mode

In the JTAG configuration mode all dual-purpose configuration pins are unused and behave exactly like user-I/O pins, as shown in Table 79. See Table 75 for Mode Select pin settings required for JTAG mode.

Dual-Purpose Pin I/O Standard During Configuration

During configuration, the dual-purpose pins default to CMOS input and output levels for the associated VCCO voltage supply pins. For example, in the Parallel configuration modes, both VCCO_4 and VCCO_5 are required. If connected to +2.5V, then the associated pins conform to the LVCMOS25 I/O standard. If connected to +3.3V, then the pins drive LVCMOS output levels and accept either LVTTL or LVCMOS input levels.

Dual-Purpose Pin Behavior After Configuration

After the configuration process completes, these pins, if they were borrowed during configuration, become user-I/O pins available to the application. If a dual-purpose configuration pin is not used during the configuration process—*i.e.*, the parallel configuration pins when using serial mode—then the pin behaves exactly like a general-purpose I/O. See I/O Type: Unrestricted, General-purpose I/O Pins section.

DCI: User I/O or Digitally Controlled Impedance Resistor Reference Input

These pins are individual user-I/O pins unless one of the I/O standards used in the bank requires the Digitally Controlled Impedance (DCI) feature. If DCI is used, then 1% precision resistors connected to the VRP_# and VRN_# pins match the impedance on the input or output buffers of the I/O standards that use DCI within the bank. The '#' character in the pin name indicates the associated I/O bank and is an integer, 0 through 7.

There are two DCI pins per I/O bank, except in the CP132 and TQ144 packages, which do not have any DCI inputs for Bank 5.

VRP and VRN Impedance Resistor Reference Inputs

The 1% precision impedance-matching resistor attached to the VRP_# pin controls the pull-up impedance of PMOS transistor in the input or output buffer. Consequently, the VRP_# pin must connect to ground. The 'P' character in "VRP" indicates that this pin controls the I/O buffer's PMOS transistor impedance. The VRP_# pin is used for both single and split termination.

VREF: User I/O or Input Buffer Reference Voltage for Special Interface Standards

These pins are individual user-I/O pins unless collectively they supply an input reference voltage, VREF_#, for any SSTL, HSTL, GTL, or GTLP I/Os implemented in the associated I/O bank. The '#' character in the pin name represents an integer, 0 through 7, that indicates the associated I/O bank.

The VREF function becomes active for this pin whenever a signal standard requiring a reference voltage is used in the associated bank. If used as a user I/O, then each pin behaves as an independent I/O described in the I/O type section. If used for a reference voltage within a bank, then *all* VREF pins within the bank must be connected to the same reference voltage.

Spartan-3 devices are designed and characterized to support certain I/O standards when VREF is connected to +1.25V, +1.10V, +1.00V, +0.90V, +0.80V, and +0.75V. During configuration, the VREF pins behave exactly like user-I/O pins.

If designing for footprint compatibility across the range of devices in a specific package, and if the VREF_# pins within a bank connect to an input reference voltage, then also connect any N.C. (not connected) pins on the smaller devices in that package to the input reference voltage. More details are provided later for each package type.

N.C. Type: Unconnected Package Pins

Pins marked as "N.C." are unconnected for the specific device/package combination. For other devices in this same package, this pin may be used as an I/O or VREF connection. In both the pinout tables and the footprint diagrams, unconnected pins are noted with either a black diamond symbol (◆) or a black square symbol (■).

If designing for footprint compatibility across multiple device densities, check the pin types of the other Spartan-3 devices available in the same footprint. If the N.C. pin matches to VREF pins in other devices, and the VREF pins are used in the associated I/O bank, then connect the N.C. to the VREF voltage source.

VCCO Type: Output Voltage Supply for I/O Bank

Each I/O bank has its own set of voltage supply pins that determines the output voltage for the output buffers in the I/O bank. Furthermore, for some I/O standards such as LVCMOS, LVCMOS25, LVTTL, etc., VCCO sets the input threshold voltage on the associated input buffers.

Spartan-3 devices are designed and characterized to support various I/O standards for VCCO values of +1.2V, +1.5V, +1.8V, +2.5V, and +3.3V.

Most VCCO pins are labeled as VCCO_# where the '#' symbol represents the associated I/O bank number, an integer ranging from 0 to 7. In the 144-pin TQFP package (TQ144) however, the VCCO pins along an edge of the device are combined into a single VCCO input. For example, the VCCO inputs for Bank 0 and Bank 1 along the top edge of the package are combined and relabeled VCCO_TOP. The bottom, left, and right edges are similarly combined.

In Serial configuration mode, VCCO_4 must be at a level compatible with the attached configuration memory or data source. In Parallel configuration mode, both VCCO_4 and VCCO_5 must be at the same compatible voltage level.

All VCCO inputs to a bank must be connected together and to the voltage supply. Furthermore, there must be sufficient supply decoupling to guarantee problem-free operation, as described in XAPP623: *Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors*.

VCCINT Type: Voltage Supply for Internal Core Logic

Internal core logic circuits such as the configurable logic blocks (CLBs) and programmable interconnect operate from the VCCINT voltage supply inputs. VCCINT must be +1.2V.

All VCCINT inputs must be connected together and to the +1.2V voltage supply. Furthermore, there must be sufficient supply decoupling to guarantee problem-free operation, as described in XAPP623.

VCCAUX Type: Voltage Supply for Auxiliary Logic

The VCCAUX pins supply power to various auxiliary circuits, such as to the Digital Clock Managers (DCMs), the JTAG pins, and to the dedicated configuration pins (CONFIG type). VCCAUX must be +2.5V.

Table 87: **VQ100 Package Pinout *(Cont'd)***

Bank	XC3S50 XC3S200 Pin Name	VQ100 Pin Number	Type
2	IO_L40N_2	P65	I/O
2	IO_L40P_2/VREF_2	P64	VREF
2	VCCO_2	P70	VCCO
3	IO	P55	I/O
3	IO	P59	I/O
3	IO_L01N_3/VRP_3	P54	DCI
3	IO_L01P_3/VRN_3	P53	DCI
3	IO_L24N_3	P61	I/O
3	IO_L24P_3	P60	I/O
3	IO_L40N_3/VREF_3	P63	VREF
3	IO_L40P_3	P62	I/O
3	VCCO_3	P57	VCCO
4	IO_L01N_4/VRP_4	P50	DCI
4	IO_L01P_4/VRN_4	P49	DCI
4	IO_L27N_4/DIN/D0	P48	DUAL
4	IO_L27P_4/D1	P47	DUAL
4	IO_L30N_4/D2	P44	DUAL
4	IO_L30P_4/D3	P43	DUAL
4	IO_L31N_4/INIT_B	P42	DUAL
4	IO_L31P_4/DOUT/BUSY	P40	DUAL
4	IO_L32N_4/GCLK1	P39	GCLK
4	IO_L32P_4/GCLK0	P38	GCLK
4	VCCO_4	P46	VCCO
5	IO_L01N_5/RDWR_B	P28	DUAL
5	IO_L01P_5/CS_B	P27	DUAL
5	IO_L28N_5/D6	P32	DUAL
5	IO_L28P_5/D7	P30	DUAL
5	IO_L31N_5/D4	P35	DUAL
5	IO_L31P_5/D5	P34	DUAL
5	IO_L32N_5/GCLK3	P37	GCLK
5	IO_L32P_5/GCLK2	P36	GCLK
5	VCCO_5	P31	VCCO
6	IO	P17	I/O
6	IO	P21	I/O
6	IO_L01N_6/VRP_6	P23	DCI
6	IO_L01P_6/VRN_6	P22	DCI
6	IO_L24N_6/VREF_6	P16	VREF
6	IO_L24P_6	P15	I/O
6	IO_L40N_6	P14	I/O

FG320: 320-lead Fine-pitch Ball Grid Array

The 320-lead fine-pitch ball grid array package, FG320, supports three different Spartan-3 devices, including the XC3S400, the XC3S1000, and the XC3S1500. The footprint for all three devices is identical, as shown in Table 98 and Figure 50.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

All the package pins appear in Table 98 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 98: **FG320 Package Pinout**

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
0	IO	D9	I/O
0	IO	E7	I/O
0	IO/VREF_0	B3	VREF
0	IO/VREF_0	D6	VREF
0	IO_L01N_0/VRP_0	A2	DCI
0	IO_L01P_0/VRN_0	A3	DCI
0	IO_L09N_0	B4	I/O
0	IO_L09P_0	C4	I/O
0	IO_L10N_0	C5	I/O
0	IO_L10P_0	D5	I/O
0	IO_L15N_0	A4	I/O
0	IO_L15P_0	A5	I/O
0	IO_L25N_0	B5	I/O
0	IO_L25P_0	B6	I/O
0	IO_L27N_0	C7	I/O
0	IO_L27P_0	D7	I/O
0	IO_L28N_0	C8	I/O
0	IO_L28P_0	D8	I/O
0	IO_L29N_0	E8	I/O
0	IO_L29P_0	F8	I/O
0	IO_L30N_0	A7	I/O
0	IO_L30P_0	A8	I/O
0	IO_L31N_0	B9	I/O
0	IO_L31P_0/VREF_0	A9	VREF
0	IO_L32N_0/GCLK7	E9	GCLK
0	IO_L32P_0/GCLK6	F9	GCLK
0	VCCO_0	B8	VCCO
0	VCCO_0	C6	VCCO
0	VCCO_0	G8	VCCO

FG456: 456-lead Fine-pitch Ball Grid Array

The 456-lead fine-pitch ball grid array package, FG456, supports four different Spartan-3 devices, including the XC3S400, the XC3S1000, the XC3S1500, and the XC3S2000. The footprints for the XC3S1000, the XC3S1500, and the XC3S2000 are identical, as shown in Table 100 and Figure 51. The XC3S400, however, has fewer I/O pins which consequently results in 69 unconnected pins on the FG456 package, labeled as "N.C." In Table 100 and Figure 51, these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in Table 100 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S400 pinout and the pinout for the XC3S1000, the XC3S1500, or the XC3S2000, then that difference is highlighted in Table 100. If the table entry is shaded grey, then there is an unconnected pin on the XC3S400 that maps to a user-I/O pin on the XC3S1000, XC3S1500, and XC3S2000. If the table entry is shaded tan, then the unconnected pin on the XC3S400 maps to a VREF-type pin on the XC3S1000, the XC3S1500, or the XC3S2000. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S400 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S400 device to an XC3S1000, an XC3S1500, or an XC3S2000 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 100: **FG456 Package Pinout**

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
0	IO	IO	A10	I/O
0	IO	IO	D9	I/O
0	IO	IO	D10	I/O
0	IO	IO	F6	I/O
0	IO/VREF_0	IO/VREF_0	A3	VREF
0	IO/VREF_0	IO/VREF_0	C7	VREF
0	N.C. (◆)	IO/VREF_0	E5	VREF
0	IO/VREF_0	IO/VREF_0	F7	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L06N_0	IO_L06N_0	D5	I/O
0	IO_L06P_0	IO_L06P_0	C5	I/O
0	IO_L09N_0	IO_L09N_0	B5	I/O
0	IO_L09P_0	IO_L09P_0	A5	I/O
0	IO_L10N_0	IO_L10N_0	E6	I/O
0	IO_L10P_0	IO_L10P_0	D6	I/O
0	IO_L15N_0	IO_L15N_0	C6	I/O
0	IO_L15P_0	IO_L15P_0	B6	I/O
0	IO_L16N_0	IO_L16N_0	E7	I/O
0	IO_L16P_0	IO_L16P_0	D7	I/O
0	N.C. (◆)	IO_L19N_0	B7	I/O
0	N.C. (◆)	IO_L19P_0	A7	I/O

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
0	N.C. (◆)	IO_L22N_0	E8	I/O
0	N.C. (◆)	IO_L22P_0	D8	I/O
0	IO_L24N_0	IO_L24N_0	B8	I/O
0	IO_L24P_0	IO_L24P_0	A8	I/O
0	IO_L25N_0	IO_L25N_0	F9	I/O
0	IO_L25P_0	IO_L25P_0	E9	I/O
0	IO_L27N_0	IO_L27N_0	B9	I/O
0	IO_L27P_0	IO_L27P_0	A9	I/O
0	IO_L28N_0	IO_L28N_0	F10	I/O
0	IO_L28P_0	IO_L28P_0	E10	I/O
0	IO_L29N_0	IO_L29N_0	C10	I/O
0	IO_L29P_0	IO_L29P_0	B10	I/O
0	IO_L30N_0	IO_L30N_0	F11	I/O
0	IO_L30P_0	IO_L30P_0	E11	I/O
0	IO_L31N_0	IO_L31N_0	D11	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C11	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B11	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A11	GCLK
0	VCCO_0	VCCO_0	C8	VCCO
0	VCCO_0	VCCO_0	F8	VCCO
0	VCCO_0	VCCO_0	G9	VCCO
0	VCCO_0	VCCO_0	G10	VCCO
0	VCCO_0	VCCO_0	G11	VCCO
1	IO	IO	A12	I/O
1	IO	IO	E16	I/O
1	IO	IO	F12	I/O
1	IO	IO	F13	I/O
1	IO	IO	F16	I/O
1	IO	IO	F17	I/O
1	IO/VREF_1	IO/VREF_1	E13	VREF
1	N.C. (◆)	IO/VREF_1	F14	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	C19	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B20	DCI
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	A19	VREF
1	IO_L06P_1	IO_L06P_1	B19	I/O
1	IO_L09N_1	IO_L09N_1	C18	I/O
1	IO_L09P_1	IO_L09P_1	D18	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	A18	VREF
1	IO_L10P_1	IO_L10P_1	B18	I/O
1	IO_L15N_1	IO_L15N_1	D17	I/O

User I/Os by Bank

Table 101 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S400 in the FG456 package. Similarly, Table 102 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1000, XC3S1500, and XC3S2000 in the FG456 package.

Table 101: **User I/Os Per Bank for XC3S400 in FG456 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	35	27	0	2	4	2
	1	35	27	0	2	4	2
Right	2	31	25	0	2	4	0
	3	31	25	0	2	4	0
Bottom	4	35	21	6	2	4	2
	5	35	21	6	2	4	2
Left	6	31	25	0	2	4	0
	7	31	25	0	2	4	0

Table 102: **User I/Os Per Bank for XC3S1000, XC3S1500, and XC3S2000 in FG456 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	40	31	0	2	5	2
	1	40	31	0	2	5	2
Right	2	43	37	0	2	4	0
	3	43	37	0	2	4	0
Bottom	4	41	26	6	2	5	2
	5	40	25	6	2	5	2
Left	6	43	37	0	2	4	0
	7	43	37	0	2	4	0

FG456 Footprint

Left Half of FG456 Package (Top View)

XC3S400 (264 max. user I/O)

196 **I/O:** Unrestricted, general-purpose user I/O

32 **VREF:** User I/O or input voltage reference for bank

69 **N.C.:** Unconnected pins for XC3S400 (◆)

XC3S1000, XC3S1500, XC3S2000 (333 max user I/O)

261 **I/O:** Unrestricted, general-purpose user I/O

36 **VREF:** User I/O or input voltage reference for bank

0 **N.C.:** No unconnected pins in this package

All devices

12 **DUAL:** Configuration pin, then possible user I/O

8 **GCLK:** User I/O or global clock buffer input

16 **DCI:** User I/O or reference resistor input for bank

7 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

12 **VCCINT:** Internal core voltage supply (+1.2V)

40 **VCCO:** Output voltage supply for bank

8 **VCCAUX:** Auxiliary voltage supply (+2.5V)

52 **GND:** Ground

	Bank 0										
	1	2	3	4	5	6	7	8	9	10	11
A	GND	PROG_B	IO VREF_0	I/O L01P_0 VRN_0	I/O L09P_0	VCCAUX	I/O L19P_0 ◆	I/O L24P_0	I/O L27P_0	I/O	I/O L32P_0 GCLK6
B	TDI	GND	HSWAP_EN	I/O L01N_0 VRP_0	I/O L09N_0	I/O L15P_0	I/O L19N_0 ◆	I/O L24N_0	I/O L27N_0	I/O L29P_0	I/O L32N_0 GCLK7
C	I/O L16P_7 VREF_7	I/O	I/O L01N_7 VRP_7	I/O L01P_7 VRN_7	I/O L06P_0	I/O L15N_0	IO VREF_0	VCCO_0	GND	I/O L29N_0	I/O L31P_0 VREF_0
D	I/O L16N_7	I/O L19P_7	I/O L19N_7 VREF_7	I/O L17P_7	I/O L06N_0	I/O L10P_0	I/O L16P_0	I/O L22P_0 ◆	I/O	I/O	I/O L31N_0
E	I/O L21N_7	I/O L21P_7	I/O L20P_7	I/O L17N_7	IO VREF_0 ◆	I/O L10N_0	I/O L16N_0	I/O L22N_0 ◆	I/O L25P_0	I/O L28P_0	I/O L30P_0
F	VCCAUX	I/O L23N_7	I/O L23P_7	I/O L20N_7	I/O L22P_7	I/O	IO VREF_0	VCCO_0	I/O L25N_0	I/O L28N_0	I/O L30N_0
G	I/O L27N_7	I/O L27P_7 VREF_7	I/O L26N_7 ◆	I/O L26P_7 ◆	I/O L24P_7	I/O L22N_7	VCCINT	VCCINT	VCCO_0	VCCO_0	VCCO_0
H	I/O L28N_7 ◆	I/O L28P_7 ◆	VCCO_7	I/O L29P_7 ◆	I/O L24N_7	VCCO_7	VCCINT				
J	I/O L32N_7 ◆	I/O L32P_7 ◆	GND	I/O L29N_7 ◆	I/O L31N_7 ◆	I/O L31P_7 ◆	VCCO_7		GND	GND	GND
K	I/O L35N_7	I/O L35P_7	I/O L34N_7	I/O L34P_7	I/O L33N_7 ◆	I/O L33P_7 ◆	VCCO_7		GND	GND	GND
L	I/O L40N_7 VREF_7	I/O L40P_7	I/O L39N_7	I/O L39P_7	I/O L38N_7	I/O L38P_7	VCCO_7		GND	GND	GND
M	I/O L40P_6 VREF_6	I/O L40N_6	I/O L39P_6	I/O L39N_6	I/O L38P_6	I/O L38N_6	VCCO_6		GND	GND	GND
N	I/O L35P_6	I/O L35N_6	I/O L34P_6	I/O L34N_6 VREF_6	I/O L33P_6 ◆	I/O L33N_6 ◆	VCCO_6		GND	GND	GND
P	I/O L32P_6 ◆	I/O L32N_6 ◆	GND	I/O L31P_6 ◆	I/O L31N_6 ◆	I/O L28P_6 ◆	VCCO_6		GND	GND	GND
R	I/O L29P_6 ◆	I/O L29N_6 ◆	VCCO_6	I/O L26P_6 ◆	I/O L28N_6 ◆	VCCO_6	VCCINT				
T	I/O L27P_6	I/O L27N_6	I/O L26N_6 ◆	I/O L23P_6	I/O L22P_6	I/O L22N_6	VCCINT	VCCINT	VCCO_5	VCCO_5	VCCO_5
U	VCCAUX	I/O L24P_6	I/O L24N_6 VREF_6	I/O L23N_6	I/O L19P_6	IO VREF_5	I/O	VCCO_5	I/O ◆	I/O	I/O
V	I/O L21P_6	I/O L21N_6	I/O L20P_6	I/O L20N_6	I/O L19N_6	I/O L15P_5	I/O	I/O L24P_5	I/O L27P_5	I/O	I/O L31P_5 D5
W	I/O L17P_6 VREF_6	I/O L17N_6	I/O L16P_6	I/O L16N_6	I/O L09P_5	I/O L15N_5	I/O L19P_5 VREF_5 ◆	I/O L24N_5	I/O L27N_5 VREF_5	I/O L29P_5 VREF_5	I/O L31N_5 D4
Y	I/O	I/O L01P_6 VRN_6	I/O L01N_6 VRP_6	I/O L01N_5 RDWR_B	I/O L09N_5	I/O L16P_5	I/O L19N_5 ◆	VCCO_5	GND	I/O L29N_5	I/O L32P_5 GCLK2
AA	M1	GND	I/O L01P_5 CS_B	I/O L06P_5	I/O L10P_5 VRN_5	I/O L16N_5	I/O L22P_5 ◆	I/O L25P_5	I/O L28P_5 D7	I/O L30P_5	I/O L32N_5 GCLK3
AB	GND	M0	M2	I/O L06N_5	I/O L10N_5 VRP_5	VCCAUX	I/O L22N_5 ◆	I/O L25N_5	I/O L28N_5 D6	I/O L30N_5	IO VREF_5

Bank 7 (rows G–L) · Bank 6 (rows M–T) · Bank 5 (columns 7–11)

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Figure 51: **FG456 Package Footprint (Top View)**

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
2	N.C. (◆)	IO_L06N_2	IO_L06N_2	IO_L06N_2	IO_L06N_2	G20	I/O
2	N.C. (◆)	IO_L06P_2	IO_L06P_2	IO_L06P_2	IO_L06P_2	G21	I/O
2	N.C. (◆)	IO_L07N_2	IO_L07N_2	IO_L07N_2	IO_L07N_2	F23	I/O
2	N.C. (◆)	IO_L07P_2	IO_L07P_2	IO_L07P_2	IO_L07P_2	F24	I/O
2	N.C. (◆)	IO_L08N_2	IO_L08N_2	IO_L08N_2	IO_L08N_2	G22	I/O
2	N.C. (◆)	IO_L08P_2	IO_L08P_2	IO_L08P_2	IO_L08P_2	G23	I/O
2	N.C. (◆)	IO_L09N_2/VREF_2(1)	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	F25	VREF(1)
2	N.C. (◆)	IO_L09P_2	IO_L09P_2	IO_L09P_2	IO_L09P_2	F26	I/O
2	N.C. (◆)	IO_L10N_2	IO_L10N_2	IO_L10N_2	IO_L10N_2	G25	I/O
2	N.C. (◆)	IO_L10P_2	IO_L10P_2	IO_L10P_2	IO_L10P_2	G26	I/O
2	IO_L14N_2	IO_L14N_2	IO_L14N_2(2)	IO_L11N_2(2)	IO_L11N_2	H20	I/O
2	IO_L14P_2	IO_L14P_2	IO_L14P_2(2)	IO_L11P_2(2)	IO_L11P_2	H21	I/O
2	IO_L16N_2	IO_L16N_2	IO_L16N_2(2)	IO_L12N_2(2)	IO_L12N_2	H22	I/O
2	IO_L16P_2	IO_L16P_2	IO_L16P_2(2)	IO_L12P_2(2)	IO_L12P_2	J21	I/O
2	IO_L17N_2	IO_L17N_2	IO_L17N_2(2)	IO_L13N_2(2)	IO(3)	H23	I/O
2	IO_L17P_2/VREF_2	IO_L17P_2/VREF_2	IO_L17P_2(2)/VREF_2	IO_L13P_2(2)/VREF_2	IO/VREF_2(3)	H24	VREF
2	IO_L19N_2	IO_L19N_2	IO_L19N_2	IO_L19N_2	IO_L19N_2	H25	I/O
2	IO_L19P_2	IO_L19P_2	IO_L19P_2	IO_L19P_2	IO_L19P_2	H26	I/O
2	IO_L20N_2	IO_L20N_2	IO_L20N_2	IO_L20N_2	IO_L20N_2	J20	I/O
2	IO_L20P_2	IO_L20P_2	IO_L20P_2	IO_L20P_2	IO_L20P_2	K20	I/O
2	IO_L21N_2	IO_L21N_2	IO_L21N_2	IO_L21N_2	IO_L21N_2	J22	I/O
2	IO_L21P_2	IO_L21P_2	IO_L21P_2	IO_L21P_2	IO_L21P_2	J23	I/O
2	IO_L22N_2	IO_L22N_2	IO_L22N_2	IO_L22N_2	IO_L22N_2	J24	I/O
2	IO_L22P_2	IO_L22P_2	IO_L22P_2	IO_L22P_2	IO_L22P_2	J25	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	K21	VREF
2	IO_L23P_2	IO_L23P_2	IO_L23P_2	IO_L23P_2	IO_L23P_2	K22	I/O
2	IO_L24N_2	IO_L24N_2	IO_L24N_2	IO_L24N_2	IO_L24N_2	K23	I/O
2	IO_L24P_2	IO_L24P_2	IO_L24P_2	IO_L24P_2	IO_L24P_2	K24	I/O
2	IO_L26N_2	IO_L26N_2	IO_L26N_2	IO_L26N_2	IO_L26N_2	K25	I/O
2	IO_L26P_2	IO_L26P_2	IO_L26P_2	IO_L26P_2	IO_L26P_2	K26	I/O
2	IO_L27N_2	IO_L27N_2	IO_L27N_2	IO_L27N_2	IO_L27N_2	L19	I/O
2	IO_L27P_2	IO_L27P_2	IO_L27P_2	IO_L27P_2	IO_L27P_2	L20	I/O
2	IO_L28N_2	IO_L28N_2	IO_L28N_2	IO_L28N_2	IO_L28N_2	L21	I/O
2	IO_L28P_2	IO_L28P_2	IO_L28P_2	IO_L28P_2	IO_L28P_2	L22	I/O
2	IO_L29N_2	IO_L29N_2	IO_L29N_2	IO_L29N_2	IO_L29N_2	L25	I/O
2	IO_L29P_2	IO_L29P_2	IO_L29P_2	IO_L29P_2	IO_L29P_2	L26	I/O
2	IO_L31N_2	IO_L31N_2	IO_L31N_2	IO_L31N_2	IO_L31N_2	M19	I/O
2	IO_L31P_2	IO_L31P_2	IO_L31P_2	IO_L31P_2	IO_L31P_2	M20	I/O
2	IO_L32N_2	IO_L32N_2	IO_L32N_2	IO_L32N_2	IO_L32N_2	M21	I/O
2	IO_L32P_2	IO_L32P_2	IO_L32P_2	IO_L32P_2	IO_L32P_2	M22	I/O
2	IO_L33N_2	IO_L33N_2	IO_L33N_2	IO_L33N_2	IO_L33N_2	L23	I/O
2	IO_L33P_2	IO_L33P_2	IO_L33P_2	IO_L33P_2	IO_L33P_2	M24	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	Y24	VCCO
4	IO	IO	IO	IO	IO	AA20	I/O
4	IO	IO	IO	IO	IO	AD15	I/O
4	N.C. (◆)	IO	IO	IO	IO	AD19	I/O
4	IO	IO	IO	IO	IO	AD23	I/O
4	IO	IO	IO	IO	IO	AF21	I/O
4	IO	IO	IO	IO	IO	AF22	I/O
4	IO	IO	IO	IO	IO	W15	I/O
4	IO	IO	IO	IO	IO	W16	I/O
4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	AB14	VREF
4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	AD25	VREF
4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	Y17	VREF
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	AB22	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	AC22	DCI
4	IO_L04N_4	IO_L04N_4	IO_L04N_4	IO_L04N_4	IO_L04N_4	AE24	I/O
4	IO_L04P_4	IO_L04P_4	IO_L04P_4	IO_L04P_4	IO_L04P_4	AF24	I/O
4	IO_L05N_4	IO_L05N_4	IO_L05N_4	IO_L05N_4	IO_L05N_4	AE23	I/O
4	IO_L05P_4	IO_L05P_4	IO_L05P_4	IO_L05P_4	IO_L05P_4	AF23	I/O
4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	AD22	VREF
4	IO_L06P_4	IO_L06P_4	IO_L06P_4	IO_L06P_4	IO_L06P_4	AE22	I/O
4	IO_L07N_4	IO_L07N_4	IO_L07N_4	IO_L07N_4	IO_L07N_4	AB21	I/O
4	IO_L07P_4	IO_L07P_4	IO_L07P_4	IO_L07P_4	IO_L07P_4	AC21	I/O
4	IO_L08N_4	IO_L08N_4	IO_L08N_4	IO_L08N_4	IO_L08N_4	AD21	I/O
4	IO_L08P_4	IO_L08P_4	IO_L08P_4	IO_L08P_4	IO_L08P_4	AE21	I/O
4	IO_L09N_4	IO_L09N_4	IO_L09N_4	IO_L09N_4	IO_L09N_4	AB20	I/O
4	IO_L09P_4	IO_L09P_4	IO_L09P_4	IO_L09P_4	IO_L09P_4	AC20	I/O
4	IO_L10N_4	IO_L10N_4	IO_L10N_4	IO_L10N_4	IO_L10N_4	AE20	I/O
4	IO_L10P_4	IO_L10P_4	IO_L10P_4	IO_L10P_4	IO_L10P_4	AF20	I/O
4	N.C. (◆)	IO_L11N_4	IO_L11N_4	IO_L11N_4	IO_L11N_4	Y19	I/O
4	N.C. (◆)	IO_L11P_4	IO_L11P_4	IO_L11P_4	IO_L11P_4	AA19	I/O
4	N.C. (◆)	IO_L12N_4	IO_L12N_4	IO_L12N_4	IO_L12N_4	AB19	I/O
4	N.C. (◆)	IO_L12P_4	IO_L12P_4	IO_L12P_4	IO_L12P_4	AC19	I/O
4	IO_L15N_4	IO_L15N_4	IO_L15N_4	IO_L15N_4	IO_L15N_4	AE19	I/O
4	IO_L15P_4	IO_L15P_4	IO_L15P_4	IO_L15P_4	IO_L15P_4	AF19	I/O
4	IO_L16N_4	IO_L16N_4	IO_L16N_4	IO_L16N_4	IO_L16N_4	Y18	I/O
4	IO_L16P_4	IO_L16P_4	IO_L16P_4	IO_L16P_4	IO_L16P_4	AA18	I/O
4	N.C. (◆)	IO_L17N_4	IO_L17N_4	IO_L17N_4	IO_L17N_4	AB18	I/O
4	N.C. (◆)	IO_L17P_4	IO_L17P_4	IO_L17P_4	IO_L17P_4	AC18	I/O
4	N.C. (◆)	IO_L18N_4	IO_L18N_4	IO_L18N_4	IO_L18N_4	AD18	I/O
4	N.C. (◆)	IO_L18P_4	IO_L18P_4	IO_L18P_4	IO_L18P_4	AE18	I/O
4	IO_L19N_4	IO_L19N_4	IO_L19N_4	IO_L19N_4	IO_L19N_4	AC17	I/O
4	IO_L19P_4	IO_L19P_4	IO_L19P_4	IO_L19P_4	IO_L19P_4	AA17	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
1	IO_L07N_1	IO_L07N_1	D27	I/O
1	IO_L07P_1	IO_L07P_1	E27	I/O
1	IO_L08N_1	IO_L08N_1	A27	I/O
1	IO_L08P_1	IO_L08P_1	B27	I/O
1	IO_L09N_1	IO_L09N_1	F26	I/O
1	IO_L09P_1	IO_L09P_1	G26	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	C26	VREF
1	IO_L10P_1	IO_L10P_1	D26	I/O
1	IO_L11N_1	IO_L11N_1	H25	I/O
1	IO_L11P_1	IO_L11P_1	J25	I/O
1	IO_L12N_1	IO_L12N_1	F25	I/O
1	IO_L12P_1	IO_L12P_1	G25	I/O
1	IO_L13N_1	IO_L13N_1	C25	I/O
1	IO_L13P_1	IO_L13P_1	D25	I/O
1	IO_L14N_1	IO_L14N_1	A25	I/O
1	IO_L14P_1	IO_L14P_1	B25	I/O
1	IO_L15N_1	IO_L15N_1	A24	I/O
1	IO_L15P_1	IO_L15P_1	B24	I/O
1	IO_L16N_1	IO_L16N_1	J23	I/O
1	IO_L16P_1	IO_L16P_1	K23	I/O
1	IO_L17N_1/VREF_1	IO_L17N_1/VREF_1	F23	VREF
1	IO_L17P_1	IO_L17P_1	G23	I/O
1	IO_L18N_1	IO_L18N_1	D23	I/O
1	IO_L18P_1	IO_L18P_1	E23	I/O
1	IO_L19N_1	IO_L19N_1	A23	I/O
1	IO_L19P_1	IO_L19P_1	B23	I/O
1	IO_L20N_1	IO_L20N_1	K22	I/O
1	IO_L20P_1	IO_L20P_1	L22	I/O
1	IO_L21N_1	IO_L21N_1	G22	I/O
1	IO_L21P_1	IO_L21P_1	H22	I/O
1	IO_L22N_1	IO_L22N_1	C22	I/O
1	IO_L22P_1	IO_L22P_1	D22	I/O
1	IO_L23N_1	IO_L23N_1	H21	I/O
1	IO_L23P_1	IO_L23P_1	J21	I/O
1	IO_L24N_1	IO_L24N_1	F21	I/O
1	IO_L24P_1	IO_L24P_1	G21	I/O
1	IO_L25N_1	IO_L25N_1	C21	I/O
1	IO_L25P_1	IO_L25P_1	D21	I/O
1	IO_L26N_1	IO_L26N_1	A21	I/O
1	IO_L26P_1	IO_L26P_1	B21	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
6	IO_L37N_6	IO_L37N_6	W3	I/O
6	IO_L37P_6	IO_L37P_6	W2	I/O
6	IO_L38N_6	IO_L38N_6	V6	I/O
6	IO_L38P_6	IO_L38P_6	V5	I/O
6	IO_L39N_6	IO_L39N_6	V4	I/O
6	IO_L39P_6	IO_L39P_6	V3	I/O
6	IO_L40N_6	IO_L40N_6	V2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	V1	VREF
6	N.C. (◆)	IO_L41N_6	AH4	I/O
6	N.C. (◆)	IO_L41P_6	AH3	I/O
6	N.C. (◆)	IO_L44N_6	AD7	I/O
6	N.C. (◆)	IO_L44P_6	AD6	I/O
6	IO_L45N_6	IO_L45N_6	AC4	I/O
6	IO_L45P_6	IO_L45P_6	AC3	I/O
6	N.C. (◆)	IO_L46N_6	AA10	I/O
6	N.C. (◆)	IO_L46P_6	AA9	I/O
6	IO_L48N_6	IO_L48N_6	Y7	I/O
6	IO_L48P_6	IO_L48P_6	Y6	I/O
6	N.C. (◆)	IO_L49N_6	W11	I/O
6	N.C. (◆)	IO_L49P_6	V11	I/O
6	IO_L52N_6	IO_L52N_6	V8	I/O
6	IO_L52P_6	IO_L52P_6	V7	I/O
6	VCCO_6	VCCO_6	AA12	VCCO
6	VCCO_6	VCCO_6	AB12	VCCO
6	VCCO_6	VCCO_6	AB2	VCCO
6	VCCO_6	VCCO_6	AB6	VCCO
6	VCCO_6	VCCO_6	AD4	VCCO
6	VCCO_6	VCCO_6	AD8	VCCO
6	VCCO_6	VCCO_6	AG3	VCCO
6	VCCO_6	VCCO_6	AG7	VCCO
6	VCCO_6	VCCO_6	AL3	VCCO
6	VCCO_6	VCCO_6	W12	VCCO
6	VCCO_6	VCCO_6	W4	VCCO
6	VCCO_6	VCCO_6	Y12	VCCO
6	VCCO_6	VCCO_6	Y8	VCCO
7	IO	IO	G1	I/O
7	IO	IO	G2	I/O
7	IO	IO	U10	I/O
7	IO	IO	U9	I/O
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	C1	DCI

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	GND	GND	J22	GND
N/A	GND	GND	J30	GND
N/A	GND	GND	J34	GND
N/A	GND	GND	J5	GND
N/A	GND	GND	K10	GND
N/A	GND	GND	K25	GND
N/A	GND	GND	L3	GND
N/A	GND	GND	L32	GND
N/A	GND	GND	N1	GND
N/A	GND	GND	N17	GND
N/A	GND	GND	N18	GND
N/A	GND	GND	N26	GND
N/A	GND	GND	N30	GND
N/A	GND	GND	N34	GND
N/A	GND	GND	N5	GND
N/A	GND	GND	N9	GND
N/A	GND	GND	P14	GND
N/A	GND	GND	P15	GND
N/A	GND	GND	P16	GND
N/A	GND	GND	P17	GND
N/A	GND	GND	P18	GND
N/A	GND	GND	P19	GND
N/A	GND	GND	P20	GND
N/A	GND	GND	P21	GND
N/A	GND	GND	R14	GND
N/A	GND	GND	R15	GND
N/A	GND	GND	R16	GND
N/A	GND	GND	R17	GND
N/A	GND	GND	R18	GND
N/A	GND	GND	R19	GND
N/A	GND	GND	R20	GND
N/A	GND	GND	R21	GND
N/A	GND	GND	T1	GND
N/A	GND	GND	T14	GND
N/A	GND	GND	T15	GND
N/A	GND	GND	T16	GND
N/A	GND	GND	T17	GND
N/A	GND	GND	T18	GND
N/A	GND	GND	T19	GND
N/A	GND	GND	T20	GND

User I/Os by Bank

Note: The FG(G)1156 package is discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Table 111 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S4000 in the FG1156 package. Similarly, Table 112 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S5000 in the FG1156 package.

Table 111: **User I/Os Per Bank for XC3S4000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	90	79	0	2	7	2
	1	90	79	0	2	7	2
Right	2	88	80	0	2	6	0
	3	88	79	0	2	7	0
Bottom	4	90	73	6	2	7	2
	5	90	73	6	2	7	2
Left	6	88	79	0	2	7	0
	7	88	79	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

Table 112: **User I/Os Per Bank for XC3S5000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	100	89	0	2	7	2
	1	100	89	0	2	7	2
Right	2	96	87	0	2	7	0
	3	96	87	0	2	7	0
Bottom	4	100	83	6	2	7	2
	5	100	83	6	2	7	2
Left	6	96	87	0	2	7	0
	7	96	87	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
GND	GND	GND	GND	GND	VCCINT	I/O L51N_3 ◆	I/O	I/O	I/O L37P_3	I/O L37N_3	I/O L38P_3	I/O L38N_3	I/O L39P_3	I/O L39N_3	I/O L40P_3	I/O L40N_3 VREF_3	V
GND	GND	GND	GND	VCCINT	VCCO_3	I/O L51P_3 ◆	I/O L33N_3	GND	VCCAUX	I/O L34P_3 VREF_3	I/O L34N_3	GND	VCCO_3	I/O L35P_3	I/O L35N_3	GND	W
GND	GND	GND	GND	VCCINT	VCCO_3	I/O L50P_3	I/O L50N_3	I/O L33P_3	VCCO_3	I/O L30P_3	I/O L30N_3	VCCAUX	I/O L31P_3	I/O L31N_3	I/O L32P_3	I/O L32N_3	Y
GND	GND	GND	GND	VCCINT	VCCO_3	I/O L48N_3	I/O L49P_3 ◆	I/O L49N_3 ◆	I/O L26P_3	I/O L26N_3	I/O L27P_3	I/O L27N_3	I/O L28P_3	I/O L28N_3	I/O L29P_3	I/O L29N_3	AA
GND	VCCINT	VCCINT	VCCINT	VCCINT	VCCO_3	I/O L48P_3	I/O L24N_3	GND	I/O L46P_3	I/O L46N_3	VCCO_3	GND	I/O L47P_3	I/O L47N_3	VCCO_3	GND	AB
VCCINT	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCINT	I/O L20P_3	I/O L20N_3	I/O L24P_3	I/O L21P_3	I/O L21N_3	I/O L22P_3	I/O L22N_3	I/O L23P_3 VREF_3	I/O L23N_3	I/O L45P_3	I/O L45N_3	AC
I/O	I/O	I/O	I/O L18N_4	I/O	I/O L11N_4	DONE	I/O L17P_3 VREF_3	I/O L17N_3	VCCO_3	I/O L44P_3 ◆	I/O L44N_3 ◆	VCCAUX	VCCO_3	GND	I/O L19P_3	I/O L19N_3	AD
I/O	I/O	I/O L23N_4	I/O L18P_4	I/O	I/O L11P_4	I/O ◆	GND	I/O L12N_3	I/O L13P_3	I/O L13N_3 VREF_3	I/O L14P_3	I/O L14N_3	I/O L15P_3	I/O L15N_3	I/O L16P_3	I/O L16N_3	AE
I/O L29N_4	GND	I/O L23P_4	IO VREF_4	GND	I/O L12N_4	I/O	I/O L07N_4	I/O ◆	I/O L12P_3	I/O L09P_3 VREF_3	I/O L09N_3	GND	I/O L10N_3	I/O L11P_3	I/O L11N_3	GND	AF
I/O L29P_4	VCCAUX	VCCO_4	I/O L19N_4	I/O L16N_4	I/O L12P_4	VCCO_4	I/O L07P_4	I/O	I/O	VCCO_3	I/O L07P_3	I/O L07N_3	I/O L10P_3	VCCO_3	I/O L08P_3	I/O L08N_3	AG
I/O L30N_4 D2	I/O L27N_4 DIN D0	I/O L24N_4	I/O L19P_4	I/O L16P_4	IO VREF_4	I/O L39N_4 ◆	I/O L08N_4	I/O L05N_4	VCCO_4	GND	I/O L06P_3	I/O L06N_3	I/O L41P_3 ◆	I/O L41N_3 ◆	I/O	I/O	AH
I/O L30P_4 D3	I/O L27P_4 D1	I/O L24P_4	I/O L20N_4	VCCO_4	I/O L13N_4	I/O L39P_4 ◆	I/O L08P_4	I/O L05P_4	I/O	I/O L35N_4	I/O	VCCAUX	I/O L04P_3	I/O L04N_3	I/O L05P_3	I/O L05N_3	AJ
IO VREF_4	GND	VCCAUX	I/O L20P_4	GND	I/O L13P_4	VCCAUX	I/O	GND	I/O L38N_4	I/O L35P_4	VCCAUX	GND	N.C. ◆ ■	I/O L03P_3	I/O L03N_3	GND	AK
I/O L31N_4 INIT_B	VCCO_4	I/O L25N_4	I/O L21N_4	I/O L17N_4	I/O L14N_4	VCCO_4	I/O L09N_4	I/O L06N_4 VREF_4	I/O L38P_4	I/O L36N_4 ◆	I/O L33N_4	IO VREF_4	CCLK	VCCO_3	I/O L02P_3	I/O L02N_3 VREF_3	AL
I/O L31P_4 DOUT BUSY	I/O L28N_4	I/O L25P_4	I/O L21P_4	I/O L17P_4	I/O L14P_4	GND	I/O L09P_4	I/O L06P_4	VCCO_4	I/O L36P_4 ◆	I/O L33P_4	I/O L03N_4	VCCO_4	GND	I/O L01P_3 VRN_3	I/O L01N_3 VRP_3	AM
I/O L32N_4 GCLK1	I/O L28P_4	I/O L26N_4	I/O L22N_4 VREF_4	VCCO_4	I/O L15N_4	I/O L40N_4 ◆	I/O L10N_4	I/O	I/O L04N_4	I/O L37N_4 ◆	I/O L34N_4	I/O L03P_4	I/O L02N_4	I/O L01N_4 VRP_4	GND	GND	AN
I/O L32P_4 GCLK0	GND	I/O L26P_4 VREF_4	I/O L22P_4	GND	I/O L15P_4	I/O L40P_4 ◆	I/O L10P_4	GND	I/O L04P_4	I/O L37P_4 ◆	I/O L34P_4	GND	I/O L02P_4	I/O L01P_4 VRN_4	GND	GND	AP

Bank 3

Bank 4

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Bottom Right Corner of FG1156 Package (Top View)

Figure 60: FG1156 Package Footprint (Top View) Continued