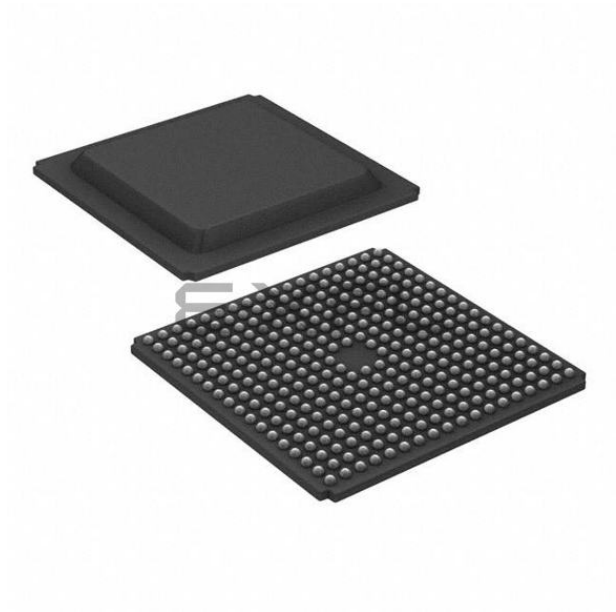

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3328
Number of Logic Elements/Cells	29952
Total RAM Bits	589824
Number of I/O	221
Number of Gates	1500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1500-4fg320c

power, the configuration data is written to the FPGA using any of five different modes: Master Parallel, Slave Parallel, Master Serial, Slave Serial, and Boundary Scan (JTAG). The Master and Slave Parallel modes use an 8-bit-wide SelectMAP port.

The recommended memory for storing the configuration data is the low-cost Xilinx Platform Flash PROM family, which includes the XCF00S PROMs for serial configuration and the higher density XCF00P PROMs for parallel or serial configuration.

I/O Capabilities

The SelectIO feature of Spartan-3 devices supports eighteen single-ended standards and eight differential standards as listed in Table 2. Many standards support the DCI feature, which uses integrated terminations to eliminate unwanted signal reflections.

Table 2: **Signal Standards Supported by the Spartan-3 Family**

Standard Category	Description	V_{CCO} (V)	Class	Symbol (IOSTANDARD)	DCI Option
Single-Ended					
GTL	Gunning Transceiver Logic	N/A	Terminated	GTL	Yes
			Plus	GTLP	Yes
HSTL	High-Speed Transceiver Logic	1.5	I	HSTL_I	Yes
			III	HSTL_III	Yes
		1.8	I	HSTL_I_18	Yes
			II	HSTL_II_18	Yes
			III	HSTL_III_18	Yes
LVCMOS	Low-Voltage CMOS	1.2	N/A	LVCMOS12	No
		1.5	N/A	LVCMOS15	Yes
		1.8	N/A	LVCMOS18	Yes
		2.5	N/A	LVCMOS25	Yes
		3.3	N/A	LVCMOS33	Yes
LVTTL	Low-Voltage Transistor-Transistor Logic	3.3	N/A	LVTTL	No
PCI	Peripheral Component Interconnect	3.0	33 MHz(1)	PCI33_3	No
SSTL	Stub Series Terminated Logic	1.8	N/A (±6.7 mA)	SSTL18_I	Yes
			N/A (±13.4 mA)	SSTL18_II	No
		2.5	I	SSTL2_I	Yes
			II	SSTL2_II	Yes
Differential					
LDT (ULVDS)	Lightning Data Transport (HyperTransport™) Logic	2.5	N/A	LDT_25	No
LVDS	Low-Voltage Differential Signaling		Standard	LVDS_25	Yes
			Bus	BLVDS_25	No
			Extended Mode	LVDSEXT_25	Yes
LVPECL	Low-Voltage Positive Emitter-Coupled Logic	2.5	N/A	LVPECL_25	No
RSDS	Reduced-Swing Differential Signaling	2.5	N/A	RSDS_25	No
HSTL	Differential High-Speed Transceiver Logic	1.8	II	DIFF_HSTL_II_18	Yes
SSTL	Differential Stub Series Terminated Logic	2.5	II	DIFF_SSTL2_II	Yes

Notes:

1. 66 MHz PCI is not supported by the Xilinx IP core although PCI66_3 is an available I/O standard.

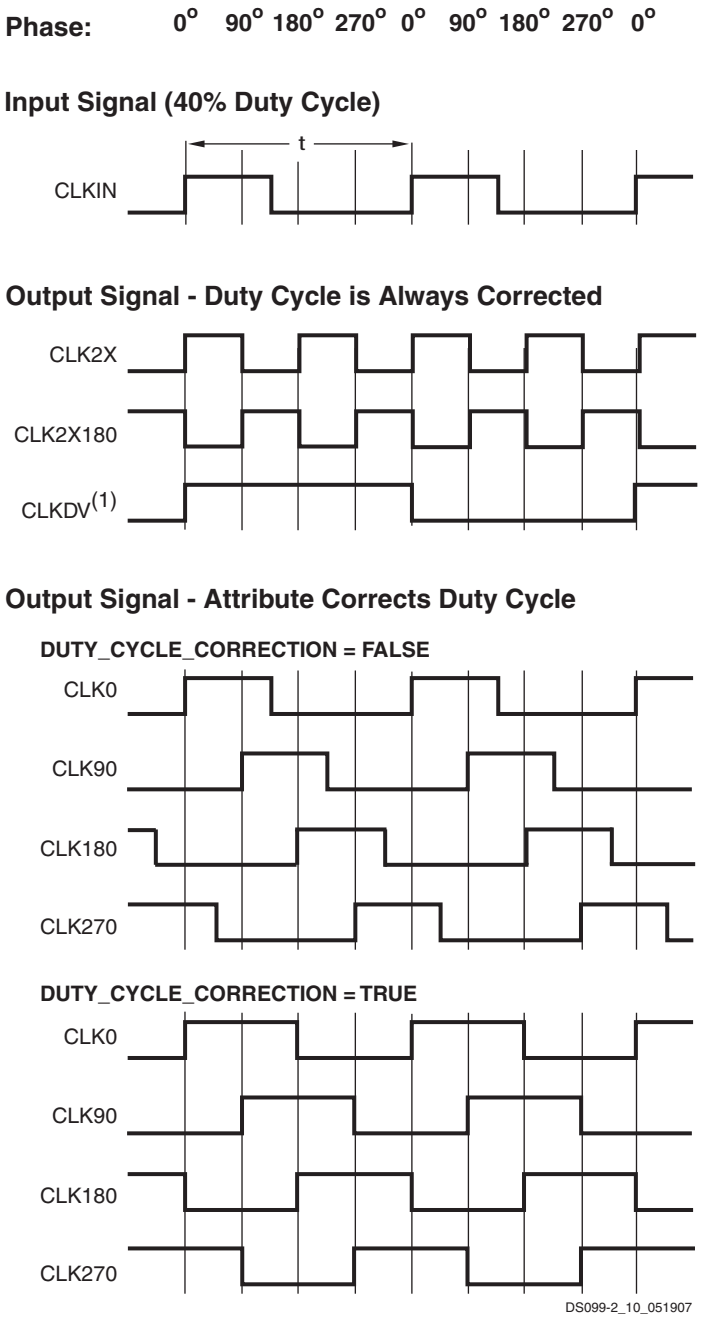

Figure 22: **Characteristics of the DLL Clock Outputs**

Digital Frequency Synthesizer (DFS)

The DFS component generates clock signals the frequency of which is a product of the clock frequency at the CLKIN input and a ratio of two user-determined integers. Because of the wide range of possible output frequencies such a ratio permits, the DFS feature provides still further flexibility than the DLL's basic synthesis options as described in the preceding section. The DFS component's two dedicated outputs, CLKFX and CLKFX180, are defined in Table 19.

The signal at the CLKFX180 output is essentially an inversion of the CLKFX signal. These two outputs always exhibit a 50% duty cycle. This is true even when the CLKIN signal does not. These DFS clock outputs are driven at the same time as the DLL's seven clock outputs.

The numerator of the ratio is the integer value assigned to the attribute CLKFX_MULTIPLY and the denominator is the integer value assigned to the attribute CLKFX_DIVIDE. These attributes are described in Table 18.

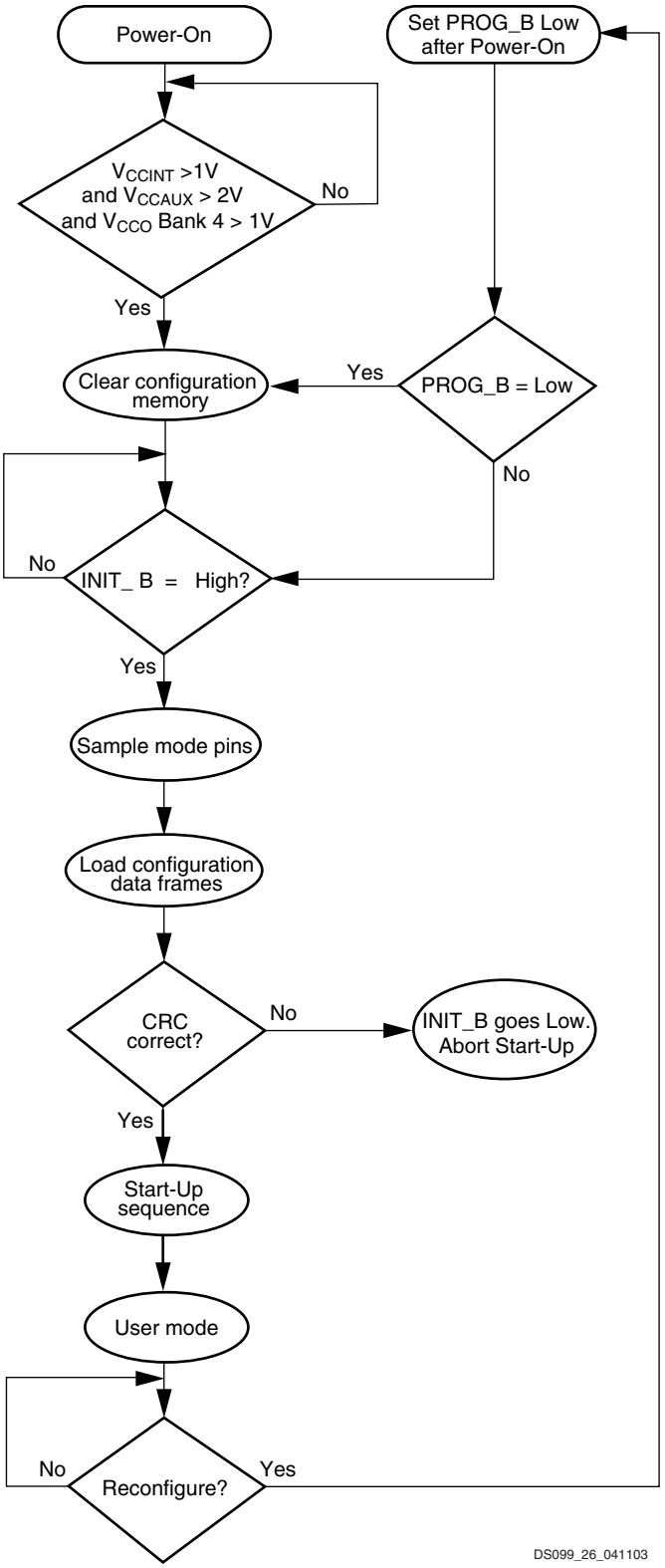

Figure 29: **Configuration Flow Diagram for the Serial and Parallel Modes**

Table 34: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical(1)	Commercial Maximum(1)	Industrial Maximum(1)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50	5	24	31	mA
		XC3S200	10	54	80	mA
		XC3S400	15	110	157	mA
		XC3S1000	35	160	262	mA
		XC3S1500	45	260	332	mA
		XC3S2000	60	360	470	mA
		XC3S4000	100	450	810	mA
		XC3S5000	120	600	870	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50	1.5	2.0	2.5	mA
		XC3S200	1.5	3.0	3.5	mA
		XC3S400	1.5	3.0	3.5	mA
		XC3S1000	2.0	4.0	5.0	mA
		XC3S1500	2.5	4.0	5.0	mA
		XC3S2000	3.0	5.0	6.0	mA
		XC3S4000	3.5	5.0	6.0	mA
		XC3S5000	3.5	5.0	6.0	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50	7	20	22	mA
		XC3S200	10	30	33	mA
		XC3S400	15	40	44	mA
		XC3S1000	20	50	55	mA
		XC3S1500	35	75	85	mA
		XC3S2000	45	90	100	mA
		XC3S4000	55	110	125	mA
		XC3S5000	70	130	145	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using devices with typical processing at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). Maximum values are the production test limits measured for each device at the maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.465V, and V_{CCAUX} = 2.625V. The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements, the use of DCI standards, etc.), measured quiescent current levels may be different than the values in the table. Use the XPower Estimator or XPower Analyzer for more accurate estimates. See Note 2.
2. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3 XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer, part of the Xilinx ISE development software, uses the FPGA netlist as input to provide more accurate maximum and typical estimates.
3. The maximum numbers in this table also indicate the minimum current each power rail requires in order for the FPGA to power-on successfully, once all three rails are supplied. If V_{CCINT} is applied before V_{CCAUX}, there may be temporary additional I_{CCINT} current until V_{CCAUX} is applied. See Surplus I_{CCINT} if V_{CCINT} Applied before V_{CCAUX}, page 54

Table 45: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max[3]	Max[3]	
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OTCLK input to data appearing at the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.46	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.94	2.23	ns
T_{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin		XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	XC3S200 XC3S400	2.10	2.41	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	2.77	3.18	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) net to setting/resetting data at the Output pin		All	8.07	9.28	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 47.
3. For minimums, use the values reported by the Xilinx timing analyzer.

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS33	Slow	2 mA	6.38	7.34	ns
		4 mA	4.83	5.55	ns
		6 mA	4.01	4.61	ns
		8 mA	3.92	4.51	ns
		12 mA	2.91	3.35	ns
		16 mA	2.81	3.23	ns
		24 mA	2.49	2.86	ns
	Fast	2 mA	3.86	4.44	ns
		4 mA	1.87	2.15	ns
		6 mA	0.62	0.71	ns
		8 mA	0.61	0.70	ns
		12 mA	0.16	0.19	ns
		16 mA	0.14	0.16	ns
		24 mA	0.06	0.07	ns
LVDCI_33			0.28	0.32	ns
LVDCI_DV2_33			0.26	0.30	ns
LVTTL	Slow	2 mA	7.27	8.36	ns
		4 mA	4.94	5.69	ns
		6 mA	3.98	4.58	ns
		8 mA	3.98	4.58	ns
		12 mA	2.97	3.42	ns
		16 mA	2.84	3.26	ns
		24 mA	2.65	3.04	ns
	Fast	2 mA	4.32	4.97	ns
		4 mA	1.87	2.15	ns
		6 mA	1.27	1.47	ns
		8 mA	1.19	1.37	ns
		12 mA	0.42	0.48	ns
		16 mA	0.27	0.32	ns
		24 mA	0.16	0.18	ns

Table 54: **Synchronous 18 x 18 Multiplier Timing**

Symbol	Description	P Outputs	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Clock-to-Output Times							
T_{MULTCK}	When reading from the Multiplier, the time from the active transition at the C clock input to data appearing at the P outputs	P[0]	–	1.00	–	1.15	ns
		P[15]	–	1.15	–	1.32	ns
		P[17]	–	1.30	–	1.50	ns
		P[19]	–	1.45	–	1.67	ns
		P[23]	–	1.76	–	2.02	ns
		P[31]	–	2.37	–	2.72	ns
		P[35]	–	2.67	–	3.07	ns
Setup Times							
$T_{MULIDCK}$	Time from the setup of data at the A and B inputs to the active transition at the C input of the Multiplier	-	1.84	–	2.11	–	ns
Hold Times							
$T_{MULCKID}$	Time from the active transition at the Multiplier's C input to the point where data is last held at the A and B inputs	-	0	–	0	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.

Table 55: **Asynchronous 18 x 18 Multiplier Timing**

Symbol	Description	P Outputs	Speed Grade		Units
			-5	-4	
			Max	Max	
Propagation Times					
T_{MULT}	The time it takes for data to travel from the A and B inputs to the P outputs	P[0]	1.55	1.78	ns
		P[15]	3.15	3.62	ns
		P[17]	3.36	3.86	ns
		P[19]	3.49	4.01	ns
		P[23]	3.73	4.29	ns
		P[31]	4.23	4.86	ns
		P[35]	4.47	5.14	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.

Table 67: **Timing for the Master and Slave Parallel Configuration Modes *(Cont'd)***

Symbol	Description			Slave/ Master	All Speed Grades		Units
					Min	Max	
Clock Timing							
T_{CCH}	CCLK input pin High pulse width			Slave	5	∞	ns
T_{CCL}	CCLK input pin Low pulse width				5	∞	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Not using the BUSY pin(4)		0	50	MHz
			Using the BUSY pin		0	66	MHz
		With bitstream compression			0	20	MHz
		During STARTUP phase			0	50	MHz
ΔF_{CCPAR}	Variation from the CCLK output frequency set using the BitGen option ConfigRate			Master	–50%	+50%	–

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. Some Xilinx documents may refer to Parallel modes as "SelectMAP" modes.
3. RDWR_B is synchronized to CCLK for the purpose of performing the Abort operation. The same pin asynchronously controls the driver impedance of the D0 - D7 pins. To avoid contention when writing configuration data to the D0 - D7 bus, do not bring RDWR_B High when CS_B is Low.
4. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.

Table 93: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
N/A	GND	GND	P14	GND
N/A	GND	GND	P25	GND
N/A	VCCAUX	VCCAUX	P193	VCCAUX
N/A	VCCAUX	VCCAUX	P173	VCCAUX
N/A	VCCAUX	VCCAUX	P142	VCCAUX
N/A	VCCAUX	VCCAUX	P121	VCCAUX
N/A	VCCAUX	VCCAUX	P89	VCCAUX
N/A	VCCAUX	VCCAUX	P69	VCCAUX
N/A	VCCAUX	VCCAUX	P38	VCCAUX
N/A	VCCAUX	VCCAUX	P17	VCCAUX
N/A	VCCINT	VCCINT	P192	VCCINT
N/A	VCCINT	VCCINT	P174	VCCINT
N/A	VCCINT	VCCINT	P88	VCCINT
N/A	VCCINT	VCCINT	P70	VCCINT
VCCAUX	CCLK	CCLK	P104	CONFIG
VCCAUX	DONE	DONE	P103	CONFIG
VCCAUX	HSWAP_EN	HSWAP_EN	P206	CONFIG
VCCAUX	M0	M0	P55	CONFIG
VCCAUX	M1	M1	P54	CONFIG
VCCAUX	M2	M2	P56	CONFIG
VCCAUX	PROG_B	PROG_B	P207	CONFIG
VCCAUX	TCK	TCK	P159	JTAG
VCCAUX	TDI	TDI	P208	JTAG
VCCAUX	TDO	TDO	P158	JTAG
VCCAUX	TMS	TMS	P160	JTAG

FT256: 256-lead Fine-pitch Thin Ball Grid Array

The 256-lead fine-pitch thin ball grid array package, FT256, supports three different Spartan-3 devices, including the XC3S200, the XC3S400, and the XC3S1000. The footprints for all three devices are identical, as shown in Table 96 and Figure 49.

All the package pins appear in Table 96 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 96: **FT256 Package Pinout**

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
0	IO	A5	I/O
0	IO	A7	I/O
0	IO/VREF_0	A3	VREF
0	IO/VREF_0	D5	VREF
0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L25N_0	C5	I/O
0	IO_L25P_0	B5	I/O
0	IO_L27N_0	E6	I/O
0	IO_L27P_0	D6	I/O
0	IO_L28N_0	C6	I/O
0	IO_L28P_0	B6	I/O
0	IO_L29N_0	E7	I/O
0	IO_L29P_0	D7	I/O
0	IO_L30N_0	C7	I/O
0	IO_L30P_0	B7	I/O
0	IO_L31N_0	D8	I/O
0	IO_L31P_0/VREF_0	C8	VREF
0	IO_L32N_0/GCLK7	B8	GCLK
0	IO_L32P_0/GCLK6	A8	GCLK
0	VCCO_0	E8	VCCO
0	VCCO_0	F7	VCCO
0	VCCO_0	F8	VCCO
1	IO	A9	I/O
1	IO	A12	I/O
1	IO	C10	I/O
1	IO/VREF_1	D12	VREF
1	IO_L01N_1/VRP_1	A14	DCI
1	IO_L01P_1/VRN_1	B14	DCI

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
3	IO_L16P_3	IO_L16P_3	Y22	I/O
3	IO_L17N_3	IO_L17N_3	V19	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	W19	VREF
3	IO_L19N_3	IO_L19N_3	W21	I/O
3	IO_L19P_3	IO_L19P_3	W20	I/O
3	IO_L20N_3	IO_L20N_3	U19	I/O
3	IO_L20P_3	IO_L20P_3	V20	I/O
3	IO_L21N_3	IO_L21N_3	V22	I/O
3	IO_L21P_3	IO_L21P_3	V21	I/O
3	IO_L22N_3	IO_L22N_3	T17	I/O
3	IO_L22P_3	IO_L22P_3	U18	I/O
3	IO_L23N_3	IO_L23N_3	U21	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	U20	VREF
3	IO_L24N_3	IO_L24N_3	R18	I/O
3	IO_L24P_3	IO_L24P_3	T18	I/O
3	N.C. (◆)	IO_L26N_3	T20	I/O
3	N.C. (◆)	IO_L26P_3	T19	I/O
3	IO_L27N_3	IO_L27N_3	T22	I/O
3	IO_L27P_3	IO_L27P_3	T21	I/O
3	N.C. (◆)	IO_L28N_3	R22	I/O
3	N.C. (◆)	IO_L28P_3	R21	I/O
3	N.C. (◆)	IO_L29N_3	P19	I/O
3	N.C. (◆)	IO_L29P_3	R19	I/O
3	N.C. (◆)	IO_L31N_3	P18	I/O
3	N.C. (◆)	IO_L31P_3	P17	I/O
3	N.C. (◆)	IO_L32N_3	P22	I/O
3	N.C. (◆)	IO_L32P_3	P21	I/O
3	N.C. (◆)	IO_L33N_3	N18	I/O
3	N.C. (◆)	IO_L33P_3	N17	I/O
3	IO_L34N_3	IO_L34N_3	N20	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	N19	VREF
3	IO_L35N_3	IO_L35N_3	N22	I/O
3	IO_L35P_3	IO_L35P_3	N21	I/O
3	IO_L38N_3	IO_L38N_3	M18	I/O
3	IO_L38P_3	IO_L38P_3	M17	I/O
3	IO_L39N_3	IO_L39N_3	M20	I/O
3	IO_L39P_3	IO_L39P_3	M19	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	M22	VREF
3	IO_L40P_3	IO_L40P_3	M21	I/O
3	VCCO_3	VCCO_3	M16	VCCO

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
6	N.C. (◆)	IO_L28N_6	R5	I/O
6	N.C. (◆)	IO_L28P_6	P6	I/O
6	N.C. (◆)	IO_L29N_6	R2	I/O
6	N.C. (◆)	IO_L29P_6	R1	I/O
6	N.C. (◆)	IO_L31N_6	P5	I/O
6	N.C. (◆)	IO_L31P_6	P4	I/O
6	N.C. (◆)	IO_L32N_6	P2	I/O
6	N.C. (◆)	IO_L32P_6	P1	I/O
6	N.C. (◆)	IO_L33N_6	N6	I/O
6	N.C. (◆)	IO_L33P_6	N5	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	N4	VREF
6	IO_L34P_6	IO_L34P_6	N3	I/O
6	IO_L35N_6	IO_L35N_6	N2	I/O
6	IO_L35P_6	IO_L35P_6	N1	I/O
6	IO_L38N_6	IO_L38N_6	M6	I/O
6	IO_L38P_6	IO_L38P_6	M5	I/O
6	IO_L39N_6	IO_L39N_6	M4	I/O
6	IO_L39P_6	IO_L39P_6	M3	I/O
6	IO_L40N_6	IO_L40N_6	M2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	M1	VREF
6	VCCO_6	VCCO_6	M7	VCCO
6	VCCO_6	VCCO_6	N7	VCCO
6	VCCO_6	VCCO_6	P7	VCCO
6	VCCO_6	VCCO_6	R3	VCCO
6	VCCO_6	VCCO_6	R6	VCCO
7	IO	IO	C2	I/O
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	C3	DCI
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	C4	DCI
7	IO_L16N_7	IO_L16N_7	D1	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	C1	VREF
7	IO_L17N_7	IO_L17N_7	E4	I/O
7	IO_L17P_7	IO_L17P_7	D4	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	D3	VREF
7	IO_L19P_7	IO_L19P_7	D2	I/O
7	IO_L20N_7	IO_L20N_7	F4	I/O
7	IO_L20P_7	IO_L20P_7	E3	I/O
7	IO_L21N_7	IO_L21N_7	E1	I/O
7	IO_L21P_7	IO_L21P_7	E2	I/O
7	IO_L22N_7	IO_L22N_7	G6	I/O
7	IO_L22P_7	IO_L22P_7	F5	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	F6	DCI
7	IO_L02N_7	IO_L02N_7	IO_L02N_7	IO_L02N_7	IO_L02N_7	E3	I/O
7	IO_L02P_7	IO_L02P_7	IO_L02P_7	IO_L02P_7	IO_L02P_7	E4	I/O
7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	D1	VREF
7	IO_L03P_7	IO_L03P_7	IO_L03P_7	IO_L03P_7	IO_L03P_7	D2	I/O
7	N.C. (◆)	IO_L05N_7	IO_L05N_7	IO_L05N_7	IO_L05N_7	G6	I/O
7	N.C. (◆)	IO_L05P_7	IO_L05P_7	IO_L05P_7	IO_L05P_7	G7	I/O
7	N.C. (◆)	IO_L06N_7	IO_L06N_7	IO_L06N_7	IO_L06N_7	E1	I/O
7	N.C. (◆)	IO_L06P_7	IO_L06P_7	IO_L06P_7	IO_L06P_7	E2	I/O
7	N.C. (◆)	IO_L07N_7	IO_L07N_7	IO_L07N_7	IO_L07N_7	F3	I/O
7	N.C. (◆)	IO_L07P_7	IO_L07P_7	IO_L07P_7	IO_L07P_7	F4	I/O
7	N.C. (◆)	IO_L08N_7	IO_L08N_7	IO_L08N_7	IO_L08N_7	G4	I/O
7	N.C. (◆)	IO_L08P_7	IO_L08P_7	IO_L08P_7	IO_L08P_7	G5	I/O
7	N.C. (◆)	IO_L09N_7	IO_L09N_7	IO_L09N_7	IO_L09N_7	F1	I/O
7	N.C. (◆)	IO_L09P_7	IO_L09P_7	IO_L09P_7	IO_L09P_7	F2	I/O
7	N.C. (◆)	IO_L10N_7	IO_L10N_7	IO_L10N_7	IO_L10N_7	H6	I/O
7	N.C. (◆)	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	H7	VREF
7	IO_L14N_7	IO_L14N_7	IO_L14N_7	IO_L14N_7	IO_L14N_7	G1	I/O
7	IO_L14P_7	IO_L14P_7	IO_L14P_7	IO_L14P_7	IO_L14P_7	G2	I/O
7	IO_L16N_7	IO_L16N_7	IO_L16N_7	IO_L16N_7	IO_L16N_7	J6	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	H5	VREF
7	IO_L17N_7	IO_L17N_7	IO_L17N_7	IO_L17N_7	IO_L17N_7	H3	I/O
7	IO_L17P_7	IO_L17P_7	IO_L17P_7	IO_L17P_7	IO_L17P_7	H4	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	H1	VREF
7	IO_L19P_7	IO_L19P_7	IO_L19P_7	IO_L19P_7	IO_L19P_7	H2	I/O
7	IO_L20N_7	IO_L20N_7	IO_L20N_7	IO_L20N_7	IO_L20N_7	K7	I/O
7	IO_L20P_7	IO_L20P_7	IO_L20P_7	IO_L20P_7	IO_L20P_7	J7	I/O
7	IO_L21N_7	IO_L21N_7	IO_L21N_7	IO_L21N_7	IO_L21N_7	J4	I/O
7	IO_L21P_7	IO_L21P_7	IO_L21P_7	IO_L21P_7	IO_L21P_7	J5	I/O
7	IO_L22N_7	IO_L22N_7	IO_L22N_7	IO_L22N_7	IO_L22N_7	J2	I/O
7	IO_L22P_7	IO_L22P_7	IO_L22P_7	IO_L22P_7	IO_L22P_7	J3	I/O
7	IO_L23N_7	IO_L23N_7	IO_L23N_7	IO_L23N_7	IO_L23N_7	K5	I/O
7	IO_L23P_7	IO_L23P_7	IO_L23P_7	IO_L23P_7	IO_L23P_7	K6	I/O
7	IO_L24N_7	IO_L24N_7	IO_L24N_7	IO_L24N_7	IO_L24N_7	K3	I/O
7	IO_L24P_7	IO_L24P_7	IO_L24P_7	IO_L24P_7	IO_L24P_7	K4	I/O
7	IO_L26N_7	IO_L26N_7	IO_L26N_7	IO_L26N_7	IO_L26N_7	K1	I/O
7	IO_L26P_7	IO_L26P_7	IO_L26P_7	IO_L26P_7	IO_L26P_7	K2	I/O
7	IO_L27N_7	IO_L27N_7	IO_L27N_7	IO_L27N_7	IO_L27N_7	L7	I/O
7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	L8	VREF
7	IO_L28N_7	IO_L28N_7	IO_L28N_7	IO_L28N_7	IO_L28N_7	L5	I/O
7	IO_L28P_7	IO_L28P_7	IO_L28P_7	IO_L28P_7	IO_L28P_7	L6	I/O
7	IO_L29N_7	IO_L29N_7	IO_L29N_7	IO_L29N_7	IO_L29N_7	L1	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
1	IO_L05P_1	IO_L05P_1	F25	I/O
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	C24	VREF
1	IO_L06P_1	IO_L06P_1	D24	I/O
1	IO_L07N_1	IO_L07N_1	A24	I/O
1	IO_L07P_1	IO_L07P_1	B24	I/O
1	IO_L08N_1	IO_L08N_1	H23	I/O
1	IO_L08P_1	IO_L08P_1	G24	I/O
1	IO_L09N_1	IO_L09N_1	F23	I/O
1	IO_L09P_1	IO_L09P_1	G23	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	C23	VREF
1	IO_L10P_1	IO_L10P_1	D23	I/O
1	IO_L11N_1	IO_L11N_1	A23	I/O
1	IO_L11P_1	IO_L11P_1	B23	I/O
1	IO_L12N_1	IO_L12N_1	H22	I/O
1	IO_L12P_1	IO_L12P_1	J22	I/O
1	IO_L13N_1	IO_L13N_1	F22	I/O
1	IO_L13P_1	IO_L13P_1	E23	I/O
1	IO_L14N_1	IO_L14N_1	D22	I/O
1	IO_L14P_1	IO_L14P_1	E22	I/O
1	IO_L15N_1	IO_L15N_1	A22	I/O
1	IO_L15P_1	IO_L15P_1	B22	I/O
1	IO_L16N_1	IO_L16N_1	F21	I/O
1	IO_L16P_1	IO_L16P_1	G21	I/O
1	IO_L17N_1/VREF_1	IO_L17N_1/VREF_1	B21	VREF
1	IO_L17P_1	IO_L17P_1	C21	I/O
1	IO_L18N_1	IO_L18N_1	G20	I/O
1	IO_L18P_1	IO_L18P_1	H20	I/O
1	IO_L19N_1	IO_L19N_1	E20	I/O
1	IO_L19P_1	IO_L19P_1	F20	I/O
1	IO_L20N_1	IO_L20N_1	C20	I/O
1	IO_L20P_1	IO_L20P_1	D20	I/O
1	IO_L21N_1	IO_L21N_1	A20	I/O
1	IO_L21P_1	IO_L21P_1	B20	I/O
1	IO_L22N_1	IO_L22N_1	J19	I/O
1	IO_L22P_1	IO_L22P_1	K19	I/O
1	IO_L23N_1	IO_L23N_1	G19	I/O
1	IO_L23P_1	IO_L23P_1	H19	I/O
1	IO_L24N_1	IO_L24N_1	E19	I/O
1	IO_L24P_1	IO_L24P_1	F19	I/O
1	IO_L25N_1	IO_L25N_1	C19	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
4	IO_L31P_4/DOUT/BUSY	IO_L31P_4/DOUT/BUSY	AH16	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	AJ16	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	AK16	GCLK
4	N.C. (◆)	IO_L33N_4	AH25	I/O
4	N.C. (◆)	IO_L33P_4	AJ25	I/O
4	N.C. (◆)	IO_L34N_4	AE25	I/O
4	N.C. (◆)	IO_L34P_4	AE24	I/O
4	N.C. (◆)	IO_L35N_4	AG24	I/O
4	N.C. (◆)	IO_L35P_4	AH24	I/O
4	N.C. (◆)	IO_L38N_4	AJ24	I/O
4	N.C. (◆)	IO_L38P_4	AK24	I/O
4	VCCO_4	VCCO_4	Y17	VCCO
4	VCCO_4	VCCO_4	Y18	VCCO
4	VCCO_4	VCCO_4	AD18	VCCO
4	VCCO_4	VCCO_4	AH18	VCCO
4	VCCO_4	VCCO_4	Y19	VCCO
4	VCCO_4	VCCO_4	AB20	VCCO
4	VCCO_4	VCCO_4	AD22	VCCO
4	VCCO_4	VCCO_4	AH22	VCCO
4	VCCO_4	VCCO_4	AF24	VCCO
4	VCCO_4	VCCO_4	AH26	VCCO
5	IO	IO	AE6	I/O
5	IO	IO	AB10	I/O
5	IO	IO	AA11	I/O
5	IO	IO	AA15	I/O
5	IO	IO	AE15	I/O
5	IO/VREF_5	IO/VREF_5	AH4	VREF
5	IO/VREF_5	IO/VREF_5	AK15	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	AK4	DUAL
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AJ4	DUAL
5	IO_L02N_5	IO_L02N_5	AK5	I/O
5	IO_L02P_5	IO_L02P_5	AJ5	I/O
5	IO_L03N_5	IO_L03N_5	AF6	I/O
5	IO_L03P_5	IO_L03P_5	AG5	I/O
5	IO_L04N_5	IO_L04N_5	AJ6	I/O
5	IO_L04P_5	IO_L04P_5	AH6	I/O
5	IO_L05N_5	IO_L05N_5	AE7	I/O
5	IO_L05P_5	IO_L05P_5	AD7	I/O
5	IO_L06N_5	IO_L06N_5	AH7	I/O
5	IO_L06P_5	IO_L06P_5	AG7	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
6	IO_L05P_6	IO_L05P_6	AE5	I/O
6	IO_L06N_6	IO_L06N_6	AE3	I/O
6	IO_L06P_6	IO_L06P_6	AE2	I/O
6	IO_L07N_6	IO_L07N_6	AD4	I/O
6	IO_L07P_6	IO_L07P_6	AD3	I/O
6	IO_L08N_6	IO_L08N_6	AD2	I/O
6	IO_L08P_6	IO_L08P_6	AD1	I/O
6	IO_L09N_6/VREF_6	IO_L09N_6/VREF_6	AD6	VREF
6	IO_L09P_6	IO_L09P_6	AC7	I/O
6	IO_L10N_6	IO_L10N_6	AC6	I/O
6	IO_L10P_6	IO_L10P_6	AC5	I/O
6	IO_L11N_6	IO_L11N_6	AC4	I/O
6	IO_L11P_6	IO_L11P_6	AC3	I/O
6	IO_L13N_6	IO_L13N_6	AC2	I/O
6	IO_L13P_6/VREF_6	IO_L13P_6/VREF_6	AC1	VREF
6	IO_L14N_6	IO_L14N_6	AB5	I/O
6	IO_L14P_6	IO_L14P_6	AB4	I/O
6	IO_L15N_6	IO_L15N_6	AB2	I/O
6	IO_L15P_6	IO_L15P_6	AB1	I/O
6	IO_L16N_6	IO_L16N_6	AB8	I/O
6	IO_L16P_6	IO_L16P_6	AA9	I/O
6	IO_L17N_6	IO_L17N_6	AA7	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	AA6	VREF
6	IO_L19N_6	IO_L19N_6	AA3	I/O
6	IO_L19P_6	IO_L19P_6	AA2	I/O
6	IO_L20N_6	IO_L20N_6	AA10	I/O
6	IO_L20P_6	IO_L20P_6	Y10	I/O
6	IO_L21N_6	IO_L21N_6	Y8	I/O
6	IO_L21P_6	IO_L21P_6	Y7	I/O
6	IO_L22N_6	IO_L22N_6	Y6	I/O
6	IO_L22P_6	IO_L22P_6	Y5	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	Y2	VREF
6	IO_L24P_6	IO_L24P_6	Y1	I/O
6	N.C. (◆)	IO_L25N_6	W9	I/O
6	N.C. (◆)	IO_L25P_6	W8	I/O
6	IO_L26N_6	IO_L26N_6	W7	I/O
6	IO_L26P_6	IO_L26P_6	W6	I/O
6	IO_L27N_6	IO_L27N_6	W4	I/O
6	IO_L27P_6	IO_L27P_6	W3	I/O
6	IO_L28N_6	IO_L28N_6	W2	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
0	VCCO_0	VCCO_0	F13	VCCO
0	VCCO_0	VCCO_0	G8	VCCO
0	VCCO_0	VCCO_0	H11	VCCO
0	VCCO_0	VCCO_0	H15	VCCO
0	VCCO_0	VCCO_0	M13	VCCO
0	VCCO_0	VCCO_0	M14	VCCO
0	VCCO_0	VCCO_0	M15	VCCO
0	VCCO_0	VCCO_0	M16	VCCO
1	IO	IO	B26	I/O
1	IO	IO	A18	I/O
1	IO	IO	C23	I/O
1	IO	IO	E21	I/O
1	IO	IO	E25	I/O
1	IO	IO	F18	I/O
1	IO	IO	F27	I/O
1	IO	IO	F29	I/O
1	IO	IO	H23	I/O
1	IO	IO	H26	I/O
1	N.C. (◆)	IO	J26	I/O
1	IO	IO	K19	I/O
1	IO	IO	L19	I/O
1	IO	IO	L20	I/O
1	IO	IO	L21	I/O
1	N.C. (◆)	IO	L23	I/O
1	IO	IO	L24	I/O
1	IO/VREF_1	IO/VREF_1	D30	VREF
1	IO/VREF_1	IO/VREF_1	K21	VREF
1	IO/VREF_1	IO/VREF_1	L18	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	A32	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B32	DCI
1	IO_L02N_1	IO_L02N_1	A31	I/O
1	IO_L02P_1	IO_L02P_1	B31	I/O
1	IO_L03N_1	IO_L03N_1	B30	I/O
1	IO_L03P_1	IO_L03P_1	C30	I/O
1	IO_L04N_1	IO_L04N_1	C29	I/O
1	IO_L04P_1	IO_L04P_1	D29	I/O
1	IO_L05N_1	IO_L05N_1	A29	I/O
1	IO_L05P_1	IO_L05P_1	B29	I/O
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	E28	VREF
1	IO_L06P_1	IO_L06P_1	F28	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
1	IO_L07N_1	IO_L07N_1	D27	I/O
1	IO_L07P_1	IO_L07P_1	E27	I/O
1	IO_L08N_1	IO_L08N_1	A27	I/O
1	IO_L08P_1	IO_L08P_1	B27	I/O
1	IO_L09N_1	IO_L09N_1	F26	I/O
1	IO_L09P_1	IO_L09P_1	G26	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	C26	VREF
1	IO_L10P_1	IO_L10P_1	D26	I/O
1	IO_L11N_1	IO_L11N_1	H25	I/O
1	IO_L11P_1	IO_L11P_1	J25	I/O
1	IO_L12N_1	IO_L12N_1	F25	I/O
1	IO_L12P_1	IO_L12P_1	G25	I/O
1	IO_L13N_1	IO_L13N_1	C25	I/O
1	IO_L13P_1	IO_L13P_1	D25	I/O
1	IO_L14N_1	IO_L14N_1	A25	I/O
1	IO_L14P_1	IO_L14P_1	B25	I/O
1	IO_L15N_1	IO_L15N_1	A24	I/O
1	IO_L15P_1	IO_L15P_1	B24	I/O
1	IO_L16N_1	IO_L16N_1	J23	I/O
1	IO_L16P_1	IO_L16P_1	K23	I/O
1	IO_L17N_1/VREF_1	IO_L17N_1/VREF_1	F23	VREF
1	IO_L17P_1	IO_L17P_1	G23	I/O
1	IO_L18N_1	IO_L18N_1	D23	I/O
1	IO_L18P_1	IO_L18P_1	E23	I/O
1	IO_L19N_1	IO_L19N_1	A23	I/O
1	IO_L19P_1	IO_L19P_1	B23	I/O
1	IO_L20N_1	IO_L20N_1	K22	I/O
1	IO_L20P_1	IO_L20P_1	L22	I/O
1	IO_L21N_1	IO_L21N_1	G22	I/O
1	IO_L21P_1	IO_L21P_1	H22	I/O
1	IO_L22N_1	IO_L22N_1	C22	I/O
1	IO_L22P_1	IO_L22P_1	D22	I/O
1	IO_L23N_1	IO_L23N_1	H21	I/O
1	IO_L23P_1	IO_L23P_1	J21	I/O
1	IO_L24N_1	IO_L24N_1	F21	I/O
1	IO_L24P_1	IO_L24P_1	G21	I/O
1	IO_L25N_1	IO_L25N_1	C21	I/O
1	IO_L25P_1	IO_L25P_1	D21	I/O
1	IO_L26N_1	IO_L26N_1	A21	I/O
1	IO_L26P_1	IO_L26P_1	B21	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
1	VCCO_1	VCCO_1	M22	VCCO
2	IO	IO	G33	I/O
2	IO	IO	G34	I/O
2	IO	IO	U25	I/O
2	IO	IO	U26	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C33	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C34	DCI
2	IO_L02N_2	IO_L02N_2	D33	I/O
2	IO_L02P_2	IO_L02P_2	D34	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	E32	VREF
2	IO_L03P_2	IO_L03P_2	E33	I/O
2	IO_L04N_2	IO_L04N_2	F31	I/O
2	IO_L04P_2	IO_L04P_2	F32	I/O
2	IO_L05N_2	IO_L05N_2	G29	I/O
2	IO_L05P_2	IO_L05P_2	G30	I/O
2	IO_L06N_2	IO_L06N_2	H29	I/O
2	IO_L06P_2	IO_L06P_2	H30	I/O
2	IO_L07N_2	IO_L07N_2	H33	I/O
2	IO_L07P_2	IO_L07P_2	H34	I/O
2	IO_L08N_2	IO_L08N_2	J28	I/O
2	IO_L08P_2	IO_L08P_2	J29	I/O
2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	H31	VREF
2	IO_L09P_2	IO_L09P_2	J31	I/O
2	IO_L10N_2	IO_L10N_2	J32	I/O
2	IO_L10P_2	IO_L10P_2	J33	I/O
2	IO_L11N_2	IO_L11N_2	J27	I/O
2	IO_L11P_2	IO_L11P_2	K26	I/O
2	IO_L12N_2	IO_L12N_2	K27	I/O
2	IO_L12P_2	IO_L12P_2	K28	I/O
2	IO_L13N_2	IO_L13N_2	K29	I/O
2	IO_L13P_2/VREF_2	IO_L13P_2/VREF_2	K30	VREF
2	IO_L14N_2	IO_L14N_2	K31	I/O
2	IO_L14P_2	IO_L14P_2	K32	I/O
2	IO_L15N_2	IO_L15N_2	K33	I/O
2	IO_L15P_2	IO_L15P_2	K34	I/O
2	IO_L16N_2	IO_L16N_2	L25	I/O
2	IO_L16P_2	IO_L16P_2	L26	I/O
2	N.C. (◆)	IO_L17N_2	L28	I/O
2	N.C. (◆)	IO_L17P_2/ VREF_2	L29	VREF

All Devices

Top Right Corner of FG1156 Package (Top View)

12	**DUAL:** Configuration pin, then possible user I/O	16	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	104	**VCCO:** Output voltage supply for bank
40	**VCCINT:** Internal core voltage supply (+1.2V)	32	**VCCAUX:** Auxiliary voltage supply (+2.5V)	184	**GND:** Ground

Bank 1

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
I/O	GND	I/O L40N_1	I/O L26N_1	GND	I/O L19N_1	I/O L15N_1	I/O L14N_1	GND	I/O L08N_1	I/O L34N_1 ◆	I/O L05N_1	GND	I/O L02N_1	I/O L01N_1 VRP_1	GND	GND	A
I/O L32N_1 GCLK5	I/O L28N_1	I/O L40P_1	I/O L26P_1	VCCO_1	I/O L19P_1	I/O L15P_1	I/O L14P_1	I/O	I/O L08P_1	I/O L34P_1 ◆	I/O L05P_1	I/O L03N_1	I/O L02P_1	I/O L01P_1 VRN_1	GND	GND	B
I/O L32P_1 GCLK4	I/O L28P_1	I/O L39N_1	I/O L25N_1	I/O L22N_1	I/O	GND	I/O L13N_1	I/O L10N_1 VREF_1	VCCO_1	I/O L33N_1 ◆	I/O L04N_1	I/O L03P_1	VCCO_1	GND	I/O L01N_2 VRP_2	I/O L01P_2 VRN_2	C
I/O L31N_1 VREF_1	VCCO_1	I/O L39P_1	I/O L25P_1	I/O L22P_1	I/O L18N_1	VCCO_1	I/O L13P_1	I/O L10P_1	I/O L07N_1	I/O L33P_1 ◆	I/O L04P_1	IO VREF_1	TCK	VCCO_2	I/O L02N_2	I/O L02P_2	D
I/O L31P_1	GND	VCCAUX	I/O	GND	I/O L18P_1	VCCAUX	I/O	GND	I/O L07P_1	I/O L06N_1 VREF_1	VCCAUX	GND	TDO	I/O L03N_2 VREF_2	I/O L03P_2	GND	E
I/O	I/O L27N_1	I/O L38N_1	I/O L24N_1	VCCO_1	I/O L17N_1 VREF_1	I/O L36N_1 ◆	I/O L12N_1	I/O L09N_1	I/O	I/O L06P_1	I/O	VCCAUX	I/O L04N_2	I/O L04P_2	I/O L41N_2	I/O L41P_2	F
I/O L30N_1	I/O L27P_1	I/O L38P_1	I/O L24P_1	I/O L21N_1	I/O L17P_1	I/O L36P_1 ◆	I/O L12P_1	I/O L09P_1	VCCO_1	GND	I/O L05N_2	I/O L05P_2	I/O L42N_2 ◆	I/O L42P_2 ◆	I/O	I/O	G
I/O L30P_1	VCCAUX	VCCO_1	I/O L23N_1	I/O L21P_1	I/O	VCCO_1	I/O L11N_1	I/O	TMS	VCCO_2	I/O L06N_2	I/O L06P_2	I/O L09N_2 VREF_2	VCCO_2	I/O L07N_2	I/O L07P_2	H
I/O L29N_1	GND	I/O L37N_1	I/O L23P_1	GND	I/O L16N_1	I/O L35N_1 ◆	I/O L11P_1	I/O ◆	I/O L11N_2	I/O L08N_2	I/O L08P_2	GND	I/O L09P_2	I/O L10N_2	I/O L10P_2	GND	J
I/O L29P_1	I/O	I/O L37P_1	IO VREF_1	I/O L20N_1	I/O L16P_1	I/O L35P_1 ◆	GND	I/O L11P_2	I/O L12N_2	I/O L12P_2	I/O L13N_2	I/O L13P_2 VREF_2	I/O L14N_2	I/O L14P_2	I/O L15N_2	I/O L15P_2	K
IO VREF_1	I/O	I/O	I/O	I/O L20P_1	I/O ◆	I/O	I/O L16N_2	I/O L16P_2	VCCO_2	I/O L17N_2 ◆	I/O L17P_2 VREF_2 ◆	VCCAUX	VCCO_2	GND	I/O L45N_2	I/O L45P_2	L
VCCINT	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCINT	I/O L46N_2	I/O L46P_2	I/O L21N_2	I/O L47N_2	I/O L47P_2	I/O L19N_2	I/O L19P_2	I/O L20N_2	I/O L20P_2	I/O L48N_2	I/O L48P_2	M
GND	VCCINT	VCCINT	VCCINT	VCCINT	VCCO_2	I/O L24N_2	I/O L21P_2	GND	I/O L22N_2	I/O L22P_2	VCCO_2	GND	I/O L23N_2 VREF_2	I/O L23P_2	VCCO_2	GND	N
GND	GND	GND	GND	VCCINT	VCCO_2	I/O L24P_2	I/O L49N_2 ◆	I/O L49P_2 ◆	I/O L50N_2	I/O L50P_2	I/O L26N_2	I/O L26P_2	I/O L27N_2	I/O L27P_2	I/O L28N_2	I/O L28P_2	P
GND	GND	GND	GND	VCCINT	VCCO_2	I/O L29N_2	I/O L29P_2	I/O L33N_2	VCCO_2	I/O L30N_2	I/O L30P_2	VCCAUX	I/O L31N_2	I/O L31P_2	I/O L32N_2	I/O L32P_2	R
GND	GND	GND	GND	VCCINT	VCCO_2	I/O L51N_2 ◆	I/O L33P_2	GND	VCCAUX	I/O L34N_2 VREF_2	I/O L34P_2	GND	VCCO_2	I/O L35N_2	I/O L35P_2	GND	T
GND	GND	GND	GND	GND	VCCINT	I/O L51P_2 ◆	I/O	I/O	I/O L37N_2	I/O L37P_2	I/O L38N_2	I/O L38P_2	I/O L39N_2	I/O L39P_2	I/O L40N_2	I/O L40P_2 VREF_2	U

Bank 2

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Figure 58: FG1156 Package Footprint (Top View) Continued