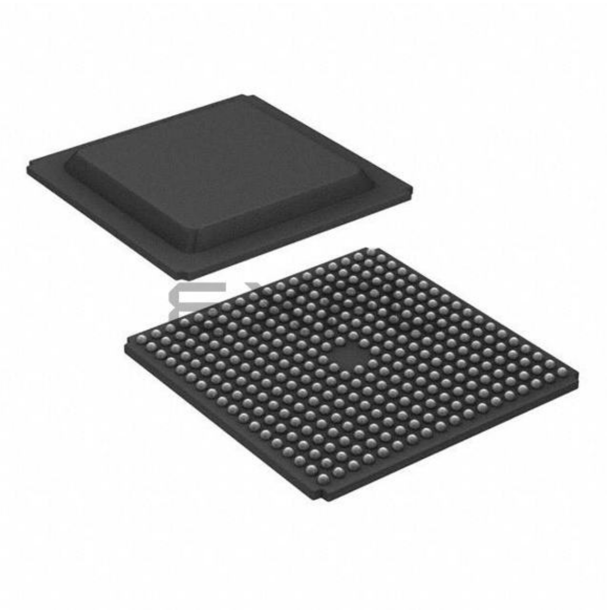

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 3328 |
| Number of Logic Elements/Cells | 29952 |
| Total RAM Bits | 589824 |
| Number of I/O | 221 |
| Number of Gates | 1500000 |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 320-BGA |
| Supplier Device Package | 320-FBGA (19x19) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc3s1500-4fg320i |

# IOBs

For additional information, refer to the chapter entitled "Using I/O Resources" in UG331: *Spartan-3 Generation FPGA User Guide*.

## IOB Overview

The Input/Output Block (IOB) provides a programmable, bidirectional interface between an I/O pin and the FPGA's internal logic.

A simplified diagram of the IOB's internal structure appears in Figure 7. There are three main signal paths within the IOB: the output path, input path, and 3-state path. Each path has its own pair of storage elements that can act as either registers or latches. For more information, see the Storage Element Functions section. The three main signal paths are as follows:

- The input path carries data from the pad, which is bonded to a package pin, through an optional programmable delay element directly to the I line. There are alternate routes through a pair of storage elements to the IQ1 and IQ2 lines. The IOB outputs I, IQ1, and IQ2 all lead to the FPGA's internal logic. The delay element can be set to ensure a hold time of zero.
- The output path, starting with the O1 and O2 lines, carries data from the FPGA's internal logic through a multiplexer and then a three-state driver to the IOB pad. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.
- The 3-state path determines when the output driver is high impedance. The T1 and T2 lines carry data from the FPGA's internal logic through a multiplexer to the output driver. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements. When the T1 or T2 lines are asserted High, the output driver is high-impedance (floating, hi-Z). The output driver is active-Low enabled.
- All signal paths entering the IOB, including those associated with the storage elements, have an inverter option. Any inverter placed on these paths is automatically absorbed into the IOB.

## Storage Element Functions

There are three pairs of storage elements in each IOB, one pair for each of the three paths. It is possible to configure each of these storage elements as an edge-triggered D-type flip-flop (FD) or a level-sensitive latch (LD).

The storage-element-pair on either the Output path or the Three-State path can be used together with a special multiplexer to produce Double-Data-Rate (DDR) transmission. This is accomplished by taking data synchronized to the clock signal's rising edge and converting them to bits synchronized on both the rising and the falling edge. The combination of two registers and a multiplexer is referred to as a Double-Data-Rate D-type flip-flop (FDDR). See Double-Data-Rate Transmission, page 12 for more information.

The signal paths associated with the storage element are described in Table 5.

*Table 5:* **Storage Element Signal Description**

| Storage Element Signal | Description | Function |
|---|---|---|
| D | Data input | Data at this input is stored on the active edge of CK enabled by CE. For latch operation when the input is enabled, data passes directly to the output Q. |
| Q | Data output | The data on this output reflects the state of the storage element. For operation as a latch in transparent mode, Q will mirror the data at D. |
| CK | Clock input | A signal's active edge on this input with CE asserted, loads data into the storage element. |
| CE | Clock Enable input | When asserted, this input enables CK. If not connected, CE defaults to the asserted state. |
| SR | Set/Reset | Forces storage element into the state specified by the SRHIGH/SRLOW attributes. The SYNC/ASYNC attribute setting determines if the SR input is synchronized to the clock or not. |
| REV | Reverse | Used together with SR. Forces storage element into the state opposite from what SR does. |

### DFS Clock Output Connections

There are two basic cases that determine how to connect the DFS clock outputs: on-chip and off-chip, which are illustrated in sections [a] and [c], respectively, of Figure 21. This is similar to what has already been described for the DLL component. See DLL Clock Output and Feedback Connections, page 34.

In the on-chip case, it is possible to connect either of the DFS's two output clock signals through general routing resources to the FPGA's internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. The optional feedback loop is formed in this way, routing CLK0 to a global clock net, which in turn drives the CLKFB input.

In the off-chip case, the DFS's two output clock signals, plus CLK0 for an optional feedback loop, can exit the FPGA using output buffers (OBUF) to drive a clock network plus registers on the board. The feedback loop is formed by feeding the CLK0 signal back into the FPGA using an IBUFG, which directly accesses the global clock network, or an IBUF. Then, the global clock net is connected directly to the CLKFB input.

## Phase Shifter (PS)

The DCM provides two approaches to controlling the phase of a DCM clock output signal relative to the CLKIN signal: First, there are nine clock outputs that employ the DLL to achieve a desired phase relationship: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, CLKDV CLKFX, and CLKFX180. These outputs afford "coarse" phase control.

The second approach uses the PS component described in this section to provide a still finer degree of control. The PS component is only available when the DLL is operating in its low-frequency mode. The PS component phase shifts the DCM output clocks by introducing a "fine phase shift" ($T_{PS}$) between the CLKFB and CLKIN signals inside the DLL component. The user can control this fine phase shift down to a resolution of 1/256 of a CLKIN cycle or one tap delay (DCM_TAP), whichever is greater. When in use, the PS component shifts the phase of all nine DCM clock output signals together. If the PS component is used together with a DCM clock output such as the CLK90, CLK180, CLK270, CLK2X180 and CLKFX180, then the fine phase shift of the former gets added to the coarse phase shift of the latter.

### PS Component Enabling and Mode Selection

The CLKOUT_PHASE_SHIFT attribute enables the PS component for use in addition to selecting between two operating modes. As described in Table 20, this attribute has three possible values: NONE, FIXED and VARIABLE. When CLKOUT_PHASE_SHIFT is set to NONE, the PS component is disabled and its inputs, PSEN, PSCLK, and PSINCDEC, must be tied to GND. The set of waveforms in section [a] of Figure 22 shows the disabled case, where the DLL maintains a zero-phase alignment of signals CLKFB and CLKIN upon which the PS component has no effect. The PS component is enabled by setting the attribute to either the FIXED or VARIABLE values, which select the Fixed Phase mode and the Variable Phase mode, respectively. These two modes are described in the sections that follow

### Determining the Fine Phase Shift

The user controls the phase shift of CLKFB relative to CLKIN by setting and/or adjusting the value of the PHASE_SHIFT attribute. This value must be an integer ranging from –255 to +255. The PS component uses this value to calculate the desired fine phase shift ($T_{PS}$) as a fraction of the CLKIN period ($T_{CLKIN}$). Given values for PHASE-SHIFT and $T_{CLKIN}$, it is possible to calculate $T_{PS}$ as follows:

$$T_{PS} = T_{CLKIN}(PHASE\_SHIFT/256) \quad \textit{Equation 4}$$

Both the Fixed Phase and Variable Phase operating modes employ this calculation. If the PHASE_SHIFT value is zero, then CLKFB and CLKIN will be in phase, the same as when the PS component is disabled. When the PHASE_SHIFT value is positive, the CLKFB signal will be shifted later in time with respect to CLKIN. If the attribute value is negative, the CLKFB signal will be shifted earlier in time with respect to CLKIN.

### The Fixed Phase Mode

This mode fixes the desired fine phase shift to a fraction of the $T_{CLKIN}$, as determined by Equation 4 and its user-selected PHASE_SHIFT value P. The set of waveforms insection [b] of Figure 22 illustrates the relationship between CLKFB and CLKIN in the Fixed Phase mode. In the Fixed Phase mode, the PSEN, PSCLK and PSINCDEC inputs are not used and must be tied to GND. Fixed phase shift requires ISE software version 10.1.03 or later.

Each BUFGMUX element, shown in Figure 24, is a 2-to-1 multiplexer that can receive signals from any of the four following sources:

- One of the four Global Clock inputs on the same side of the die—top or bottom—as the BUFGMUX element in use.
- Any of four nearby horizontal Double lines.
- Any of four outputs from the DCM in the right-hand quadrant that is on the same side of the die as the BUFGMUX element in use.
- Any of four outputs from the DCM in the left-hand quadrant that is on the same side of the die as the BUFGMUX element in use.

The multiplexer select line, S, chooses which of the two inputs, I0 or I1, drives the BUFGMUX's output signal, O, as described in Table 25. The switching from one clock to the other is glitchless, and done in such a way that the output High and Low times are never shorter than the shortest High or Low time of either input clock.

*Table 25:* **BUFGMUX Select Mechanism**

| S Input | O Output |
|---|---|
| 0 | I0 Input |
| 1 | I1 Input |

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

The BUFG clock buffer primitive drives a single clock signal onto the clock network and is essentially the same element as a BUFGMUX, just without the clock select mechanism. Similarly, the BUFGCE primitive creates an enabled clock buffer using the BUFGMUX select mechanism.

Each BUFGMUX buffers incoming clock signals to two possible destinations:

- The vertical spine belonging to the same side of the die—top or bottom—as the BUFGMUX element in use. The two spines—top and bottom—each comprise four vertical clock lines, each running from one of the BUFGMUX elements on the same side towards the center of the die. At the center of the die, clock signals reach the eight-line horizontal spine, which spans the width of the die. In turn, the horizontal spine branches out into a subsidiary clock interconnect that accesses the CLBs.
- The clock input of either DCM on the same side of the die—top or bottom—as the BUFGMUX element in use.

Use either a BUFGMUX element or a BUFG (Global Clock Buffer) element to place a Global input in the design. For the purpose of minimizing the dynamic power dissipation of the clock network, the Xilinx development software automatically disables all clock line segments that a design does not use.

A global clock line ideally drives clock inputs on the various clocked elements within the FPGA, such as CLB or IOB flip-flops or block RAMs. A global clock line also optionally drives combinatorial inputs. However, doing so provides additional loading on the clock line that might also affect clock jitter. Ideally, drive combinatorial inputs using the signal that also drives the input to the BUFGMUX or BUFG element.

For more details, refer to the chapter entitled "Using Global Clock Resources" in UG331.

*Table 33:* **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**

| Symbol | Description | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $I_L$ (2)(4) | Leakage current at User I/O, Dual-Purpose, and Dedicated pins | Driver is Hi-Z, $V_{IN}$ = 0V or $V_{CCO}$ max, sample-tested | $V_{CCO} \geq 3.0V$ | – | - | ±25 | µA |
| | | | $V_{CCO} < 3.0V$ | – | - | ±10 | µA |
| $I_{RPU}$ (3) | Current through pull-up resistor at User I/O, Dual-Purpose, and Dedicated pins | $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V | | –0.84 | - | –2.35 | mA |
| | | $V_{IN}$ = 0V, $V_{CCO}$ = 3.0V | | –0.69 | - | –1.99 | mA |
| | | $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V | | –0.47 | - | –1.41 | mA |
| | | $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | | –0.21 | - | –0.69 | mA |
| | | $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | | –0.13 | - | –0.43 | mA |
| | | $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | | –0.06 | - | –0.22 | mA |
| $R_{PU}$ (3) | Equivalent resistance of pull-up resistor at User I/O, Dual-Purpose, and Dedicated pins, derived from $I_{RPU}$ | $V_{CCO}$ = 3.0V to 3.465V | | 1.27 | - | 4.11 | kΩ |
| | | $V_{CCO}$ = 2.3V to 2.7V | | 1.15 | - | 3.25 | kΩ |
| | | $V_{CCO}$ = 1.7V to 1.9V | | 2.45 | - | 9.10 | kΩ |
| | | $V_{CCO}$ = 1.4V to 1.6V | | 3.25 | - | 12.10 | kΩ |
| | | $V_{CCO}$ = 1.14 to 1.26V | | 5.15 | - | 21.00 | kΩ |
| $I_{RPD}$ (3) | Current through pull-down resistor at User I/O, Dual-Purpose, and Dedicated pins | $V_{IN} = V_{CCO}$ | | 0.37 | - | 1.67 | mA |
| $R_{PD}$ (3) | Equivalent resistance of pull-down resistor at User I/O, Dual-Purpose, and Dedicated pins, driven from $I_{RPD}$ | $V_{IN} = V_{CCO}$ = 3.0V to 3.465V | | 1.75 | - | 9.35 | kΩ |
| | | $V_{IN} = V_{CCO}$ = 2.3V to 2.7V | | 1.35 | - | 7.30 | kΩ |
| | | $V_{IN} = V_{CCO}$ = 1.7V to 1.9V | | 1.00 | - | 5.15 | kΩ |
| | | $V_{IN} = V_{CCO}$ = 1.4V to 1.6V | | 0.85 | - | 4.35 | kΩ |
| | | $V_{IN} = V_{CCO}$ = 1.14 to 1.26V | | 0.68 | - | 3.465 | kΩ |
| $R_{DCI}$ | Value of external reference resistor to support DCI I/O standards | | | 20 | - | 100 | Ω |
| $I_{REF}$ | $V_{REF}$ current per pin | $V_{CCO} \geq 3.0V$ | | – | - | ±25 | µA |
| | | $V_{CCO} < 3.0V$ | | – | - | ±10 | µA |
| $C_{IN}$ | Input capacitance | | | 3 | - | 10 | pF |

**Notes:**

1. The numbers in this table are based on the conditions set forth in Table 32.
2. The $I_L$ specification applies to every I/O pin throughout power-on as long as the voltage on that pin stays between the absolute $V_{IN}$ minimum and maximum values (Table 28). For hot-swap applications, at the time of card connection, be sure to keep all I/O voltages within this range before applying $V_{CCO}$ power. Consider applying $V_{CCO}$ power before connecting the signal lines, to avoid turning on the ESD protection diodes, shown in Module 2: Figure 7, page 11. When the FPGA is completely unpowered, the I/O pins are high impedance, but there is a path through the upper and lower ESD protection diodes.
3. This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPU}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$. Spartan-3 family values for both resistances are stronger than they have been for previous FPGA families.
4. For single-ended signals that are placed on a differential-capable I/O, $V_{IN}$ of –0.2V to –0.3V is supported but can cause increased leakage between the two pins. See the *Parasitic Leakage* section in UG331, *Spartan-3 Generation FPGA User Guide*.

*Table 47:* **Output Timing Adjustments for IOB *(Cont'd)***

| Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD) | | | Add the Adjustment Below Speed Grade -5 | -4 | Units |
|---|---|---|---|---|---|
| LVCMOS18 | Slow | 2 mA | 5.49 | 6.31 | ns |
| | | 4 mA | 3.45 | 3.97 | ns |
| | | 6 mA | 2.84 | 3.26 | ns |
| | | 8 mA | 2.62 | 3.01 | ns |
| | | 12 mA | 2.11 | 2.43 | ns |
| | | 16 mA | 2.07 | 2.38 | ns |
| | Fast | 2 mA | 2.50 | 2.88 | ns |
| | | 4 mA | 1.15 | 1.32 | ns |
| | | 6 mA | 0.96 | 1.10 | ns |
| | | 8 mA | 0.87 | 1.01 | ns |
| | | 12 mA | 0.79 | 0.91 | ns |
| | | 16 mA | 0.76 | 0.87 | ns |
| LVDCI_18 | | | 0.81 | 0.94 | ns |
| LVDCI_DV2_18 | | | 0.67 | 0.77 | ns |
| LVCMOS25 | Slow | 2 mA | 6.43 | 7.39 | ns |
| | | 4 mA | 4.15 | 4.77 | ns |
| | | 6 mA | 3.38 | 3.89 | ns |
| | | 8 mA | 2.99 | 3.44 | ns |
| | | 12 mA | 2.53 | 2.91 | ns |
| | | 16 mA | 2.50 | 2.87 | ns |
| | | 24 mA | 2.22 | 2.55 | ns |
| | Fast | 2 mA | 3.27 | 3.76 | ns |
| | | 4 mA | 1.87 | 2.15 | ns |
| | | 6 mA | 0.32 | 0.37 | ns |
| | | 8 mA | 0.19 | 0.22 | ns |
| | | 12 mA | 0 | 0 | ns |
| | | 16 mA | –0.02 | –0.01 | ns |
| | | 24 mA | –0.04 | –0.02 | ns |
| LVDCI_25 | | | 0.27 | 0.31 | ns |
| LVDCI_DV2_25 | | | 0.16 | 0.19 | ns |

*Table 59:* **Switching Characteristics for the DLL *(Cont'd)***

| Symbol | Description | Frequency Mode / FCLKIN Range | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | -5 | | -4 | | |
| | | | | Min | Max | Min | Max | |
| **Lock Time** | | | | | | | | |
| LOCK_DLL | When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase | 18 MHz ≤ $F_{CLKIN}$ ≤ 30 MHz | All | – | 2.88 | – | 2.88 | ms |
| | | 30 MHz < $F_{CLKIN}$ ≤ 40 MHz | | – | 2.16 | – | 2.16 | ms |
| | | 40 MHz < $F_{CLKIN}$ ≤ 50 MHz | | – | 1.20 | – | 1.20 | ms |
| | | 50 MHz < $F_{CLKIN}$ ≤ 60 MHz | | – | 0.60 | – | 0.60 | ms |
| | | $F_{CLKIN}$ > 60 MHz | | – | 0.48 | – | 0.48 | ms |
| **Delay Lines** | | | | | | | | |
| DCM_TAP | Delay tap resolution | All | All | 30.0 | 60.0 | 30.0 | 60.0 | ps |

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 32 and Table 58.
2. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
3. Only mask revision 'E' and later devices (see Mask and Fab Revisions, page 58) and all revisions of the XC3S50 and the XC3S1000 support DLL feedback using the CLK2X output. For all other Spartan-3 devices, use feedback from the CLK0 output (instead of the CLK2X output) and set the CLK_FEEDBACK attribute to 1X.
4. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
5. This specification only applies if the attribute DUTY_CYCLE_CORRECTION = TRUE.

## Digital Frequency Synthesizer (DFS)

*Table 60:* **Recommended Operating Conditions for the DFS**

| Symbol | | Description | Frequency Mode | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | -5 | | -4 | | |
| | | | | Min | Max | Min | Max | |
| **Input Frequency Ranges**[2] | | | | | | | | |
| $F_{CLKIN}$ | CLKIN_FREQ_FX | Frequency for the CLKIN input | All | 1 | 280 | 1 | 280 | MHz |
| **Input Clock Jitter Tolerance**[3] | | | | | | | | |
| CLKIN_CYC_JITT_FX_LF | | Cycle-to-cycle jitter at the CLKIN input | Low | – | ±300 | – | ±300 | ps |
| CLKIN_CYC_JITT_FX_HF | | | High | – | ±150 | – | ±150 | ps |
| CLKIN_PER_JITT_FX | | Period jitter at the CLKIN input | All | – | ±1 | – | ±1 | ns |

**Notes:**

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 58.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.

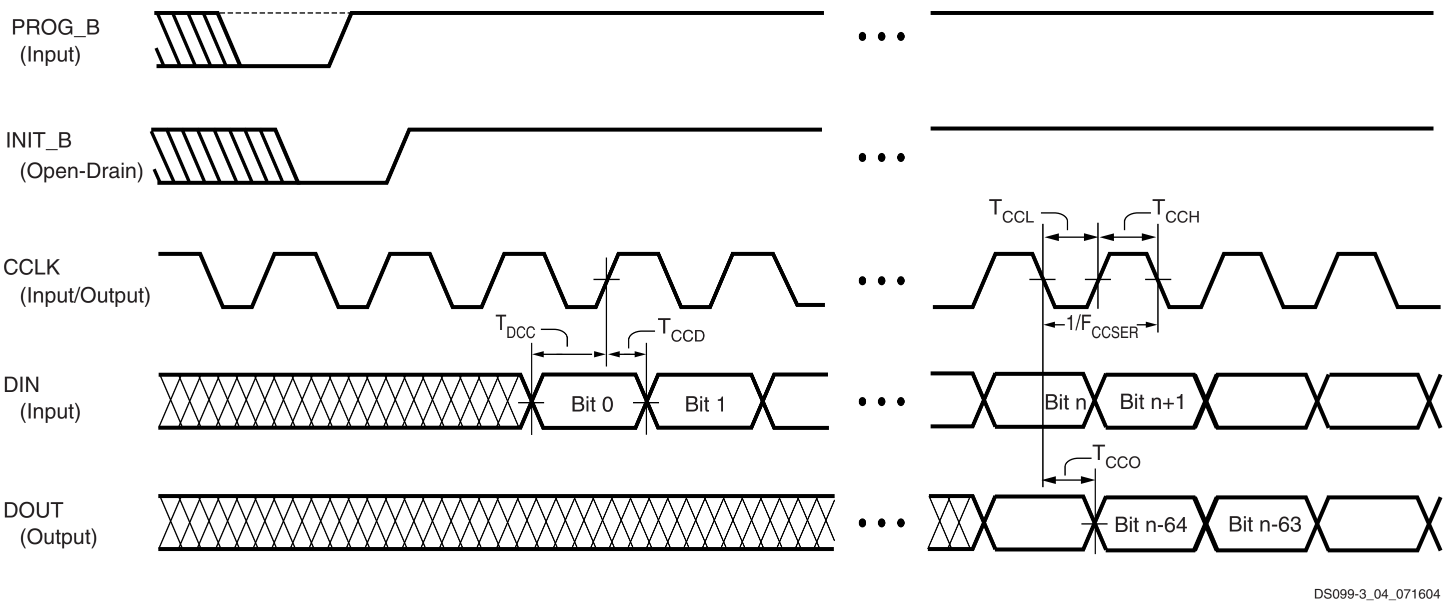


*Figure 37:* **Waveforms for Master and Slave Serial Configuration**

*Table 66:* **Timing for the Master and Slave Serial Configuration Modes**

| Symbol | Description | | Slave/ Master | All Speed Grades Min | All Speed Grades Max | Units |
|---|---|---|---|---|---|---|
| **Clock-to-Output Times** | | | | | | |
| $T_{CCO}$ | The time from the falling transition on the CCLK pin to data appearing at the DOUT pin | | Both | 1.5 | 12.0 | ns |
| **Setup Times** | | | | | | |
| $T_{DCC}$ | The time from the setup of data at the DIN pin to the rising transition at the CCLK pin | | Both | 10.0 | – | ns |
| **Hold Times** | | | | | | |
| $T_{CCD}$ | The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin | | Both | 0 | – | ns |
| **Clock Timing** | | | | | | |
| $T_{CCH}$ | CCLK input pin High pulse width | | Slave | 5.0 | ∞ | ns |
| $T_{CCL}$ | CCLK input pin Low pulse width | | | 5.0 | ∞ | ns |
| $F_{CCSER}$ | Frequency of the clock signal at the CCLK input pin | No bitstream compression | | 0 | 66(2) | MHz |
| | | With bitstream compression | | 0 | 20 | MHz |
| | | During STARTUP phase | | 0 | 50 | MHz |
| $\Delta F_{CCSER}$ | Variation from the CCLK output frequency set using the ConfigRate BitGen option | | Master | –50% | +50% | – |

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

*Table 72:* **Dual-Purpose Configuration Pins for Parallel (SelectMAP) Configuration Modes *(Cont'd)***

<table>
<tr><th>Pin Name</th><th>Direction</th><th>Description</th></tr>
<tr><td>BUSY</td><td>Output</td><td>Configuration Data Rate Control for Parallel Mode:<br>In the Slave and Master Parallel modes, BUSY throttles the rate at which configuration data is loaded. BUSY is only necessary if CCLK operates at greater than 50 MHz. Ignore BUSY for frequencies of 50 MHz and below.<br>When BUSY is Low, the FPGA accepts the next configuration data byte on the next rising CCLK edge for which CS_B and RDWR_B are Low. When BUSY is High, the FPGA ignores the next configuration data byte. The next configuration data value must be held or reloaded until the next rising CCLK edge when BUSY is Low. When CS_B is High, BUSY is in a high impedance state.
<table>
<tr><th>BUSY</th><th>Function</th></tr>
<tr><td>0</td><td>The FPGA is ready to accept the next configuration data byte.</td></tr>
<tr><td>1</td><td>The FPGA is busy processing the current configuration data byte and is not ready to accept the next byte.</td></tr>
<tr><td>Hi-Z</td><td>If CS_B is High, then BUSY is high impedance.</td></tr>
</table>
This signal is located in Bank 4 and its output voltage is determined by VCCO_4. The BitGen option Persist permits this pin to retain its configuration function in the User mode.</td></tr>
<tr><td>INIT_B</td><td>Bidirectional (open-drain)</td><td>Initializing Configuration Memory/Configuration Error (active-Low):<br>See description under Serial Configuration Modes, page 112.</td></tr>
</table>

### JTAG Configuration Mode

In the JTAG configuration mode all dual-purpose configuration pins are unused and behave exactly like user-I/O pins, as shown in Table 79. See Table 75 for Mode Select pin settings required for JTAG mode.

### Dual-Purpose Pin I/O Standard During Configuration

During configuration, the dual-purpose pins default to CMOS input and output levels for the associated VCCO voltage supply pins. For example, in the Parallel configuration modes, both VCCO_4 and VCCO_5 are required. If connected to +2.5V, then the associated pins conform to the LVCMOS25 I/O standard. If connected to +3.3V, then the pins drive LVCMOS output levels and accept either LVTTL or LVCMOS input levels.

### Dual-Purpose Pin Behavior After Configuration

After the configuration process completes, these pins, if they were borrowed during configuration, become user-I/O pins available to the application. If a dual-purpose configuration pin is not used during the configuration process—*i.e.*, the parallel configuration pins when using serial mode—then the pin behaves exactly like a general-purpose I/O. See I/O Type: Unrestricted, General-purpose I/O Pins section.

## DCI: User I/O or Digitally Controlled Impedance Resistor Reference Input

These pins are individual user-I/O pins unless one of the I/O standards used in the bank requires the Digitally Controlled Impedance (DCI) feature. If DCI is used, then 1% precision resistors connected to the VRP_# and VRN_# pins match the impedance on the input or output buffers of the I/O standards that use DCI within the bank. The '#' character in the pin name indicates the associated I/O bank and is an integer, 0 through 7.

There are two DCI pins per I/O bank, except in the CP132 and TQ144 packages, which do not have any DCI inputs for Bank 5.

### VRP and VRN Impedance Resistor Reference Inputs

The 1% precision impedance-matching resistor attached to the VRP_# pin controls the pull-up impedance of PMOS transistor in the input or output buffer. Consequently, the VRP_# pin must connect to ground. The 'P' character in "VRP" indicates that this pin controls the I/O buffer's PMOS transistor impedance. The VRP_# pin is used for both single and split termination.

*Table 87:* **VQ100 Package Pinout *(Cont'd)***

| Bank | XC3S50 XC3S200 Pin Name | VQ100 Pin Number | Type |
|---|---|---|---|
| 6 | IO_L40P_6/VREF_6 | P13 | VREF |
| 6 | VCCO_6 | P19 | VCCO |
| 7 | IO_L01N_7/VRP_7 | P2 | DCI |
| 7 | IO_L01P_7/VRN_7 | P1 | DCI |
| 7 | IO_L21N_7 | P5 | I/O |
| 7 | IO_L21P_7 | P4 | I/O |
| 7 | IO_L23N_7 | P9 | I/O |
| 7 | IO_L23P_7 | P8 | I/O |
| 7 | IO_L40N_7/VREF_7 | P12 | VREF |
| 7 | IO_L40P_7 | P11 | I/O |
| 7 | VCCO_7 | P6 | VCCO |
| N/A | GND | P3 | GND |
| N/A | GND | P10 | GND |
| N/A | GND | P20 | GND |
| N/A | GND | P29 | GND |
| N/A | GND | P41 | GND |
| N/A | GND | P56 | GND |
| N/A | GND | P66 | GND |
| N/A | GND | P73 | GND |
| N/A | GND | P82 | GND |
| N/A | GND | P95 | GND |
| N/A | VCCAUX | P7 | VCCAUX |
| N/A | VCCAUX | P33 | VCCAUX |
| N/A | VCCAUX | P58 | VCCAUX |
| N/A | VCCAUX | P84 | VCCAUX |
| N/A | VCCINT | P18 | VCCINT |
| N/A | VCCINT | P45 | VCCINT |
| N/A | VCCINT | P69 | VCCINT |
| N/A | VCCINT | P93 | VCCINT |
| VCCAUX | CCLK | P52 | CONFIG |
| VCCAUX | DONE | P51 | CONFIG |
| VCCAUX | HSWAP_EN | P98 | CONFIG |
| VCCAUX | M0 | P25 | CONFIG |
| VCCAUX | M1 | P24 | CONFIG |
| VCCAUX | M2 | P26 | CONFIG |
| VCCAUX | PROG_B | P99 | CONFIG |
| VCCAUX | TCK | P77 | JTAG |
| VCCAUX | TDI | P100 | JTAG |

*Table 91:* **TQ144 Package Pinout *(Cont'd)***

| Bank | XC3S50, XC3S200, XC3S400 Pin Name | TQ144 Pin Number | Type |
|---|---|---|---|
| 6,7 | VCCO_LEFT | P34 | VCCO |
| 6,7 | VCCO_LEFT | P3 | VCCO |
| N/A | GND | P136 | GND |
| N/A | GND | P139 | GND |
| N/A | GND | P114 | GND |
| N/A | GND | P117 | GND |
| N/A | GND | P94 | GND |
| N/A | GND | P101 | GND |
| N/A | GND | P81 | GND |
| N/A | GND | P88 | GND |
| N/A | GND | P64 | GND |
| N/A | GND | P67 | GND |
| N/A | GND | P42 | GND |
| N/A | GND | P45 | GND |
| N/A | GND | P22 | GND |
| N/A | GND | P29 | GND |
| N/A | GND | P9 | GND |
| N/A | GND | P16 | GND |
| N/A | VCCAUX | P134 | VCCAUX |
| N/A | VCCAUX | P120 | VCCAUX |
| N/A | VCCAUX | P62 | VCCAUX |
| N/A | VCCAUX | P48 | VCCAUX |
| N/A | VCCINT | P133 | VCCINT |
| N/A | VCCINT | P121 | VCCINT |
| N/A | VCCINT | P61 | VCCINT |
| N/A | VCCINT | P49 | VCCINT |
| VCCAUX | CCLK | P72 | CONFIG |
| VCCAUX | DONE | P71 | CONFIG |
| VCCAUX | HSWAP_EN | P142 | CONFIG |
| VCCAUX | M0 | P38 | CONFIG |
| VCCAUX | M1 | P37 | CONFIG |
| VCCAUX | M2 | P39 | CONFIG |
| VCCAUX | PROG_B | P143 | CONFIG |
| VCCAUX | TCK | P110 | JTAG |
| VCCAUX | TDI | P144 | JTAG |
| VCCAUX | TDO | P109 | JTAG |
| VCCAUX | TMS | P111 | JTAG |

## FG320 Footprint

Bank 0 (top, columns 2–9) · Bank 1 (top, columns 9–17) · Bank 7 (left, rows A–J) · Bank 6 (left, rows K–V) · Bank 2 (right, rows A–J) · Bank 3 (right, rows K–V) · Bank 5 (bottom, columns 2–9) · Bank 4 (bottom, columns 9–17)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | I/O L01N_0 VRP_0 | I/O L01P_0 VRN_0 | I/O L15N_0 | I/O L15P_0 | GND | I/O L30N_0 | I/O L30P_0 | I/O L31P_0 VREF_0 | I/O L31N_1 VREF_1 | I/O | I/O VREF_1 | GND | I/O L16N_1 | I/O L10N_1 VREF_1 | I/O L01N_1 VRP_1 | I/O L01P_1 VRN_1 | GND |
| B | I/O L16P_7 VREF_7 | GND | I/O VREF_0 | I/O L09N_0 | I/O L25N_0 | I/O L25P_0 | VCCAUX | VCCO_0 | I/O L31N_0 | I/O L31P_1 | VCCO_1 | VCCAUX | I/O | I/O L16P_1 | I/O L10P_1 | TMS | GND | I/O L16N_2 |
| C | I/O L16N_7 | I/O L01P_7 VRN_7 | I/O L01N_7 VRP_7 | I/O L09P_0 | I/O L10N_0 | VCCO_0 | I/O L27N_0 | I/O L28N_0 | GND | GND | I/O L30N_1 | I/O L28N_1 | VCCO_1 | I/O L15N_1 | I/O L15P_1 | I/O L01N_2 VRP_2 | I/O L01P_2 VRN_2 | I/O L16P_2 |
| D | I/O L17N_7 | I/O L17P_7 | I/O L19P_7 | TDI | I/O L10P_0 | I/O VREF_0 | I/O L27P_0 | I/O L28P_0 | I/O | I/O | I/O L30P_1 | I/O L28P_1 | I/O L24P_1 | I/O L24N_1 | TDO | I/O L19N_2 | I/O L17N_2 | I/O L17P_2 VREF_2 |
| E | I/O L20P_7 | I/O L20N_7 | I/O L19N_7 VREF_7 | I/O L21N_7 | PROG_B | HSWAP_EN | I/O | I/O L29N_0 | I/O L32N_0 GCLK7 | I/O L32N_1 GCLK5 | I/O L29P_1 | I/O L27P_1 | I/O L27N_1 | TCK | I/O L21P_2 | I/O L19P_2 | I/O L20N_2 | I/O L20P_2 |
| F | GND | I/O L23P_7 | VCCO_7 | I/O L21P_7 | I/O L22P_7 | VCCINT | VCCINT | I/O L29P_0 | I/O L32P_0 GCLK6 | I/O L32P_1 GCLK4 | I/O L29N_1 | VCCINT | VCCINT | I/O L22N_2 | I/O L21N_2 | VCCO_2 | I/O L23P_2 | GND |
| G | I/O L23N_7 | VCCAUX | I/O L24P_7 | I/O L24N_7 | I/O L22N_7 | VCCINT | GND | VCCO_0 | VCCO_0 | VCCO_1 | VCCO_1 | GND | VCCINT | I/O L22P_2 | I/O L24N_2 | I/O L24P_2 | VCCAUX | I/O L23N_2 VREF_2 |
| H | I/O L35N_7 | I/O L35P_7 | I/O L34P_7 | I/O L34N_7 | I/O L27N_7 | I/O L27P_7 VREF_7 | VCCO_7 | GND | GND | GND | GND | VCCO_2 | I/O L27N_2 | I/O L27P_2 | I/O L34P_2 | I/O L34N_2 VREF_2 | I/O L35N_2 | I/O L35P_2 |
| J | I/O L39N_7 | I/O L39P_7 | GND | I/O L40P_7 | I/O L40N_7 VREF_7 | I/O | VCCO_7 | GND | X | X | GND | VCCO_2 | I/O | I/O L40P_2 VREF_2 | I/O L40N_2 | GND | I/O L39P_2 | I/O L39N_2 |
| K | I/O L40N_6 | I/O L40P_6 VREF_6 | GND | I/O L39P_6 | I/O L39N_6 | I/O | VCCO_6 | GND | X | X | GND | VCCO_3 | I/O L39N_3 | I/O L39P_3 | I/O | GND | I/O L40N_3 VREF_3 | I/O L40P_3 |
| L | I/O L35P_6 | I/O L35N_6 | I/O L34N_6 VREF_6 | I/O L34P_6 | I/O L27P_6 | I/O L27N_6 | VCCO_6 | GND | GND | GND | GND | VCCO_3 | I/O L27P_3 | I/O L27N_3 | I/O L34N_3 | I/O L34P_3 VREF_3 | I/O L35P_3 | I/O L35N_3 |
| M | I/O L24P_6 | VCCAUX | I/O L23N_6 | I/O L23P_6 | I/O L22P_6 | VCCINT | GND | VCCO_5 | VCCO_5 | VCCO_4 | VCCO_4 | GND | VCCINT | I/O L22N_3 | I/O L23N_3 | I/O L23P_3 VREF_3 | VCCAUX | I/O L24N_3 |
| N | GND | I/O L24N_6 VREF_6 | VCCO_6 | I/O L21N_6 | I/O L22N_6 | VCCINT | VCCINT | I/O | I/O L32N_5 GCLK3 | I/O L32N_4 GCLK1 | I/O L30N_4 D2 | VCCINT | VCCINT | I/O L22P_3 | I/O L21P_3 | VCCO_3 | I/O L24P_3 | GND |
| P | I/O L20P_6 | I/O L20N_6 | I/O L19P_6 | I/O L21P_6 | M0 | I/O L27N_5 VREF_5 | I/O L27P_5 | I/O | I/O L32P_5 GCLK2 | I/O L32P_4 GCLK0 | I/O L30P_4 D3 | I/O | I/O L25P_4 | I/O L06N_4 VREF_4 | I/O L21N_3 | I/O L17N_3 | I/O L20P_3 | I/O L20N_3 |
| R | I/O L17P_6 VREF_6 | I/O L17N_6 | I/O L19N_6 | M2 | I/O L15P_5 | I/O L15N_5 | I/O L28N_5 D6 | I/O L30N_5 | I/O VREF_5 | I/O VREF_4 | I/O L29N_4 | I/O L27P_4 D1 | I/O L25N_4 | I/O L06P_4 | DONE | I/O L17P_3 VREF_3 | I/O L19N_3 | I/O L19P_3 |
| T | I/O L16P_6 | I/O L01P_6 VRN_6 | I/O L01N_6 VRP_6 | I/O L06P_5 | I/O L06N_5 | VCCO_5 | I/O L28P_5 D7 | I/O L30P_5 | GND | GND | I/O L29P_4 | I/O L27N_4 DIN D0 | VCCO_4 | I/O L10N_4 | CCLK | I/O L01P_3 VRN_3 | I/O L01N_3 VRP_3 | I/O L16N_3 |
| U | I/O L16N_6 | GND | M1 | I/O L10P_5 VRN_5 | I/O L16P_5 | I/O | VCCAUX | VCCO_5 | I/O L31N_5 D4 | I/O L31N_4 INIT_B | VCCO_4 | VCCAUX | I/O VREF_4 | I/O L10P_4 | I/O L09N_4 | I/O L01N_4 VRP_4 | GND | I/O L16P_3 |
| V | GND | I/O L01P_5 CS_B | I/O L01N_5 RDWR_B | I/O L10N_5 VRP_5 | I/O L16N_5 | GND | I/O L29P_5 VREF_5 | I/O L29N_5 | I/O L31P_5 D5 | I/O L31P_4 DOUT BUSY | I/O L28P_4 | I/O L28N_4 | GND | I/O | I/O L09P_4 | I/O L01P_4 VRN_4 | I/O VREF_4 | GND |

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*Figure 50:* **FG320 Package Footprint (Top View)**

| | | | | | |
|---|---|---|---|---|---|
| 156 | **I/O:** Unrestricted, general-purpose user I/O | 12 | **DUAL:** Configuration pin, then possible user I/O | 29 | **VREF:** User I/O or input voltage reference for bank |
| 16 | **DCI:** User I/O or reference resistor input for bank | 8 | **GCLK:** User I/O or global clock buffer input | 28 | **VCCO:** Output voltage supply for bank |
| 7 | **CONFIG:** Dedicated configuration pins | 4 | **JTAG:** Dedicated JTAG port pins | 12 | **VCCINT:** Internal core voltage supply (+1.2V) |
| 0 | **N.C.:** No unconnected pins in this package | 40 | **GND:** Ground | 8 | **VCCAUX:** Auxiliary voltage supply (+2.5V) |

## FG456: 456-lead Fine-pitch Ball Grid Array

The 456-lead fine-pitch ball grid array package, FG456, supports four different Spartan-3 devices, including the XC3S400, the XC3S1000, the XC3S1500, and the XC3S2000. The footprints for the XC3S1000, the XC3S1500, and the XC3S2000 are identical, as shown in Table 100 and Figure 51. The XC3S400, however, has fewer I/O pins which consequently results in 69 unconnected pins on the FG456 package, labeled as "N.C." In Table 100 and Figure 51, these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in Table 100 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S400 pinout and the pinout for the XC3S1000, the XC3S1500, or the XC3S2000, then that difference is highlighted in Table 100. If the table entry is shaded grey, then there is an unconnected pin on the XC3S400 that maps to a user-I/O pin on the XC3S1000, XC3S1500, and XC3S2000. If the table entry is shaded tan, then the unconnected pin on the XC3S400 maps to a VREF-type pin on the XC3S1000, the XC3S1500, or the XC3S2000. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S400 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S400 device to an XC3S1000, an XC3S1500, or an XC3S2000 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

### Pinout Table

*Table 100:* **FG456 Package Pinout**

| Bank | 3S400 Pin Name | 3S1000, 3S1500, 3S2000 Pin Name | FG456 Pin Number | Type |
|---|---|---|---|---|
| 0 | IO | IO | A10 | I/O |
| 0 | IO | IO | D9 | I/O |
| 0 | IO | IO | D10 | I/O |
| 0 | IO | IO | F6 | I/O |
| 0 | IO/VREF_0 | IO/VREF_0 | A3 | VREF |
| 0 | IO/VREF_0 | IO/VREF_0 | C7 | VREF |
| 0 | N.C. (◆) | IO/VREF_0 | E5 | VREF |
| 0 | IO/VREF_0 | IO/VREF_0 | F7 | VREF |
| 0 | IO_L01N_0/VRP_0 | IO_L01N_0/VRP_0 | B4 | DCI |
| 0 | IO_L01P_0/VRN_0 | IO_L01P_0/VRN_0 | A4 | DCI |
| 0 | IO_L06N_0 | IO_L06N_0 | D5 | I/O |
| 0 | IO_L06P_0 | IO_L06P_0 | C5 | I/O |
| 0 | IO_L09N_0 | IO_L09N_0 | B5 | I/O |
| 0 | IO_L09P_0 | IO_L09P_0 | A5 | I/O |
| 0 | IO_L10N_0 | IO_L10N_0 | E6 | I/O |
| 0 | IO_L10P_0 | IO_L10P_0 | D6 | I/O |
| 0 | IO_L15N_0 | IO_L15N_0 | C6 | I/O |
| 0 | IO_L15P_0 | IO_L15P_0 | B6 | I/O |
| 0 | IO_L16N_0 | IO_L16N_0 | E7 | I/O |
| 0 | IO_L16P_0 | IO_L16P_0 | D7 | I/O |
| 0 | N.C. (◆) | IO_L19N_0 | B7 | I/O |
| 0 | N.C. (◆) | IO_L19P_0 | A7 | I/O |

*Table 100:* **FG456 Package Pinout *(Cont'd)***

| Bank | 3S400 Pin Name | 3S1000, 3S1500, 3S2000 Pin Name | FG456 Pin Number | Type |
|---|---|---|---|---|
| N/A | GND | GND | P13 | GND |
| N/A | GND | GND | P14 | GND |
| N/A | GND | GND | P20 | GND |
| N/A | GND | GND | Y9 | GND |
| N/A | GND | GND | Y14 | GND |
| N/A | VCCAUX | VCCAUX | A6 | VCCAUX |
| N/A | VCCAUX | VCCAUX | A17 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AB6 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AB17 | VCCAUX |
| N/A | VCCAUX | VCCAUX | F1 | VCCAUX |
| N/A | VCCAUX | VCCAUX | F22 | VCCAUX |
| N/A | VCCAUX | VCCAUX | U1 | VCCAUX |
| N/A | VCCAUX | VCCAUX | U22 | VCCAUX |
| N/A | VCCINT | VCCINT | G7 | VCCINT |
| N/A | VCCINT | VCCINT | G8 | VCCINT |
| N/A | VCCINT | VCCINT | G15 | VCCINT |
| N/A | VCCINT | VCCINT | G16 | VCCINT |
| N/A | VCCINT | VCCINT | H7 | VCCINT |
| N/A | VCCINT | VCCINT | H16 | VCCINT |
| N/A | VCCINT | VCCINT | R7 | VCCINT |
| N/A | VCCINT | VCCINT | R16 | VCCINT |
| N/A | VCCINT | VCCINT | T7 | VCCINT |
| N/A | VCCINT | VCCINT | T8 | VCCINT |
| N/A | VCCINT | VCCINT | T15 | VCCINT |
| N/A | VCCINT | VCCINT | T16 | VCCINT |
| VCCAUX | CCLK | CCLK | AA22 | CONFIG |
| VCCAUX | DONE | DONE | AB21 | CONFIG |
| VCCAUX | HSWAP_EN | HSWAP_EN | B3 | CONFIG |
| VCCAUX | M0 | M0 | AB2 | CONFIG |
| VCCAUX | M1 | M1 | AA1 | CONFIG |
| VCCAUX | M2 | M2 | AB3 | CONFIG |
| VCCAUX | PROG_B | PROG_B | A2 | CONFIG |
| VCCAUX | TCK | TCK | A21 | JTAG |
| VCCAUX | TDI | TDI | B1 | JTAG |
| VCCAUX | TDO | TDO | B22 | JTAG |
| VCCAUX | TMS | TMS | A20 | JTAG |

*Table 107:* **FG900 Package Pinout *(Cont'd)***

| Bank | XC3S2000 Pin Name | XC3S4000, XC3S5000 Pin Name | FG900 Pin Number | Type |
|---|---|---|---|---|
| N/A | GND | GND | R17 | GND |
| N/A | GND | GND | T17 | GND |
| N/A | GND | GND | U17 | GND |
| N/A | GND | GND | V17 | GND |
| N/A | GND | GND | AC17 | GND |
| N/A | GND | GND | AF17 | GND |
| N/A | GND | GND | AK17 | GND |
| N/A | GND | GND | N18 | GND |
| N/A | GND | GND | P18 | GND |
| N/A | GND | GND | R18 | GND |
| N/A | GND | GND | T18 | GND |
| N/A | GND | GND | U18 | GND |
| N/A | GND | GND | V18 | GND |
| N/A | GND | GND | R19 | GND |
| N/A | GND | GND | T19 | GND |
| N/A | GND | GND | A21 | GND |
| N/A | GND | GND | E21 | GND |
| N/A | GND | GND | H21 | GND |
| N/A | GND | GND | AC21 | GND |
| N/A | GND | GND | AF21 | GND |
| N/A | GND | GND | AK21 | GND |
| N/A | GND | GND | K23 | GND |
| N/A | GND | GND | P23 | GND |
| N/A | GND | GND | U23 | GND |
| N/A | GND | GND | AA23 | GND |
| N/A | GND | GND | A25 | GND |
| N/A | GND | GND | AK25 | GND |
| N/A | GND | GND | E26 | GND |
| N/A | GND | GND | K26 | GND |
| N/A | GND | GND | P26 | GND |
| N/A | GND | GND | U26 | GND |
| N/A | GND | GND | AA26 | GND |
| N/A | GND | GND | AF26 | GND |
| N/A | GND | GND | A29 | GND |
| N/A | GND | GND | B29 | GND |
| N/A | GND | GND | AJ29 | GND |
| N/A | GND | GND | AK29 | GND |
| N/A | GND | GND | A30 | GND |
| N/A | GND | GND | B30 | GND |
| N/A | GND | GND | F30 | GND |

## FG900 Footprint

### *Left Half of FG900 Package (Top View)*

**XC3S2000 (565 max. user I/O)**

- 481 — **I/O:** Unrestricted, general-purpose user I/O
- 48 — **VREF:** User I/O or input voltage reference for bank
- 68 — **N.C.:** Unconnected pins for XC3S2000 (◆)

**XC3S4000, XC3S5000 (633 max user I/O)**

- 549 — **I/O:** Unrestricted, general-purpose user I/O
- 48 — **VREF:** User I/O or input voltage reference for bank
- 0 — **N.C.:** No unconnected pins in this package

**All devices**

- 12 — **DUAL:** Configuration pin, then possible user I/O
- 8 — **GCLK:** User I/O or global clock buffer input
- 16 — **DCI:** User I/O or reference resistor input for bank
- 7 — **CONFIG:** Dedicated configuration pins
- 4 — **JTAG:** Dedicated JTAG port pins
- 32 — **VCCINT:** Internal core voltage supply (+1.2V)
- 80 — **VCCO:** Output voltage supply for bank
- 24 — **VCCAUX:** Auxiliary voltage supply (+2.5V)
- 120 — **GND:** Ground

Bank 0 (top, columns 4–15); Bank 7 (left, rows C–R); Bank 6 (left, rows T–AH); Bank 5 (bottom, columns 4–15)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | GND | HSWAP_EN | I/O L01P_0 VRN_0 | I/O L02P_0 | GND | I/O L35P_0 ◆ | I/O L09P_0 | I/O L38P_0 ◆ | GND | I/O L17P_0 | I/O L22P_0 | I/O L25P_0 | GND | I/O L32P_0 GCLK6 |
| B | GND | GND | PROG_B | I/O L01N_0 VRP_0 | I/O L02N_0 | I/O L04P_0 | I/O L35N_0 ◆ | I/O L09N_0 | I/O L38N_0 ◆ | I/O L12P_0 | I/O L17N_0 | I/O L22N_0 | I/O L25N_0 | I/O L28P_0 | I/O L32N_0 GCLK7 |
| C | I/O L01N_7 VRP_7 | I/O L01P_7 VRN_7 | TDI | IO VREF_0 | VCCO_0 | I/O L04N_0 | I/O L06P_0 | I/O L08P_0 | VCCO_0 | I/O L12N_0 | I/O L16P_0 | I/O L21P_0 | VCCO_0 | I/O L28N_0 | I/O L31P_0 VREF_0 |
| D | I/O L03N_7 VREF_7 | I/O L03P_7 | I/O L02N_7 | I/O L02P_7 | I/O L03N_0 | VCCAUX | I/O L06N_0 | I/O L08N_0 | I/O L37P_0 ◆ | VCCAUX | I/O L16N_0 | I/O L21N_0 | I/O | VCCAUX | I/O L31N_0 |
| E | I/O L04N_7 | I/O L04P_7 | VCCO_7 | I/O L05P_7 | GND | I/O L03P_0 | VCCO_0 | I/O L07P_0 | I/O L37N_0 ◆ | GND | I/O L15P_0 | I/O L20P_0 | I/O L24P_0 | GND | I/O |
| F | GND | I/O L06N_7 | I/O L06P_7 | VCCAUX | I/O L05N_7 | I/O L05N_0 | I/O L05P_0 VREF_0 | I/O L07N_0 | IO VREF_0 | I/O L11P_0 | I/O L15N_0 | I/O L20N_0 | I/O L24N_0 | I/O L27P_0 | I/O L30P_0 |
| G | I/O L08N_7 | I/O L08P_7 | I/O L07N_7 | I/O L07P_7 | VCCO_7 | I/O L09P_7 | I/O L36N_0 ◆ | I/O | VCCO_0 | I/O L11N_0 | I/O L14P_0 | I/O L19P_0 | VCCO_0 | I/O L27N_0 | I/O L30N_0 |
| H | I/O L13N_7 | I/O L13P_7 | I/O L11N_7 | I/O L11P_7 | I/O L10N_7 | I/O L10P_7 VREF_7 | I/O L09N_7 | I/O L36P_0 ◆ | I/O L10P_0 | GND | I/O L14N_0 | I/O L19N_0 | I/O L23P_0 | GND | I/O L29P_0 |
| J | I/O L15N_7 | I/O L15P_7 | VCCO_7 | I/O L14N_7 | I/O L14P_7 | I/O | VCCO_7 | I/O L16P_7 VREF_7 | I/O L10N_0 | I/O L13N_0 | VCCO_0 | I/O L18P_0 | I/O L23N_0 | I/O L26P_0 VREF_0 | I/O L29N_0 |
| K | GND | I/O L19N_7 VREF_7 | I/O L19P_7 | VCCAUX | GND | I/O L17N_7 | I/O L17P_7 | GND | I/O L16N_7 | I/O L20P_7 | I/O L13P_0 | I/O L18N_0 | I/O | I/O L26N_0 | I/O |
| L | I/O L24N_7 | I/O L24P_7 | I/O L23N_7 | I/O L23P_7 | I/O L22N_7 | I/O L22P_7 | I/O L21N_7 | I/O L21P_7 | VCCO_7 | I/O L20N_7 | VCCINT | VCCO_0 | VCCO_0 | VCCO_0 | VCCINT |
| M | I/O L27N_7 | I/O L27P_7 VREF_7 | I/O L26N_7 | I/O L26P_7 | I/O L49P_7 ◆ | I/O L25N_7 ◆ | I/O L25P_7 ◆ | I/O L46N_7 ◆ | I/O L46P_7 ◆ | I/O L28P_7 | VCCO_7 | VCCINT | VCCINT | VCCINT | GND |
| N | I/O L31N_7 | I/O L31P_7 | VCCO_7 | I/O L50N_7 ◆ | I/O L50P_7 ◆ | I/O L49N_7 ◆ | VCCO_7 | I/O L29N_7 | I/O L29P_7 | I/O L28N_7 | VCCO_7 | VCCINT | GND | GND | GND |
| P | GND | I/O L34N_7 | I/O L34P_7 | VCCAUX | GND | I/O L33N_7 | I/O L33P_7 | GND | I/O L32N_7 | I/O L32P_7 | VCCO_7 | VCCINT | GND | GND | GND |
| R | I/O L40N_7 VREF_7 | I/O L40P_7 | I/O L39N_7 | I/O L39P_7 | I/O L38N_7 | I/O L38P_7 | I/O L37N_7 | I/O L37P_7 VREF_7 | I/O L35N_7 | I/O L35P_7 | VCCINT | GND | GND | GND | GND |
| T | I/O L40P_6 VREF_6 | I/O L40N_6 | I/O L39P_6 | I/O L39N_6 | I/O L38P_6 | I/O L38N_6 | I/O L52P_6 ◆ | I/O L52N_6 ◆ | I/O L37P_6 | I/O L37N_6 | VCCINT | GND | GND | GND | GND |
| U | GND | I/O L36P_6 ◆ | I/O L36N_6 ◆ | VCCAUX | GND | I/O L35P_6 | I/O L35N_6 | GND | I/O L34P_6 | I/O L34N_6 VREF_6 | VCCO_6 | VCCINT | GND | GND | GND |
| V | I/O L33P_6 | I/O L33N_6 | VCCO_6 | I/O L32P_6 | I/O L32N_6 | I/O L31P_6 | VCCO_6 | I/O L30P_6 ◆ | I/O L30N_6 ◆ | I/O L29P_6 | VCCO_6 | VCCINT | GND | GND | GND |
| W | I/O L28P_6 | I/O L28N_6 | I/O L27P_6 | I/O L27N_6 | I/O L31N_6 | I/O L26P_6 | I/O L26N_6 | I/O L25P_6 ◆ | I/O L25N_6 ◆ | I/O L29N_6 | VCCO_6 | VCCINT | VCCINT | VCCINT | GND |
| Y | I/O L24P_6 | I/O L24N_6 VREF_6 | I/O L45P_6 ◆ | I/O L45N_6 ◆ | I/O L22P_6 | I/O L22N_6 | I/O L21P_6 | I/O L21N_6 | VCCO_6 | I/O L20P_6 | VCCINT | VCCO_5 | VCCO_5 | VCCO_5 | VCCINT |
| AA | GND | I/O L19P_6 | I/O L19N_6 | VCCAUX | GND | I/O L17P_6 VREF_6 | I/O L17N_6 | GND | I/O L16P_6 | I/O L20N_6 | I/O | I/O L22P_5 | I/O L22N_5 | I/O L26P_5 | I/O |
| AB | I/O L15P_6 | I/O L15N_6 | VCCO_6 | I/O L14P_6 | I/O L14N_6 | I/O | VCCO_6 | I/O L16N_6 | I/O L08P_5 | I/O | VCCO_5 | I/O L17N_5 | I/O L23P_5 | I/O L26N_5 | I/O L29P_5 VREF_5 |
| AC | I/O L13P_6 VREF_6 | I/O L13N_6 | I/O L11P_6 | I/O L11N_6 | I/O L10P_6 | I/O L10N_6 | I/O L09P_6 | I/O L36P_5 ◆ | I/O L08N_5 | GND | I/O L17P_5 | I/O L18P_5 | I/O L23N_5 | GND | I/O L29N_5 |
| AD | I/O L08P_6 | I/O L08N_6 | I/O L07P_6 | I/O L07N_6 | VCCO_6 | I/O L09N_6 VREF_6 | I/O L05P_5 | I/O L36N_5 ◆ | VCCO_5 | I/O L13P_5 | I/O L13N_5 | I/O L18N_5 | VCCO_5 | I/O L30P_5 | I/O L30N_5 |
| AE | GND | I/O L06P_6 | I/O L06N_6 | VCCAUX | I/O L05P_6 | I/O | I/O L05N_5 | I/O L37P_5 ◆ | I/O L11P_5 | I/O L11N_5 VREF_5 | I/O L14P_5 | I/O L19P_5 VREF_5 | I/O L27P_5 | I/O L27N_5 VREF_5 | I/O |
| AF | I/O L04P_6 | I/O L04N_6 | VCCO_6 | I/O L05N_6 | GND | I/O L03N_5 | VCCO_5 | I/O L37N_5 ◆ | I/O L09P_5 | GND | I/O L14N_5 | I/O L19N_5 | I/O L24P_5 | GND | I/O L31P_5 D5 |
| AG | I/O L03P_6 | I/O L03N_6 VREF_6 | I/O L02P_6 | I/O L02N_6 | I/O L03P_5 | VCCAUX | I/O L06P_5 | I/O L38P_5 ◆ | I/O L09N_5 | VCCAUX | I/O L15P_5 | I/O L20P_5 | I/O L24N_5 | VCCAUX | I/O L31N_5 D4 |
| AH | I/O L01P_6 VRN_6 | I/O L01N_6 VRP_6 | M1 | IO VREF_5 | VCCO_5 | I/O L04P_5 | I/O L06N_5 | I/O L38N_5 ◆ | VCCO_5 | I/O L12P_5 | I/O L15N_5 | I/O L20N_5 | VCCO_5 | I/O L28P_5 D7 | I/O L32P_5 GCLK2 |
| AJ | GND | GND | M0 | I/O L01P_5 CS_B | I/O L02P_5 | I/O L04N_5 | I/O L35P_5 ◆ | I/O L07P_5 | I/O L10P_5 VRN_5 | I/O L12N_5 | I/O L16P_5 | I/O L21P_5 | I/O L25P_5 | I/O L28N_5 D6 | I/O L32N_5 GCLK3 |
| AK | GND | GND | M2 | I/O L01N_5 RDWR_B | I/O L02N_5 | GND | I/O L35N_5 ◆ | I/O L07N_5 | I/O L10N_5 VRP_5 | GND | I/O L16N_5 | I/O L21N_5 | I/O L25N_5 | GND | IO VREF_5 |

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*Figure 55:* **FG900 Package Footprint (Top View)**

***Right Half of FG900 Package (Top View)***

Bank 1 (top), Bank 2 (right, rows A–R), Bank 3 (right, rows T–AK), Bank 4 (bottom)

| | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | I/O | GND | I/O L39N_1 ◆ | I/O L26N_1 | I/O L21N_1 | GND | I/O L15N_1 | I/O L11N_1 | I/O L07N_1 | GND | I/O L03N_1 | I/O L01N_1 VRP_1 | TMS | GND | GND |
| B | I/O L32N_1 GCLK5 | I/O L28N_1 | I/O L39P_1 ◆ | I/O L26P_1 | I/O L21P_1 | I/O L17N_1 VREF_1 | I/O L15P_1 | I/O L11P_1 | I/O L07P_1 | I/O L04N_1 | I/O L03P_1 | I/O L01P_1 VRN_1 | TCK | GND | GND |
| C | I/O L32P_1 GCLK4 | I/O L28P_1 | VCCO_1 | I/O L25N_1 | I/O L20N_1 | I/O L17P_1 | VCCO_1 | I/O L10N_1 VREF_1 | I/O L06N_1 VREF_1 | I/O L04P_1 | VCCO_1 | I/O L02P_1 | TDO | I/O L01N_2 VRP_2 | I/O L01P_2 VRN_2 |
| D | I/O L31N_1 VREF_1 | VCCAUX | I/O L38N_1 ◆ | I/O L25P_1 | I/O L20P_1 | VCCAUX | I/O L14N_1 | I/O L10P_1 | I/O L06P_1 | VCCAUX | I/O L02N_1 | I/O L02N_2 | I/O L02P_2 | I/O L03N_2 VREF_2 | I/O L03P_2 |
| E | I/O L31P_1 | GND | I/O L38P_1 ◆ | I/O L24N_1 | I/O L19N_1 | GND | I/O L14P_1 | I/O L13P_1 | VCCO_1 | I/O | GND | I/O L41N_2 ◆ | VCCO_2 | I/O L04N_2 | I/O L04P_2 |
| F | I/O | I/O L27N_1 | I/O | I/O L24P_1 | I/O L19P_1 | I/O L16N_1 | I/O L13N_1 | I/O L09N_1 | I/O L05N_1 | I/O L05P_1 | I/O L41P_2 ◆ | VCCAUX | I/O L05N_2 | I/O L05P_2 | GND |
| G | I/O L30N_1 | I/O L27P_1 | VCCO_1 | I/O L23N_1 | I/O L18N_1 | I/O L16P_1 | VCCO_1 | I/O L09P_1 | I/O L08P_1 | I/O L08N_2 | VCCO_2 | I/O L06N_2 | I/O L06P_2 | I/O L07N_2 | I/O L07P_2 |
| H | I/O L30P_1 | GND | I/O L37N_1 ◆ | I/O L23P_1 | I/O L18P_1 | GND | I/O L12N_1 | I/O L08N_1 | I/O L08P_2 | I/O L09N_2 VREF_2 | I/O L09P_2 | I/O L10N_2 | I/O L10P_2 | I/O L12N_2 | I/O L12P_2 |
| J | I/O L29N_1 | IO VREF_1 | I/O L37P_1 ◆ | I/O L22N_1 | VCCO_1 | I/O | I/O L12P_1 | I/O L15N_2 | VCCO_2 | I/O | I/O L13N_2 | I/O L13P_2 VREF_2 | VCCO_2 | I/O L14N_2 | I/O L14P_2 |
| K | I/O L29P_1 | I/O L40N_1 ◆ | I/O L40P_1 ◆ | I/O L22P_1 | I/O | I/O L46N_2 ◆ | I/O L15P_2 | GND | I/O L16N_2 | I/O L16P_2 | GND | VCCAUX | I/O L45N_2 ◆ | I/O L45P_2 ◆ | GND |
| L | VCCINT | VCCO_1 | VCCO_1 | VCCO_1 | VCCINT | I/O L46P_2 ◆ | VCCO_2 | I/O L47N_2 ◆ | I/O L47P_2 ◆ | I/O L19N_2 | I/O L19P_2 | I/O L20N_2 | I/O L20P_2 | I/O L21N_2 | I/O L21P_2 |
| M | GND | VCCINT | VCCINT | VCCINT | VCCO_2 | I/O L26N_2 | I/O L22N_2 | I/O L22P_2 | I/O L23N_2 VREF_2 | I/O L23P_2 | I/O L28N_2 | I/O L24N_2 | I/O L24P_2 | I/O L50N_2 ◆ | I/O L50P_2 ◆ |
| N | GND | GND | GND | VCCINT | VCCO_2 | I/O L26P_2 | I/O L27N_2 | I/O L27P_2 | VCCO_2 | I/O L28P_2 | I/O L29N_2 | I/O L29P_2 | VCCO_2 | I/O L31N_2 | I/O L31P_2 |
| P | GND | GND | GND | VCCINT | VCCO_2 | I/O L32N_2 | I/O L32P_2 | GND | I/O L33N_2 | I/O L33P_2 | GND | VCCAUX | I/O L34N_2 VREF_2 | I/O L34P_2 | GND |
| R | GND | GND | GND | GND | VCCINT | I/O L35N_2 | I/O L35P_2 | I/O L37N_2 | I/O L37P_2 | I/O L38N_2 | I/O L38P_2 | I/O L39N_2 | I/O L39P_2 | I/O L40N_2 | I/O L40P_2 VREF_2 |
| T | GND | GND | GND | GND | VCCINT | I/O L35P_3 | I/O L35N_3 | I/O L37P_3 | I/O L37N_3 | I/O L38P_3 | I/O L38N_3 | I/O L39P_3 | I/O L39N_3 | I/O L40P_3 | I/O L40N_3 VREF_3 |
| U | GND | GND | GND | VCCINT | VCCO_3 | I/O L32P_3 | I/O L32N_3 | GND | I/O L33P_3 | I/O L33N_3 | GND | VCCAUX | I/O L34P_3 VREF_3 | I/O L34N_3 | GND |
| V | GND | GND | GND | VCCINT | VCCO_3 | I/O L27N_3 | I/O L28P_3 | I/O L28N_3 | VCCO_3 | I/O L29N_3 | I/O L50P_3 ◆ | I/O L50N_3 ◆ | VCCO_3 | I/O L31P_3 | I/O L31N_3 |
| W | GND | VCCINT | VCCINT | VCCINT | VCCO_3 | I/O L27P_3 | I/O L46P_3 ◆ | I/O L46N_3 ◆ | I/O L47P_3 ◆ | I/O L47N_3 ◆ | I/O L29P_3 | I/O L48P_3 ◆ | I/O L48N_3 ◆ | I/O L26P_3 | I/O L26N_3 |
| Y | VCCINT | VCCO_4 | VCCO_4 | VCCO_4 | VCCINT | I/O L20N_3 | VCCO_3 | I/O L21P_3 | I/O L21N_3 | I/O L22P_3 | I/O L22N_3 | I/O L23P_3 VREF_3 | I/O L23N_3 | I/O L24P_3 | I/O L24N_3 |
| AA | I/O | I/O L26N_4 | I/O | I/O L18N_4 | I/O L13P_4 | I/O L20P_3 | I/O L16N_3 | GND | I/O L17P_3 VREF_3 | I/O L17N_3 | GND | VCCAUX | I/O L19P_3 | I/O L19N_3 | GND |
| AB | I/O L29N_4 | I/O L26P_4 VREF_4 | I/O L23N_4 | I/O L18P_4 | VCCO_4 | I/O L13N_4 | I/O L08N_4 | I/O L16P_3 | VCCO_3 | I/O | I/O L14P_3 | I/O L14N_3 | VCCO_3 | I/O L15P_3 | I/O L15N_3 |
| AC | I/O L29P_4 | GND | I/O L23P_4 | I/O L19N_4 | I/O L14N_4 | GND | I/O L08P_4 | I/O L04P_4 | I/O L09N_3 | I/O L10P_3 | I/O L10N_3 | I/O L11P_3 | I/O L11N_3 | I/O L13P_3 | I/O L13N_3 VREF_3 |
| AD | I/O L30N_4 D2 | I/O L27N_4 DIN D0 | VCCO_4 | I/O L19P_4 | I/O L14P_4 | I/O L11N_4 | VCCO_4 | I/O | I/O L04N_4 | I/O L09P_3 VREF_3 | VCCO_3 | I/O L07P_3 | I/O L07N_3 | I/O L08P_3 | I/O L08N_3 |
| AE | I/O L30P_4 D3 | I/O L27P_4 D1 | I/O L24N_4 | I/O L20N_4 | I/O L15N_4 | I/O L11P_4 | I/O | I/O L05N_4 | I/O L34P_4 ◆ | I/O L34N_4 ◆ | I/O L05N_3 | VCCAUX | I/O L06P_3 | I/O L06N_3 | GND |
| AF | I/O VREF_4 | GND | I/O L24P_4 | I/O L20P_4 | I/O L15P_4 | GND | I/O L09N_4 | I/O L05P_4 | VCCO_4 | I/O L03P_4 | GND | I/O L05P_3 | VCCO_3 | I/O L04P_3 | I/O L04N_3 |
| AG | I/O L31N_4 INIT_B | VCCAUX | I/O | I/O L21N_4 | I/O L16N_4 | VCCAUX | I/O L09P_4 | I/O L06N_4 VREF_4 | I/O L35N_4 ◆ | VCCAUX | I/O L03N_4 | I/O L02P_3 | I/O L02N_3 VREF_3 | I/O L03P_3 | I/O L03N_3 |
| AH | I/O L31P_4 DOUT BUSY | I/O L28N_4 | VCCO_4 | I/O L21P_4 | I/O L16P_4 | I/O L12N_4 | VCCO_4 | I/O L06P_4 | I/O L35P_4 ◆ | I/O L33N_4 ◆ | VCCO_4 | I/O | CCLK | I/O L01P_3 VRN_3 | I/O L01N_3 VRP_3 |
| AJ | I/O L32N_4 GCLK1 | I/O L28P_4 | I/O L25N_4 | I/O L22N_4 VREF_4 | I/O L17N_4 | I/O L12P_4 | I/O L10N_4 | I/O L07N_4 | I/O L38N_4 ◆ | I/O L33P_4 ◆ | I/O L02N_4 | I/O L01N_4 VRP_4 | DONE | GND | GND |
| AK | I/O L32P_4 GCLK0 | GND | I/O L25P_4 | I/O L22P_4 | I/O L17P_4 | GND | I/O L10P_4 | I/O L07P_4 | I/O L38P_4 ◆ | GND | I/O L02P_4 | I/O L01P_4 VRN_4 | IO VREF_4 | GND | GND |

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**Figure 56: FG900 Package Footprint (Top View) Continued**

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| 3 | IO_L48P_3 | IO_L48P_3 | AB24 | I/O |
| 3 | N.C. (◆) | IO_L49N_3 | AA26 | I/O |
| 3 | N.C. (◆) | IO_L49P_3 | AA25 | I/O |
| 3 | IO_L50N_3 | IO_L50N_3 | Y25 | I/O |
| 3 | IO_L50P_3 | IO_L50P_3 | Y24 | I/O |
| 3 | N.C. (◆) | IO_L51N_3 | V24 | I/O |
| 3 | N.C. (◆) | IO_L51P_3 | W24 | I/O |
| 3 | VCCO_3 | VCCO_3 | AA23 | VCCO |
| 3 | VCCO_3 | VCCO_3 | AB23 | VCCO |
| 3 | VCCO_3 | VCCO_3 | AB29 | VCCO |
| 3 | VCCO_3 | VCCO_3 | AB33 | VCCO |
| 3 | VCCO_3 | VCCO_3 | AD27 | VCCO |
| 3 | VCCO_3 | VCCO_3 | AD31 | VCCO |
| 3 | VCCO_3 | VCCO_3 | AG28 | VCCO |
| 3 | VCCO_3 | VCCO_3 | AG32 | VCCO |
| 3 | VCCO_3 | VCCO_3 | AL32 | VCCO |
| 3 | VCCO_3 | VCCO_3 | W23 | VCCO |
| 3 | VCCO_3 | VCCO_3 | W31 | VCCO |
| 3 | VCCO_3 | VCCO_3 | Y23 | VCCO |
| 3 | VCCO_3 | VCCO_3 | Y27 | VCCO |
| 4 | IO | IO | AD18 | I/O |
| 4 | IO | IO | AD19 | I/O |
| 4 | IO | IO | AD20 | I/O |
| 4 | IO | IO | AD22 | I/O |
| 4 | IO | IO | AE18 | I/O |
| 4 | IO | IO | AE19 | I/O |
| 4 | IO | IO | AE22 | I/O |
| 4 | N.C. (◆) | IO | AE24 | I/O |
| 4 | IO | IO | AF24 | I/O |
| 4 | N.C. (◆) | IO | AF26 | I/O |
| 4 | IO | IO | AG26 | I/O |
| 4 | IO | IO | AG27 | I/O |
| 4 | IO | IO | AJ27 | I/O |
| 4 | IO | IO | AJ29 | I/O |
| 4 | IO | IO | AK25 | I/O |
| 4 | IO | IO | AN26 | I/O |
| 4 | IO/VREF_4 | IO/VREF_4 | AF21 | VREF |
| 4 | IO/VREF_4 | IO/VREF_4 | AH23 | VREF |
| 4 | IO/VREF_4 | IO/VREF_4 | AK18 | VREF |
| 4 | IO/VREF_4 | IO/VREF_4 | AL30 | VREF |

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| 6 | IO_L16N_6 | IO_L16N_6 | AE2 | I/O |
| 6 | IO_L16P_6 | IO_L16P_6 | AE1 | I/O |
| 6 | IO_L17N_6 | IO_L17N_6 | AD10 | I/O |
| 6 | IO_L17P_6/VREF_6 | IO_L17P_6/VREF_6 | AD9 | VREF |
| 6 | IO_L19N_6 | IO_L19N_6 | AD2 | I/O |
| 6 | IO_L19P_6 | IO_L19P_6 | AD1 | I/O |
| 6 | IO_L20N_6 | IO_L20N_6 | AC11 | I/O |
| 6 | IO_L20P_6 | IO_L20P_6 | AC10 | I/O |
| 6 | IO_L21N_6 | IO_L21N_6 | AC8 | I/O |
| 6 | IO_L21P_6 | IO_L21P_6 | AC7 | I/O |
| 6 | IO_L22N_6 | IO_L22N_6 | AC6 | I/O |
| 6 | IO_L22P_6 | IO_L22P_6 | AC5 | I/O |
| 6 | IO_L23N_6 | IO_L23N_6 | AC2 | I/O |
| 6 | IO_L23P_6 | IO_L23P_6 | AC1 | I/O |
| 6 | IO_L24N_6/VREF_6 | IO_L24N_6/VREF_6 | AC9 | VREF |
| 6 | IO_L24P_6 | IO_L24P_6 | AB10 | I/O |
| 6 | IO_L25N_6 | IO_L25N_6 | AB8 | I/O |
| 6 | IO_L25P_6 | IO_L25P_6 | AB7 | I/O |
| 6 | IO_L26N_6 | IO_L26N_6 | AB4 | I/O |
| 6 | IO_L26P_6 | IO_L26P_6 | AB3 | I/O |
| 6 | IO_L27N_6 | IO_L27N_6 | AB11 | I/O |
| 6 | IO_L27P_6 | IO_L27P_6 | AA11 | I/O |
| 6 | IO_L28N_6 | IO_L28N_6 | AA8 | I/O |
| 6 | IO_L28P_6 | IO_L28P_6 | AA7 | I/O |
| 6 | IO_L29N_6 | IO_L29N_6 | AA6 | I/O |
| 6 | IO_L29P_6 | IO_L29P_6 | AA5 | I/O |
| 6 | IO_L30N_6 | IO_L30N_6 | AA4 | I/O |
| 6 | IO_L30P_6 | IO_L30P_6 | AA3 | I/O |
| 6 | IO_L31N_6 | IO_L31N_6 | AA2 | I/O |
| 6 | IO_L31P_6 | IO_L31P_6 | AA1 | I/O |
| 6 | IO_L32N_6 | IO_L32N_6 | Y11 | I/O |
| 6 | IO_L32P_6 | IO_L32P_6 | Y10 | I/O |
| 6 | IO_L33N_6 | IO_L33N_6 | Y4 | I/O |
| 6 | IO_L33P_6 | IO_L33P_6 | Y3 | I/O |
| 6 | IO_L34N_6/VREF_6 | IO_L34N_6/VREF_6 | Y2 | VREF |
| 6 | IO_L34P_6 | IO_L34P_6 | Y1 | I/O |
| 6 | IO_L35N_6 | IO_L35N_6 | Y9 | I/O |
| 6 | IO_L35P_6 | IO_L35P_6 | W10 | I/O |
| 6 | IO_L36N_6 | IO_L36N_6 | W7 | I/O |
| 6 | IO_L36P_6 | IO_L36P_6 | W6 | I/O |

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| N/A | GND | GND | AN1 | GND |
| N/A | GND | GND | AN2 | GND |
| N/A | GND | GND | AN33 | GND |
| N/A | GND | GND | AN34 | GND |
| N/A | GND | GND | AP1 | GND |
| N/A | GND | GND | AP13 | GND |
| N/A | GND | GND | AP16 | GND |
| N/A | GND | GND | AP19 | GND |
| N/A | GND | GND | AP2 | GND |
| N/A | GND | GND | AP22 | GND |
| N/A | GND | GND | AP26 | GND |
| N/A | GND | GND | AP30 | GND |
| N/A | GND | GND | AP33 | GND |
| N/A | GND | GND | AP34 | GND |
| N/A | GND | GND | AP5 | GND |
| N/A | GND | GND | AP9 | GND |
| N/A | GND | GND | B1 | GND |
| N/A | GND | GND | B2 | GND |
| N/A | GND | GND | B33 | GND |
| N/A | GND | GND | B34 | GND |
| N/A | GND | GND | C11 | GND |
| N/A | GND | GND | C24 | GND |
| N/A | GND | GND | C3 | GND |
| N/A | GND | GND | C32 | GND |
| N/A | GND | GND | E1 | GND |
| N/A | GND | GND | E13 | GND |
| N/A | GND | GND | E16 | GND |
| N/A | GND | GND | E19 | GND |
| N/A | GND | GND | E22 | GND |
| N/A | GND | GND | E26 | GND |
| N/A | GND | GND | E30 | GND |
| N/A | GND | GND | E34 | GND |
| N/A | GND | GND | E5 | GND |
| N/A | GND | GND | E9 | GND |
| N/A | GND | GND | G28 | GND |
| N/A | GND | GND | G7 | GND |
| N/A | GND | GND | J1 | GND |
| N/A | GND | GND | J13 | GND |
| N/A | GND | GND | J16 | GND |
| N/A | GND | GND | J19 | GND |

## FG1156 Footprint

***Top Left Corner of FG1156 Package (Top View)***

**XC3S4000 (712 max. user I/O)**

| | |
|---|---|
| 621 | **I/O:** Unrestricted, general-purpose user I/O |
| 55 | **VREF:** User I/O or input voltage reference for bank |
| 73 | **N.C.:** Unconnected pins for XC3S4000 (◆) |

**XC3S5000 (784 max. user I/O)**

| | |
|---|---|
| 692 | **I/O:** Unrestricted, general-purpose user I/O |
| 56 | **VREF:** User I/O or input voltage reference for bank |
| 1 | **N.C.:** Unconnected pins for XC3S5000 (■) |

Bank 0 (columns 3–17); Bank 7 (rows C–U)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | GND | GND | I/O L01P_0 VRN_0 | I/O L02P_0 | GND | I/O L05P_0 VREF_0 | I/O L34P_0 ◆ | I/O L36P_0 | GND | I/O L38P_0 | I/O L40P_0 ◆ | I/O L15P_0 | GND | I/O L22P_0 | I/O L26P_0 VREF_0 | GND | I/O L32P_0 GCLK6 |
| **B** | GND | GND | I/O L01N_0 VRP_0 | I/O L02N_0 | I/O L03P_0 | I/O L05N_0 | I/O L34N_0 ◆ | I/O L36N_0 | I/O | I/O L38N_0 | I/O L40N_0 ◆ | I/O L15N_0 | VCCO_0 | I/O L22N_0 | I/O L26N_0 | I/O L28P_0 | I/O L32N_0 GCLK7 |
| **C** | I/O L01N_7 VRP_7 | I/O L01P_7 VRN_7 | GND | VCCO_0 | I/O L03N_0 | I/O L04P_0 | I/O L33P_0 ◆ | VCCO_0 | I/O L08P_0 | I/O L37P_0 | GND | I/O L14P_0 | I/O L17P_0 | I/O L21P_0 | I/O L25P_0 | I/O L28N_0 | I/O L31P_0 VREF_0 |
| **D** | I/O L02N_7 | I/O L02P_7 | VCCO_7 | PROG_B | IO VREF_0 | I/O L04N_0 | I/O L33N_0 ◆ | I/O L35P_0 | I/O L08N_0 | I/O L37N_0 | VCCO_0 | I/O L14N_0 | I/O L17N_0 | I/O L21N_0 | I/O L25N_0 | VCCO_0 | I/O L31N_0 |
| **E** | GND | I/O L03N_7 VREF_7 | I/O L03P_7 | TDI | GND | VCCAUX | I/O L06P_0 | I/O L35N_0 | GND | IO VREF_0 | VCCAUX | I/O L13P_0 | GND | I/O L20P_0 | VCCAUX | GND | I/O |
| **F** | I/O L05N_7 | I/O L05P_7 | I/O L04N_7 | I/O L04P_7 | VCCAUX | I/O | I/O L06N_0 | I/O | I/O L07P_0 | I/O L10P_0 | I/O L39P_0 ◆ | I/O L13N_0 | VCCO_0 | I/O L20N_0 | I/O L24P_0 | I/O L27P_0 | I/O L30P_0 |
| **G** | I/O | I/O | I/O L41N_7 ◆ | I/O L41P_7 ◆ | I/O L06N_7 | I/O L06P_7 | GND | VCCO_0 | I/O L07N_0 | I/O L10N_0 | I/O L39N_0 ◆ | I/O | I/O L16P_0 | I/O L19P_0 | I/O L24N_0 | I/O L27N_0 | I/O L30N_0 |
| **H** | I/O L08N_7 | I/O L08P_7 | VCCO_7 | I/O L10P_7 VREF_7 | I/O L07N_7 | I/O L07P_7 | VCCO_7 | I/O | I/O | I/O L09P_0 | VCCO_0 | I/O L12P_0 | I/O L16N_0 | I/O L19N_0 | VCCO_0 | VCCAUX | I/O L29P_0 |
| **J** | GND | I/O L11N_7 | I/O L11P_7 | I/O L10N_7 | GND | I/O L09N_7 | I/O L09P_7 | I/O L12P_7 | I/O ◆ | I/O L09N_0 | I/O | I/O L12N_0 | GND | IO VREF_0 | I/O L23P_0 | GND | I/O L29N_0 |
| **K** | I/O L16N_7 | I/O L16P_7 VREF_7 | I/O L15N_7 | I/O L15P_7 | I/O L14N_7 | I/O L14P_7 | I/O L13N_7 | I/O L13P_7 | I/O L12N_7 | GND | I/O ◆ | I/O L11P_0 | I/O | I/O L18P_0 | I/O L23N_0 | I/O | I/O |
| **L** | I/O L19N_7 VREF_7 | I/O L19P_7 | GND | VCCO_7 | VCCAUX | I/O L44N_7 ◆ | I/O L44P_7 ◆ | VCCO_7 | I/O L17N_7 | I/O L17P_7 | HSWAP_EN | I/O L11N_0 | I/O | I/O L18N_0 | IO VREF_0 | I/O | I/O |
| **M** | I/O L45N_7 | I/O L45P_7 | I/O L23N_7 | I/O L23P_7 | I/O L22N_7 | I/O L22P_7 | I/O L21N_7 | I/O L21P_7 | I/O L24P_7 | I/O L20N_7 | I/O L20P_7 | VCCINT | VCCO_0 | VCCO_0 | VCCO_0 | VCCO_0 | VCCINT |
| **N** | GND | VCCO_7 | I/O L25N_7 | I/O L25P_7 | GND | VCCO_7 | I/O L46N_7 | I/O L46P_7 | GND | I/O L24N_7 | I/O L26P_7 | VCCO_7 | VCCINT | VCCINT | VCCINT | VCCINT | GND |
| **P** | I/O L49N_7 | I/O L49P_7 | I/O L29N_7 | I/O L29P_7 | I/O L28N_7 | I/O L28P_7 | I/O L27N_7 | I/O L27P_7 VREF_7 | I/O L47N_7 ◆ | I/O L47P_7 ◆ | I/O L26N_7 | VCCO_7 | VCCINT | GND | GND | GND | GND |
| **R** | I/O L32N_7 | I/O L32P_7 | I/O L31N_7 | I/O L31P_7 | VCCAUX | I/O L30N_7 | I/O L30P_7 | VCCO_7 | I/O L33P_7 | I/O L50N_7 | I/O L50P_7 | VCCO_7 | VCCINT | GND | GND | GND | GND |
| **T** | GND | I/O L35N_7 | I/O L35P_7 | VCCO_7 | GND | I/O L34N_7 | I/O L34P_7 | VCCAUX | GND | I/O L33N_7 | I/O L51P_7 ◆ | VCCO_7 | VCCINT | GND | GND | GND | GND |
| **U** | I/O L40N_7 VREF_7 | I/O L40P_7 | I/O L39N_7 | I/O L39P_7 | I/O L38N_7 | I/O L38P_7 | I/O L37N_7 | I/O L37P_7 VREF_7 | I/O | I/O | I/O L51N_7 ◆ | VCCINT | GND | GND | GND | GND | GND |

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*Figure 57:* **FG1156 Package Footprint (Top View)**