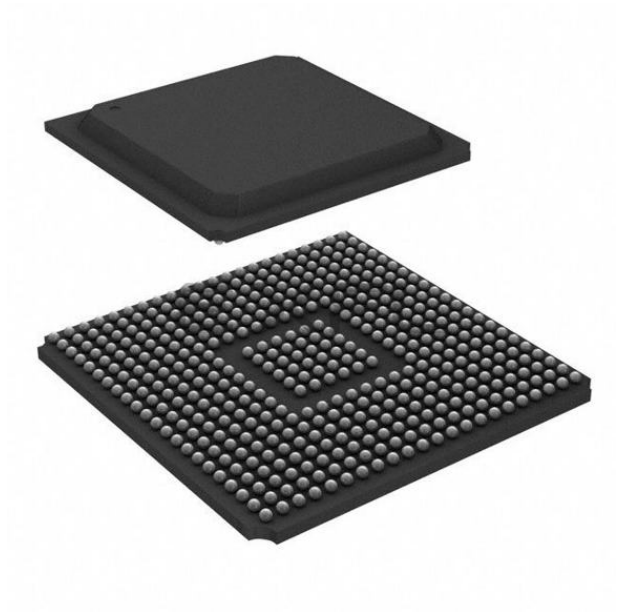

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3328
Number of Logic Elements/Cells	29952
Total RAM Bits	589824
Number of I/O	333
Number of Gates	1500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1500-4fg456c

The DLL component has two clock inputs, CLKIN and CLKFB, as well as seven clock outputs, CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV as described in Table 16. The clock outputs drive simultaneously; however, the High Frequency mode only supports a subset of the outputs available in the Low Frequency mode. See DLL Frequency Modes, page 35. Signals that initialize and report the state of the DLL are discussed in The Status Logic Component, page 41.

Table 16: **DLL Signals**

Signal	Direction	Description	Mode Support	
			Low Frequency	High Frequency
CLKIN	Input	Accepts original clock signal.	Yes	Yes
CLKFB	Input	Accepts either CLK0 or CLK2X as feed back signal. (Set CLK_FEEDBACK attribute accordingly).	Yes	Yes
CLK0	Output	Generates clock signal with same frequency and phase as CLKIN.	Yes	Yes
CLK90	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 90°.	Yes	No
CLK180	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 180°.	Yes	Yes
CLK270	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 270°.	Yes	No
CLK2X	Output	Generates clock signal with same phase as CLKIN, only twice the frequency.	Yes	No
CLK2X180	Output	Generates clock signal with twice the frequency of CLKIN, phase-shifted 180° with respect to CLKIN.	Yes	No
CLKDV	Output	Divides the CLKIN frequency by CLKDV_DIVIDE value to generate lower frequency clock signal that is phase-aligned to CLKIN.	Yes	Yes

The clock signal supplied to the CLKIN input serves as a reference waveform, with which the DLL seeks to align the feedback signal at the CLKFB input. When eliminating clock skew, the common approach to using the DLL is as follows: The CLK0 signal is passed through the clock distribution network to all the registers it synchronizes. These registers are either internal or external to the FPGA. After passing through the clock distribution network, the clock signal returns to the DLL via a feedback line called CLKFB. The control block inside the DLL measures the phase error between CLKFB and CLKIN. This phase error is a measure of the clock skew that the clock distribution network introduces. The control block activates the appropriate number of delay elements to cancel out the clock skew. Once the DLL has brought the CLK0 signal in phase with the CLKIN signal, it asserts the LOCKED output, indicating a “lock” on to the CLKIN signal.

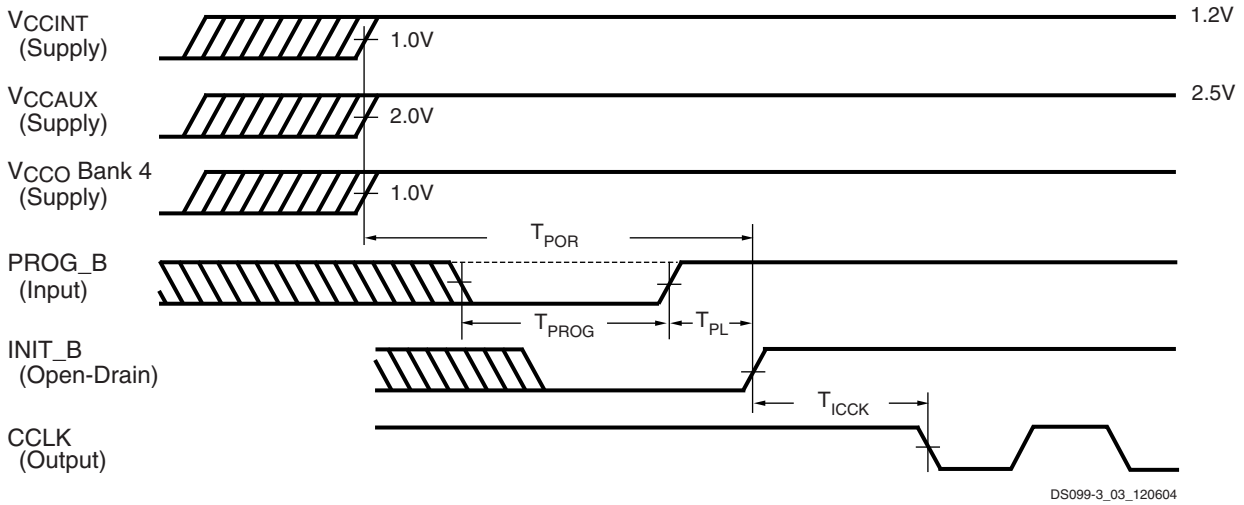
DLL Attributes and Related Functions

A number of different functional options can be set for the DLL component through the use of the attributes described in Table 17. Each attribute is described in detail in the sections that follow:

Table 17: **DLL Attributes**

Attribute	Description	Values
CLK_FEEDBACK	Chooses either the CLK0 or CLK2X output to drive the CLKFB input	NONE, 1X, 2X
DLL_FREQUENCY_MODE	Chooses between High Frequency and Low Frequency modes	LOW, HIGH
CLKIN_DIVIDE_BY_2	Halves the frequency of the CLKIN signal just as it enters the DCM	TRUE, FALSE
CLKDV_DIVIDE	Selects constant used to divide the CLKIN input frequency to generate the CLKDV output frequency	1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6.0, 6.5, 7.0, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.
DUTY_CYCLE_CORRECTION	Enables 50% duty cycle correction for the CLK0, CLK90, CLK180, and CLK270 outputs	TRUE, FALSE

Configuration and JTAG Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 36: **Waveforms for Power-On and the Beginning of Configuration**

Table 65: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 4 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XC3S50	–	5	ms
		XC3S200	–	5	ms
		XC3S400	–	5	ms
		XC3S1000	–	5	ms
		XC3S1500	–	7	ms
		XC3S2000	–	7	ms
		XC3S4000	–	7	ms
		XC3S5000	–	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.3	–	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S50	–	2	ms
		XC3S200	–	2	ms
		XC3S400	–	2	ms
		XC3S1000	–	2	ms
		XC3S1500	–	3	ms
		XC3S2000	–	3	ms
		XC3S4000	–	3	ms
		XC3S5000	–	3	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	–	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.25	4.0	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only for the Master Serial and Master Parallel modes.

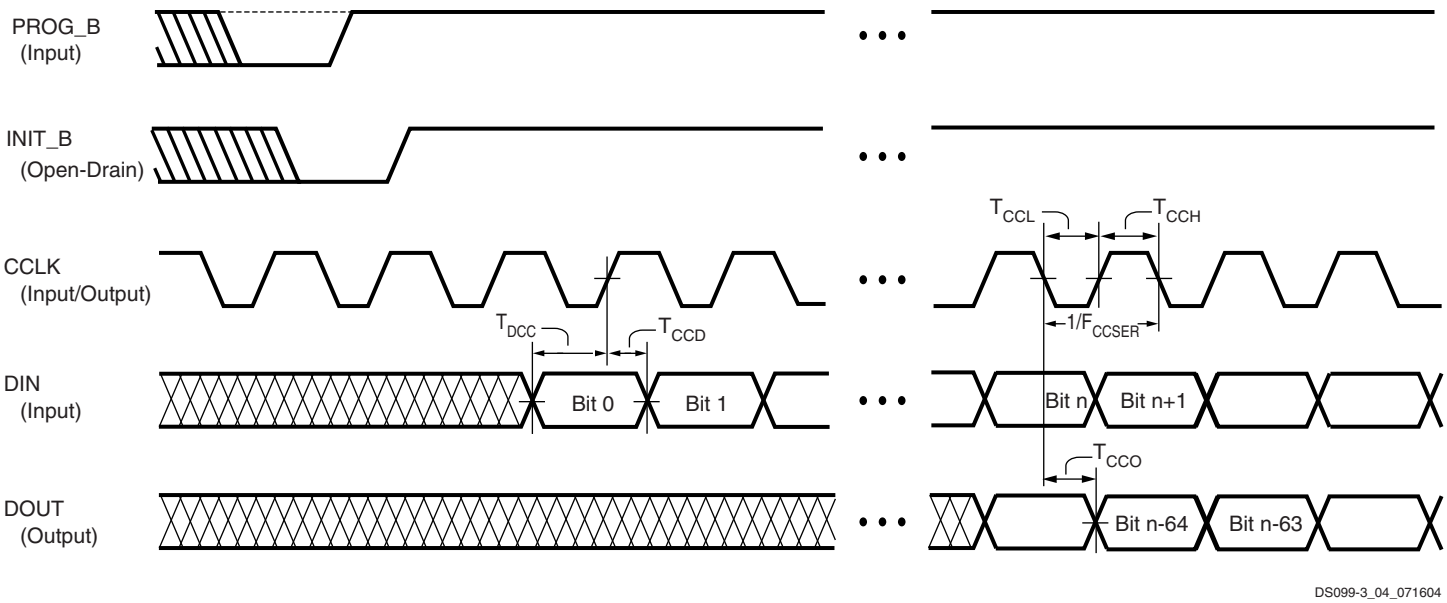


Figure 37: **Waveforms for Master and Slave Serial Configuration**

Table 66: **Timing for the Master and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	12.0	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		Both	10.0	–	ns
Hold Times						
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		Both	0	–	ns
Clock Timing						
T_{CCH}	CCLK input pin High pulse width		Slave	5.0	∞	ns
T_{CCL}	CCLK input pin Low pulse width			5.0	∞	ns
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression		0	66(2)	MHz
		With bitstream compression		0	20	MHz
		During STARTUP phase		0	50	MHz
ΔF_{CCSER}	Variation from the CCLK output frequency set using the ConfigRate BitGen option		Master	–50%	+50%	–

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Spartan-3 FPGA Family: Pinout Descriptions

DS099 (v3.0) October 29, 2012 **Product Specification**

Introduction

This data sheet module describes the various pins on a Spartan®-3 FPGA and how they connect to the supported component packages.

- The Pin Types section categorizes all of the FPGA pins by their function type.
- The Pin Definitions section provides a top-level description for each pin on the device.
- The Detailed, Functional Pin Descriptions section offers significantly more detail about each pin, especially for the dual- or special-function pins used during device configuration.
- Some pins have associated behavior that is controlled by settings in the configuration bitstream. These options are described in the Bitstream Options section.
- The Package Overview section describes the various packaging options available for Spartan-3 FPGAs. Detailed pin list tables and footprint diagrams are provided for each package solution.

Pin Descriptions

Pin Types

A majority of the pins on a Spartan-3 FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3 device packages, as outlined in Table 69. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 69: **Types of Pins on Spartan-3 FPGAs**

Pin Type/ Color Code	Description	Pin Name
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO, IO_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. There are 12 dual-purpose configuration pins on every package. The INIT_B pin has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM during configuration.	IO_Lxxy_#/DIN/D0, IO_Lxxy_#/D1, IO_Lxxy_#/D2, IO_Lxxy_#/D3, IO_Lxxy_#/D4, IO_Lxxy_#/D5, IO_Lxxy_#/D6, IO_Lxxy_#/D7, IO_Lxxy_#/CS_B, IO_Lxxy_#/RDWR_B, IO_Lxxy_#/BUSY/DOUT, IO_Lxxy_#/INIT_B
CONFIG	Dedicated configuration pin. Not available as a user-I/O pin. Every package has seven dedicated configuration pins. These pins are powered by VCCAUX and have a dedicated internal pull-up resistor to VCCAUX during configuration.	CCLK, DONE, M2, M1, M0, PROG_B, HSWAP_EN
JTAG	Dedicated JTAG pin. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX and have a dedicated internal pull-up resistor to VCCAUX during configuration.	TDI, TMS, TCK, TDO
DCI	Dual-purpose pin that is either a user-I/O pin or used to calibrate output buffer impedance for a specific bank using Digital Controlled Impedance (DCI). There are two DCI pins per I/O bank.	IO/VRN_# IO_Lxxy_#/VRN_# IO/VRP_# IO_Lxxy_#/VRP_#

All VCCAUX inputs must be connected together and to the +2.5V voltage supply. Furthermore, there must be sufficient supply decoupling to guarantee problem-free operation, as described in XAPP623.

Because VCCAUX connects to the DCMs and the DCMs are sensitive to voltage changes, be sure that the VCCAUX supply and the ground return paths are designed for low noise and low voltage drop, especially that caused by a large number of simultaneous switching I/Os.

GND Type: Ground

All GND pins must be connected and have a low resistance path back to the various VCCO, VCCINT, and VCCAUX supplies.

Pin Behavior During Configuration

Table 79 shows how various pins behave during the FPGA configuration process. The actual behavior depends on the values applied to the M2, M1, and M0 mode select pins and the HSWAP_EN pin. The mode select pins determine which of the DUAL type pins are active during configuration. In JTAG configuration mode, none of the DUAL-type pins are used for configuration and all behave as user-I/O pins.

All DUAL-type pins not actively used during configuration and all I/O-type, DCI-type, VREF-type, GCLK-type pins are high impedance (floating, three-stated, Hi-Z) during the configuration process. These pins are indicated in Table 79 as shaded table entries or cells. These pins have a pull-up resistor to their associated VCCO if the HSWAP_EN pin is Low. When HSWAP_EN is High, these pull-up resistors are disabled during configuration.

Some pins always have an active pull-up resistor during configuration, regardless of the value applied to the HSWAP_EN pin. After configuration, these pull-up resistors are controlled by Bitstream Options.

- All the dedicated CONFIG-type configuration pins (CCLK, PROG_B, DONE, M2, M1, M0, and HSWAP_EN) have a pull-up resistor to VCCAUX.
- All JTAG-type pins (TCK, TDI, TMS, TDO) have a pull-up resistor to VCCAUX.
- The INIT_B DUAL-purpose pin has a pull-up resistor to VCCO_4 or VCCO_BOTTOM, depending on package style.

After configuration completes, some pins have optional behavior controlled by the configuration bitstream loaded into the part. For example, via the bitstream, all unused I/O pins can be collectively configured as input pins with either a pull-up resistor, a pull-down resistor, or be left in a high-impedance state.

Table 79: **Pin Behavior After Power-Up, During Configuration**

Pin Name	Configuration Mode Settings <M2:M1:M0>					Bitstream Configuration Option
	Serial Modes		SelectMap Parallel Modes		JTAG Mode <1:0:1>	
	Master <0:0:0>	Slave <1:1:1>	Master <0:1:1>	Slave <1:1:0>		
I/O: General-purpose I/O pins						
IO						UnusedPin
IO_Lxxy_#						UnusedPin
DUAL: Dual-purpose configuration pins						
IO_Lxxy_#/ DIN/D0	DIN (I)	DIN (I)	D0 (I/O)	D0 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D1			D1 (I/O)	D1 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D2			D2 (I/O)	D2 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D3			D3 (I/O)	D3 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D4			D4 (I/O)	D4 (I/O)		Persist UnusedPin

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3 FPGA is reported using either the XPower Estimator (XPE) or the XPower Analyzer integrated in the Xilinx ISE development software. Table 86 provides the thermal characteristics for the various Spartan-3 device/package offerings.

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference per watt between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 86: **Spartan-3 FPGA Package Thermal Characteristics**

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
VQ(G)100	XC3S50	12.0	–	46.2	38.4	35.8	34.9	°C/Watt
	XC3S200	10.0	–	40.5	33.7	31.3	30.5	°C/Watt
CP(G)132(1)	XC3S50	14.5	32.8	53.0	46.4	44.0	42.5	°C/Watt
TQ(G)144	XC3S50	7.6	–	41.0	31.9	27.2	25.6	°C/Watt
	XC3S200	6.6	–	34.5	26.9	23.0	21.6	°C/Watt
	XC3S400	6.1	–	32.8	25.5	21.8	20.4	°C/Watt
PQ(G)208	XC3S50	10.6	–	37.4	27.6	24.4	22.6	°C/Watt
	XC3S200	8.6	–	36.2	26.7	23.6	21.9	°C/Watt
	XC3S400	7.5	–	35.4	26.1	23.1	21.4	°C/Watt
FT(G)256	XC3S200	9.9	22.9	31.7	25.6	24.5	24.2	°C/Watt
	XC3S400	7.9	19.0	28.4	22.8	21.5	21.0	°C/Watt
	XC3S1000	5.6	14.7	24.8	19.2	18.0	17.5	°C/Watt
FG(G)320	XC3S400	8.9	13.9	24.4	19.0	17.8	17.0	°C/Watt
	XC3S1000	7.8	11.8	22.3	17.0	15.8	15.0	°C/Watt
	XC3S1500	6.7	9.8	20.3	15.18	13.8	13.1	°C/Watt
FG(G)456	XC3S400	8.4	13.6	20.8	15.1	13.9	13.4	°C/Watt
	XC3S1000	6.4	10.6	19.3	13.4	12.3	11.7	°C/Watt
	XC3S1500	4.9	8.3	18.3	12.4	11.2	10.7	°C/Watt
	XC3S2000	3.7	6.5	17.7	11.7	10.5	10.0	°C/Watt
FG(G)676	XC3S1000	6.0	10.4	17.9	13.7	12.6	12.0	°C/Watt
	XC3S1500	4.9	8.8	16.8	12.4	11.3	10.7	°C/Watt
	XC3S2000	4.1	7.9	15.6	11.1	9.9	9.3	°C/Watt
	XC3S4000	3.6	7.0	15.0	10.5	9.3	8.7	°C/Watt
	XC3S5000	3.4	6.3	14.7	10.3	9.1	8.5	°C/Watt
FG(G)900	XC3S2000	3.7	7.0	14.3	10.3	9.3	8.8	°C/Watt
	XC3S4000	3.3	6.4	13.6	9.7	8.7	8.2	°C/Watt
	XC3S5000	2.9	5.9	13.1	9.2	8.1	7.6	°C/Watt

PQ208 Footprint

Left Half of Package (Top View)

XC3S50
(124 max. user I/O)

72 **I/O:** Unrestricted, general-purpose user I/O

16 **VREF:** User I/O or input voltage reference for bank

17 **N.C.:** Unconnected pins for XC3S50 (◆)

XC3S200, XC3S400
(141 max user I/O)

83 **I/O:** Unrestricted, general-purpose user I/O

22 **VREF:** User I/O or input voltage reference for bank

0 **N.C.:** No unconnected pins in this package

All devices

12 **DUAL:** Configuration pin, then possible user I/O

8 **GCLK:** User I/O or global clock buffer input

16 **DCI:** User I/O or reference resistor input for bank

7 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

4 **VCCINT:** Internal core voltage supply (+1.2V)

12 **VCCO:** Output voltage supply for bank

8 **VCCAUX:** Auxiliary voltage supply (+2.5V)

28 **GND:** Ground

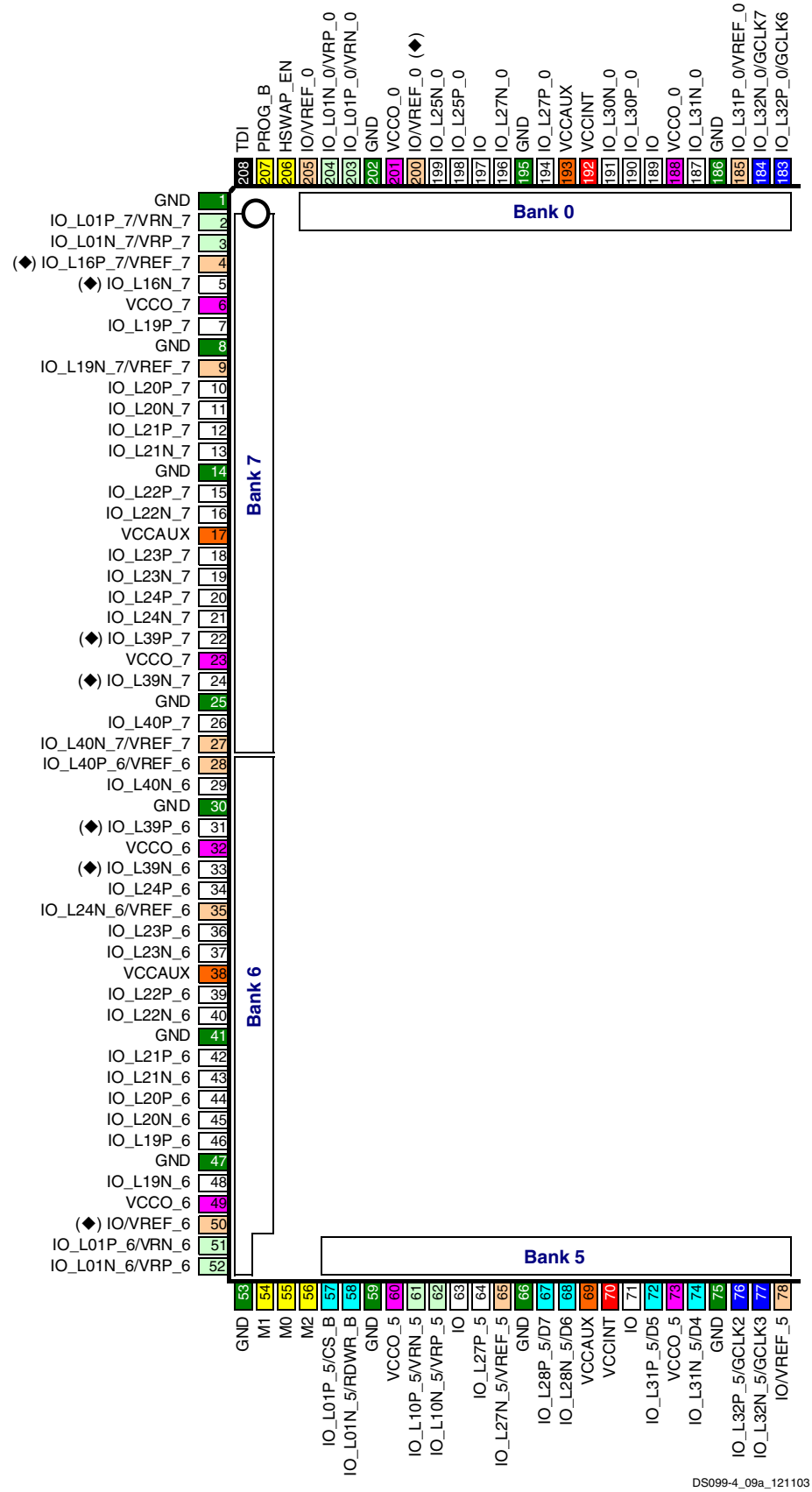


Figure 47: **PQ208 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

FT256: 256-lead Fine-pitch Thin Ball Grid Array

The 256-lead fine-pitch thin ball grid array package, FT256, supports three different Spartan-3 devices, including the XC3S200, the XC3S400, and the XC3S1000. The footprints for all three devices are identical, as shown in Table 96 and Figure 49.

All the package pins appear in Table 96 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 96: **FT256 Package Pinout**

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
0	IO	A5	I/O
0	IO	A7	I/O
0	IO/VREF_0	A3	VREF
0	IO/VREF_0	D5	VREF
0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L25N_0	C5	I/O
0	IO_L25P_0	B5	I/O
0	IO_L27N_0	E6	I/O
0	IO_L27P_0	D6	I/O
0	IO_L28N_0	C6	I/O
0	IO_L28P_0	B6	I/O
0	IO_L29N_0	E7	I/O
0	IO_L29P_0	D7	I/O
0	IO_L30N_0	C7	I/O
0	IO_L30P_0	B7	I/O
0	IO_L31N_0	D8	I/O
0	IO_L31P_0/VREF_0	C8	VREF
0	IO_L32N_0/GCLK7	B8	GCLK
0	IO_L32P_0/GCLK6	A8	GCLK
0	VCCO_0	E8	VCCO
0	VCCO_0	F7	VCCO
0	VCCO_0	F8	VCCO
1	IO	A9	I/O
1	IO	A12	I/O
1	IO	C10	I/O
1	IO/VREF_1	D12	VREF
1	IO_L01N_1/VRP_1	A14	DCI
1	IO_L01P_1/VRN_1	B14	DCI

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
N/A	GND	T16	GND
N/A	VCCAUX	A6	VCCAUX
N/A	VCCAUX	A11	VCCAUX
N/A	VCCAUX	F1	VCCAUX
N/A	VCCAUX	F16	VCCAUX
N/A	VCCAUX	L1	VCCAUX
N/A	VCCAUX	L16	VCCAUX
N/A	VCCAUX	T6	VCCAUX
N/A	VCCAUX	T11	VCCAUX
N/A	VCCINT	D4	VCCINT
N/A	VCCINT	D13	VCCINT
N/A	VCCINT	E5	VCCINT
N/A	VCCINT	E12	VCCINT
N/A	VCCINT	M5	VCCINT
N/A	VCCINT	M12	VCCINT
N/A	VCCINT	N4	VCCINT
N/A	VCCINT	N13	VCCINT
VCCAUX	CCLK	T15	CONFIG
VCCAUX	DONE	R14	CONFIG
VCCAUX	HSWAP_EN	C4	CONFIG
VCCAUX	M0	P3	CONFIG
VCCAUX	M1	T2	CONFIG
VCCAUX	M2	P4	CONFIG
VCCAUX	PROG_B	B3	CONFIG
VCCAUX	TCK	C14	JTAG
VCCAUX	TDI	A2	JTAG
VCCAUX	TDO	A15	JTAG
VCCAUX	TMS	C13	JTAG

FG320: 320-lead Fine-pitch Ball Grid Array

The 320-lead fine-pitch ball grid array package, FG320, supports three different Spartan-3 devices, including the XC3S400, the XC3S1000, and the XC3S1500. The footprint for all three devices is identical, as shown in Table 98 and Figure 50.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

All the package pins appear in Table 98 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 98: **FG320 Package Pinout**

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
0	IO	D9	I/O
0	IO	E7	I/O
0	IO/VREF_0	B3	VREF
0	IO/VREF_0	D6	VREF
0	IO_L01N_0/VRP_0	A2	DCI
0	IO_L01P_0/VRN_0	A3	DCI
0	IO_L09N_0	B4	I/O
0	IO_L09P_0	C4	I/O
0	IO_L10N_0	C5	I/O
0	IO_L10P_0	D5	I/O
0	IO_L15N_0	A4	I/O
0	IO_L15P_0	A5	I/O
0	IO_L25N_0	B5	I/O
0	IO_L25P_0	B6	I/O
0	IO_L27N_0	C7	I/O
0	IO_L27P_0	D7	I/O
0	IO_L28N_0	C8	I/O
0	IO_L28P_0	D8	I/O
0	IO_L29N_0	E8	I/O
0	IO_L29P_0	F8	I/O
0	IO_L30N_0	A7	I/O
0	IO_L30P_0	A8	I/O
0	IO_L31N_0	B9	I/O
0	IO_L31P_0/VREF_0	A9	VREF
0	IO_L32N_0/GCLK7	E9	GCLK
0	IO_L32P_0/GCLK6	F9	GCLK
0	VCCO_0	B8	VCCO
0	VCCO_0	C6	VCCO
0	VCCO_0	G8	VCCO

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
3	VCCO_3	VCCO_3	N16	VCCO
3	VCCO_3	VCCO_3	P16	VCCO
3	VCCO_3	VCCO_3	R17	VCCO
3	VCCO_3	VCCO_3	R20	VCCO
4	IO	IO	U16	I/O
4	IO	IO	U17	I/O
4	IO	IO	W13	I/O
4	IO	IO	W14	I/O
4	IO/VREF_4	IO/VREF_4	AB13	VREF
4	IO/VREF_4	IO/VREF_4	V18	VREF
4	IO/VREF_4	IO/VREF_4	Y16	VREF
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	AA20	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	AB20	DCI
4	N.C. (◆)	IO_L05N_4	AA19	I/O
4	N.C. (◆)	IO_L05P_4	AB19	I/O
4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	W18	VREF
4	IO_L06P_4	IO_L06P_4	Y18	I/O
4	IO_L09N_4	IO_L09N_4	AA18	I/O
4	IO_L09P_4	IO_L09P_4	AB18	I/O
4	IO_L10N_4	IO_L10N_4	V17	I/O
4	IO_L10P_4	IO_L10P_4	W17	I/O
4	IO_L15N_4	IO_L15N_4	Y17	I/O
4	IO_L15P_4	IO_L15P_4	AA17	I/O
4	IO_L16N_4	IO_L16N_4	V16	I/O
4	IO_L16P_4	IO_L16P_4	W16	I/O
4	N.C. (◆)	IO_L19N_4	AA16	I/O
4	N.C. (◆)	IO_L19P_4	AB16	I/O
4	N.C. (◆)	IO_L22N_4/ VREF_4	V15	VREF
4	N.C. (◆)	IO_L22P_4	W15	I/O
4	IO_L24N_4	IO_L24N_4	AA15	I/O
4	IO_L24P_4	IO_L24P_4	AB15	I/O
4	IO_L25N_4	IO_L25N_4	U14	I/O
4	IO_L25P_4	IO_L25P_4	V14	I/O
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	AA14	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	AB14	DUAL
4	IO_L28N_4	IO_L28N_4	U13	I/O
4	IO_L28P_4	IO_L28P_4	V13	I/O
4	IO_L29N_4	IO_L29N_4	Y13	I/O
4	IO_L29P_4	IO_L29P_4	AA13	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	H9	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	H10	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	J11	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	J12	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	J13	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	K13	VCCO
1	IO	IO	IO	IO	IO	A14	I/O
1	IO	IO	IO	IO	IO	A22	I/O
1	IO	IO	IO	IO	IO	A23	I/O
1	IO	IO	IO	IO	IO	D16	I/O
1	IO	IO	IO	IO	IO_L17P_1(3)	E18	I/O
1	IO	IO	IO	IO	IO	F14	I/O
1	IO	IO	IO	IO	IO	F20	I/O
1	IO	IO	IO	IO	IO	G19	I/O
1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	C15	VREF
1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	C17	VREF
1	N.C. (◆)	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO_L17N_1/VREF_1(3)	D18	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	D22	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	E22	DCI
1	IO_L04N_1	IO_L04N_1	IO_L04N_1	IO_L04N_1	IO_L04N_1	B23	I/O
1	IO_L04P_1	IO_L04P_1	IO_L04P_1	IO_L04P_1	IO_L04P_1	C23	I/O
1	IO_L05N_1	IO_L05N_1	IO_L05N_1	IO_L05N_1	IO_L05N_1	E21	I/O
1	IO_L05P_1	IO_L05P_1	IO_L05P_1	IO_L05P_1	IO_L05P_1	F21	I/O
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	B22	VREF
1	IO_L06P_1	IO_L06P_1	IO_L06P_1	IO_L06P_1	IO_L06P_1	C22	I/O
1	IO_L07N_1	IO_L07N_1	IO_L07N_1	IO_L07N_1	IO_L07N_1	C21	I/O
1	IO_L07P_1	IO_L07P_1	IO_L07P_1	IO_L07P_1	IO_L07P_1	D21	I/O
1	IO_L08N_1	IO_L08N_1	IO_L08N_1	IO_L08N_1	IO_L08N_1	A21	I/O
1	IO_L08P_1	IO_L08P_1	IO_L08P_1	IO_L08P_1	IO_L08P_1	B21	I/O
1	IO_L09N_1	IO_L09N_1	IO_L09N_1	IO_L09N_1	IO_L09N_1	D20	I/O
1	IO_L09P_1	IO_L09P_1	IO_L09P_1	IO_L09P_1	IO_L09P_1	E20	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	A20	VREF
1	IO_L10P_1	IO_L10P_1	IO_L10P_1	IO_L10P_1	IO_L10P_1	B20	I/O
1	N.C. (◆)	IO_L11N_1	IO_L11N_1	IO_L11N_1	IO_L11N_1	E19	I/O
1	N.C. (◆)	IO_L11P_1	IO_L11P_1	IO_L11P_1	IO_L11P_1	F19	I/O
1	N.C. (◆)	IO_L12N_1	IO_L12N_1	IO_L12N_1	IO_L12N_1	C19	I/O
1	N.C. (◆)	IO_L12P_1	IO_L12P_1	IO_L12P_1	IO_L12P_1	D19	I/O
1	IO_L15N_1	IO_L15N_1	IO_L15N_1	IO_L15N_1	IO_L15N_1	A19	I/O
1	IO_L15P_1	IO_L15P_1	IO_L15P_1	IO_L15P_1	IO_L15P_1	B19	I/O
1	IO_L16N_1	IO_L16N_1	IO_L16N_1	IO_L16N_1	IO_L16N_1	F18	I/O
1	IO_L16P_1	IO_L16P_1	IO_L16P_1	IO_L16P_1	IO_L16P_1	G18	I/O
1	N.C. (◆)	IO_L18N_1	IO_L18N_1	IO_L18N_1	IO(3)	B18	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
7	IO_L29P_7	IO_L29P_7	IO_L29P_7	IO_L29P_7	IO_L29P_7	L2	I/O
7	IO_L31N_7	IO_L31N_7	IO_L31N_7	IO_L31N_7	IO_L31N_7	M7	I/O
7	IO_L31P_7	IO_L31P_7	IO_L31P_7	IO_L31P_7	IO_L31P_7	M8	I/O
7	IO_L32N_7	IO_L32N_7	IO_L32N_7	IO_L32N_7	IO_L32N_7	M6	I/O
7	IO_L32P_7	IO_L32P_7	IO_L32P_7	IO_L32P_7	IO_L32P_7	M5	I/O
7	IO_L33N_7	IO_L33N_7	IO_L33N_7	IO_L33N_7	IO_L33N_7	M3	I/O
7	IO_L33P_7	IO_L33P_7	IO_L33P_7	IO_L33P_7	IO_L33P_7	L4	I/O
7	IO_L34N_7	IO_L34N_7	IO_L34N_7	IO_L34N_7	IO_L34N_7	M1	I/O
7	IO_L34P_7	IO_L34P_7	IO_L34P_7	IO_L34P_7	IO_L34P_7	M2	I/O
7	IO_L35N_7	IO_L35N_7	IO_L35N_7	IO_L35N_7	IO_L35N_7	N7	I/O
7	IO_L35P_7	IO_L35P_7	IO_L35P_7	IO_L35P_7	IO_L35P_7	N8	I/O
7	IO_L38N_7	IO_L38N_7	IO_L38N_7	IO_L38N_7	IO_L38N_7	N5	I/O
7	IO_L38P_7	IO_L38P_7	IO_L38P_7	IO_L38P_7	IO_L38P_7	N6	I/O
7	IO_L39N_7	IO_L39N_7	IO_L39N_7	IO_L39N_7	IO_L39N_7	N3	I/O
7	IO_L39P_7	IO_L39P_7	IO_L39P_7	IO_L39P_7	IO_L39P_7	N4	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	N1	VREF
7	IO_L40P_7	IO_L40P_7	IO_L40P_7	IO_L40P_7	IO_L40P_7	N2	I/O
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	G3	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	J8	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	K8	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	L3	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	L9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	M9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	N9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	N10	VCCO
N/A	GND	GND	GND	GND	GND	A1	GND
N/A	GND	GND	GND	GND	GND	A26	GND
N/A	GND	GND	GND	GND	GND	AC4	GND
N/A	GND	GND	GND	GND	GND	AC12	GND
N/A	GND	GND	GND	GND	GND	AC15	GND
N/A	GND	GND	GND	GND	GND	AC23	GND
N/A	GND	GND	GND	GND	GND	AD3	GND
N/A	GND	GND	GND	GND	GND	AD24	GND
N/A	GND	GND	GND	GND	GND	AE2	GND
N/A	GND	GND	GND	GND	GND	AE25	GND
N/A	GND	GND	GND	GND	GND	AF1	GND
N/A	GND	GND	GND	GND	GND	AF26	GND
N/A	GND	GND	GND	GND	GND	B2	GND
N/A	GND	GND	GND	GND	GND	B25	GND
N/A	GND	GND	GND	GND	GND	C3	GND
N/A	GND	GND	GND	GND	GND	C24	GND
N/A	GND	GND	GND	GND	GND	D4	GND
N/A	GND	GND	GND	GND	GND	D12	GND

User I/Os by Bank

Table 104 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1000 in the FG676 package. Similarly, Table 105 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1500 in the FG676 package. Finally, Table 106 shows the same information for the XC3S2000, XC3S4000, and XC3S5000 in the FG676 package.

Table 104: **User I/Os Per Bank for XC3S1000 in FG676 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	49	40	0	2	5	2
	1	50	41	0	2	5	2
Right	2	48	41	0	2	5	0
	3	48	41	0	2	5	0
Bottom	4	50	35	6	2	5	2
	5	50	35	6	2	5	2
Left	6	48	41	0	2	5	0
	7	48	41	0	2	5	0

Table 105: **User I/Os Per Bank for XC3S1500 in FG676 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	62	52	0	2	6	2
	1	61	51	0	2	6	2
Right	2	60	52	0	2	6	0
	3	60	52	0	2	6	0
Bottom	4	63	47	6	2	6	2
	5	61	45	6	2	6	2
Left	6	60	52	0	2	6	0
	7	60	52	0	2	6	0

Table 106: **User I/Os Per Bank for XC3S2000, XC3S4000, and XC3S5000 in FG676 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	62	52	0	2	6	2
	1	61	51	0	2	6	2
Right	2	61	53	0	2	6	0
	3	60	52	0	2	6	0
Bottom	4	63	47	6	2	6	2
	5	61	45	6	2	6	2
Left	6	61	53	0	2	6	0
	7	60	52	0	2	6	0

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
1	IO_L25P_1	IO_L25P_1	D19	I/O
1	IO_L26N_1	IO_L26N_1	A19	I/O
1	IO_L26P_1	IO_L26P_1	B19	I/O
1	IO_L27N_1	IO_L27N_1	F17	I/O
1	IO_L27P_1	IO_L27P_1	G17	I/O
1	IO_L28N_1	IO_L28N_1	B17	I/O
1	IO_L28P_1	IO_L28P_1	C17	I/O
1	IO_L29N_1	IO_L29N_1	J16	I/O
1	IO_L29P_1	IO_L29P_1	K16	I/O
1	IO_L30N_1	IO_L30N_1	G16	I/O
1	IO_L30P_1	IO_L30P_1	H16	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D16	VREF
1	IO_L31P_1	IO_L31P_1	E16	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B16	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C16	GCLK
1	N.C. (◆)	IO_L37N_1	H18	I/O
1	N.C. (◆)	IO_L37P_1	J18	I/O
1	N.C. (◆)	IO_L38N_1	D18	I/O
1	N.C. (◆)	IO_L38P_1	E18	I/O
1	N.C. (◆)	IO_L39N_1	A18	I/O
1	N.C. (◆)	IO_L39P_1	B18	I/O
1	N.C. (◆)	IO_L40N_1	K17	I/O
1	N.C. (◆)	IO_L40P_1	K18	I/O
1	VCCO_1	VCCO_1	L17	VCCO
1	VCCO_1	VCCO_1	C18	VCCO
1	VCCO_1	VCCO_1	G18	VCCO
1	VCCO_1	VCCO_1	L18	VCCO
1	VCCO_1	VCCO_1	L19	VCCO
1	VCCO_1	VCCO_1	J20	VCCO
1	VCCO_1	VCCO_1	C22	VCCO
1	VCCO_1	VCCO_1	G22	VCCO
1	VCCO_1	VCCO_1	E24	VCCO
1	VCCO_1	VCCO_1	C26	VCCO
2	IO	IO	J25	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C29	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C30	DCI
2	IO_L02N_2	IO_L02N_2	D27	I/O
2	IO_L02P_2	IO_L02P_2	D28	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	D29	VREF
2	IO_L03P_2	IO_L03P_2	D30	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
4	IO_L11P_4	IO_L11P_4	AE21	I/O
4	IO_L12N_4	IO_L12N_4	AH21	I/O
4	IO_L12P_4	IO_L12P_4	AJ21	I/O
4	IO_L13N_4	IO_L13N_4	AB21	I/O
4	IO_L13P_4	IO_L13P_4	AA20	I/O
4	IO_L14N_4	IO_L14N_4	AC20	I/O
4	IO_L14P_4	IO_L14P_4	AD20	I/O
4	IO_L15N_4	IO_L15N_4	AE20	I/O
4	IO_L15P_4	IO_L15P_4	AF20	I/O
4	IO_L16N_4	IO_L16N_4	AG20	I/O
4	IO_L16P_4	IO_L16P_4	AH20	I/O
4	IO_L17N_4	IO_L17N_4	AJ20	I/O
4	IO_L17P_4	IO_L17P_4	AK20	I/O
4	IO_L18N_4	IO_L18N_4	AA19	I/O
4	IO_L18P_4	IO_L18P_4	AB19	I/O
4	IO_L19N_4	IO_L19N_4	AC19	I/O
4	IO_L19P_4	IO_L19P_4	AD19	I/O
4	IO_L20N_4	IO_L20N_4	AE19	I/O
4	IO_L20P_4	IO_L20P_4	AF19	I/O
4	IO_L21N_4	IO_L21N_4	AG19	I/O
4	IO_L21P_4	IO_L21P_4	AH19	I/O
4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	AJ19	VREF
4	IO_L22P_4	IO_L22P_4	AK19	I/O
4	IO_L23N_4	IO_L23N_4	AB18	I/O
4	IO_L23P_4	IO_L23P_4	AC18	I/O
4	IO_L24N_4	IO_L24N_4	AE18	I/O
4	IO_L24P_4	IO_L24P_4	AF18	I/O
4	IO_L25N_4	IO_L25N_4	AJ18	I/O
4	IO_L25P_4	IO_L25P_4	AK18	I/O
4	IO_L26N_4	IO_L26N_4	AA17	I/O
4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	AB17	VREF
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	AD17	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	AE17	DUAL
4	IO_L28N_4	IO_L28N_4	AH17	I/O
4	IO_L28P_4	IO_L28P_4	AJ17	I/O
4	IO_L29N_4	IO_L29N_4	AB16	I/O
4	IO_L29P_4	IO_L29P_4	AC16	I/O
4	IO_L30N_4/D2	IO_L30N_4/D2	AD16	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	AE16	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	AG16	DUAL

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
6	IO_L05P_6	IO_L05P_6	AE5	I/O
6	IO_L06N_6	IO_L06N_6	AE3	I/O
6	IO_L06P_6	IO_L06P_6	AE2	I/O
6	IO_L07N_6	IO_L07N_6	AD4	I/O
6	IO_L07P_6	IO_L07P_6	AD3	I/O
6	IO_L08N_6	IO_L08N_6	AD2	I/O
6	IO_L08P_6	IO_L08P_6	AD1	I/O
6	IO_L09N_6/VREF_6	IO_L09N_6/VREF_6	AD6	VREF
6	IO_L09P_6	IO_L09P_6	AC7	I/O
6	IO_L10N_6	IO_L10N_6	AC6	I/O
6	IO_L10P_6	IO_L10P_6	AC5	I/O
6	IO_L11N_6	IO_L11N_6	AC4	I/O
6	IO_L11P_6	IO_L11P_6	AC3	I/O
6	IO_L13N_6	IO_L13N_6	AC2	I/O
6	IO_L13P_6/VREF_6	IO_L13P_6/VREF_6	AC1	VREF
6	IO_L14N_6	IO_L14N_6	AB5	I/O
6	IO_L14P_6	IO_L14P_6	AB4	I/O
6	IO_L15N_6	IO_L15N_6	AB2	I/O
6	IO_L15P_6	IO_L15P_6	AB1	I/O
6	IO_L16N_6	IO_L16N_6	AB8	I/O
6	IO_L16P_6	IO_L16P_6	AA9	I/O
6	IO_L17N_6	IO_L17N_6	AA7	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	AA6	VREF
6	IO_L19N_6	IO_L19N_6	AA3	I/O
6	IO_L19P_6	IO_L19P_6	AA2	I/O
6	IO_L20N_6	IO_L20N_6	AA10	I/O
6	IO_L20P_6	IO_L20P_6	Y10	I/O
6	IO_L21N_6	IO_L21N_6	Y8	I/O
6	IO_L21P_6	IO_L21P_6	Y7	I/O
6	IO_L22N_6	IO_L22N_6	Y6	I/O
6	IO_L22P_6	IO_L22P_6	Y5	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	Y2	VREF
6	IO_L24P_6	IO_L24P_6	Y1	I/O
6	N.C. (◆)	IO_L25N_6	W9	I/O
6	N.C. (◆)	IO_L25P_6	W8	I/O
6	IO_L26N_6	IO_L26N_6	W7	I/O
6	IO_L26P_6	IO_L26P_6	W6	I/O
6	IO_L27N_6	IO_L27N_6	W4	I/O
6	IO_L27P_6	IO_L27P_6	W3	I/O
6	IO_L28N_6	IO_L28N_6	W2	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
1	IO_L07N_1	IO_L07N_1	D27	I/O
1	IO_L07P_1	IO_L07P_1	E27	I/O
1	IO_L08N_1	IO_L08N_1	A27	I/O
1	IO_L08P_1	IO_L08P_1	B27	I/O
1	IO_L09N_1	IO_L09N_1	F26	I/O
1	IO_L09P_1	IO_L09P_1	G26	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	C26	VREF
1	IO_L10P_1	IO_L10P_1	D26	I/O
1	IO_L11N_1	IO_L11N_1	H25	I/O
1	IO_L11P_1	IO_L11P_1	J25	I/O
1	IO_L12N_1	IO_L12N_1	F25	I/O
1	IO_L12P_1	IO_L12P_1	G25	I/O
1	IO_L13N_1	IO_L13N_1	C25	I/O
1	IO_L13P_1	IO_L13P_1	D25	I/O
1	IO_L14N_1	IO_L14N_1	A25	I/O
1	IO_L14P_1	IO_L14P_1	B25	I/O
1	IO_L15N_1	IO_L15N_1	A24	I/O
1	IO_L15P_1	IO_L15P_1	B24	I/O
1	IO_L16N_1	IO_L16N_1	J23	I/O
1	IO_L16P_1	IO_L16P_1	K23	I/O
1	IO_L17N_1/VREF_1	IO_L17N_1/VREF_1	F23	VREF
1	IO_L17P_1	IO_L17P_1	G23	I/O
1	IO_L18N_1	IO_L18N_1	D23	I/O
1	IO_L18P_1	IO_L18P_1	E23	I/O
1	IO_L19N_1	IO_L19N_1	A23	I/O
1	IO_L19P_1	IO_L19P_1	B23	I/O
1	IO_L20N_1	IO_L20N_1	K22	I/O
1	IO_L20P_1	IO_L20P_1	L22	I/O
1	IO_L21N_1	IO_L21N_1	G22	I/O
1	IO_L21P_1	IO_L21P_1	H22	I/O
1	IO_L22N_1	IO_L22N_1	C22	I/O
1	IO_L22P_1	IO_L22P_1	D22	I/O
1	IO_L23N_1	IO_L23N_1	H21	I/O
1	IO_L23P_1	IO_L23P_1	J21	I/O
1	IO_L24N_1	IO_L24N_1	F21	I/O
1	IO_L24P_1	IO_L24P_1	G21	I/O
1	IO_L25N_1	IO_L25N_1	C21	I/O
1	IO_L25P_1	IO_L25P_1	D21	I/O
1	IO_L26N_1	IO_L26N_1	A21	I/O
1	IO_L26P_1	IO_L26P_1	B21	I/O

User I/Os by Bank

Note: The FG(G)1156 package is discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Table 111 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S4000 in the FG1156 package. Similarly, Table 112 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S5000 in the FG1156 package.

Table 111: **User I/Os Per Bank for XC3S4000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	90	79	0	2	7	2
	1	90	79	0	2	7	2
Right	2	88	80	0	2	6	0
	3	88	79	0	2	7	0
Bottom	4	90	73	6	2	7	2
	5	90	73	6	2	7	2
Left	6	88	79	0	2	7	0
	7	88	79	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

Table 112: **User I/Os Per Bank for XC3S5000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	100	89	0	2	7	2
	1	100	89	0	2	7	2
Right	2	96	87	0	2	7	0
	3	96	87	0	2	7	0
Bottom	4	100	83	6	2	7	2
	5	100	83	6	2	7	2
Left	6	96	87	0	2	7	0
	7	96	87	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

FG1156 Footprint

Top Left Corner of FG1156 Package (Top View)

XC3S4000 (712 max. user I/O)

621 **I/O:** Unrestricted, general-purpose user I/O

55 **VREF:** User I/O or input voltage reference for bank

73 **N.C.:** Unconnected pins for XC3S4000 (◆)

XC3S5000 (784 max. user I/O)

692 **I/O:** Unrestricted, general-purpose user I/O

56 **VREF:** User I/O or input voltage reference for bank

1 **N.C.:** Unconnected pins for XC3S5000 (■)

Bank 0

Bank 7

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	GND	GND	I/O L01P_0 VRN_0	I/O L02P_0	GND	I/O L05P_0 VREF_0	I/O L34P_0 ◆	I/O L36P_0	GND	I/O L38P_0	I/O L40P_0 ◆	I/O L15P_0	GND	I/O L22P_0	I/O L26P_0 VREF_0	GND	I/O L32P_0 GCLK6
B	GND	GND	I/O L01N_0 VRP_0	I/O L02N_0	I/O L03P_0	I/O L05N_0	I/O L34N_0 ◆	I/O L36N_0	I/O	I/O L38N_0	I/O L40N_0 ◆	I/O L15N_0	VCCO_0	I/O L22N_0	I/O L26N_0	I/O L28P_0	I/O L32N_0 GCLK7
C	I/O L01N_7 VRP_7	I/O L01P_7 VRN_7	GND	VCCO_0	I/O L03N_0	I/O L04P_0	I/O L33P_0 ◆	VCCO_0	I/O L08P_0	I/O L37P_0	GND	I/O L14P_0	I/O L17P_0	I/O L21P_0	I/O L25P_0	I/O L28N_0	I/O L31P_0 VREF_0
D	I/O L02N_7	I/O L02P_7	VCCO_7	PROG_B	IO VREF_0	I/O L04N_0	I/O L33N_0 ◆	I/O L35P_0	I/O L08N_0	I/O L37N_0	VCCO_0	I/O L14N_0	I/O L17N_0	I/O L21N_0	I/O L25N_0	VCCO_0	I/O L31N_0
E	GND	I/O L03N_7 VREF_7	I/O L03P_7	TDI	GND	VCCAUX	I/O L06P_0	I/O L35N_0	GND	IO VREF_0	VCCAUX	I/O L13P_0	GND	I/O L20P_0	VCCAUX	GND	I/O
F	I/O L05N_7	I/O L05P_7	I/O L04N_7	I/O L04P_7	VCCAUX	I/O	I/O L06N_0	I/O	I/O L07P_0	I/O L10P_0	I/O L39P_0 ◆	I/O L13N_0	VCCO_0	I/O L20N_0	I/O L24P_0	I/O L27P_0	I/O L30P_0
G	I/O	I/O	I/O L41N_7 ◆	I/O L41P_7 ◆	I/O L06N_7	I/O L06P_7	GND	VCCO_0	I/O L07N_0	I/O L10N_0	I/O L39N_0 ◆	I/O	I/O L16P_0	I/O L19P_0	I/O L24N_0	I/O L27N_0	I/O L30N_0
H	I/O L08N_7	I/O L08P_7	VCCO_7	I/O L10P_7 VREF_7	I/O L07N_7	I/O L07P_7	VCCO_7	I/O	I/O	I/O L09P_0	VCCO_0	I/O L12P_0	I/O L16N_0	I/O L19N_0	VCCO_0	VCCAUX	I/O L29P_0
J	GND	I/O L11N_7	I/O L11P_7	I/O L10N_7	GND	I/O L09N_7	I/O L09P_7	I/O L12P_7	I/O ◆	I/O L09N_0	I/O	I/O L12N_0	GND	IO VREF_0	I/O L23P_0	GND	I/O L29N_0
K	I/O L16N_7	I/O L16P_7 VREF_7	I/O L15N_7	I/O L15P_7	I/O L14N_7	I/O L14P_7	I/O L13N_7	I/O L13P_7	I/O L12N_7	GND	I/O ◆	I/O L11P_0	I/O	I/O L18P_0	I/O L23N_0	I/O	I/O
L	I/O L19N_7 VREF_7	I/O L19P_7	GND	VCCO_7	VCCAUX	I/O L44N_7 ◆	I/O L44P_7 ◆	VCCO_7	I/O L17N_7	I/O L17P_7	HSWAP_ EN	I/O L11N_0	I/O	I/O L18N_0	IO VREF_0	I/O	I/O
M	I/O L45N_7	I/O L45P_7	I/O L23N_7	I/O L23P_7	I/O L22N_7	I/O L22P_7	I/O L21N_7	I/O L21P_7	I/O L24P_7	I/O L20N_7	I/O L20P_7	VCCINT	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCINT
N	GND	VCCO_7	I/O L25N_7	I/O L25P_7	GND	VCCO_7	I/O L46N_7	I/O L46P_7	GND	I/O L24N_7	I/O L26P_7	VCCO_7	VCCINT	VCCINT	VCCINT	VCCINT	GND
P	I/O L49N_7	I/O L49P_7	I/O L29N_7	I/O L29P_7	I/O L28N_7	I/O L28P_7	I/O L27N_7	I/O L27P_7 VREF_7	I/O L47N_7 ◆	I/O L47P_7 ◆	I/O L26N_7	VCCO_7	VCCINT	GND	GND	GND	GND
R	I/O L32N_7	I/O L32P_7	I/O L31N_7	I/O L31P_7	VCCAUX	I/O L30N_7	I/O L30P_7	VCCO_7	I/O L33P_7	I/O L50N_7	I/O L50P_7	VCCO_7	VCCINT	GND	GND	GND	GND
T	GND	I/O L35N_7	I/O L35P_7	VCCO_7	GND	I/O L34N_7	I/O L34P_7	VCCAUX	GND	I/O L33N_7	I/O L51P_7 ◆	VCCO_7	VCCINT	GND	GND	GND	GND
U	I/O L40N_7 VREF_7	I/O L40P_7	I/O L39N_7	I/O L39P_7	I/O L38N_7	I/O L38P_7	I/O L37N_7	I/O L37P_7 VREF_7	I/O	I/O	I/O L51N_7 ◆	VCCINT	GND	GND	GND	GND	GND

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Figure 57: **FG1156 Package Footprint (Top View)**