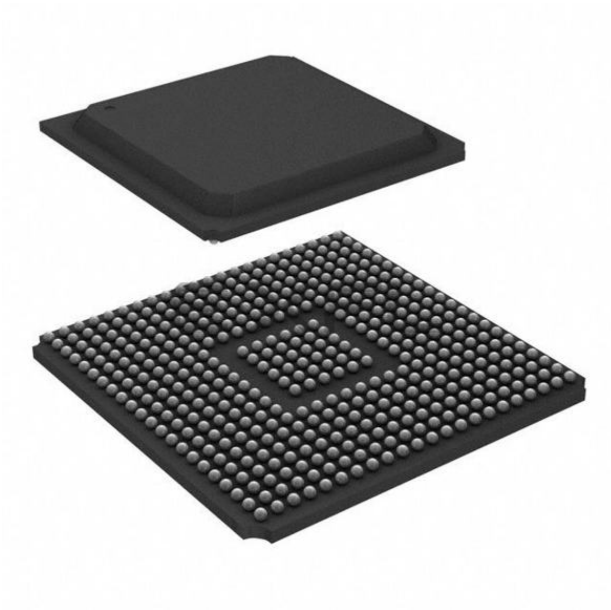

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Details	
Product Status	Active
Number of LABs/CLBs	3328
Number of Logic Elements/Cells	29952
Total RAM Bits	589824
Number of I/O	333
Number of Gates	1500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1500-4fg456i

Table 3 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

Table 3: **Spartan-3 Device I/O Chart**

Available User I/Os and Differential (Diff) I/O Pairs by Package Type																				
Package	**VQ100 VQG100**		**CP132[(1)] CPG132**		**TQ144 TQG144**		**PQ208 PQG208**		**FT256 FTG256**		**FG320 FGG320**		**FG456 FGG456**		**FG676 FGG676**		**FG900 FGG900**		**FG1156[(1)] FGG1156**	
Footprint (mm)	**16 x 16**		**8 x 8**		**22 x 22**		**30.6 x 30.6**		**17 x 17**		**19 x 19**		**23 x 23**		**27 x 27**		**31 x 31**		**35 x 35**	
Device	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**
XC3S50	63	29	89[(1)]	44[(1)]	97	46	124	56	–	–	–	–	–	–	–	–	–	–	–	–
XC3S200	63	29	–	–	97	46	141	62	173	76	–	–	–	–	–	–	–	–	–	–
XC3S400	–	–	–	–	97	46	141	62	173	76	221	100	264	116	–	–	–	–	–	–
XC3S1000	–	–	–	–	–	–	–	–	173	76	221	100	333	149	391	175	–	–	–	–
XC3S1500	–	–	–	–	–	–	–	–	–	–	221	100	333	149	487	221	–	–	–	–
XC3S2000	–	–	–	–	–	–	–	–	–	–	–	–	333	149	489	221	565	270	–	–
XC3S4000	–	–	–	–	–	–	–	–	–	–	–	–	–	–	489	221	633	300	712[(1)]	312[(1)]
XC3S5000	–	–	–	–	–	–	–	–	–	–	–	–	–	–	489	221	633	300	784[(1)]	344[(1)]

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.
2. All device options listed in a given package column are pin-compatible.
3. User = Single-ended user I/O pins. Diff = Differential I/O pairs.

Package Marking

Figure 2 shows the top marking for Spartan-3 FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3 FPGAs in BGA packages except the 132-ball chip-scale package (CP132 and CPG132). The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for Spartan-3 FPGAs in the CP132 and CPG132 packages.

The "5C" and "4I" part combinations may be dual marked as "5C/4I". Devices with the dual mark can be used as either -5C or -4I devices. Devices with a single mark are only guaranteed for the marked speed grade and temperature range. Some specifications vary according to mask revision. Mask revision E devices are errata-free. All shipments since 2006 have been mask revision E.

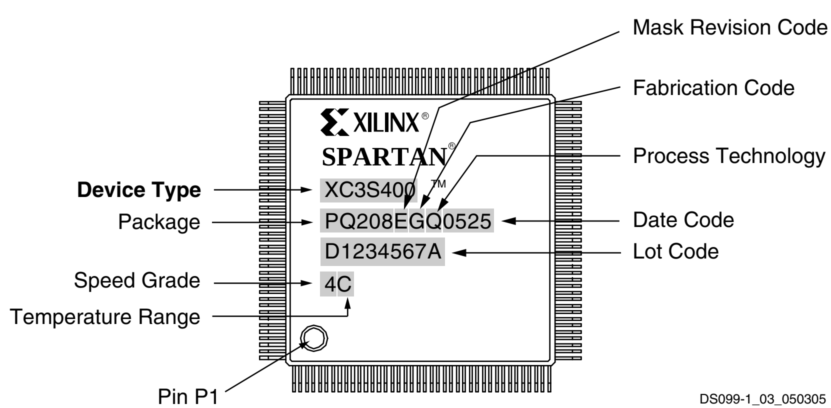


Figure 2: **Spartan-3 FPGA QFP Package Marking Example for Part Number XC3S400-4PQ208C**

Each BUFGMUX element, shown in Figure 24, is a 2-to-1 multiplexer that can receive signals from any of the four following sources:

- One of the four Global Clock inputs on the same side of the die—top or bottom—as the BUFGMUX element in use.
- Any of four nearby horizontal Double lines.
- Any of four outputs from the DCM in the right-hand quadrant that is on the same side of the die as the BUFGMUX element in use.
- Any of four outputs from the DCM in the left-hand quadrant that is on the same side of the die as the BUFGMUX element in use.

The multiplexer select line, S, chooses which of the two inputs, I0 or I1, drives the BUFGMUX's output signal, O, as described in Table 25. The switching from one clock to the other is glitchless, and done in such a way that the output High and Low times are never shorter than the shortest High or Low time of either input clock.

Table 25: **BUFGMUX Select Mechanism**

S Input	O Output
0	I0 Input
1	I1 Input

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

The BUFG clock buffer primitive drives a single clock signal onto the clock network and is essentially the same element as a BUFGMUX, just without the clock select mechanism. Similarly, the BUFGCE primitive creates an enabled clock buffer using the BUFGMUX select mechanism.

Each BUFGMUX buffers incoming clock signals to two possible destinations:

- The vertical spine belonging to the same side of the die—top or bottom—as the BUFGMUX element in use. The two spines—top and bottom—each comprise four vertical clock lines, each running from one of the BUFGMUX elements on the same side towards the center of the die. At the center of the die, clock signals reach the eight-line horizontal spine, which spans the width of the die. In turn, the horizontal spine branches out into a subsidiary clock interconnect that accesses the CLBs.
- The clock input of either DCM on the same side of the die—top or bottom—as the BUFGMUX element in use.

Use either a BUFGMUX element or a BUFG (Global Clock Buffer) element to place a Global input in the design. For the purpose of minimizing the dynamic power dissipation of the clock network, the Xilinx development software automatically disables all clock line segments that a design does not use.

A global clock line ideally drives clock inputs on the various clocked elements within the FPGA, such as CLB or IOB flip-flops or block RAMs. A global clock line also optionally drives combinatorial inputs. However, doing so provides additional loading on the clock line that might also affect clock jitter. Ideally, drive combinatorial inputs using the signal that also drives the input to the BUFGMUX or BUFG element.

For more details, refer to the chapter entitled "Using Global Clock Resources" in UG331.

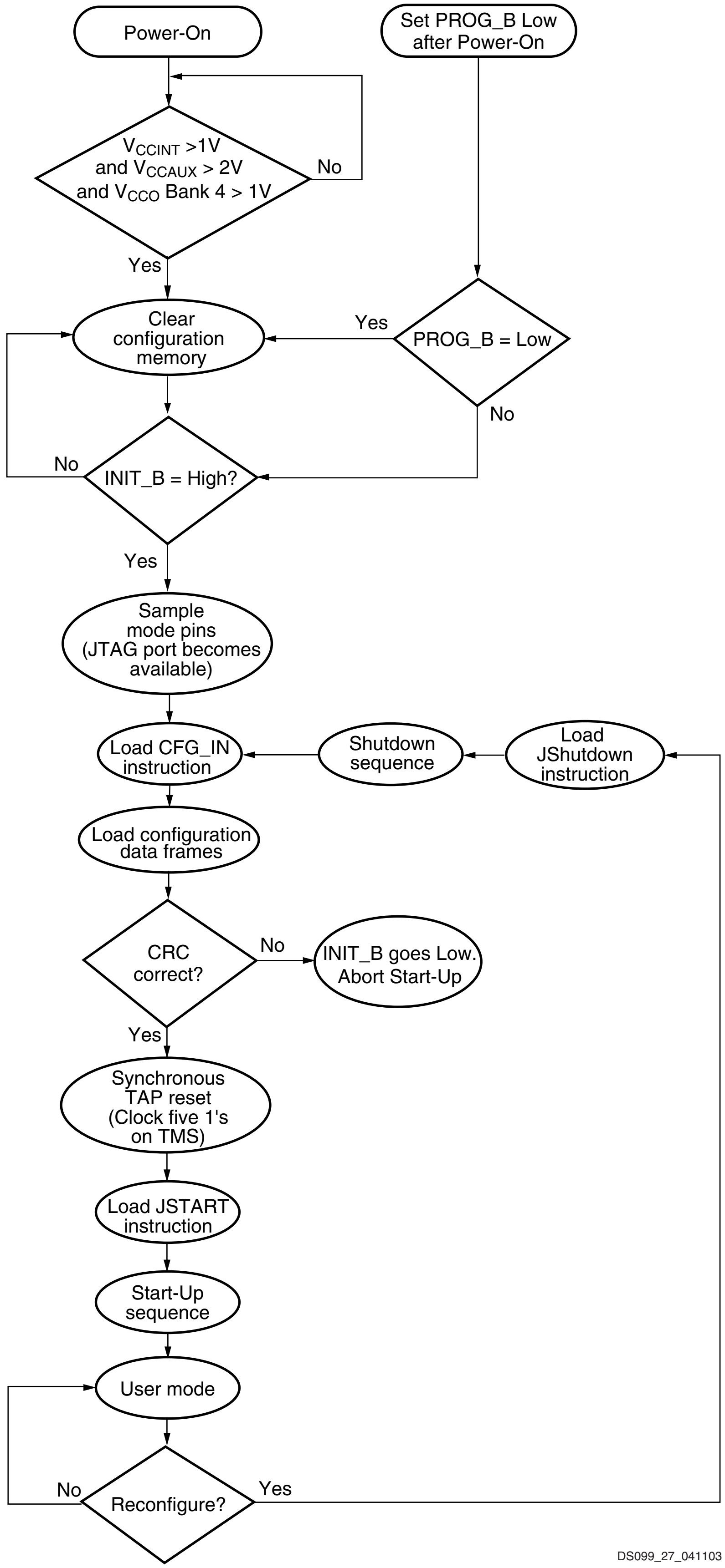


Figure 30: **Boundary-Scan Configuration Flow Diagram**

Initial Spartan-3 FPGA mask revisions have a limit on how fast the V_{CCO} supply can ramp. The minimum allowed V_{CCO} ramp rate appears as T_{CCO} in Table 30, page 60. The minimum rate is affected by the package inductance. Consequently, the ball grid array and chip-scale packages (CP132, FT256, FG456, FG676, and FG900) allow a faster ramp rate than the quad-flat packages (VQ100, TQ144, and PQ208).

Configuration Data Retention, Brown-Out

The FPGA's configuration data is stored in robust CMOS configuration latches. The data in these latches is retained even when the voltages drop to the minimum levels necessary to preserve RAM contents. This is specified in Table 31, page 60.

If, after configuration, the V_{CCAUX} or V_{CCINT} supply drops below its data retention voltage, clear the current device configuration using one of the following methods:

- Force the V_{CCAUX} or V_{CCINT} supply voltage below the minimum Power On Reset (POR) voltage threshold Table 29, page 59).
- Assert PROG_B Low.

The POR circuit does not monitor the VCCO_4 supply after configuration. Consequently, dropping the VCCO_4 voltage does not reset the device by triggering a Power-On Reset (POR) event.

No Internal Charge Pumps or Free-Running Oscillators

Some system applications are sensitive to sources of analog noise. Spartan-3 FPGA circuitry is fully static and does not employ internal charge pumps.

The CCLK configuration clock is active during the FPGA configuration process. After configuration completes, the CCLK oscillator is automatically disabled unless the Bitstream Generator (BitGen) option ***Persist=Yes***. See Module 4: Table 80, page 125.

Spartan-3 FPGAs optionally support a featured called Digitally Controlled Impedance (DCI). When used in an application, the DCI logic uses an internal oscillator. The DCI logic is only enabled if the FPGA application specifies an I/O standard that requires DCI (LVDCI_33, LVDCI_25, etc.). If DCI is not used, the associated internal oscillator is also disabled.

In summary, unless an application uses the ***Persist=Yes*** option or specifies a DCI I/O standard, an FPGA with no external switching remains fully static.

Table 36: **DC Characteristics of User I/Os Using Single-Ended Standards**

Signal Standard (IOSTANDARD) and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
GTL		32	–	0.4	–
GTL_DCI		Note 3	Note 3		
GTLP		36	–	0.6	–
GTLP_DCI		Note 3	Note 3		
HSLVDCI_15		Note 3	Note 3	0.4	V_{CCO} – 0.4
HSLVDCI_18					
HSLVDCI_25					
HSLVDCI_33					
HSTL_I		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI		Note 3	Note 3		
HSTL_III		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI		Note 3	Note 3		
HSTL_I_18		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI_18		Note 3	Note 3		
HSTL_II_18		16	–16	0.4	V_{CCO} – 0.4
HSTL_II_DCI_18		Note 3	Note 3		
HSTL_III_18		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI_18		Note 3	Note 3		
LVCMOS12(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
LVCMOS15(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
LVDCI_15, LVDCI_DV2_15		Note 3	Note 3		
LVCMOS18(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
LVDCI_18, LVDCI_DV2_18		Note 3	Note 3		
LVCMOS25(4,5)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_25, LVDCI_DV2_25		Note 3	Note 3		

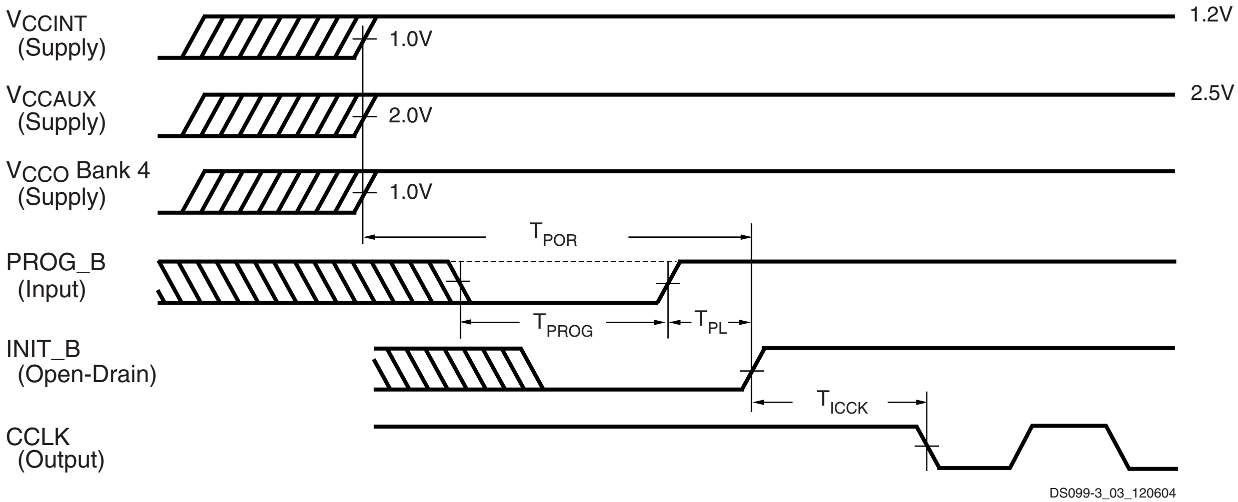
Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below Speed Grade -5	-4	Units
HSLVDCI_25			0.27	0.31	ns
HSLVDCI_33			0.28	0.32	ns
HSTL_I			0.60	0.69	ns
HSTL_I_DCI			0.59	0.68	ns
HSTL_III			0.19	0.22	ns
HSTL_III_DCI			0.20	0.23	ns
HSTL_I_18			0.18	0.21	ns
HSTL_I_DCI_18			0.17	0.19	ns
HSTL_II_18			–0.02	–0.01	ns
HSTL_II_DCI_18			0.75	0.86	ns
HSTL_III_18			0.28	0.32	ns
HSTL_III_DCI_18			0.28	0.32	ns
LVCMOS12	Slow	2 mA	7.60	8.73	ns
		4 mA	7.42	8.53	ns
		6 mA	6.67	7.67	ns
	Fast	2 mA	3.16	3.63	ns
		4 mA	2.70	3.10	ns
		6 mA	2.41	2.77	ns
LVCMOS15	Slow	2 mA	4.55	5.23	ns
		4 mA	3.76	4.32	ns
		6 mA	3.57	4.11	ns
		8 mA	3.55	4.09	ns
		12 mA	3.00	3.45	ns
	Fast	2 mA	3.11	3.57	ns
		4 mA	1.71	1.96	ns
		6 mA	1.44	1.66	ns
		8 mA	1.26	1.44	ns
		12 mA	1.11	1.27	ns
LVDCI_15			1.51	1.74	ns
LVDCI_DV2_15			1.32	1.52	ns

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below Speed Grade -5	-4	Units
LVCMOS18	Slow	2 mA	5.49	6.31	ns
		4 mA	3.45	3.97	ns
		6 mA	2.84	3.26	ns
		8 mA	2.62	3.01	ns
		12 mA	2.11	2.43	ns
		16 mA	2.07	2.38	ns
	Fast	2 mA	2.50	2.88	ns
		4 mA	1.15	1.32	ns
		6 mA	0.96	1.10	ns
		8 mA	0.87	1.01	ns
		12 mA	0.79	0.91	ns
		16 mA	0.76	0.87	ns
LVDCI_18			0.81	0.94	ns
LVDCI_DV2_18			0.67	0.77	ns
LVCMOS25	Slow	2 mA	6.43	7.39	ns
		4 mA	4.15	4.77	ns
		6 mA	3.38	3.89	ns
		8 mA	2.99	3.44	ns
		12 mA	2.53	2.91	ns
		16 mA	2.50	2.87	ns
		24 mA	2.22	2.55	ns
	Fast	2 mA	3.27	3.76	ns
		4 mA	1.87	2.15	ns
		6 mA	0.32	0.37	ns
		8 mA	0.19	0.22	ns
		12 mA	0	0	ns
		16 mA	–0.02	–0.01	ns
		24 mA	–0.04	–0.02	ns
LVDCI_25			0.27	0.31	ns
LVDCI_DV2_25			0.16	0.19	ns

Configuration and JTAG Timing



Notes:
1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 36: **Waveforms for Power-On and the Beginning of Configuration**

Table 65: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}[(2)]	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 4 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XC3S50	–	5	ms
		XC3S200	–	5	ms
		XC3S400	–	5	ms
		XC3S1000	–	5	ms
		XC3S1500	–	7	ms
		XC3S2000	–	7	ms
		XC3S4000	–	7	ms
		XC3S5000	–	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.3	–	µs
T_{PL}[(2)]	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S50	–	2	ms
		XC3S200	–	2	ms
		XC3S400	–	2	ms
		XC3S1000	–	2	ms
		XC3S1500	–	3	ms
		XC3S2000	–	3	ms
		XC3S4000	–	3	ms
		XC3S5000	–	3	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	–	ns
T_{ICCK}[(3)]	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.25	4.0	µs

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 32. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only for the Master Serial and Master Parallel modes.

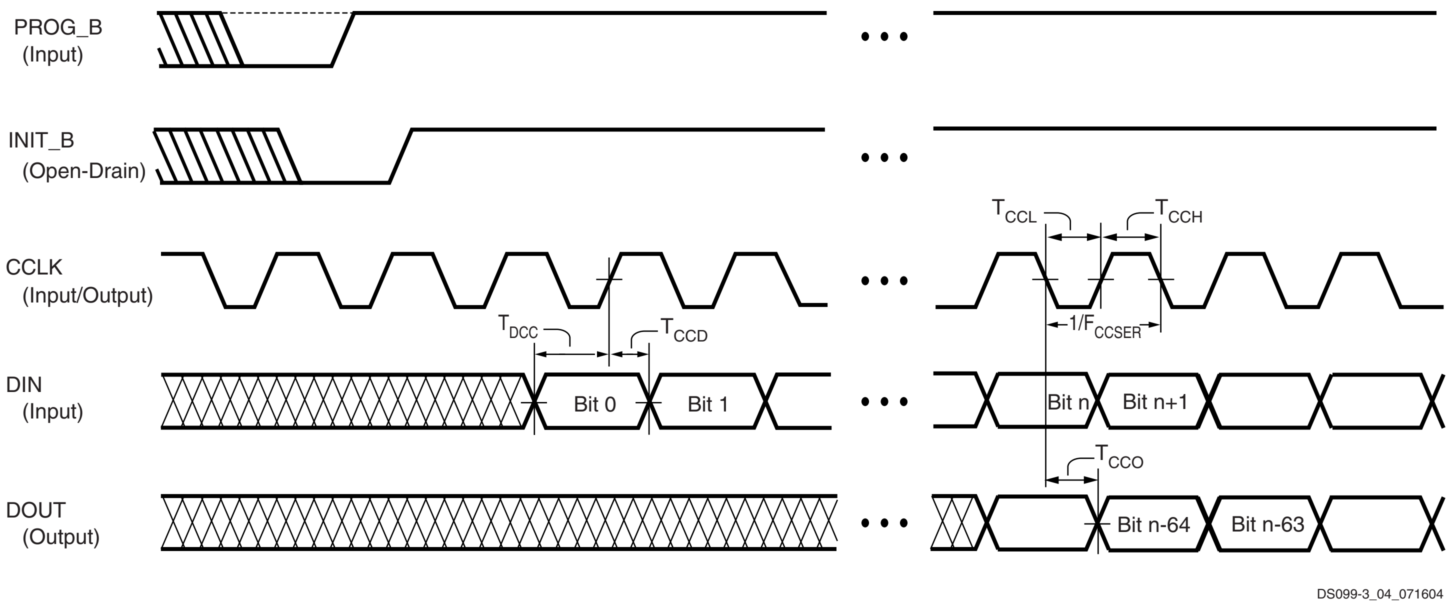


Figure 37: **Waveforms for Master and Slave Serial Configuration**

Table 66: **Timing for the Master and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	12.0	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		Both	10.0	–	ns
Hold Times						
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		Both	0	–	ns
Clock Timing						
T_{CCH}	CCLK input pin High pulse width		Slave	5.0	∞	ns
T_{CCL}	CCLK input pin Low pulse width			5.0	∞	ns
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression		0	66[2]	MHz
		With bitstream compression		0	20	MHz
		During STARTUP phase		0	50	MHz
ΔF_{CCSER}	Variation from the CCLK output frequency set using the ConfigRate BitGen option		Master	–50%	+50%	–

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Revision History

Date	Version	Description
04/11/03	1.0	Initial Xilinx release.
07/11/03	1.1	Extended Absolute Maximum Rating for junction temperature in Table 28. Added numbers for typical quiescent supply current (Table 34) and DLL timing.
02/06/04	1.2	Revised V_{IN} maximum rating (Table 28). Added power-on requirements (Table 30), leakage current number (Table 33), and differential output voltage levels (Table 38) for Rev. 0. Published new quiescent current numbers (Table 34). Updated pull-up and pull-down resistor strengths (Table 33). Added LVDCI_DV2 and LVPECL standards (Table 37 and Table 38). Changed CCLK setup time (Table 66 and Table 67).
03/04/04	1.3	Added timing numbers from v1.29 speed files as well as DCM timing (Table 58 through Table 63).
08/24/04	1.4	Added reference to errata documents on page 49. Clarified Absolute Maximum Ratings and added ESD information (Table 28). Explained V_{CCO} ramp time measurement (Table 30). Clarified I_L specification (Table 33). Updated quiescent current numbers and added information on power-on and surplus current (Table 34). Adjusted V_{REF} range for HSTL_III and HSTL_I_18 and changed V_{IH} min for LVCMOS12 (Table 35). Added note limiting V_{TT} range for SSTL2_II signal standards (Table 36). Calculated V_{OH} and V_{OL} levels for differential standards (Table 38). Updated Switching Characteristics with speed file v1.32 (Table 40 through Table 48 and Table 51 through Table 56). Corrected IOB test conditions (Table 41). Updated DCM timing with latest characterization data (Table 58 through Table 62). Improved DCM CLKIN pulse width specification (Table 58). Recommended use of Virtex-II FPGA Jitter calculator (Table 61). Improved DCM PSCLK pulse width specification (Table 62). Changed Phase Shifter lock time parameter (Table 63). Because the BitGen option Centered_x#_y# is not necessary for Variable Phase Shift mode, removed BitGen command table and referring text. Adjusted maximum CCLK frequency for the slave serial and parallel configuration modes (Table 66). Inverted CCLK waveform (Figure 37). Adjusted JTAG setup times (Table 68).
12/17/04	1.5	Updated timing parameters to match v1.35 speed file. Improved V_{CCO} ramp time specification (Table 30). Added a note limiting the rate of change of V_{CCAUX} (Table 32). Added typical quiescent current values for the XC3S2000, XC3S4000, and XC3S5000 (Table 34). Increased I_{OH} and I_{OL} for SSTL2-I and SSTL2-II standards (Table 36). Added SSO guidelines for the VQ, TQ, and PQ packages as well as edited SSO guidelines for the FT and FG packages (Table 50). Added maximum CCLK frequencies for configuration using compressed bitstreams (Table 66 and Table 67). Added specifications for the HSLVDCI standards (Table 35, Table 36, Table 44, Table 47, Table 48, and Table 50).
08/19/05	1.6	Updated timing parameters to match v1.37 speed file. All Spartan-3 FPGA part types, except XC3S5000, promoted to Production status. Removed V_{CCO} ramp rate restriction from all mask revision 'E' and later devices (Table 30). Added equivalent resistance values for internal pull-up and pull-down resistors (Table 33). Added worst-case quiescent current values for XC3S2000, XC3S4000, XC3S5000 (Table 34). Added industrial temperature range specification and improved typical quiescent current values (Table 34). Improved the DLL minimum clock input frequency specification from 24 MHz down to 18 MHz (Table 58). Improved the DFS minimum and maximum clock output frequency specifications (Table 60, Table 61). Added new miscellaneous DCM specifications (Table 64), primarily affecting Industrial temperature range applications. Updated Simultaneously Switching Output Guidelines and Table 50 for QFP packages. Added information on SSTL18_II I/O standard and timing to support DDR2 SDRAM interfaces. Added differential (or complementary single-ended) DIFF_HSTL_II_18 and DIFF_SSTL2_II I/O standards, including DCI terminated versions. Added electro-static discharge (ESD) data for the XC3S2000 and larger FPGAs (Table 28). Added link to Spartan-3 FPGA errata notices and how to receive automatic notifications of data sheet or errata changes.
04/03/06	2.0	Upgraded Module 3, removing Preliminary status. Moved XC3S5000 to Production status in Table 39. Finalized I/O timing on XC3S5000 for v1.38 speed files. Added minimum timing values for various logic and I/O paths. Corrected labels for R_{PU} and R_{PD} and updated R_{PD} conditions for in Table 33. Added final mask revision 'E' specifications for LVDS_25, RSDS_25, LVDSEXT_25 differential outputs to Table 38. Added BLVDS termination requirements to Figure 34. Improved recommended Simultaneous Switching Outputs (SSOs) limits in Table 50 for quad-flat packaged based on silicon testing using devices soldered on a printed circuit board. Updated Note 2 in Table 63. Updated Note 6 in Table 30. Added INIT_B minimum pulse width specification, T_{INIT}, to Table 65.
04/26/06	2.1	Updated document links.

Table 71: **Dual-Purpose Pins Used in Master or Slave Serial Mode**

Pin Name	Direction	Description
DIN	Input	**Serial Data Input:** During the Master or Slave Serial configuration modes, DIN is the serial configuration data input, and all data is synchronized to the rising CCLK edge. After configuration, this pin is available as a user I/O. This signal is located in Bank 4 and its output voltage determined by VCCO_4. The BitGen option ***Persist*** permits this pin to retain its configuration function in the User mode.
DOUT	Output	**Serial Data Output:** In a multi-FPGA design where all the FPGAs use serial mode, connect the DOUT output of one FPGA—in either Master or Slave Serial mode—to the DIN input of the next FPGA—in Slave Serial mode—so that configuration data passes from one to the next, in daisy-chain fashion. This “daisy chain” permits sequential configuration of multiple FPGAs. This signal is located in Bank 4 and its output voltage determined by VCCO_4. The BitGen option ***Persist*** permits this pin to retain its configuration function in the User mode.
INIT_B	Bidirectional (open-drain)	**Initializing Configuration Memory/Configuration Error:** Just after power is applied, the FPGA produces a Low-to-High transition on this pin indicating that initialization (*i.e.*, clearing) of the configuration memory has finished. Before entering the User mode, this pin functions as an open-drain output, which requires a pull-up resistor in order to produce a High logic level. In a multi-FPGA design, tie (wire AND) the INIT_B pins from all FPGAs together so that the common node transitions High only after all of the FPGAs have been successfully initialized. Externally holding this pin Low beyond the initialization phase delays the start of configuration. This action stalls the FPGA at the configuration step just before the mode select pins are sampled. During configuration, the FPGA indicates the occurrence of a data (i.e., CRC) error by asserting INIT_B Low. This signal is located in Bank 4 and its output voltage determined by VCCO_4. The BitGen option ***Persist*** permits this pin to retain its configuration function in the User mode.

	I/O Bank 4 (VCCO_4)				*I/O Bank 5 (VCCO_5)*			
	High Nibble				*Low Nibble*			
Configuration Data Byte	**D0**	**D1**	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**
0xFC =	1	1	1	1	1	1	0	0
	(MSB)							***(LSB)***

Figure 41: **Configuration Data Byte Mapping to D0-D7 Bits**

Parallel Configuration Modes (SelectMAP)

This section describes the dual-purpose configuration pins used during the Master and Slave Parallel configuration modes, sometimes also called the SelectMAP modes. In both Master and Slave Parallel configuration modes, D0-D7 form the byte-wide configuration data input. See Table 75 for Mode Select pin settings required for Parallel modes.

As shown in Figure 41, D0 is the most-significant bit while D7 is the least-significant bit. Bits D0-D3 form the high nibble of the byte and bits D4-D7 form the low nibble.

In the Parallel configuration modes, both the VCCO_4 and VCCO_5 voltage supplies are required and must both equal the voltage of the attached configuration device, typically either 2.5V or 3.3V.

Assert Low both the chip-select pin, CS_B, and the read/write control pin, RDWR_B, to write the configuration data byte presented on the D0-D7 pins to the FPGA on a rising-edge of the configuration clock, CCLK. The order of CS_B and RDWR_B does not matter, although RDWR_B must be asserted throughout the configuration process. If RDWR_B is de-asserted during configuration, the FPGA aborts the configuration operation.

After configuration, these pins are available as general-purpose user I/O. However, the SelectMAP configuration interface is optionally available for debugging and dynamic reconfiguration. To use these SelectMAP pins after configuration, set the Persist bitstream generation option.

The Readback debugging option, for example, requires the Persist bitstream generation option. During Readback mode, assert CS_B Low, along with RDWR_B High, to read a configuration data byte from the FPGA to the D0-D7 bus on a rising CCLK edge. During Readback mode, D0-D7 are output pins.

In all the cases, the configuration data and control signals are synchronized to the rising edge of the CCLK clock signal.

Table 89: **CP132 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	CP132 Ball	Type
2	IO_L24P_2	G13	I/O
2	IO_L40N_2	G14	I/O
2	IO_L40P_2/VREF_2	H12	VREF
3	IO_L01N_3/VRP_3	N13	DCI
3	IO_L01P_3/VRN_3	N14	DCI
3	IO_L20N_3	L12	I/O
3	IO_L20P_3	M14	I/O
3	IO_L22N_3	L14	I/O
3	IO_L22P_3	L13	I/O
3	IO_L23N_3	K13	I/O
3	IO_L23P_3/VREF_3	K12	VREF
3	IO_L24N_3	J12	I/O
3	IO_L24P_3	K14	I/O
3	IO_L40N_3/VREF_3	H14	VREF
3	IO_L40P_3	J13	I/O
4	IO/VREF_4	N12	VREF
4	IO_L01N_4/VRP_4	P12	DCI
4	IO_L01P_4/VRN_4	M11	DCI
4	IO_L27N_4/DIN/D0	M10	DUAL
4	IO_L27P_4/D1	N10	DUAL
4	IO_L30N_4/D2	N9	DUAL
4	IO_L30P_4/D3	P9	DUAL
4	IO_L31N_4/INIT_B	M8	DUAL
4	IO_L31P_4/DOUT/BUSY	N8	DUAL
4	IO_L32N_4/GCLK1	P8	GCLK
4	IO_L32P_4/GCLK0	M7	GCLK
5	IO_L01N_5/RDWR_B	P2	DUAL
5	IO_L01P_5/CS_B	N2	DUAL
5	IO_L27N_5/VREF_5	M4	VREF
5	IO_L27P_5	P3	I/O
5	IO_L28N_5/D6	P4	DUAL
5	IO_L28P_5/D7	N4	DUAL
5	IO_L31N_5/D4	M6	DUAL
5	IO_L31P_5/D5	P5	DUAL
5	IO_L32N_5/GCLK3	P7	GCLK
5	IO_L32P_5/GCLK2	P6	GCLK
6	IO_L01N_6/VRP_6	L3	DCI
6	IO_L01P_6/VRN_6	M1	DCI
6	IO_L20N_6	K3	I/O
6	IO_L20P_6	K2	I/O

User I/Os by Bank

Table 92 indicates how the available user-I/O pins are distributed between the eight I/O banks on the TQ144 package.

Table 92: **User I/Os Per Bank in TQ144 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	10	5	0	2	1	2
	1	9	4	0	2	1	2
Right	2	14	10	0	2	2	0
	3	15	11	0	2	2	0
Bottom	4	11	0	6	2	1	2
	5	9	0	6	0	1	2
Left	6	14	10	0	2	2	0
	7	15	11	0	2	2	0

PQ208: 208-lead Plastic Quad Flat Pack

The 208-lead plastic quad flat package, PQ208, supports three different Spartan-3 devices, including the XC3S50, the XC3S200, and the XC3S400. The footprints for the XC3S200 and XC3S400 are identical, as shown in Table 93 and Figure 47. The XC3S50, however, has fewer I/O pins resulting in 17 unconnected pins on the PQ208 package, labeled as "N.C." In Table 93 and Figure 47, these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in Table 93 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S50 pinout and the pinout for the XC3S200 and XC3S400, then that difference is highlighted in Table 93. If the table entry is shaded grey, then there is an unconnected pin on the XC3S50 that maps to a user-I/O pin on the XC3S200 and XC3S400. If the table entry is shaded tan, then the unconnected pin on the XC3S50 maps to a VREF-type pin on the XC3S200 and XC3S400. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S50 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S50 device to an XC3S200 or XC3S400 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip

Pinout Table

Table 93: **PQ208 Package Pinout**

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
0	IO	IO	P189	I/O
0	IO	IO	P197	I/O
0	N.C. (◆)	IO/VREF_0	P200	VREF
0	IO/VREF_0	IO/VREF_0	P205	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	P204	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	P203	DCI
0	IO_L25N_0	IO_L25N_0	P199	I/O
0	IO_L25P_0	IO_L25P_0	P198	I/O
0	IO_L27N_0	IO_L27N_0	P196	I/O
0	IO_L27P_0	IO_L27P_0	P194	I/O
0	IO_L30N_0	IO_L30N_0	P191	I/O
0	IO_L30P_0	IO_L30P_0	P190	I/O
0	IO_L31N_0	IO_L31N_0	P187	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	P185	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	P184	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	P183	GCLK
0	VCCO_0	VCCO_0	P188	VCCO
0	VCCO_0	VCCO_0	P201	VCCO
1	IO	IO	P167	I/O
1	IO	IO	P175	I/O
1	IO	IO	P182	I/O
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	P162	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	P161	DCI

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
N/A	GND	J3	GND
N/A	GND	J8	GND
N/A	GND	K11	GND
N/A	GND	K16	GND
N/A	GND	K3	GND
N/A	GND	K8	GND
N/A	GND	L10	GND
N/A	GND	L11	GND
N/A	GND	L8	GND
N/A	GND	L9	GND
N/A	GND	M12	GND
N/A	GND	M7	GND
N/A	GND	N1	GND
N/A	GND	N18	GND
N/A	GND	T10	GND
N/A	GND	T9	GND
N/A	GND	U17	GND
N/A	GND	U2	GND
N/A	GND	V1	GND
N/A	GND	V13	GND
N/A	GND	V18	GND
N/A	GND	V6	GND
N/A	VCCAUX	B12	VCCAUX
N/A	VCCAUX	B7	VCCAUX
N/A	VCCAUX	G17	VCCAUX
N/A	VCCAUX	G2	VCCAUX
N/A	VCCAUX	M17	VCCAUX
N/A	VCCAUX	M2	VCCAUX
N/A	VCCAUX	U12	VCCAUX
N/A	VCCAUX	U7	VCCAUX
N/A	VCCINT	F12	VCCINT
N/A	VCCINT	F13	VCCINT
N/A	VCCINT	F6	VCCINT
N/A	VCCINT	F7	VCCINT
N/A	VCCINT	G13	VCCINT
N/A	VCCINT	G6	VCCINT
N/A	VCCINT	M13	VCCINT
N/A	VCCINT	M6	VCCINT
N/A	VCCINT	N12	VCCINT
N/A	VCCINT	N13	VCCINT

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
1	IO_L15P_1	IO_L15P_1	E17	I/O
1	IO_L16N_1	IO_L16N_1	B17	I/O
1	IO_L16P_1	IO_L16P_1	C17	I/O
1	N.C. (◆)	IO_L19N_1	C16	I/O
1	N.C. (◆)	IO_L19P_1	D16	I/O
1	N.C. (◆)	IO_L22N_1	A16	I/O
1	N.C. (◆)	IO_L22P_1	B16	I/O
1	IO_L24N_1	IO_L24N_1	D15	I/O
1	IO_L24P_1	IO_L24P_1	E15	I/O
1	IO_L25N_1	IO_L25N_1	B15	I/O
1	IO_L25P_1	IO_L25P_1	A15	I/O
1	IO_L27N_1	IO_L27N_1	D14	I/O
1	IO_L27P_1	IO_L27P_1	E14	I/O
1	IO_L28N_1	IO_L28N_1	A14	I/O
1	IO_L28P_1	IO_L28P_1	B14	I/O
1	IO_L29N_1	IO_L29N_1	C13	I/O
1	IO_L29P_1	IO_L29P_1	D13	I/O
1	IO_L30N_1	IO_L30N_1	A13	I/O
1	IO_L30P_1	IO_L30P_1	B13	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D12	VREF
1	IO_L31P_1	IO_L31P_1	E12	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B12	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C12	GCLK
1	VCCO_1	VCCO_1	C15	VCCO
1	VCCO_1	VCCO_1	F15	VCCO
1	VCCO_1	VCCO_1	G12	VCCO
1	VCCO_1	VCCO_1	G13	VCCO
1	VCCO_1	VCCO_1	G14	VCCO
2	IO	IO	C22	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C20	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C21	DCI
2	IO_L16N_2	IO_L16N_2	D20	I/O
2	IO_L16P_2	IO_L16P_2	D19	I/O
2	IO_L17N_2	IO_L17N_2	D21	I/O
2	IO_L17P_2/VREF_2	IO_L17P_2/VREF_2	D22	VREF
2	IO_L19N_2	IO_L19N_2	E18	I/O
2	IO_L19P_2	IO_L19P_2	F18	I/O
2	IO_L20N_2	IO_L20N_2	E19	I/O
2	IO_L20P_2	IO_L20P_2	E20	I/O
2	IO_L21N_2	IO_L21N_2	E21	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
0	IO_L09N_0	IO_L09N_0	IO_L09N_0	IO_L09N_0	IO_L09N_0	E7	I/O
0	IO_L09P_0	IO_L09P_0	IO_L09P_0	IO_L09P_0	IO_L09P_0	D7	I/O
0	IO_L10N_0	IO_L10N_0	IO_L10N_0	IO_L10N_0	IO_L10N_0	B7	I/O
0	IO_L10P_0	IO_L10P_0	IO_L10P_0	IO_L10P_0	IO_L10P_0	A7	I/O
0	N.C. (◆)	IO_L11N_0	IO_L11N_0	IO_L11N_0	IO_L11N_0	G8	I/O
0	N.C. (◆)	IO_L11P_0	IO_L11P_0	IO_L11P_0	IO_L11P_0	F8	I/O
0	N.C. (◆)	IO_L12N_0	IO_L12N_0	IO_L12N_0	IO[(3)]	E8	I/O
0	N.C. (◆)	IO_L12P_0	IO_L12P_0	IO_L12P_0	IO[(3)]	D8	I/O
0	IO_L15N_0	IO_L15N_0	IO_L15N_0	IO_L15N_0	IO_L13P_0[(3)]	B8	I/O
0	IO_L15P_0	IO_L15P_0	IO_L15P_0	IO_L15P_0	IO[(3)]	A8	I/O
0	IO_L16N_0	IO_L16N_0	IO_L16N_0	IO_L16N_0	IO_L16N_0	G9	I/O
0	IO_L16P_0	IO_L16P_0	IO_L16P_0	IO_L16P_0	IO_L16P_0	F9	I/O
0	N.C. (◆)	IO_L17N_0	IO_L17N_0	IO_L17N_0	IO_L17N_0	E9	I/O
0	N.C. (◆)	IO_L17P_0	IO_L17P_0	IO_L17P_0	IO_L17P_0	D9	I/O
0	N.C. (◆)	IO_L18N_0	IO_L18N_0	IO_L18N_0	IO_L18N_0	C9	I/O
0	N.C. (◆)	IO_L18P_0	IO_L18P_0	IO_L18P_0	IO_L18P_0	B9	I/O
0	IO_L19N_0	IO_L19N_0	IO_L19N_0	IO_L19N_0	IO_L19N_0	F10	I/O
0	IO_L19P_0	IO_L19P_0	IO_L19P_0	IO_L19P_0	IO_L19P_0	E10	I/O
0	IO_L22N_0	IO_L22N_0	IO_L22N_0	IO_L22N_0	IO_L22N_0	D10	I/O
0	IO_L22P_0	IO_L22P_0	IO_L22P_0	IO_L22P_0	IO_L22P_0	C10	I/O
0	N.C. (◆)	IO_L23N_0	IO_L23N_0	IO_L23N_0	IO_L23N_0	B10	I/O
0	N.C. (◆)	IO_L23P_0	IO_L23P_0	IO_L23P_0	IO_L23P_0	A10	I/O
0	IO_L24N_0	IO_L24N_0	IO_L24N_0	IO_L24N_0	IO_L24N_0	G11	I/O
0	IO_L24P_0	IO_L24P_0	IO_L24P_0	IO_L24P_0	IO_L24P_0	F11	I/O
0	IO_L25N_0	IO_L25N_0	IO_L25N_0	IO_L25N_0	IO_L25N_0	E11	I/O
0	IO_L25P_0	IO_L25P_0	IO_L25P_0	IO_L25P_0	IO_L25P_0	D11	I/O
0	N.C. (◆)	IO_L26N_0	IO_L26N_0	IO_L26N_0	IO_L26N_0	B11	I/O
0	N.C. (◆)	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	A11	VREF
0	IO_L27N_0	IO_L27N_0	IO_L27N_0	IO_L27N_0	IO_L27N_0	G12	I/O
0	IO_L27P_0	IO_L27P_0	IO_L27P_0	IO_L27P_0	IO_L27P_0	H13	I/O
0	IO_L28N_0	IO_L28N_0	IO_L28N_0	IO_L28N_0	IO_L28N_0	F12	I/O
0	IO_L28P_0	IO_L28P_0	IO_L28P_0	IO_L28P_0	IO_L28P_0	E12	I/O
0	IO_L29N_0	IO_L29N_0	IO_L29N_0	IO_L29N_0	IO_L29N_0	B12	I/O
0	IO_L29P_0	IO_L29P_0	IO_L29P_0	IO_L29P_0	IO_L29P_0	A12	I/O
0	IO_L30N_0	IO_L30N_0	IO_L30N_0	IO_L30N_0	IO_L30N_0	G13	I/O
0	IO_L30P_0	IO_L30P_0	IO_L30P_0	IO_L30P_0	IO_L30P_0	F13	I/O
0	IO_L31N_0	IO_L31N_0	IO_L31N_0	IO_L31N_0	IO_L31N_0	D13	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C13	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B13	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A13	GCLK
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	C7	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	C11	VCCO

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO_L30N_0	IO_L30N_0	G15	I/O
0	IO_L30P_0	IO_L30P_0	F15	I/O
0	IO_L31N_0	IO_L31N_0	D15	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C15	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B15	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A15	GCLK
0	N.C. (◆)	IO_L35N_0	B7	I/O
0	N.C. (◆)	IO_L35P_0	A7	I/O
0	N.C. (◆)	IO_L36N_0	G7	I/O
0	N.C. (◆)	IO_L36P_0	H8	I/O
0	N.C. (◆)	IO_L37N_0	E9	I/O
0	N.C. (◆)	IO_L37P_0	D9	I/O
0	N.C. (◆)	IO_L38N_0	B9	I/O
0	N.C. (◆)	IO_L38P_0	A9	I/O
0	VCCO_0	VCCO_0	C5	VCCO
0	VCCO_0	VCCO_0	E7	VCCO
0	VCCO_0	VCCO_0	C9	VCCO
0	VCCO_0	VCCO_0	G9	VCCO
0	VCCO_0	VCCO_0	J11	VCCO
0	VCCO_0	VCCO_0	L12	VCCO
0	VCCO_0	VCCO_0	C13	VCCO
0	VCCO_0	VCCO_0	G13	VCCO
0	VCCO_0	VCCO_0	L13	VCCO
0	VCCO_0	VCCO_0	L14	VCCO
1	IO	IO	E25	I/O
1	IO	IO	J21	I/O
1	IO	IO	K20	I/O
1	IO	IO	F18	I/O
1	IO	IO	F16	I/O
1	IO	IO	A16	I/O
1	IO/VREF_1	IO/VREF_1	J17	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	A27	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B27	DCI
1	IO_L02N_1	IO_L02N_1	D26	I/O
1	IO_L02P_1	IO_L02P_1	C27	I/O
1	IO_L03N_1	IO_L03N_1	A26	I/O
1	IO_L03P_1	IO_L03P_1	B26	I/O
1	IO_L04N_1	IO_L04N_1	B25	I/O
1	IO_L04P_1	IO_L04P_1	C25	I/O
1	IO_L05N_1	IO_L05N_1	F24	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
4	IO_L31P_4/DOUT/BUSY	IO_L31P_4/DOUT/BUSY	AH16	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	AJ16	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	AK16	GCLK
4	N.C. (◆)	IO_L33N_4	AH25	I/O
4	N.C. (◆)	IO_L33P_4	AJ25	I/O
4	N.C. (◆)	IO_L34N_4	AE25	I/O
4	N.C. (◆)	IO_L34P_4	AE24	I/O
4	N.C. (◆)	IO_L35N_4	AG24	I/O
4	N.C. (◆)	IO_L35P_4	AH24	I/O
4	N.C. (◆)	IO_L38N_4	AJ24	I/O
4	N.C. (◆)	IO_L38P_4	AK24	I/O
4	VCCO_4	VCCO_4	Y17	VCCO
4	VCCO_4	VCCO_4	Y18	VCCO
4	VCCO_4	VCCO_4	AD18	VCCO
4	VCCO_4	VCCO_4	AH18	VCCO
4	VCCO_4	VCCO_4	Y19	VCCO
4	VCCO_4	VCCO_4	AB20	VCCO
4	VCCO_4	VCCO_4	AD22	VCCO
4	VCCO_4	VCCO_4	AH22	VCCO
4	VCCO_4	VCCO_4	AF24	VCCO
4	VCCO_4	VCCO_4	AH26	VCCO
5	IO	IO	AE6	I/O
5	IO	IO	AB10	I/O
5	IO	IO	AA11	I/O
5	IO	IO	AA15	I/O
5	IO	IO	AE15	I/O
5	IO/VREF_5	IO/VREF_5	AH4	VREF
5	IO/VREF_5	IO/VREF_5	AK15	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	AK4	DUAL
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AJ4	DUAL
5	IO_L02N_5	IO_L02N_5	AK5	I/O
5	IO_L02P_5	IO_L02P_5	AJ5	I/O
5	IO_L03N_5	IO_L03N_5	AF6	I/O
5	IO_L03P_5	IO_L03P_5	AG5	I/O
5	IO_L04N_5	IO_L04N_5	AJ6	I/O
5	IO_L04P_5	IO_L04P_5	AH6	I/O
5	IO_L05N_5	IO_L05N_5	AE7	I/O
5	IO_L05P_5	IO_L05P_5	AD7	I/O
5	IO_L06N_5	IO_L06N_5	AH7	I/O
5	IO_L06P_5	IO_L06P_5	AG7	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L48P_3	IO_L48P_3	AB24	I/O
3	N.C. (◆)	IO_L49N_3	AA26	I/O
3	N.C. (◆)	IO_L49P_3	AA25	I/O
3	IO_L50N_3	IO_L50N_3	Y25	I/O
3	IO_L50P_3	IO_L50P_3	Y24	I/O
3	N.C. (◆)	IO_L51N_3	V24	I/O
3	N.C. (◆)	IO_L51P_3	W24	I/O
3	VCCO_3	VCCO_3	AA23	VCCO
3	VCCO_3	VCCO_3	AB23	VCCO
3	VCCO_3	VCCO_3	AB29	VCCO
3	VCCO_3	VCCO_3	AB33	VCCO
3	VCCO_3	VCCO_3	AD27	VCCO
3	VCCO_3	VCCO_3	AD31	VCCO
3	VCCO_3	VCCO_3	AG28	VCCO
3	VCCO_3	VCCO_3	AG32	VCCO
3	VCCO_3	VCCO_3	AL32	VCCO
3	VCCO_3	VCCO_3	W23	VCCO
3	VCCO_3	VCCO_3	W31	VCCO
3	VCCO_3	VCCO_3	Y23	VCCO
3	VCCO_3	VCCO_3	Y27	VCCO
4	IO	IO	AD18	I/O
4	IO	IO	AD19	I/O
4	IO	IO	AD20	I/O
4	IO	IO	AD22	I/O
4	IO	IO	AE18	I/O
4	IO	IO	AE19	I/O
4	IO	IO	AE22	I/O
4	N.C. (◆)	IO	AE24	I/O
4	IO	IO	AF24	I/O
4	N.C. (◆)	IO	AF26	I/O
4	IO	IO	AG26	I/O
4	IO	IO	AG27	I/O
4	IO	IO	AJ27	I/O
4	IO	IO	AJ29	I/O
4	IO	IO	AK25	I/O
4	IO	IO	AN26	I/O
4	IO/VREF_4	IO/VREF_4	AF21	VREF
4	IO/VREF_4	IO/VREF_4	AH23	VREF
4	IO/VREF_4	IO/VREF_4	AK18	VREF
4	IO/VREF_4	IO/VREF_4	AL30	VREF