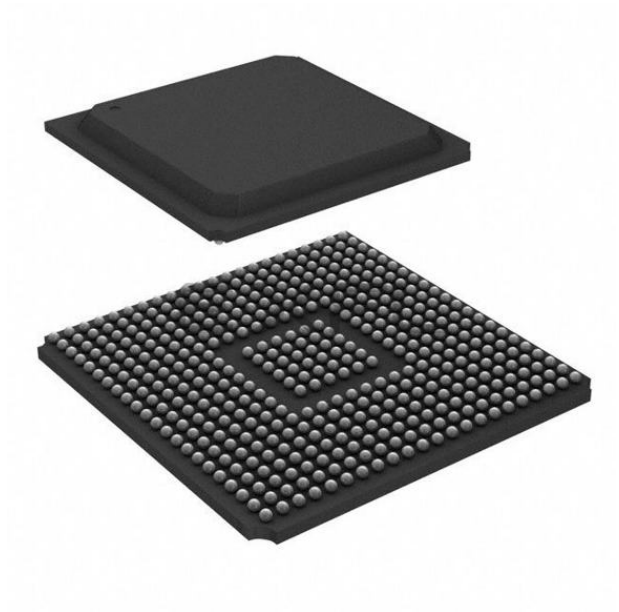
AMD Xilinx - XC3S1500-4FGG456C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3328
Number of Logic Elements/Cells	29952
Total RAM Bits	589824
Number of I/O	333
Number of Gates	1500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1500-4fgg456c

- **Phase Shifting:** The DCM provides the ability to shift the phase of all its output clock signals with respect to its input clock signal.

The DCM has four functional components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), the Phase Shifter (PS), and the Status Logic. Each component has its associated signals, as shown in Figure 19.

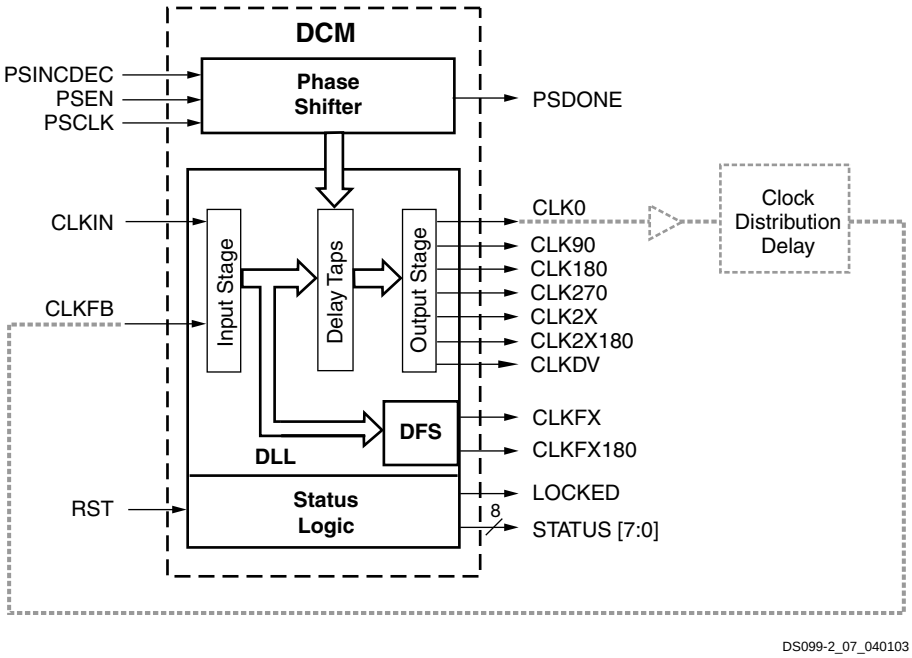


Figure 19: **DCM Functional Blocks and Associated Signals**

Delay-Locked Loop (DLL)

The most basic function of the DLL component is to eliminate clock skew. The main signal path of the DLL consists of an input stage, followed by a series of discrete delay elements or *taps,* which in turn leads to an output stage. This path together with logic for phase detection and control forms a system complete with feedback as shown in Figure 20.

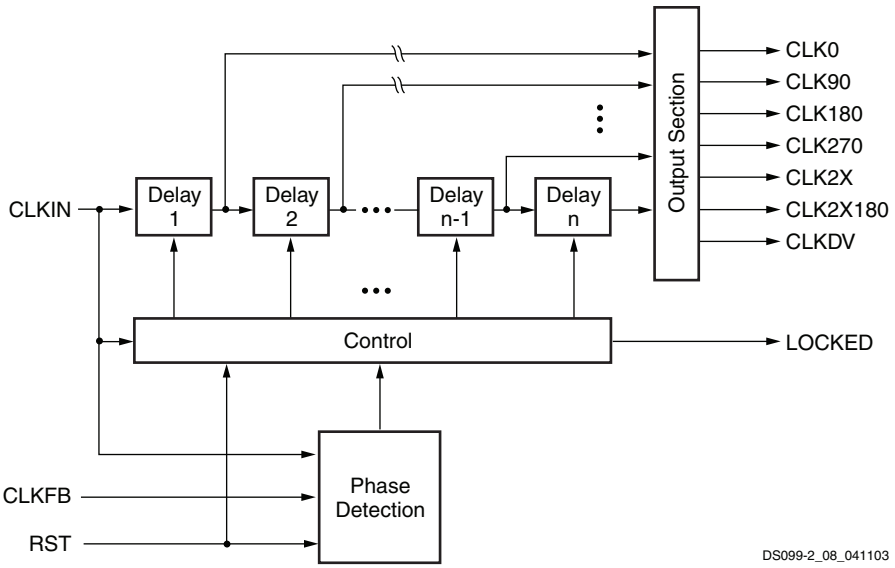


Figure 20: **Simplified Functional Diagram of DLL**

DLL Clock Input Connections

An external clock source enters the FPGA using a Global Clock Input Buffer (IBUFG), which directly accesses the global clock network or an Input Buffer (IBUF). Clock signals within the FPGA drive a global clock net using a Global Clock Multiplexer Buffer (BUFGMUX). The global clock net connects directly to the CLKIN input. The internal and external connections are shown in the [a] and [c] sections, respectively, of Figure 21. A differential clock (e.g., LVDS) can serve as an input to CLKIN.

DLL Clock Output and Feedback Connections

As many as four of the nine DCM clock outputs can simultaneously drive the four BUFGMUX buffers on the same die edge (top or bottom). All DCM clock outputs can simultaneously drive general routing resources, including interconnect leading to OBUF buffers.

The feedback loop is essential for DLL operation and is established by driving the CLKFB input with either the CLK0 or the CLK2X signal so that any undesirable clock distribution delay is included in the loop. It is possible to use either of these two signals for synchronizing any of the seven DLL outputs: CLK0, CLK90, CLK180, CLK270, CLKDV, CLK2X, or CLK2X180. The value assigned to the CLK_FEEDBACK attribute must agree with the physical feedback connection: a value of 1X for the CLK0 case, 2X for the CLK2X case. If the DCM is used in an application that does not require the DLL—i.e., only the DFS is used—then there is no feedback loop so CLK_FEEDBACK is set to NONE.

CLK2X feedback is only supported on all mask revision ‘E’ and later devices (see Mask and Fab Revisions, page 58), on devices with the "GQ" fabrication code, and on all versions of the XC3S50 and XC3S1000.

There are two basic cases that determine how to connect the DLL clock outputs and feedback connections: on-chip synchronization and off-chip synchronization, which are illustrated in Figure 21.

Coarse Phase Shift Outputs of the DLL Component

In addition to CLK0 for zero-phase alignment to the CLKIN signal, the DLL also provides the CLK90, CLK180 and CLK270 outputs for 90°, 180° and 270° phase-shifted signals, respectively. These signals are described in Table 16, page 33. Their relative timing in the Low Frequency Mode is shown in Figure 22, page 37. The CLK90, CLK180 and CLK270 outputs are not available when operating in the High Frequency mode. (See the description of the DLL_FREQUENCY_MODE attribute in Table 17, page 33.) For control in finer increments than 90°, see Phase Shifter (PS), page 39.

Basic Frequency Synthesis Outputs of the DLL Component

The DLL component provides basic options for frequency multiplication and division in addition to the more flexible synthesis capability of the DFS component, described in a later section. These operations result in output clock signals with frequencies that are either a fraction (for division) or a multiple (for multiplication) of the incoming clock frequency. The CLK2X output produces an in-phase signal that is twice the frequency of CLKIN. The CLK2X180 output also doubles the frequency, but is 180° out-of-phase with respect to CLKIN. The CLKDIV output generates a clock frequency that is a predetermined fraction of the CLKIN frequency. The CLKDV_DIVIDE attribute determines the factor used to divide the CLKIN frequency. The attribute can be set to various values as described in Table 17. The basic frequency synthesis outputs are described in Table 16. Their relative timing in the Low Frequency Mode is shown in Figure 22.

The CLK2X and CLK2X180 outputs are not available when operating in the High Frequency mode. See the description of the DLL_FREQUENCY_MODE attribute in Table 18.

Duty Cycle Correction of DLL Clock Outputs

The CLK2X[1], CLK2X180, and CLKDV[2] output signals ordinarily exhibit a 50% duty cycle—even if the incoming CLKIN signal has a different duty cycle. A 50% duty cycle means that the High and Low times of each clock cycle are equal. The DUTY_CYCLE_CORRECTION attribute determines whether or not duty cycle correction is applied to the CLK0, CLK90, CLK180 and CLK270 outputs. If DUTY_CYCLE_CORRECTION is set to TRUE, then the duty cycle of these four outputs is corrected to 50%. If DUTY_CYCLE_CORRECTION is set to FALSE, then these outputs exhibit the same duty cycle as the CLKIN signal. Figure 22 compares the characteristics of the DLL's output signals to those of the CLKIN signal.

1. The CLK2X output generates a 25% duty cycle clock at the same frequency as the CLKIN signal until the DLL has achieved lock.
2. The duty cycle of the CLKDV outputs may differ somewhat from 50% (i.e., the signal will be High for less than 50% of the period) when the CLKDV_DIVIDE attribute is set to a non-integer value *and* the DLL is operating in the High Frequency mode.

Additional Configuration Details

Additional details about the Spartan-3 FPGA configuration architecture and command set are available in UG332: *Spartan-3 Generation Configuration User Guide* and in application note XAPP452: *Spartan-3 Advanced Configuration Architecture*.

Powering Spartan-3 FPGAs

Voltage Regulators

Various power supply manufacturers offer complete power solutions for Xilinx FPGAs, including some with integrated multi-rail regulators specifically designed for Spartan-3 FPGAs. The Xilinx Power Corner web page provides links to vendor solution guides as well as Xilinx power estimation and analysis tools.

Power Distribution System (PDS) Design and Bypass/Decoupling Capacitors

Good power distribution system (PDS) design is important for all FPGA designs, especially for high-performance applications. Proper design results in better overall performance, lower clock and DCM jitter, and a generally more robust system. Before designing the printed circuit board (PCB) for the FPGA design, review application note XAPP623: *Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors*.

Power-On Behavior

Spartan-3 FPGAs have a built-in Power-On Reset (POR) circuit that monitors the three power rails required to successfully configure the FPGA. At power-up, the POR circuit holds the FPGA in a reset state until the V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 4 supplies reach their respective input threshold levels (see Table 29, page 59). After all three supplies reach their respective threshold, the POR reset is released and the FPGA begins its configuration process.

Because the three supply inputs must be valid to release the POR reset and can be supplied in any order, there are no specific voltage sequencing requirements. However, applying the FPGA's V_{CCAUX} supply before the V_{CCINT} supply uses the least I_{CCINT} current.

Once all three supplies are valid, the minimum current required to power-on the FPGA is equal to the worst-case quiescent current, as specified in Table 34, page 62. Spartan-3 FPGAs do not require Power-On Surge (POS) current to successfully configure.

Surplus I_{CCINT} if V_{CCINT} Applied before V_{CCAUX}

If the V_{CCINT} supply is applied before the V_{CCAUX} supply, the FPGA may draw a surplus I_{CCINT} current in addition to the I_{CCINT} quiescent current levels specified in Table 34. The momentary additional I_{CCINT} surplus current might be a few hundred milliamperes under nominal conditions, significantly less than the instantaneous current consumed by the bypass capacitors at power-on. However, the surplus current immediately disappears when the V_{CCAUX} supply is applied, and, in response, the FPGA's I_{CCINT} quiescent current demand drops to the levels specified in Table 34. The FPGA does not use nor does it require the surplus current to successfully power-on and configure. If applying V_{CCINT} before V_{CCAUX}, ensure that the regulator does not have a foldback feature that could inadvertently shut down in the presence of the surplus current.

Maximum Allowed V_{CCINT} Ramp Rate on Early Devices, if V_{VCCINT}Supply is Last in Sequence

All devices with a mask revision code 'E' or later do not have a V_{CCINT} ramp rate requirement. See Mask and Fab Revisions, page 58.

Early Spartan-3 FPGAs were produced at a 200 mm wafer production facility and are identified by a fabrication/process code of "FQ" on the device top marking, as shown in Package Marking, page 5. These "FQ" devices have a maximum V_{CCINT} ramp rate requirement if and only if V_{CCINT} is the last supply to ramp, after the V_{CCAUX} and V_{CCO} Bank 4 supplies. This maximum ramp rate appears as T_{CCINT} in Table 30, page 60.

Minimum Allowed V_{CCO} Ramp Rate on Early Devices

Devices shipped since 2006 essentially have no V_{CCO} ramp rate limits, shown in Table 30, page 60. Similarly, all devices with a mask revision code 'E' or later do not have a V_{CCO} ramp rate limit. See Mask and Fab Revisions, page 58.

Table 30: **Power Voltage Ramp Time Requirements**

Symbol	Description	Device	Package	Min	Max	Units
T_{CCO}	V_{CCO} ramp time for all eight banks	All	All	No limit(4)	–	N/A
T_{CCINT}	V_{CCINT} ramp time, only if V_{CCINT} is last in three-rail power-on sequence	All	All	No limit	No limit(5)	N/A

Notes:

1. If a limit exists, this specification is based on characterization.
2. The ramp time is measured from 10% to 90% of the full nominal voltage swing for all I/O standards.
3. For information on power-on current needs, see Power-On Behavior, page 54
4. For mask revisions earlier than revision E (see Mask and Fab Revisions, page 58), T_{CCO} min is limited to 2.0 ms for the XC3S200 and XC3S400 devices in QFP packages, and limited to 0.6 ms for the XC3S200, XC3S400, XC3S1500, and XC3S4000 devices in the FT and FG packages.
5. For earlier device versions with the FQ fabrication/process code (see Mask and Fab Revisions, page 58), T_{CCINT} max is limited to 500 µs.

Table 31: **Power Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:

1. RAM contents include data stored in CMOS configuration latches.
2. The level of the V_{CCO} supply has no effect on data retention.
3. If a brown-out condition occurs where V_{CCAUX} or V_{CCINT} drops below the retention voltage, then V_{CCAUX} or V_{CCINT} must drop below the minimum power-on reset voltage indicated in Table 29 in order to clear out the device configuration content.

Table 32: **General Recommended Operating Conditions**

Symbol	Description		Min	Nom	Max	Units
T_J	Junction temperature	Commercial	0	25	85	°C
		Industrial	–40	25	100	°C
V_{CCINT}	Internal supply voltage		1.140	1.200	1.260	V
V_{CCO}(1)	Output driver supply voltage		1.140	–	3.465	V
V_{CCAUX}	Auxiliary supply voltage		2.375	2.500	2.625	V
ΔV_{CCAUX}(2)	Voltage variance on VCCAUX when using a DCM		–	–	10	mV/ms
V_{IN}(3)	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND(4)(6)	V_{CCO} = 3.3V, IO	–0.3	–	3.75	V
		V_{CCO} = 3.3V, IO_Lxxy(7)	–0.3	–	3.75	V
		$V_{CCO} \le$ 2.5V, IO	–0.3	–	V_{CCO} + 0.3(4)	V
		$V_{CCO} \le$ 2.5V, IO_Lxxy(7)	–0.3	–	V_{CCO} + 0.3(4)	V
	Voltage applied to all Dedicated pins relative to GND(5)		–0.3	–	V_{CCAUX} + 0.3(5)	V

Notes:

1. The V_{CCO} range given here spans the lowest and highest operating voltages of all supported I/O standards. The recommended V_{CCO} range specific to each of the single-ended I/O standards is given in Table 35, and that specific to the differential standards is given in Table 37.
2. Only during DCM operation is it recommended that the rate of change of V_{CCAUX} not exceed 10 mV/ms.
3. Input voltages outside the recommended range are permissible provided that the I_{IK} input diode clamp diode rating is met. Refer to Table 28.
4. Each of the User I/O and Dual-Purpose pins is associated with one of the V_{CCO} rails. Meeting the V_{IN} limit ensures that the internal diode junctions that exist between these pins and their associated V_{CCO} and GND rails do not turn on. The absolute maximum rating is provided in Table 28.
5. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} and GND rails do not turn on.
6. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Generation FPGAs*.
7. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.3V is supported but can cause increased leakage between the two pins. See the *Parasitic Leakage* section in UG331, *Spartan-3 Generation FPGA User Guide*.

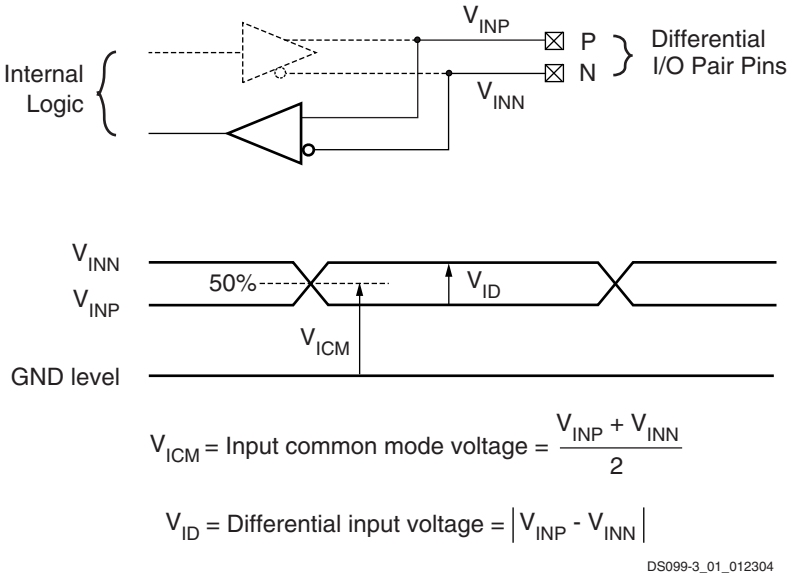


Figure 32: **Differential Input Voltages**

Table 37: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

Signal Standard (IOSTANDARD)	V_{CCO}[1]			V_{ID}[3]			V_{ICM}		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LDT_25 (ULVDS_25)	2.375	2.50	2.625	200	600	1000	0.44	0.60	0.78
LVDS_25, LVDS_25_DCI	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20
BLVDS_25	2.375	2.50	2.625	-	350	-	-	1.25	-
LVDSEXT_25, LVDSEXT_25_DCI	2.375	2.50	2.625	100	540	1000	0.30	1.20	2.20
LVPECL_25	2.375	2.50	2.625	100	-	-	0.30	1.20	2.00
RSDS_25	2.375	2.50	2.625	100	200	-	-	1.20	-
DIFF_HSTL_II_18, DIFF_HSTL_II_18_DCI	1.70	1.80	1.90	200	-	-	0.80	-	1.00
DIFF_SSTL2_II, DIFF_SSTL2_II_DCI	2.375	2.50	2.625	300	-	-	1.05	-	1.45

Notes:

1. V_{CCO} only supplies differential output drivers, not input circuits.
2. V_{REF} inputs are not used for any of the differential I/O standards.
3. V_{ID} is a differential measurement.

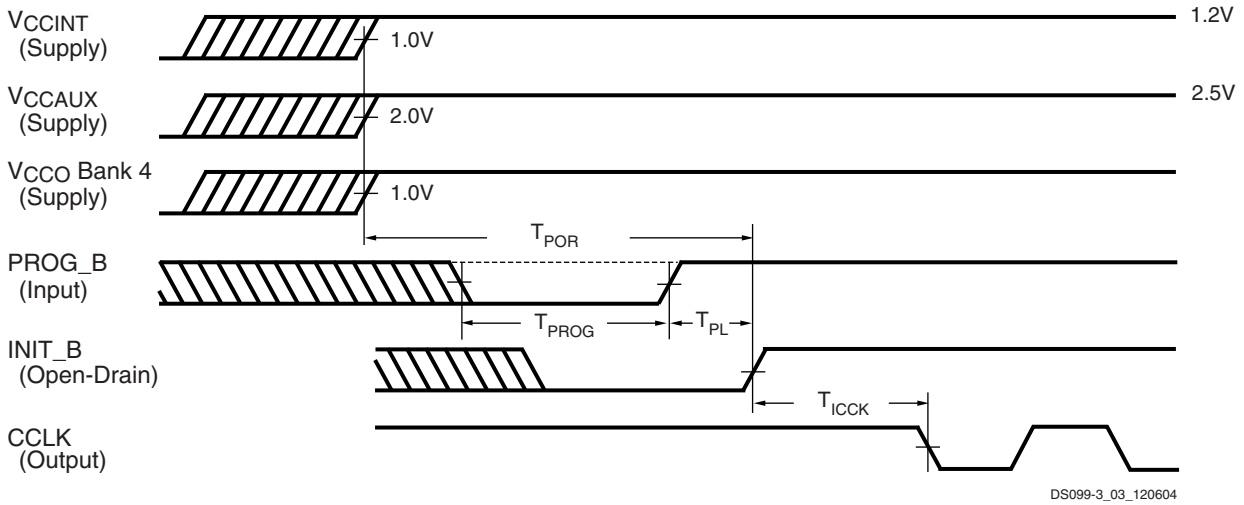
Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
HSLVDCI_25			0.27	0.31	ns
HSLVDCI_33			0.28	0.32	ns
HSTL_I			0.60	0.69	ns
HSTL_I_DCI			0.59	0.68	ns
HSTL_III			0.19	0.22	ns
HSTL_III_DCI			0.20	0.23	ns
HSTL_I_18			0.18	0.21	ns
HSTL_I_DCI_18			0.17	0.19	ns
HSTL_II_18			–0.02	–0.01	ns
HSTL_II_DCI_18			0.75	0.86	ns
HSTL_III_18			0.28	0.32	ns
HSTL_III_DCI_18			0.28	0.32	ns
LVCMOS12	Slow	2 mA	7.60	8.73	ns
		4 mA	7.42	8.53	ns
		6 mA	6.67	7.67	ns
	Fast	2 mA	3.16	3.63	ns
		4 mA	2.70	3.10	ns
		6 mA	2.41	2.77	ns
LVCMOS15	Slow	2 mA	4.55	5.23	ns
		4 mA	3.76	4.32	ns
		6 mA	3.57	4.11	ns
		8 mA	3.55	4.09	ns
		12 mA	3.00	3.45	ns
	Fast	2 mA	3.11	3.57	ns
		4 mA	1.71	1.96	ns
		6 mA	1.44	1.66	ns
		8 mA	1.26	1.44	ns
		12 mA	1.11	1.27	ns
LVDCI_15			1.51	1.74	ns
LVDCI_DV2_15			1.32	1.52	ns

Table 59: **Switching Characteristics for the DLL**

Symbol	Description	Frequency Mode / FCLKIN Range	Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_1X_LF	Frequency for the CLK0, CLK90, CLK180, and CLK270 outputs	Low	All	18	167	18	167	MHz
CLKOUT_FREQ_1X_HF	Frequency for the CLK0 and CLK180 outputs	High		48	280	48	280	MHz
CLKOUT_FREQ_2X_LF(3)	Frequency for the CLK2X and CLK2X180 outputs	Low		36	334	36	334	MHz
CLKOUT_FREQ_DV_LF	Frequency for the CLKDV output	Low		1.125	110	1.125	110	MHz
CLKOUT_FREQ_DV_HF		High		3	185	3	185	MHz
Output Clock Jitter(4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output	All	All	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			–	±200	–	±200	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			–	±300	–	±300	ps
Duty Cycle								
CLKOUT_DUTY_CYCLE_DLL(5)	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs	All	XC3S50	–	±150	–	±150	ps
			XC3S200	–	±150	–	±150	ps
			XC3S400	–	±250	–	±250	ps
			XC3S1000	–	±400	–	±400	ps
			XC3S1500	–	±400	–	±400	ps
			XC3S2000	–	±400	–	±400	ps
			XC3S4000	–	±400	–	±400	ps
			XC3S5000	–	±400	–	±400	ps
Phase Alignment								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs	All	All	–	±150	–	±150	ps
CLKOUT_PHASE	Phase offset between any two DLL outputs (except CLK2X and CLK0)			–	±140	–	±140	ps
	Phase offset between the CLK2X and CLK0 outputs			–	±250	–	±250	ps

Configuration and JTAG Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 36: **Waveforms for Power-On and the Beginning of Configuration**

Table 65: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 4 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XC3S50	–	5	ms
		XC3S200	–	5	ms
		XC3S400	–	5	ms
		XC3S1000	–	5	ms
		XC3S1500	–	7	ms
		XC3S2000	–	7	ms
		XC3S4000	–	7	ms
		XC3S5000	–	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.3	–	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S50	–	2	ms
		XC3S200	–	2	ms
		XC3S400	–	2	ms
		XC3S1000	–	2	ms
		XC3S1500	–	3	ms
		XC3S2000	–	3	ms
		XC3S4000	–	3	ms
		XC3S5000	–	3	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	–	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.25	4.0	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only for the Master Serial and Master Parallel modes.

The 1% precision impedance-matching resistor attached to the VRN_# pin controls the pull-down impedance of NMOS transistor in the input or output buffer. Consequently, the VRN_# pin must connect to VCCO. The 'N' character in "VRN" indicates that this pin controls the I/O buffer's NMOS transistor impedance. The VRN_# pin is only used for split termination.

Each VRN or VRP reference input requires its own resistor. A single resistor cannot be shared between VRN or VRP pins associated with different banks.

During configuration, these pins behave exactly like user-I/O pins. The associated DCI behavior is not active or valid until after configuration completes.

Also see Digitally Controlled Impedance (DCI), page 16.

DCI Termination Types

If the I/O in an I/O bank do not use the DCI feature, then no external resistors are required and both the VRP_# and VRN_# pins are available for user I/O, as shown in section [a] of Figure 42.

If the I/O standards within the associated I/O bank require single termination—such as GTL_DCI, GTLP_DCI, or HSTL_III_DCI—then only the VRP_# signal connects to a 1% precision impedance-matching resistor, as shown in section [b] of Figure 42. A resistor is not required for the VRN_# pin.

Finally, if the I/O standards with the associated I/O bank require split termination—such as HSTL_I_DCI, SSTL2_I_DCI, SSTL2_II_DCI, or LVDS_25_DCI and LVDSEXT_25_DCI receivers—then both the VRP_# and VRN_# pins connect to separate 1% precision impedance-matching resistors, as shown in section [c] of Figure 42. Neither pin is available for user I/O.

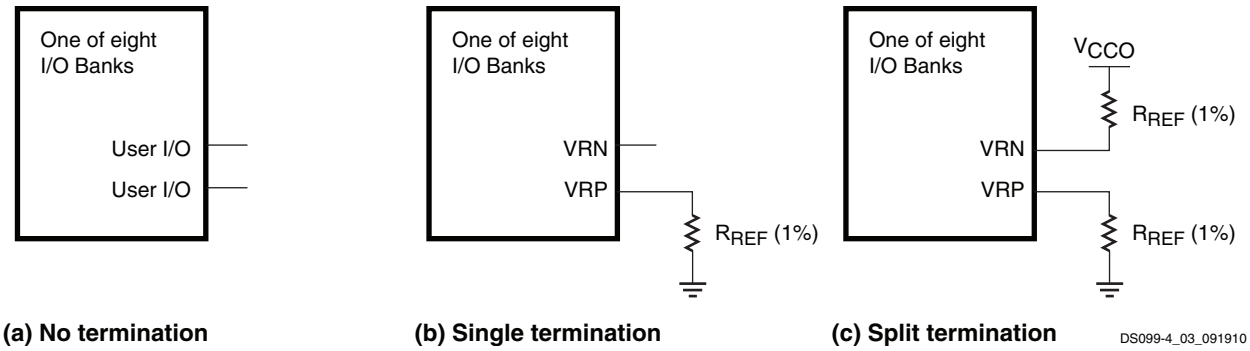


Figure 42: **DCI Termination Types**

GCLK: Global Clock Buffer Inputs or General-Purpose I/O Pins

These pins are user-I/O pins unless they specifically connect to one of the eight low-skew global clock buffers on the device, specified using the IBUFG primitive.

There are eight GCLK pins per device and two each appear in the top-edge banks, Bank 0 and 1, and the bottom-edge banks, Banks 4 and 5. See Figure 40 for a picture of bank labeling.

During configuration, these pins behave exactly like user-I/O pins.

Also see Global Clock Network, page 42.

CONFIG: Dedicated Configuration Pins

The dedicated configuration pins control the configuration process and are not available as user-I/O pins. Every package has seven dedicated configuration pins. All CONFIG-type pins are powered by the +2.5V VCCAUX supply.

Also see Configuration, page 46.

All VCCAUX inputs must be connected together and to the +2.5V voltage supply. Furthermore, there must be sufficient supply decoupling to guarantee problem-free operation, as described in XAPP623.

Because VCCAUX connects to the DCMs and the DCMs are sensitive to voltage changes, be sure that the VCCAUX supply and the ground return paths are designed for low noise and low voltage drop, especially that caused by a large number of simultaneous switching I/Os.

GND Type: Ground

All GND pins must be connected and have a low resistance path back to the various VCCO, VCCINT, and VCCAUX supplies.

Pin Behavior During Configuration

Table 79 shows how various pins behave during the FPGA configuration process. The actual behavior depends on the values applied to the M2, M1, and M0 mode select pins and the HSWAP_EN pin. The mode select pins determine which of the DUAL type pins are active during configuration. In JTAG configuration mode, none of the DUAL-type pins are used for configuration and all behave as user-I/O pins.

All DUAL-type pins not actively used during configuration and all I/O-type, DCI-type, VREF-type, GCLK-type pins are high impedance (floating, three-stated, Hi-Z) during the configuration process. These pins are indicated in Table 79 as shaded table entries or cells. These pins have a pull-up resistor to their associated VCCO if the HSWAP_EN pin is Low. When HSWAP_EN is High, these pull-up resistors are disabled during configuration.

Some pins always have an active pull-up resistor during configuration, regardless of the value applied to the HSWAP_EN pin. After configuration, these pull-up resistors are controlled by Bitstream Options.

- All the dedicated CONFIG-type configuration pins (CCLK, PROG_B, DONE, M2, M1, M0, and HSWAP_EN) have a pull-up resistor to VCCAUX.
- All JTAG-type pins (TCK, TDI, TMS, TDO) have a pull-up resistor to VCCAUX.
- The INIT_B DUAL-purpose pin has a pull-up resistor to VCCO_4 or VCCO_BOTTOM, depending on package style.

After configuration completes, some pins have optional behavior controlled by the configuration bitstream loaded into the part. For example, via the bitstream, all unused I/O pins can be collectively configured as input pins with either a pull-up resistor, a pull-down resistor, or be left in a high-impedance state.

Table 79: **Pin Behavior After Power-Up, During Configuration**

Pin Name	Configuration Mode Settings <M2:M1:M0>					Bitstream Configuration Option
	Serial Modes		SelectMap Parallel Modes		JTAG Mode <1:0:1>	
	Master <0:0:0>	Slave <1:1:1>	Master <0:1:1>	Slave <1:1:0>		
I/O: General-purpose I/O pins						
IO						UnusedPin
IO_Lxxy_#						UnusedPin
DUAL: Dual-purpose configuration pins						
IO_Lxxy_#/ DIN/D0	DIN (I)	DIN (I)	D0 (I/O)	D0 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D1			D1 (I/O)	D1 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D2			D2 (I/O)	D2 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D3			D3 (I/O)	D3 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D4			D4 (I/O)	D4 (I/O)		Persist UnusedPin

TQ144 Footprint

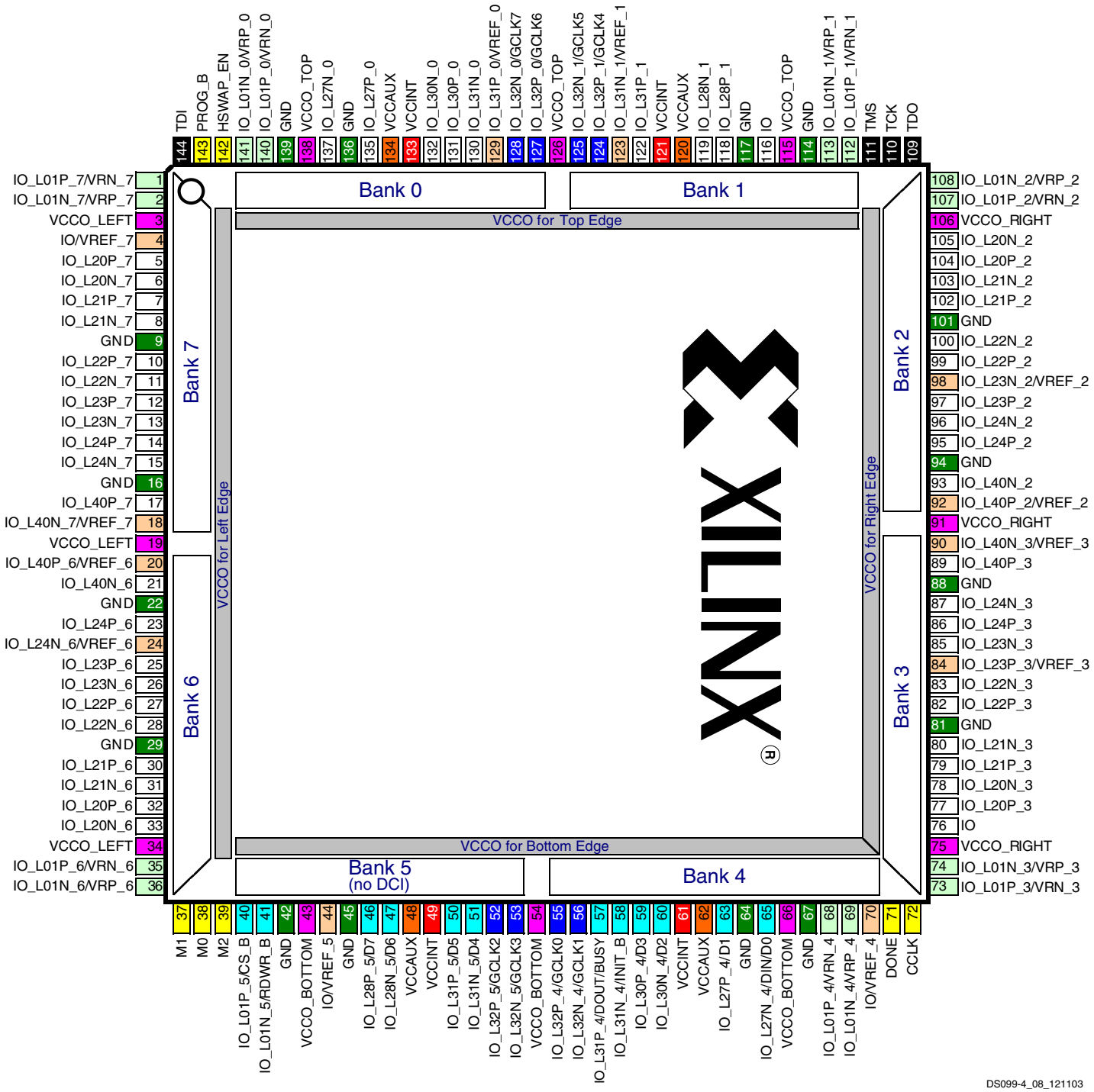


Figure 46: **TQ144 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

51 **I/O:** Unrestricted, general-purpose user I/O	12 **DUAL:** Configuration pin, then possible user I/O	12 **VREF:** User I/O or input voltage reference for bank
14 **DCI:** User I/O or reference resistor input for bank	8 **GCLK:** User I/O or global clock buffer input	12 **VCCO:** Output voltage supply for bank
7 **CONFIG:** Dedicated configuration pins	4 **JTAG:** Dedicated JTAG port pins	4 **VCCINT:** Internal core voltage supply (+1.2V)
0 **N.C.:** No unconnected pins in this package	16 **GND:** Ground	4 **VCCAUX:** Auxiliary voltage supply (+2.5V)

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
N/A	GND	J3	GND
N/A	GND	J8	GND
N/A	GND	K11	GND
N/A	GND	K16	GND
N/A	GND	K3	GND
N/A	GND	K8	GND
N/A	GND	L10	GND
N/A	GND	L11	GND
N/A	GND	L8	GND
N/A	GND	L9	GND
N/A	GND	M12	GND
N/A	GND	M7	GND
N/A	GND	N1	GND
N/A	GND	N18	GND
N/A	GND	T10	GND
N/A	GND	T9	GND
N/A	GND	U17	GND
N/A	GND	U2	GND
N/A	GND	V1	GND
N/A	GND	V13	GND
N/A	GND	V18	GND
N/A	GND	V6	GND
N/A	VCCAUX	B12	VCCAUX
N/A	VCCAUX	B7	VCCAUX
N/A	VCCAUX	G17	VCCAUX
N/A	VCCAUX	G2	VCCAUX
N/A	VCCAUX	M17	VCCAUX
N/A	VCCAUX	M2	VCCAUX
N/A	VCCAUX	U12	VCCAUX
N/A	VCCAUX	U7	VCCAUX
N/A	VCCINT	F12	VCCINT
N/A	VCCINT	F13	VCCINT
N/A	VCCINT	F6	VCCINT
N/A	VCCINT	F7	VCCINT
N/A	VCCINT	G13	VCCINT
N/A	VCCINT	G6	VCCINT
N/A	VCCINT	M13	VCCINT
N/A	VCCINT	M6	VCCINT
N/A	VCCINT	N12	VCCINT
N/A	VCCINT	N13	VCCINT

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
1	N.C. (◆)	IO_L18P_1	IO_L18P_1	IO_L18P_1	IO[3]	C18	I/O
1	IO_L19N_1	IO_L19N_1	IO_L19N_1	IO_L19N_1	IO_L19N_1	F17	I/O
1	IO_L19P_1	IO_L19P_1	IO_L19P_1	IO_L19P_1	IO_L19P_1	G17	I/O
1	IO_L22N_1	IO_L22N_1	IO_L22N_1	IO_L22N_1	IO_L22N_1	D17	I/O
1	IO_L22P_1	IO_L22P_1	IO_L22P_1	IO_L22P_1	IO_L22P_1	E17	I/O
1	N.C. (◆)	IO_L23N_1	IO_L23N_1	IO_L23N_1	IO_L23N_1	A17	I/O
1	N.C. (◆)	IO_L23P_1	IO_L23P_1	IO_L23P_1	IO_L23P_1	B17	I/O
1	IO_L24N_1	IO_L24N_1	IO_L24N_1	IO_L24N_1	IO_L24N_1	G16	I/O
1	IO_L24P_1	IO_L24P_1	IO_L24P_1	IO_L24P_1	IO_L24P_1	H16	I/O
1	IO_L25N_1	IO_L25N_1	IO_L25N_1	IO_L25N_1	IO_L25N_1	E16	I/O
1	IO_L25P_1	IO_L25P_1	IO_L25P_1	IO_L25P_1	IO_L25P_1	F16	I/O
1	N.C. (◆)	IO_L26N_1	IO_L26N_1	IO_L26N_1	IO_L26N_1	A16	I/O
1	N.C. (◆)	IO_L26P_1	IO_L26P_1	IO_L26P_1	IO_L26P_1	B16	I/O
1	IO_L27N_1	IO_L27N_1	IO_L27N_1	IO_L27N_1	IO_L27N_1	G15	I/O
1	IO_L27P_1	IO_L27P_1	IO_L27P_1	IO_L27P_1	IO_L27P_1	H15	I/O
1	IO_L28N_1	IO_L28N_1	IO_L28N_1	IO_L28N_1	IO_L28N_1	E15	I/O
1	IO_L28P_1	IO_L28P_1	IO_L28P_1	IO_L28P_1	IO_L28P_1	F15	I/O
1	IO_L29N_1	IO_L29N_1	IO_L29N_1	IO_L29N_1	IO_L29N_1	A15	I/O
1	IO_L29P_1	IO_L29P_1	IO_L29P_1	IO_L29P_1	IO_L29P_1	B15	I/O
1	IO_L30N_1	IO_L30N_1	IO_L30N_1	IO_L30N_1	IO_L30N_1	G14	I/O
1	IO_L30P_1	IO_L30P_1	IO_L30P_1	IO_L30P_1	IO_L30P_1	H14	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D14	VREF
1	IO_L31P_1	IO_L31P_1	IO_L31P_1	IO_L31P_1	IO_L31P_1	E14	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B14	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C14	GCLK
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	C16	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	C20	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	H17	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	H18	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J14	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J15	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J16	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	K14	VCCO
2	N.C. (◆)	N.C. (■)	IO	IO	IO	F22	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C25	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C26	DCI
2	IO_L02N_2	IO_L02N_2	IO_L02N_2	IO_L02N_2	IO_L02N_2	E23	I/O
2	IO_L02P_2	IO_L02P_2	IO_L02P_2	IO_L02P_2	IO_L02P_2	E24	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2[1]	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	D25	VREF[1]
2	IO_L03P_2	IO_L03P_2	IO_L03P_2	IO_L03P_2	IO_L03P_2	D26	I/O
2	N.C. (◆)	IO_L05N_2	IO_L05N_2	IO_L05N_2	IO_L05N_2	E25	I/O
2	N.C. (◆)	IO_L05P_2	IO_L05P_2	IO_L05P_2	IO_L05P_2	E26	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	M25	VREF
2	IO_L34P_2	IO_L34P_2	IO_L34P_2	IO_L34P_2	IO_L34P_2	M26	I/O
2	IO_L35N_2	IO_L35N_2	IO_L35N_2	IO_L35N_2	IO_L35N_2	N19	I/O
2	IO_L35P_2	IO_L35P_2	IO_L35P_2	IO_L35P_2	IO_L35P_2	N20	I/O
2	IO_L38N_2	IO_L38N_2	IO_L38N_2	IO_L38N_2	IO_L38N_2	N21	I/O
2	IO_L38P_2	IO_L38P_2	IO_L38P_2	IO_L38P_2	IO_L38P_2	N22	I/O
2	IO_L39N_2	IO_L39N_2	IO_L39N_2	IO_L39N_2	IO_L39N_2	N23	I/O
2	IO_L39P_2	IO_L39P_2	IO_L39P_2	IO_L39P_2	IO_L39P_2	N24	I/O
2	IO_L40N_2	IO_L40N_2	IO_L40N_2	IO_L40N_2	IO_L40N_2	N25	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	N26	VREF
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	G24	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	J19	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	K19	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	L18	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	L24	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	M18	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	N17	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	N18	VCCO
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	AA22	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	AA21	DCI
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	AB24	VREF
3	IO_L02P_3	IO_L02P_3	IO_L02P_3	IO_L02P_3	IO_L02P_3	AB23	I/O
3	IO_L03N_3	IO_L03N_3	IO_L03N_3	IO_L03N_3	IO_L03N_3	AC26	I/O
3	IO_L03P_3	IO_L03P_3	IO_L03P_3	IO_L03P_3	IO_L03P_3	AC25	I/O
3	N.C. (◆)	IO_L05N_3	IO_L05N_3	IO_L05N_3	IO_L05N_3	Y21	I/O
3	N.C. (◆)	IO_L05P_3	IO_L05P_3	IO_L05P_3	IO_L05P_3	Y20	I/O
3	N.C. (◆)	IO_L06N_3	IO_L06N_3	IO_L06N_3	IO_L06N_3	AB26	I/O
3	N.C. (◆)	IO_L06P_3	IO_L06P_3	IO_L06P_3	IO_L06P_3	AB25	I/O
3	N.C. (◆)	IO_L07N_3	IO_L07N_3	IO_L07N_3	IO_L07N_3	AA24	I/O
3	N.C. (◆)	IO_L07P_3	IO_L07P_3	IO_L07P_3	IO_L07P_3	AA23	I/O
3	N.C. (◆)	IO_L08N_3	IO_L08N_3	IO_L08N_3	IO_L08N_3	Y23	I/O
3	N.C. (◆)	IO_L08P_3	IO_L08P_3	IO_L08P_3	IO_L08P_3	Y22	I/O
3	N.C. (◆)	IO_L09N_3	IO_L09N_3	IO_L09N_3	IO_L09N_3	AA26	I/O
3	N.C. (◆)	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	AA25	VREF
3	N.C. (◆)	IO_L10N_3	IO_L10N_3	IO_L10N_3	IO_L10N_3	W21	I/O
3	N.C. (◆)	IO_L10P_3	IO_L10P_3	IO_L10P_3	IO_L10P_3	W20	I/O
3	IO_L14N_3	IO_L14N_3	IO_L14N_3	IO_L14N_3	IO_L14N_3	Y26	I/O
3	IO_L14P_3	IO_L14P_3	IO_L14P_3	IO_L14P_3	IO_L14P_3	Y25	I/O
3	IO_L16N_3	IO_L16N_3	IO_L16N_3	IO_L16N_3	IO_L16N_3	V21	I/O
3	IO_L16P_3	IO_L16P_3	IO_L16P_3	IO_L16P_3	IO_L16P_3	W22	I/O
3	IO_L17N_3	IO_L17N_3	IO_L17N_3	IO_L17N_3	IO_L17N_3	W24	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	W23	VREF

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AB5	DUAL
5	IO_L04N_5	IO_L04N_5	IO_L04N_5	IO_L04N_5	IO_L04N_5	AE4	I/O
5	IO_L04P_5	IO_L04P_5	IO_L04P_5	IO_L04P_5	IO_L04P_5	AD4	I/O
5	IO_L05N_5	IO_L05N_5	IO_L05N_5	IO_L05N_5	IO_L05N_5	AB6	I/O
5	IO_L05P_5	IO_L05P_5	IO_L05P_5	IO_L05P_5	IO_L05P_5	AA6	I/O
5	IO_L06N_5	IO_L06N_5	IO_L06N_5	IO_L06N_5	IO_L06N_5	AE5	I/O
5	IO_L06P_5	IO_L06P_5	IO_L06P_5	IO_L06P_5	IO_L06P_5	AD5	I/O
5	IO_L07N_5	IO_L07N_5	IO_L07N_5	IO_L07N_5	IO_L07N_5	AD6	I/O
5	IO_L07P_5	IO_L07P_5	IO_L07P_5	IO_L07P_5	IO_L07P_5	AC6	I/O
5	IO_L08N_5	IO_L08N_5	IO_L08N_5	IO_L08N_5	IO_L08N_5	AF6	I/O
5	IO_L08P_5	IO_L08P_5	IO_L08P_5	IO_L08P_5	IO_L08P_5	AE6	I/O
5	IO_L09N_5	IO_L09N_5	IO_L09N_5	IO_L09N_5	IO_L09N_5	AC7	I/O
5	IO_L09P_5	IO_L09P_5	IO_L09P_5	IO_L09P_5	IO_L09P_5	AB7	I/O
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	AF7	DCI
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	AE7	DCI
5	N.C. (◆)	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	AB8	VREF
5	N.C. (◆)	IO_L11P_5	IO_L11P_5	IO_L11P_5	IO_L11P_5	AA8	I/O
5	N.C. (◆)	IO_L12N_5	IO_L12N_5	IO_L12N_5	IO_L12N_5	AD8	I/O
5	N.C. (◆)	IO_L12P_5	IO_L12P_5	IO_L12P_5	IO_L12P_5	AC8	I/O
5	IO_L15N_5	IO_L15N_5	IO_L15N_5	IO_L15N_5	IO_L15N_5	AF8	I/O
5	IO_L15P_5	IO_L15P_5	IO_L15P_5	IO_L15P_5	IO_L15P_5	AE8	I/O
5	IO_L16N_5	IO_L16N_5	IO_L16N_5	IO_L16N_5	IO_L16N_5	AA9	I/O
5	IO_L16P_5	IO_L16P_5	IO_L16P_5	IO_L16P_5	IO_L16P_5	Y9	I/O
5	N.C. (◆)	IO_L18N_5	IO_L18N_5	IO_L18N_5	IO_L18N_5	AE9	I/O
5	N.C. (◆)	IO_L18P_5	IO_L18P_5	IO_L18P_5	IO_L18P_5	AD9	I/O
5	IO_L19N_5	IO_L19N_5	IO_L19N_5	IO_L19N_5	IO_L19N_5	AA10	I/O
5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	Y10	VREF
5	IO_L22N_5	IO_L22N_5	IO_L22N_5	IO_L22N_5	IO_L22N_5	AC10	I/O
5	IO_L22P_5	IO_L22P_5	IO_L22P_5	IO_L22P_5	IO_L22P_5	AB10	I/O
5	N.C. (◆)	IO_L23N_5	IO_L23N_5	IO_L23N_5	IO_L23N_5	AF10	I/O
5	N.C. (◆)	IO_L23P_5	IO_L23P_5	IO_L23P_5	IO_L23P_5	AE10	I/O
5	IO_L24N_5	IO_L24N_5	IO_L24N_5	IO_L24N_5	IO_L24N_5	Y11	I/O
5	IO_L24P_5	IO_L24P_5	IO_L24P_5	IO_L24P_5	IO_L24P_5	W11	I/O
5	IO_L25N_5	IO_L25N_5	IO_L25N_5	IO_L25N_5	IO_L25N_5	AB11	I/O
5	IO_L25P_5	IO_L25P_5	IO_L25P_5	IO_L25P_5	IO_L25P_5	AA11	I/O
5	N.C. (◆)	IO_L26N_5	IO_L26N_5	IO_L26N_5	IO_L26N_5	AF11	I/O
5	N.C. (◆)	IO_L26P_5	IO_L26P_5	IO_L26P_5	IO_L26P_5	AE11	I/O
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	Y12	VREF
5	IO_L27P_5	IO_L27P_5	IO_L27P_5	IO_L27P_5	IO_L27P_5	W12	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	AB12	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	AA12	DUAL
5	IO_L29N_5	IO_L29N_5	IO_L29N_5	IO_L29N_5	IO_L29N_5	AF12	I/O

FG900: 900-lead Fine-pitch Ball Grid Array

The 900-lead fine-pitch ball grid array package, FG900, supports three different Spartan-3 devices, including the XC3S2000, the XC3S4000, and the XC3S5000. The footprints for the XC3S4000 and XC3S5000 are identical, as shown in Table 107 and Figure 55. The XC3S2000, however, has fewer I/O pins which consequently results in 68 unconnected pins on the FG900 package, labeled as “N.C.” In Table 107 and Figure 55, these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in Table 107 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S2000 pinout and the pinout for the XC3S4000 and XC3S5000, then that difference is highlighted in Table 107. If the table entry is shaded, then there is an unconnected pin on the XC3S2000 that maps to a user-I/O pin on the XC3S4000 and XC3S5000.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 107: **FG900 Package Pinout**

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO	IO	E15	I/O
0	IO	IO	K15	I/O
0	IO	IO	D13	I/O
0	IO	IO	K13	I/O
0	IO	IO	G8	I/O
0	IO/VREF_0	IO/VREF_0	F9	VREF
0	IO/VREF_0	IO/VREF_0	C4	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L02N_0	IO_L02N_0	B5	I/O
0	IO_L02P_0	IO_L02P_0	A5	I/O
0	IO_L03N_0	IO_L03N_0	D5	I/O
0	IO_L03P_0	IO_L03P_0	E6	I/O
0	IO_L04N_0	IO_L04N_0	C6	I/O
0	IO_L04P_0	IO_L04P_0	B6	I/O
0	IO_L05N_0	IO_L05N_0	F6	I/O
0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	F7	VREF
0	IO_L06N_0	IO_L06N_0	D7	I/O
0	IO_L06P_0	IO_L06P_0	C7	I/O
0	IO_L07N_0	IO_L07N_0	F8	I/O
0	IO_L07P_0	IO_L07P_0	E8	I/O
0	IO_L08N_0	IO_L08N_0	D8	I/O
0	IO_L08P_0	IO_L08P_0	C8	I/O
0	IO_L09N_0	IO_L09N_0	B8	I/O
0	IO_L09P_0	IO_L09P_0	A8	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	GND	GND	T12	GND
N/A	GND	GND	N13	GND
N/A	GND	GND	P13	GND
N/A	GND	GND	R13	GND
N/A	GND	GND	T13	GND
N/A	GND	GND	U13	GND
N/A	GND	GND	V13	GND
N/A	GND	GND	A14	GND
N/A	GND	GND	E14	GND
N/A	GND	GND	H14	GND
N/A	GND	GND	N14	GND
N/A	GND	GND	P14	GND
N/A	GND	GND	R14	GND
N/A	GND	GND	T14	GND
N/A	GND	GND	U14	GND
N/A	GND	GND	V14	GND
N/A	GND	GND	AC14	GND
N/A	GND	GND	AF14	GND
N/A	GND	GND	AK14	GND
N/A	GND	GND	M15	GND
N/A	GND	GND	N15	GND
N/A	GND	GND	P15	GND
N/A	GND	GND	R15	GND
N/A	GND	GND	T15	GND
N/A	GND	GND	U15	GND
N/A	GND	GND	V15	GND
N/A	GND	GND	W15	GND
N/A	GND	GND	M16	GND
N/A	GND	GND	N16	GND
N/A	GND	GND	P16	GND
N/A	GND	GND	R16	GND
N/A	GND	GND	T16	GND
N/A	GND	GND	U16	GND
N/A	GND	GND	V16	GND
N/A	GND	GND	W16	GND
N/A	GND	GND	A17	GND
N/A	GND	GND	E17	GND
N/A	GND	GND	H17	GND
N/A	GND	GND	N17	GND
N/A	GND	GND	P17	GND

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	C2	DCI
7	IO_L02N_7	IO_L02N_7	D1	I/O
7	IO_L02P_7	IO_L02P_7	D2	I/O
7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	E2	VREF
7	IO_L03P_7	IO_L03P_7	E3	I/O
7	IO_L04N_7	IO_L04N_7	F3	I/O
7	IO_L04P_7	IO_L04P_7	F4	I/O
7	IO_L05N_7	IO_L05N_7	F1	I/O
7	IO_L05P_7	IO_L05P_7	F2	I/O
7	IO_L06N_7	IO_L06N_7	G5	I/O
7	IO_L06P_7	IO_L06P_7	G6	I/O
7	IO_L07N_7	IO_L07N_7	H5	I/O
7	IO_L07P_7	IO_L07P_7	H6	I/O
7	IO_L08N_7	IO_L08N_7	H1	I/O
7	IO_L08P_7	IO_L08P_7	H2	I/O
7	IO_L09N_7	IO_L09N_7	J6	I/O
7	IO_L09P_7	IO_L09P_7	J7	I/O
7	IO_L10N_7	IO_L10N_7	J4	I/O
7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	H4	VREF
7	IO_L11N_7	IO_L11N_7	J2	I/O
7	IO_L11P_7	IO_L11P_7	J3	I/O
7	IO_L12N_7	IO_L12N_7	K9	I/O
7	IO_L12P_7	IO_L12P_7	J8	I/O
7	IO_L13N_7	IO_L13N_7	K7	I/O
7	IO_L13P_7	IO_L13P_7	K8	I/O
7	IO_L14N_7	IO_L14N_7	K5	I/O
7	IO_L14P_7	IO_L14P_7	K6	I/O
7	IO_L15N_7	IO_L15N_7	K3	I/O
7	IO_L15P_7	IO_L15P_7	K4	I/O
7	IO_L16N_7	IO_L16N_7	K1	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	K2	VREF
7	IO_L17N_7	IO_L17N_7	L9	I/O
7	IO_L17P_7	IO_L17P_7	L10	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	L1	VREF
7	IO_L19P_7	IO_L19P_7	L2	I/O
7	IO_L20N_7	IO_L20N_7	M10	I/O
7	IO_L20P_7	IO_L20P_7	M11	I/O
7	IO_L21N_7	IO_L21N_7	M7	I/O
7	IO_L21P_7	IO_L21P_7	M8	I/O
7	IO_L22N_7	IO_L22N_7	M5	I/O

Date	Version	Description
11/30/07	2.3	Added XC3S5000 FG(G)676 package. Noted that the FG(G)1156 package is being discontinued. Updated Table 86 with latest thermal characteristics data.
06/25/08	2.4	Updated formatting and links.
12/04/09	2.5	Added link to UG332 in CCLK: Configuration Clock. Noted that the CP132, CPG132, FG1156, and FGG1156 packages are being discontinued in Table 81, Table 83, Table 84, Table 85, and Table 86. Updated CP132: 132-Ball Chip-Scale Package to indicate that the CP132 and CPG132 packages are being discontinued.
10/29/12	3.0	Added Notice of Disclaimer. Per XCN07022, updated the FG1156 and FGG1156 package discussion throughout document including in Table 81, Table 83, Table 84, Table 85, and Table 86. Per XCN08011, updated CP132 and CPG132 package discussion throughout document including in Table 81, Table 83, Table 84, Table 85, and Table 86. This product is not recommended for new designs.

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