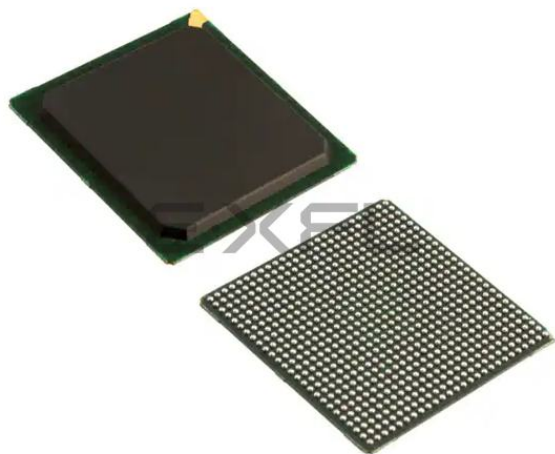




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

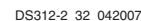
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	3328
Number of Logic Elements/Cells	29952
Total RAM Bits	589824
Number of I/O	487
Number of Gates	1500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1500-4fgg676c



- Options to invert signal polarity as well as other options that enable lines for various functions are not shown.
- The index i can be 6, 7, or 8, depending on the slice. In this position, the upper right-hand slice has an F8MUX, and the upper left-hand slice has an F7MUX. The lower right-hand and left-hand slices both have an F6MUX.

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DFS Clock Output Connections

There are two basic cases that determine how to connect the DFS clock outputs: on-chip and off-chip, which are illustrated in sections [a] and [c], respectively, of [Figure 21](#). This is similar to what has already been described for the DLL component. See [DLL Clock Output and Feedback Connections, page 34](#).

In the on-chip case, it is possible to connect either of the DFS's two output clock signals through general routing resources to the FPGA's internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. The optional feedback loop is formed in this way, routing CLK0 to a global clock net, which in turn drives the CLKFB input.

In the off-chip case, the DFS's two output clock signals, plus CLK0 for an optional feedback loop, can exit the FPGA using output buffers (OBUF) to drive a clock network plus registers on the board. The feedback loop is formed by feeding the CLK0 signal back into the FPGA using an IBUFG, which directly accesses the global clock network, or an IBUF. Then, the global clock net is connected directly to the CLKFB input.

Phase Shifter (PS)

The DCM provides two approaches to controlling the phase of a DCM clock output signal relative to the CLKIN signal: First, there are nine clock outputs that employ the DLL to achieve a desired phase relationship: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, CLKDV CLKFX, and CLKFX180. These outputs afford "coarse" phase control.

The second approach uses the PS component described in this section to provide a still finer degree of control. The PS component is only available when the DLL is operating in its low-frequency mode. The PS component phase shifts the DCM output clocks by introducing a "fine phase shift" (T_{PS}) between the CLKFB and CLKIN signals inside the DLL component. The user can control this fine phase shift down to a resolution of 1/256 of a CLKIN cycle or one tap delay (DCM_TAP), whichever is greater. When in use, the PS component shifts the phase of all nine DCM clock output signals together. If the PS component is used together with a DCM clock output such as the CLK90, CLK180, CLK270, CLK2X180 and CLKFX180, then the fine phase shift of the former gets added to the coarse phase shift of the latter.

PS Component Enabling and Mode Selection

The CLKOUT_PHASE_SHIFT attribute enables the PS component for use in addition to selecting between two operating modes. As described in [Table 20](#), this attribute has three possible values: NONE, FIXED and VARIABLE. When CLKOUT_PHASE_SHIFT is set to NONE, the PS component is disabled and its inputs, PSEN, PSCLK, and PSINCDEC, must be tied to GND. The set of waveforms in section [a] of [Figure 22](#) shows the disabled case, where the DLL maintains a zero-phase alignment of signals CLKFB and CLKIN upon which the PS component has no effect. The PS component is enabled by setting the attribute to either the FIXED or VARIABLE values, which select the Fixed Phase mode and the Variable Phase mode, respectively. These two modes are described in the sections that follow

Determining the Fine Phase Shift

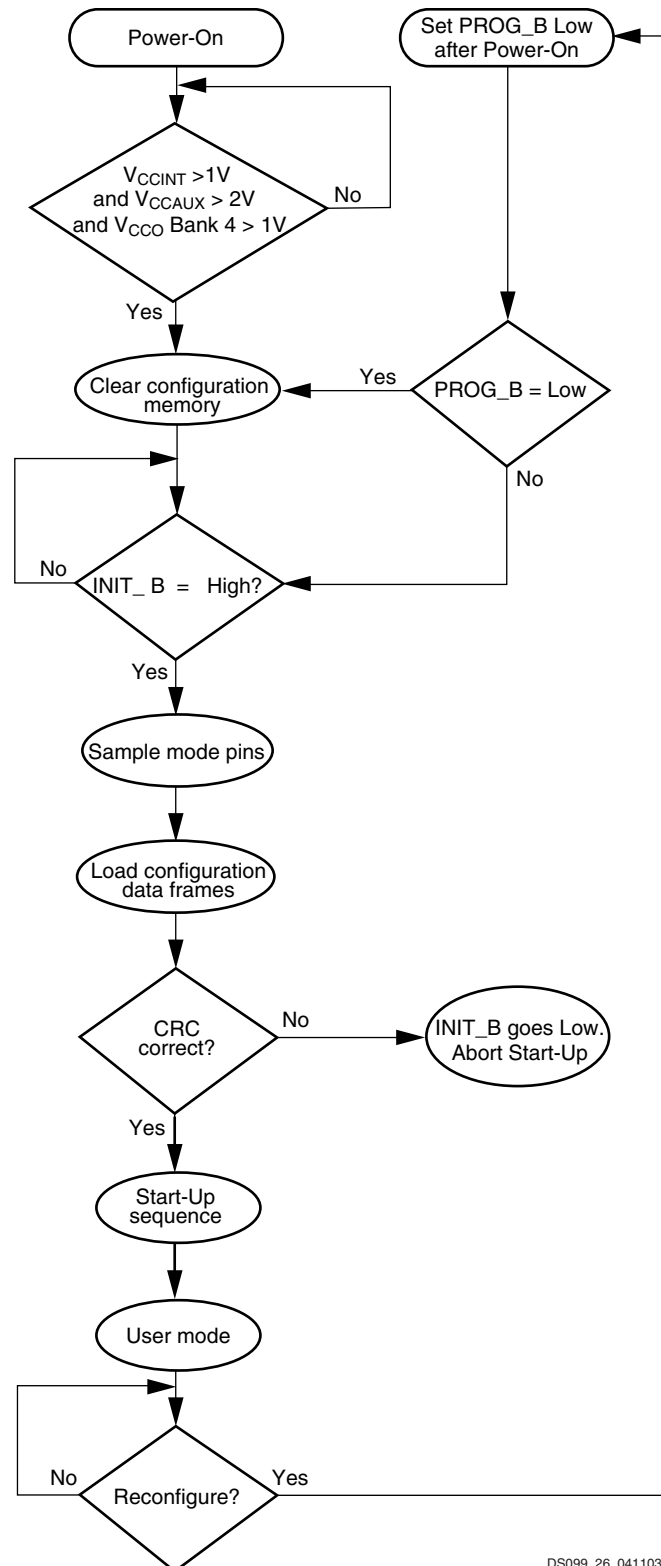
The user controls the phase shift of CLKFB relative to CLKIN by setting and/or adjusting the value of the PHASE_SHIFT attribute. This value must be an integer ranging from -255 to +255. The PS component uses this value to calculate the desired fine phase shift (T_{PS}) as a fraction of the CLKIN period (T_{CLKIN}). Given values for PHASE-SHIFT and T_{CLKIN} , it is possible to calculate T_{PS} as follows:

$$T_{PS} = T_{CLKIN}(\text{PHASE_SHIFT}/256) \quad \text{Equation 4}$$

Both the Fixed Phase and Variable Phase operating modes employ this calculation. If the PHASE_SHIFT value is zero, then CLKFB and CLKIN will be in phase, the same as when the PS component is disabled. When the PHASE_SHIFT value is positive, the CLKFB signal will be shifted later in time with respect to CLKIN. If the attribute value is negative, the CLKFB signal will be shifted earlier in time with respect to CLKIN.

The Fixed Phase Mode

This mode fixes the desired fine phase shift to a fraction of the T_{CLKIN} , as determined by [Equation 4](#) and its user-selected PHASE_SHIFT value P. The set of waveforms in section [b] of [Figure 22](#) illustrates the relationship between CLKFB and CLKIN in the Fixed Phase mode. In the Fixed Phase mode, the PSEN, PSCLK and PSINCDEC inputs are not used and must be tied to GND. Fixed phase shift requires ISE software version 10.1.03 or later.



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Figure 29: Configuration Flow Diagram for the Serial and Parallel Modes

Switching Characteristics

All Spartan-3 devices are available in two speed grades: –4 and the higher performance –5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reported delays may still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Production-quality systems must use FPGA designs compiled using a Production status speed file. FPGAs designs using a less mature speed file designation may only be used during system prototyping or preproduction qualification. FPGA designs using Advance or Preliminary status speed files should never be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

Xilinx ISE Software Updates: <http://www.xilinx.com/support/download/index.htm>

All specified limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the following applies: Parameter values apply to all Spartan-3 devices. All parameters representing voltages are measured with respect to GND.

Selected timing parameters and their representative values are included below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3 FPGA v1.38 speed files are the original source for many but not all of the values. The v1.38 speed files are available in Xilinx Integrated Software Environment (ISE) software version 8.2i.

The speed grade designations for these files are shown in [Table 39](#). For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 39: Spartan-3 FPGA Speed Grade Designations (ISE v8.2i or Later)

Device	Advance	Preliminary	Production
XC3S50			-4, -5 (v1.37 and later)
XC3S200			
XC3S400			
XC3S1000			
XC3S1500			
XC3S2000			
XC3S4000			
XC3S5000			-4, -5 (v1.38 and later)

Table 45: Timing for the IOB Output Path

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max ⁽³⁾	Max ⁽³⁾	
Clock-to-Output Times						
T _{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OTCLK input to data appearing at the Output pin	LVCMOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Propagation Times						
T _{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.46	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.94	2.23	ns
T _{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin		XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Set/Reset Times						
T _{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate	XC3S200 XC3S400	2.10	2.41	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	2.77	3.18	ns
T _{IOGSRQ}	Time from asserting the Global Set Reset (GSR) net to setting/resetting data at the Output pin		All	8.07	9.28	ns

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 48](#) and are based on the operating conditions set forth in [Table 32](#) and [Table 35](#).
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from [Table 47](#).
3. For minimums, use the values reported by the Xilinx timing analyzer.

Table 67: Timing for the Master and Slave Parallel Configuration Modes (Cont'd)

Symbol	Description			Slave/ Master	All Speed Grades		Units
					Min	Max	
Clock Timing							
T _{CCH}	CCLK input pin High pulse width			Slave	5	∞	ns
T _{CCL}	CCLK input pin Low pulse width				5	∞	ns
F _{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Not using the BUSY pin ⁽⁴⁾		0	50	MHz
			Using the BUSY pin		0	66	MHz
		With bitstream compression			0	20	MHz
		During STARTUP phase			0	50	MHz
ΔF _{CCPAR}	Variation from the CCLK output frequency set using the BitGen option ConfigRate			Master	−50%	+50%	—

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 32](#).
2. Some Xilinx documents may refer to Parallel modes as "SelectMAP" modes.
3. RDWR_B is synchronized to CCLK for the purpose of performing the Abort operation. The same pin asynchronously controls the driver impedance of the D0 - D7 pins. To avoid contention when writing configuration data to the D0 - D7 bus, do not bring RDWR_B High when CS_B is Low.
4. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.



Spartan-3 FPGA Family: Pinout Descriptions

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Introduction

This data sheet module describes the various pins on a Spartan®-3 FPGA and how they connect to the supported component packages.

- The [Pin Types](#) section categorizes all of the FPGA pins by their function type.
- The [Pin Definitions](#) section provides a top-level description for each pin on the device.
- The [Detailed, Functional Pin Descriptions](#) section offers significantly more detail about each pin, especially for the dual- or special-function pins used during device configuration.
- Some pins have associated behavior that is controlled by settings in the configuration bitstream. These options are described in the [Bitstream Options](#) section.
- The [Package Overview](#) section describes the various packaging options available for Spartan-3 FPGAs. Detailed pin list tables and footprint diagrams are provided for each package solution.

Pin Descriptions

Pin Types

A majority of the pins on a Spartan-3 FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3 device packages, as outlined in [Table 69](#). In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 69: Types of Pins on Spartan-3 FPGAs

Pin Type/ Color Code	Description	Pin Name
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO, IO_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. There are 12 dual-purpose configuration pins on every package. The INIT_B pin has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM during configuration.	IO_Lxxy_#/DIN/D0, IO_Lxxy_#/D1, IO_Lxxy_#/D2, IO_Lxxy_#/D3, IO_Lxxy_#/D4, IO_Lxxy_#/D5, IO_Lxxy_#/D6, IO_Lxxy_#/D7, IO_Lxxy_#/CS_B, IO_Lxxy_#/RDWR_B, IO_Lxxy_#/BUSY/DOUT, IO_Lxxy_#/INIT_B
CONFIG	Dedicated configuration pin. Not available as a user-I/O pin. Every package has seven dedicated configuration pins. These pins are powered by VCCAUX and have a dedicated internal pull-up resistor to VCCAUX during configuration.	CCLK, DONE, M2, M1, M0, PROG_B, HSWAP_EN
JTAG	Dedicated JTAG pin. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX and have a dedicated internal pull-up resistor to VCCAUX during configuration.	TDI, TMS, TCK, TDO
DCI	Dual-purpose pin that is either a user-I/O pin or used to calibrate output buffer impedance for a specific bank using Digital Controlled Impedance (DCI). There are two DCI pins per I/O bank.	IO/VRN_# IO_Lxxy_#/VRN_# IO/VRP_# IO_Lxxy_#/VRP_#

Table 85: Maximum User I/Os by Package

Device	Package	Maximum User I/Os	Maximum Differential Pairs	All Possible I/O Pins by Type					N.C.
				I/O	DUAL	DCI	VREF	GCLK	
XC3S50	VQ100	63	29	22	12	14	7	8	0
XC3S200	VQ100	63	29	22	12	14	7	8	0
XC3S50	CP132 ⁽¹⁾	89	44	44	12	14	11	8	0
XC3S50	TQ144	97	46	51	12	14	12	8	0
XC3S200	TQ144	97	46	51	12	14	12	8	0
XC3S400	TQ144	97	46	51	12	14	12	8	0
XC3S50	PQ208	124	56	72	12	16	16	8	17
XC3S200	PQ208	141	62	83	12	16	22	8	0
XC3S400	PQ208	141	62	83	12	16	22	8	0
XC3S200	FT256	173	76	113	12	16	24	8	0
XC3S400	FT256	173	76	113	12	16	24	8	0
XC3S1000	FT256	173	76	113	12	16	24	8	0
XC3S400	FG320	221	100	156	12	16	29	8	0
XC3S1000	FG320	221	100	156	12	16	29	8	0
XC3S1500	FG320	221	100	156	12	16	29	8	0
XC3S400	FG456	264	116	196	12	16	32	8	69
XC3S1000	FG456	333	149	261	12	16	36	8	0
XC3S1500	FG456	333	149	261	12	16	36	8	0
XC3S2000	FG456	333	149	261	12	16	36	8	0
XC3S1000	FG676	391	175	315	12	16	40	8	98
XC3S1500	FG676	487	221	403	12	16	48	8	2
XC3S2000	FG676	489	221	405	12	16	48	8	0
XC3S4000	FG676	489	221	405	12	16	48	8	0
XC3S5000	FG676	489	221	405	12	16	48	8	0
XC3S2000	FG900	565	270	481	12	16	48	8	68
XC3S4000	FG900	633	300	549	12	16	48	8	0
XC3S5000	FG900	633	300	549	12	16	48	8	0
XC3S4000	FG1156 ⁽¹⁾	712	312	621	12	16	55	8	73
XC3S5000	FG1156 ⁽¹⁾	784	344	692	12	16	56	8	1

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Electronic versions of the package pinout tables and footprints are available for download from the Xilinx website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs. Download the files from the following location:

http://www.xilinx.com/support/documentation/data_sheets/s3_pin.zip

Table 96: FT256 Package Pinout (Cont'd)

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
1	IO_L10N_1/VREF_1	A13	VREF
1	IO_L10P_1	B13	I/O
1	IO_L27N_1	B12	I/O
1	IO_L27P_1	C12	I/O
1	IO_L28N_1	D11	I/O
1	IO_L28P_1	E11	I/O
1	IO_L29N_1	B11	I/O
1	IO_L29P_1	C11	I/O
1	IO_L30N_1	D10	I/O
1	IO_L30P_1	E10	I/O
1	IO_L31N_1/VREF_1	A10	VREF
1	IO_L31P_1	B10	I/O
1	IO_L32N_1/GCLK5	C9	GCLK
1	IO_L32P_1/GCLK4	D9	GCLK
1	VCCO_1	E9	VCCO
1	VCCO_1	F9	VCCO
1	VCCO_1	F10	VCCO
2	IO	G16	I/O
2	IO_L01N_2/VRP_2	B16	DCI
2	IO_L01P_2/VRN_2	C16	DCI
2	IO_L16N_2	C15	I/O
2	IO_L16P_2	D14	I/O
2	IO_L17N_2	D15	I/O
2	IO_L17P_2/VREF_2	D16	VREF
2	IO_L19N_2	E13	I/O
2	IO_L19P_2	E14	I/O
2	IO_L20N_2	E15	I/O
2	IO_L20P_2	E16	I/O
2	IO_L21N_2	F12	I/O
2	IO_L21P_2	F13	I/O
2	IO_L22N_2	F14	I/O
2	IO_L22P_2	F15	I/O
2	IO_L23N_2/VREF_2	G12	VREF
2	IO_L23P_2	G13	I/O
2	IO_L24N_2	G14	I/O
2	IO_L24P_2	G15	I/O
2	IO_L39N_2	H13	I/O
2	IO_L39P_2	H14	I/O
2	IO_L40N_2	H15	I/O
2	IO_L40P_2/VREF_2	H16	VREF

Table 96: FT256 Package Pinout (Cont'd)

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
N/A	GND	T16	GND
N/A	VCCAUX	A6	VCCAUX
N/A	VCCAUX	A11	VCCAUX
N/A	VCCAUX	F1	VCCAUX
N/A	VCCAUX	F16	VCCAUX
N/A	VCCAUX	L1	VCCAUX
N/A	VCCAUX	L16	VCCAUX
N/A	VCCAUX	T6	VCCAUX
N/A	VCCAUX	T11	VCCAUX
N/A	VCCINT	D4	VCCINT
N/A	VCCINT	D13	VCCINT
N/A	VCCINT	E5	VCCINT
N/A	VCCINT	E12	VCCINT
N/A	VCCINT	M5	VCCINT
N/A	VCCINT	M12	VCCINT
N/A	VCCINT	N4	VCCINT
N/A	VCCINT	N13	VCCINT
VCCAUX	CCLK	T15	CONFIG
VCCAUX	DONE	R14	CONFIG
VCCAUX	HSWAP_EN	C4	CONFIG
VCCAUX	M0	P3	CONFIG
VCCAUX	M1	T2	CONFIG
VCCAUX	M2	P4	CONFIG
VCCAUX	PROG_B	B3	CONFIG
VCCAUX	TCK	C14	JTAG
VCCAUX	TDI	A2	JTAG
VCCAUX	TDO	A15	JTAG
VCCAUX	TMS	C13	JTAG

FG456 Footprint

Left Half of FG456 Package (Top View)

XC3S400

(264 max. user I/O)

196 I/O: Unrestricted, general-purpose user I/O

32 VREF: User I/O or input voltage reference for bank

69 N.C.: Unconnected pins for XC3S400 (◆)

XC3S1000, XC3S1500, XC3S2000 (333 max user I/O)

261 I/O: Unrestricted, general-purpose user I/O

36 VREF: User I/O or input voltage reference for bank

0 N.C.: No unconnected pins in this package

All devices

12 DUAL: Configuration pin, then possible user I/O

8 GCLK: User I/O or global clock buffer input

16 DCI: User I/O or reference resistor input for bank

7 CONFIG: Dedicated configuration pins

4 JTAG: Dedicated JTAG port pins

12 VCCINT: Internal core voltage supply (+1.2V)

40 VCCO: Output voltage supply for bank

8 VCCAUX: Auxiliary voltage supply (+2.5V)

52 GND: Ground

		Bank 0										
		1	2	3	4	5	6	7	8	9	10	11
Bank 7	A	GND	PROG_B	I/O VREF_0	I/O L01P_0 VRN_0	I/O L09P_0	VCCAUX	I/O L19P_0	I/O L24P_0	I/O L27P_0	I/O	I/O L32P_0 GCLK6
	B	TDI	GND	HSWAP_EN	I/O L01N_0 VRP_0	I/O L09N_0	I/O L15P_0	I/O L19N_0	I/O L24N_0	I/O L27N_0	I/O L29P_0	I/O L32N_0 GCLK7
	C	I/O L16P_7 VREF_7	I/O	I/O L01N_7 VRP_7	I/O L01P_7 VRN_7	I/O L06P_0	I/O L15N_0	I/O VREF_0	VCCO_0	GND	I/O L29N_0	I/O L31P_0 VREF_0
	D	I/O L16N_7	I/O L19P_7	I/O L19N_7 VREF_7	I/O L17P_7	I/O L06N_0	I/O L10P_0	I/O L16P_0	I/O L22P_0	I/O	I/O	I/O L31N_0
	E	I/O L21N_7	I/O L21P_7	I/O L20P_7	I/O L17N_7	I/O VREF_0	I/O L10N_0	I/O L16N_0	I/O L22N_0	I/O L25P_0	I/O L28P_0	I/O L30P_0
	F	VCCAUX	I/O L23N_7	I/O L23P_7	I/O L20N_7	I/O L22P_7	I/O	I/O VREF_0	VCCO_0	I/O L25N_0	I/O L28N_0	I/O L30N_0
	G	I/O L27N_7	I/O L27P_7 VREF_7	I/O L26N_7	I/O L26P_7	I/O L24P_7	I/O L22N_7	VCCINT	VCCINT	VCCO_0	VCCO_0	VCCO_0
	H	I/O L28N_7	I/O L28P_7	VCCO_7	I/O L29P_7	I/O L24N_7	VCCO_7	VCCINT				
	J	I/O L32N_7	I/O L32P_7	GND	I/O L29N_7	I/O L31N_7	I/O L31P_7	VCCO_7		GND	GND	GND
	K	I/O L35N_7	I/O L35P_7	I/O L34N_7	I/O L34P_7	I/O L33N_7	I/O L33P_7	VCCO_7		GND	GND	GND
	L	I/O L40N_7 VREF_7	I/O L40P_7	I/O L39N_7	I/O L39P_7	I/O L38N_7	I/O L38P_7	VCCO_7		GND	GND	GND
	M	I/O L40P_6 VREF_6	I/O L40N_6	I/O L39P_6	I/O L39N_6	I/O L38P_6	I/O L38N_6	VCCO_6		GND	GND	GND
	N	I/O L35P_6	I/O L35N_6	I/O L34P_6	I/O L34N_6 VREF_6	I/O L33P_6	I/O L33N_6	VCCO_6		GND	GND	GND
	P	I/O L32P_6	I/O L32N_6	GND	I/O L31P_6	I/O L31N_6	I/O L28P_6	VCCO_6		GND	GND	GND
	R	I/O L29P_6	I/O L29N_6	VCCO_6	I/O L26P_6	I/O L28N_6	VCCO_6	VCCINT				
Bank 6	T	I/O L27P_6	I/O L27N_6	I/O L26N_6	I/O L23P_6	I/O L22P_6	I/O L22N_6	VCCINT	VCCINT	VCCO_5	VCCO_5	VCCO_5
	U	VCCAUX	I/O L24P_6	I/O L24N_6 VREF_6	I/O L23N_6	I/O L19P_6	I/O VREF_5	I/O	VCCO_5	I/O	I/O	I/O
	V	I/O L21P_6	I/O L21N_6	I/O L20P_6	I/O L20N_6	I/O L19N_6	I/O L15P_5	I/O	I/O L24P_5	I/O L27P_5	I/O	I/O L31P_5 D5
	W	I/O L17P_6 VREF_6	I/O L17N_6	I/O L16P_6	I/O L16N_6	I/O L09P_5	I/O L15N_5	I/O L19P_5 VREF_5	I/O L24N_5	I/O L27N_5 VREF_5	I/O L29P_5	I/O L31N_5 D4
	Y	I/O	I/O L01P_6 VRN_6	I/O L01N_6 VRP_6	I/O L01N_5 RDWR_B	I/O L09N_5	I/O L16P_5	I/O L19N_5	VCCO_5	GND	I/O L29N_5	I/O L32P_5 GCLK2
	A A	M1	GND	I/O L01P_5 CS_B	I/O L06P_5	I/O L10P_5 VRN_5	I/O L16N_5	I/O L22P_5	I/O L25P_5	I/O L28P_5 D7	I/O L30P_5	I/O L32N_5 GCLK3
	A B	GND	M0	M2	I/O L06N_5	I/O L10N_5 VRP_5	VCCAUX	I/O L22N_5	I/O L25N_5	I/O L28N_5 D6	I/O L30N_5	I/O VREF_5
		Bank 5										

Figure 51: FG456 Package Footprint (Top View)

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Table 103: FG676 Package Pinout (Cont'd)

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AB5	DUAL
5	IO_L04N_5	IO_L04N_5	IO_L04N_5	IO_L04N_5	IO_L04N_5	AE4	I/O
5	IO_L04P_5	IO_L04P_5	IO_L04P_5	IO_L04P_5	IO_L04P_5	AD4	I/O
5	IO_L05N_5	IO_L05N_5	IO_L05N_5	IO_L05N_5	IO_L05N_5	AB6	I/O
5	IO_L05P_5	IO_L05P_5	IO_L05P_5	IO_L05P_5	IO_L05P_5	AA6	I/O
5	IO_L06N_5	IO_L06N_5	IO_L06N_5	IO_L06N_5	IO_L06N_5	AE5	I/O
5	IO_L06P_5	IO_L06P_5	IO_L06P_5	IO_L06P_5	IO_L06P_5	AD5	I/O
5	IO_L07N_5	IO_L07N_5	IO_L07N_5	IO_L07N_5	IO_L07N_5	AD6	I/O
5	IO_L07P_5	IO_L07P_5	IO_L07P_5	IO_L07P_5	IO_L07P_5	AC6	I/O
5	IO_L08N_5	IO_L08N_5	IO_L08N_5	IO_L08N_5	IO_L08N_5	AF6	I/O
5	IO_L08P_5	IO_L08P_5	IO_L08P_5	IO_L08P_5	IO_L08P_5	AE6	I/O
5	IO_L09N_5	IO_L09N_5	IO_L09N_5	IO_L09N_5	IO_L09N_5	AC7	I/O
5	IO_L09P_5	IO_L09P_5	IO_L09P_5	IO_L09P_5	IO_L09P_5	AB7	I/O
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	AF7	DCI
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	AE7	DCI
5	N.C. (◆)	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	AB8	VREF
5	N.C. (◆)	IO_L11P_5	IO_L11P_5	IO_L11P_5	IO_L11P_5	AA8	I/O
5	N.C. (◆)	IO_L12N_5	IO_L12N_5	IO_L12N_5	IO_L12N_5	AD8	I/O
5	N.C. (◆)	IO_L12P_5	IO_L12P_5	IO_L12P_5	IO_L12P_5	AC8	I/O
5	IO_L15N_5	IO_L15N_5	IO_L15N_5	IO_L15N_5	IO_L15N_5	AF8	I/O
5	IO_L15P_5	IO_L15P_5	IO_L15P_5	IO_L15P_5	IO_L15P_5	AE8	I/O
5	IO_L16N_5	IO_L16N_5	IO_L16N_5	IO_L16N_5	IO_L16N_5	AA9	I/O
5	IO_L16P_5	IO_L16P_5	IO_L16P_5	IO_L16P_5	IO_L16P_5	Y9	I/O
5	N.C. (◆)	IO_L18N_5	IO_L18N_5	IO_L18N_5	IO_L18N_5	AE9	I/O
5	N.C. (◆)	IO_L18P_5	IO_L18P_5	IO_L18P_5	IO_L18P_5	AD9	I/O
5	IO_L19N_5	IO_L19N_5	IO_L19N_5	IO_L19N_5	IO_L19N_5	AA10	I/O
5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	Y10	VREF
5	IO_L22N_5	IO_L22N_5	IO_L22N_5	IO_L22N_5	IO_L22N_5	AC10	I/O
5	IO_L22P_5	IO_L22P_5	IO_L22P_5	IO_L22P_5	IO_L22P_5	AB10	I/O
5	N.C. (◆)	IO_L23N_5	IO_L23N_5	IO_L23N_5	IO_L23N_5	AF10	I/O
5	N.C. (◆)	IO_L23P_5	IO_L23P_5	IO_L23P_5	IO_L23P_5	AE10	I/O
5	IO_L24N_5	IO_L24N_5	IO_L24N_5	IO_L24N_5	IO_L24N_5	Y11	I/O
5	IO_L24P_5	IO_L24P_5	IO_L24P_5	IO_L24P_5	IO_L24P_5	W11	I/O
5	IO_L25N_5	IO_L25N_5	IO_L25N_5	IO_L25N_5	IO_L25N_5	AB11	I/O
5	IO_L25P_5	IO_L25P_5	IO_L25P_5	IO_L25P_5	IO_L25P_5	AA11	I/O
5	N.C. (◆)	IO_L26N_5	IO_L26N_5	IO_L26N_5	IO_L26N_5	AF11	I/O
5	N.C. (◆)	IO_L26P_5	IO_L26P_5	IO_L26P_5	IO_L26P_5	AE11	I/O
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	Y12	VREF
5	IO_L27P_5	IO_L27P_5	IO_L27P_5	IO_L27P_5	IO_L27P_5	W12	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	AB12	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	AA12	DUAL
5	IO_L29N_5	IO_L29N_5	IO_L29N_5	IO_L29N_5	IO_L29N_5	AF12	I/O

Table 103: FG676 Package Pinout (Cont'd)

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
7	IO_L29P_7	IO_L29P_7	IO_L29P_7	IO_L29P_7	IO_L29P_7	L2	I/O
7	IO_L31N_7	IO_L31N_7	IO_L31N_7	IO_L31N_7	IO_L31N_7	M7	I/O
7	IO_L31P_7	IO_L31P_7	IO_L31P_7	IO_L31P_7	IO_L31P_7	M8	I/O
7	IO_L32N_7	IO_L32N_7	IO_L32N_7	IO_L32N_7	IO_L32N_7	M6	I/O
7	IO_L32P_7	IO_L32P_7	IO_L32P_7	IO_L32P_7	IO_L32P_7	M5	I/O
7	IO_L33N_7	IO_L33N_7	IO_L33N_7	IO_L33N_7	IO_L33N_7	M3	I/O
7	IO_L33P_7	IO_L33P_7	IO_L33P_7	IO_L33P_7	IO_L33P_7	L4	I/O
7	IO_L34N_7	IO_L34N_7	IO_L34N_7	IO_L34N_7	IO_L34N_7	M1	I/O
7	IO_L34P_7	IO_L34P_7	IO_L34P_7	IO_L34P_7	IO_L34P_7	M2	I/O
7	IO_L35N_7	IO_L35N_7	IO_L35N_7	IO_L35N_7	IO_L35N_7	N7	I/O
7	IO_L35P_7	IO_L35P_7	IO_L35P_7	IO_L35P_7	IO_L35P_7	N8	I/O
7	IO_L38N_7	IO_L38N_7	IO_L38N_7	IO_L38N_7	IO_L38N_7	N5	I/O
7	IO_L38P_7	IO_L38P_7	IO_L38P_7	IO_L38P_7	IO_L38P_7	N6	I/O
7	IO_L39N_7	IO_L39N_7	IO_L39N_7	IO_L39N_7	IO_L39N_7	N3	I/O
7	IO_L39P_7	IO_L39P_7	IO_L39P_7	IO_L39P_7	IO_L39P_7	N4	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	N1	VREF
7	IO_L40P_7	IO_L40P_7	IO_L40P_7	IO_L40P_7	IO_L40P_7	N2	I/O
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	G3	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	J8	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	K8	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	L3	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	L9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	M9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	N9	VCCO
7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	VCCO_7	N10	VCCO
N/A	GND	GND	GND	GND	GND	A1	GND
N/A	GND	GND	GND	GND	GND	A26	GND
N/A	GND	GND	GND	GND	GND	AC4	GND
N/A	GND	GND	GND	GND	GND	AC12	GND
N/A	GND	GND	GND	GND	GND	AC15	GND
N/A	GND	GND	GND	GND	GND	AC23	GND
N/A	GND	GND	GND	GND	GND	AD3	GND
N/A	GND	GND	GND	GND	GND	AD24	GND
N/A	GND	GND	GND	GND	GND	AE2	GND
N/A	GND	GND	GND	GND	GND	AE25	GND
N/A	GND	GND	GND	GND	GND	AF1	GND
N/A	GND	GND	GND	GND	GND	AF26	GND
N/A	GND	GND	GND	GND	GND	B2	GND
N/A	GND	GND	GND	GND	GND	B25	GND
N/A	GND	GND	GND	GND	GND	C3	GND
N/A	GND	GND	GND	GND	GND	C24	GND
N/A	GND	GND	GND	GND	GND	D4	GND
N/A	GND	GND	GND	GND	GND	D12	GND

Table 103: FG676 Package Pinout (Cont'd)

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	U17	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	U18	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V9	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V10	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V17	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V18	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	W8	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	W19	VCCINT
VCC AUX	CCLK	CCLK	CCLK	CCLK	CCLK	AD26	CONFIG
VCC AUX	DONE	DONE	DONE	DONE	DONE	AC24	CONFIG
VCC AUX	HSWAP_EN	HSWAP_EN	HSWAP_EN	HSWAP_EN	HSWAP_EN	C2	CONFIG
VCC AUX	M0	M0	M0	M0	M0	AE3	CONFIG
VCC AUX	M1	M1	M1	M1	M1	AC3	CONFIG
VCC AUX	M2	M2	M2	M2	M2	AF3	CONFIG
VCC AUX	PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	D3	CONFIG
VCC AUX	TCK	TCK	TCK	TCK	TCK	B24	JTAG
VCC AUX	TDI	TDI	TDI	TDI	TDI	C1	JTAG
VCC AUX	TDO	TDO	TDO	TDO	TDO	D24	JTAG
VCC AUX	TMS	TMS	TMS	TMS	TMS	A24	JTAG

Notes:

- XC3S1500 balls D25 and F25 are not VREF pins although they are designated as such. If a design uses an IOSTANDARD requiring VREF in bank 2 then apply the workaround in [Answer Record 20519](#).
- XC3S4000 is pin compatible with XC3S2000 but uses alternate differential pair labeling on six package balls (H20, H21, H22, H23, H24, J21).
- XC3S5000 is pin compatible with XC3S4000 but uses alternate differential pair functionality on fifteen package balls (A3, A8, B8, B18, C4, C8, C18, D8, D18, E8, E18, H23, H24, AB9, and AC9).

FG900: 900-lead Fine-pitch Ball Grid Array

The 900-lead fine-pitch ball grid array package, FG900, supports three different Spartan-3 devices, including the XC3S2000, the XC3S4000, and the XC3S5000. The footprints for the XC3S4000 and XC3S5000 are identical, as shown in [Table 107](#) and [Figure 55](#). The XC3S2000, however, has fewer I/O pins which consequently results in 68 unconnected pins on the FG900 package, labeled as “N.C.” In [Table 107](#) and [Figure 55](#), these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in [Table 107](#) and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S2000 pinout and the pinout for the XC3S4000 and XC3S5000, then that difference is highlighted in [Table 107](#). If the table entry is shaded, then there is an unconnected pin on the XC3S2000 that maps to a user-I/O pin on the XC3S4000 and XC3S5000.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_sheets/s3_pin.zip.

Pinout Table

Table 107: FG900 Package Pinout

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO	IO	E15	I/O
0	IO	IO	K15	I/O
0	IO	IO	D13	I/O
0	IO	IO	K13	I/O
0	IO	IO	G8	I/O
0	IO/VREF_0	IO/VREF_0	F9	VREF
0	IO/VREF_0	IO/VREF_0	C4	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L02N_0	IO_L02N_0	B5	I/O
0	IO_L02P_0	IO_L02P_0	A5	I/O
0	IO_L03N_0	IO_L03N_0	D5	I/O
0	IO_L03P_0	IO_L03P_0	E6	I/O
0	IO_L04N_0	IO_L04N_0	C6	I/O
0	IO_L04P_0	IO_L04P_0	B6	I/O
0	IO_L05N_0	IO_L05N_0	F6	I/O
0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	F7	VREF
0	IO_L06N_0	IO_L06N_0	D7	I/O
0	IO_L06P_0	IO_L06P_0	C7	I/O
0	IO_L07N_0	IO_L07N_0	F8	I/O
0	IO_L07P_0	IO_L07P_0	E8	I/O
0	IO_L08N_0	IO_L08N_0	D8	I/O
0	IO_L08P_0	IO_L08P_0	C8	I/O
0	IO_L09N_0	IO_L09N_0	B8	I/O
0	IO_L09P_0	IO_L09P_0	A8	I/O

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
1	IO_L25P_1	IO_L25P_1	D19	I/O
1	IO_L26N_1	IO_L26N_1	A19	I/O
1	IO_L26P_1	IO_L26P_1	B19	I/O
1	IO_L27N_1	IO_L27N_1	F17	I/O
1	IO_L27P_1	IO_L27P_1	G17	I/O
1	IO_L28N_1	IO_L28N_1	B17	I/O
1	IO_L28P_1	IO_L28P_1	C17	I/O
1	IO_L29N_1	IO_L29N_1	J16	I/O
1	IO_L29P_1	IO_L29P_1	K16	I/O
1	IO_L30N_1	IO_L30N_1	G16	I/O
1	IO_L30P_1	IO_L30P_1	H16	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D16	VREF
1	IO_L31P_1	IO_L31P_1	E16	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B16	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C16	GCLK
1	N.C. (◆)	IO_L37N_1	H18	I/O
1	N.C. (◆)	IO_L37P_1	J18	I/O
1	N.C. (◆)	IO_L38N_1	D18	I/O
1	N.C. (◆)	IO_L38P_1	E18	I/O
1	N.C. (◆)	IO_L39N_1	A18	I/O
1	N.C. (◆)	IO_L39P_1	B18	I/O
1	N.C. (◆)	IO_L40N_1	K17	I/O
1	N.C. (◆)	IO_L40P_1	K18	I/O
1	VCCO_1	VCCO_1	L17	VCCO
1	VCCO_1	VCCO_1	C18	VCCO
1	VCCO_1	VCCO_1	G18	VCCO
1	VCCO_1	VCCO_1	L18	VCCO
1	VCCO_1	VCCO_1	L19	VCCO
1	VCCO_1	VCCO_1	J20	VCCO
1	VCCO_1	VCCO_1	C22	VCCO
1	VCCO_1	VCCO_1	G22	VCCO
1	VCCO_1	VCCO_1	E24	VCCO
1	VCCO_1	VCCO_1	C26	VCCO
2	IO	IO	J25	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C29	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C30	DCI
2	IO_L02N_2	IO_L02N_2	D27	I/O
2	IO_L02P_2	IO_L02P_2	D28	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	D29	VREF
2	IO_L03P_2	IO_L03P_2	D30	I/O

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
4	IO_L11P_4	IO_L11P_4	AE21	I/O
4	IO_L12N_4	IO_L12N_4	AH21	I/O
4	IO_L12P_4	IO_L12P_4	AJ21	I/O
4	IO_L13N_4	IO_L13N_4	AB21	I/O
4	IO_L13P_4	IO_L13P_4	AA20	I/O
4	IO_L14N_4	IO_L14N_4	AC20	I/O
4	IO_L14P_4	IO_L14P_4	AD20	I/O
4	IO_L15N_4	IO_L15N_4	AE20	I/O
4	IO_L15P_4	IO_L15P_4	AF20	I/O
4	IO_L16N_4	IO_L16N_4	AG20	I/O
4	IO_L16P_4	IO_L16P_4	AH20	I/O
4	IO_L17N_4	IO_L17N_4	AJ20	I/O
4	IO_L17P_4	IO_L17P_4	AK20	I/O
4	IO_L18N_4	IO_L18N_4	AA19	I/O
4	IO_L18P_4	IO_L18P_4	AB19	I/O
4	IO_L19N_4	IO_L19N_4	AC19	I/O
4	IO_L19P_4	IO_L19P_4	AD19	I/O
4	IO_L20N_4	IO_L20N_4	AE19	I/O
4	IO_L20P_4	IO_L20P_4	AF19	I/O
4	IO_L21N_4	IO_L21N_4	AG19	I/O
4	IO_L21P_4	IO_L21P_4	AH19	I/O
4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	AJ19	VREF
4	IO_L22P_4	IO_L22P_4	AK19	I/O
4	IO_L23N_4	IO_L23N_4	AB18	I/O
4	IO_L23P_4	IO_L23P_4	AC18	I/O
4	IO_L24N_4	IO_L24N_4	AE18	I/O
4	IO_L24P_4	IO_L24P_4	AF18	I/O
4	IO_L25N_4	IO_L25N_4	AJ18	I/O
4	IO_L25P_4	IO_L25P_4	AK18	I/O
4	IO_L26N_4	IO_L26N_4	AA17	I/O
4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	AB17	VREF
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	AD17	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	AE17	DUAL
4	IO_L28N_4	IO_L28N_4	AH17	I/O
4	IO_L28P_4	IO_L28P_4	AJ17	I/O
4	IO_L29N_4	IO_L29N_4	AB16	I/O
4	IO_L29P_4	IO_L29P_4	AC16	I/O
4	IO_L30N_4/D2	IO_L30N_4/D2	AD16	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	AE16	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	AG16	DUAL

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	GND	GND	R17	GND
N/A	GND	GND	T17	GND
N/A	GND	GND	U17	GND
N/A	GND	GND	V17	GND
N/A	GND	GND	AC17	GND
N/A	GND	GND	AF17	GND
N/A	GND	GND	AK17	GND
N/A	GND	GND	N18	GND
N/A	GND	GND	P18	GND
N/A	GND	GND	R18	GND
N/A	GND	GND	T18	GND
N/A	GND	GND	U18	GND
N/A	GND	GND	V18	GND
N/A	GND	GND	R19	GND
N/A	GND	GND	T19	GND
N/A	GND	GND	A21	GND
N/A	GND	GND	E21	GND
N/A	GND	GND	H21	GND
N/A	GND	GND	AC21	GND
N/A	GND	GND	AF21	GND
N/A	GND	GND	AK21	GND
N/A	GND	GND	K23	GND
N/A	GND	GND	P23	GND
N/A	GND	GND	U23	GND
N/A	GND	GND	AA23	GND
N/A	GND	GND	A25	GND
N/A	GND	GND	AK25	GND
N/A	GND	GND	E26	GND
N/A	GND	GND	K26	GND
N/A	GND	GND	P26	GND
N/A	GND	GND	U26	GND
N/A	GND	GND	AA26	GND
N/A	GND	GND	AF26	GND
N/A	GND	GND	A29	GND
N/A	GND	GND	B29	GND
N/A	GND	GND	AJ29	GND
N/A	GND	GND	AK29	GND
N/A	GND	GND	A30	GND
N/A	GND	GND	B30	GND
N/A	GND	GND	F30	GND

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
6	IO_L37N_6	IO_L37N_6	W3	I/O
6	IO_L37P_6	IO_L37P_6	W2	I/O
6	IO_L38N_6	IO_L38N_6	V6	I/O
6	IO_L38P_6	IO_L38P_6	V5	I/O
6	IO_L39N_6	IO_L39N_6	V4	I/O
6	IO_L39P_6	IO_L39P_6	V3	I/O
6	IO_L40N_6	IO_L40N_6	V2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	V1	VREF
6	N.C. (◆)	IO_L41N_6	AH4	I/O
6	N.C. (◆)	IO_L41P_6	AH3	I/O
6	N.C. (◆)	IO_L44N_6	AD7	I/O
6	N.C. (◆)	IO_L44P_6	AD6	I/O
6	IO_L45N_6	IO_L45N_6	AC4	I/O
6	IO_L45P_6	IO_L45P_6	AC3	I/O
6	N.C. (◆)	IO_L46N_6	AA10	I/O
6	N.C. (◆)	IO_L46P_6	AA9	I/O
6	IO_L48N_6	IO_L48N_6	Y7	I/O
6	IO_L48P_6	IO_L48P_6	Y6	I/O
6	N.C. (◆)	IO_L49N_6	W11	I/O
6	N.C. (◆)	IO_L49P_6	V11	I/O
6	IO_L52N_6	IO_L52N_6	V8	I/O
6	IO_L52P_6	IO_L52P_6	V7	I/O
6	VCCO_6	VCCO_6	AA12	VCCO
6	VCCO_6	VCCO_6	AB12	VCCO
6	VCCO_6	VCCO_6	AB2	VCCO
6	VCCO_6	VCCO_6	AB6	VCCO
6	VCCO_6	VCCO_6	AD4	VCCO
6	VCCO_6	VCCO_6	AD8	VCCO
6	VCCO_6	VCCO_6	AG3	VCCO
6	VCCO_6	VCCO_6	AG7	VCCO
6	VCCO_6	VCCO_6	AL3	VCCO
6	VCCO_6	VCCO_6	W12	VCCO
6	VCCO_6	VCCO_6	W4	VCCO
6	VCCO_6	VCCO_6	Y12	VCCO
6	VCCO_6	VCCO_6	Y8	VCCO
7	IO	IO	G1	I/O
7	IO	IO	G2	I/O
7	IO	IO	U10	I/O
7	IO	IO	U9	I/O
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	C1	DCI

Revision History

Date	Version	Description
04/03/03	1.0	Initial Xilinx release.
04/21/03	1.1	Added information on the VQ100 package footprint, including a complete pinout table (Table 87) and footprint diagram (Figure 44). Updated Table 85 with final I/O counts for the VQ100 package. Also added final differential I/O pair counts for the TQ144 package. Added clarifying comments to HSWAP_EN pin description on page 119 . Updated the footprint diagram for the FG900 package shown in Figure 55a and Figure 55b . Some thick lines separating I/O banks were incorrect. Made cosmetic changes to Figure 40 , Figure 42 , and Figure 43 . Updated Xilinx hypertext links. Added XC3S200 and XC3S400 to Pin Name column in Table 91 .
05/12/03	1.1.1	AM32 pin was missing GND label in FG1156 package diagram (Figure 53).
07/11/03	1.1.2	Corrected misspellings of GCLK in Table 69 and Table 70 . Changed CMOS25 to LVCMOS25 in Dual-Purpose Pin I/O Standard During Configuration section. Clarified references to Module 2. For XC3S5000 in FG1156 package, corrected N.C. symbol to a black square in Table 110 , key, and package drawing.
07/29/03	1.2	Corrected pin names on FG1156 package. Some package balls incorrectly included LVDS pair names. The affected balls on the FG1156 package include G1, G2, G33, G34, U9, U10, U25, U26, V9, V10, V25, V26, AH1, AH2, AH33, AH34. The number of LVDS pairs is unaffected. Modified affected balls and re-sorted rows in Table 110 . Updated affected balls in Figure 53 . Also updated ASCII and Excel electronic versions of FG1156 pinout.
08/19/03	1.2.1	Removed 100 MHz ConfigRate option in CCLK: Configuration Clock section and in Table 80 . Added note that TDO is a totem-pole output in Table 77 .
10/09/03	1.2.2	Some pins had incorrect bank designations and were improperly sorted in Table 93 . No pin names or functions changed. Renamed DCI_IN to DCI and added black diamond to N.C. pins in Table 93 . In Figure 47 , removed some extraneous text from pin 106 and corrected spelling of pins 45, 48, and 81.
12/17/03	1.3	Added FG320 pin tables and pinout diagram (FG320: 320-lead Fine-pitch Ball Grid Array). Made cosmetic changes to the TQ144 footprint (Figure 46), the PQ208 footprint (Figure 47), the FG676 footprint (Figure 53), and the FG900 footprint (Figure 55). Clarified wording in Precautions When Using the JTAG Port in 3.3V Environments section.
02/27/04	1.4	Clarified wording in Using JTAG Port After Configuration section. In Table 81 , reduced package height for FG320 and increased maximum I/O values for the FG676, FG900, and FG1156 packages.
07/13/04	1.5	Added information on lead-free (Pb-free) package options to the Package Overview section plus Table 81 and Table 83 . Clarified the VRN_# reference resistor requirements for I/O standards that use single termination as described in the DCI Termination Types section and in Figure 42b . Graduated from Advance Product Specification to Product Specification.
08/24/04	1.5.1	Removed XC3S2000 references from FG1156: 1156-lead Fine-pitch Ball Grid Array .
01/17/05	1.6	Added XC3S50 in CP132 package option. Added XC3S2000 in FG456 package option. Added XC3S4000 in FG676 package option. Added Selecting the Right Package Option section. Modified or added Table 81 , Table 83 , Table 84 , Table 85 , Table 89 , Table 90 , Table 100 , Table 102 , Table 103 , Table 106 , Figure 45 , and Figure 53 .
08/19/05	1.7	Removed term “weak” from the description of pull-up and pull-down resistors. Added IDCODE Register values. Added signal integrity precautions to CCLK: Configuration Clock and indicated that CCLK should be treated as an I/O during Master mode in Table 79 .
04/03/06	2.0	Added Package Thermal Characteristics . Updated Figure 41 to make it a more obvious example. Added detail about which pins have dedicated pull-up resistors during configuration, regardless of the HSWAP_EN value to Table 70 and to Pin Behavior During Configuration . Updated Precautions When Using the JTAG Port in 3.3V Environments .
04/26/06	2.1	Corrected swapped data row in Table 86 . The Theta-JA with zero airflow column was swapped with the Theta-JC column. Made additional notations on CONFIG and JTAG pins that have pull-up resistors during configuration, regardless of the HSWAP_EN input.
05/25/07	2.2	Added link on page 128 to Material Declaration Data Sheets. Corrected units typo in Table 74 . Added Note 1 to Table 103 about VREF for XC3S1500 in FG676.