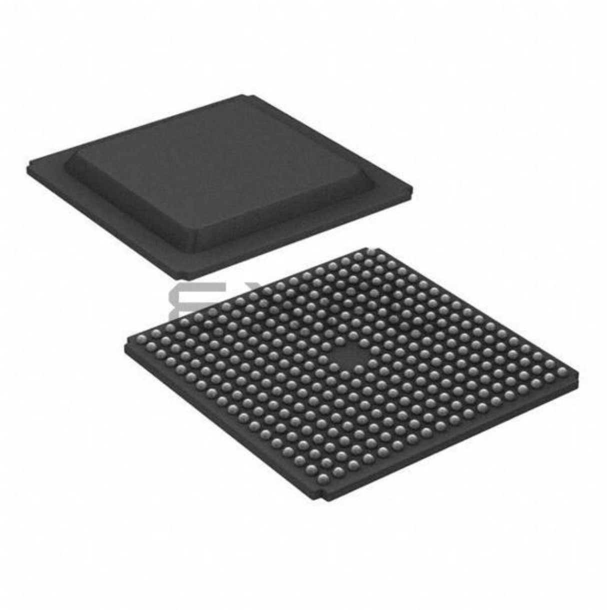

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Details	
Product Status	Active
Number of LABs/CLBs	3328
Number of Logic Elements/Cells	29952
Total RAM Bits	589824
Number of I/O	221
Number of Gates	1500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1500-5fg320c

XILINX®

Spartan-3 FPGA Family: Functional Description

DS099 (v3.0) October 29, 2012 **Product Specification**

Spartan-3 FPGA Design Documentation

The functionality of the Spartan®-3 FPGA family is described in the following documents. The topics covered in each guide are listed.

- UG331: *Spartan-3 Generation FPGA User Guide*
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Software Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
- UG332: *Spartan-3 Generation Configuration User Guide*
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx Platform Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples

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For specific hardware examples, see the Spartan-3 FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- Spartan-3 FPGA Starter Kit Board page
  http://www.xilinx.com/s3starter
- UG130: *Spartan-3 FPGA Starter Kit User Guide*

According to Figure 7, the clock line OTCLK1 connects the CK inputs of the upper registers on the output and three-state paths. Similarly, OTCLK2 connects the CK inputs for the lower registers on the output and three-state paths. The upper and lower registers on the input path have independent clock lines: ICLK1 and ICLK2. The enable line OCE connects the CE inputs of the upper and lower registers on the output path. Similarly, TCE connects the CE inputs for the register pair on the three-state path and ICE does the same for the register pair on the input path. The Set/Reset (SR) line entering the IOB is common to all six registers, as is the Reverse (REV) line.

Each storage element supports numerous options in addition to the control over signal polarity described in the IOB Overview section. These are described in Table 6.

Table 6: **Storage Element Options**

Option Switch	Function	Specificity
FF/Latch	Chooses between an edge-sensitive flip-flop or a level-sensitive latch	Independent for each storage element.
SYNC/ASYNC	Determines whether SR is synchronous or asynchronous	Independent for each storage element.
SRHIGH/SRLOW	Determines whether SR acts as a Set, which forces the storage element to a logic “1" (SRHIGH) or a Reset, which forces a logic “0” (SRLOW).	Independent for each storage element, except when using FDDR. In the latter case, the selection for the upper element (OFF1 or TFF2) applies to both elements.
INIT1/INIT0	In the event of a Global Set/Reset, after configuration or upon activation of the GSR net, this switch decides whether to set or reset a storage element. By default, choosing SRLOW also selects INIT0; choosing SRHIGH also selects INIT1.	Independent for each storage element, except when using FDDR. In the latter case, selecting INIT0 for one element applies to both elements (even though INIT1 is selected for the other).

Double-Data-Rate Transmission

Double-Data-Rate (DDR) transmission describes the technique of synchronizing signals to both the rising and falling edges of the clock signal. Spartan-3 devices use register-pairs in all three IOB paths to perform DDR operations.

The pair of storage elements on the IOB’s Output path (OFF1 and OFF2), used as registers, combine with a special multiplexer to form a DDR D-type flip-flop (FDDR). This primitive permits DDR transmission where output data bits are synchronized to both the rising and falling edges of a clock. It is possible to access this function by placing either an FDDRRSE or an FDDRCPE component or symbol into the design. DDR operation requires two clock signals (50% duty cycle), one the inverted form of the other. These signals trigger the two registers in alternating fashion, as shown in Figure 8. Commonly, the Digital Clock Manager (DCM) generates the two clock signals by mirroring an incoming signal, then shifting it 180 degrees. This approach ensures minimal skew between the two signals.

The storage-element-pair on the Three-State path (TFF1 and TFF2) can also be combined with a local multiplexer to form an FDDR primitive. This permits synchronizing the output enable to both the rising and falling edges of a clock. This DDR operation is realized in the same way as for the output path.

The storage-element-pair on the input path (IFF1 and IFF2) allows an I/O to receive a DDR signal. An incoming DDR clock signal triggers one register and the inverted clock signal triggers the other register. In this way, the registers take turns capturing bits of the incoming DDR data signal.

Table 9: **Differential I/O Standards**

Signal Standard (IOSTANDARD)	V_{CCO} (Volts)		V_{REF} for Inputs (Volts)
	For Outputs	For Inputs	
LDT_25 (ULVDS_25)	2.5	–	–
LVDS_25	2.5	–	–
BLVDS_25	2.5	–	–
LVDSEXT_25	2.5	–	–
LVPECL_25	2.5	–	–
RSDS_25	2.5	–	–
DIFF_HSTL_II_18	1.8	–	–
DIFF_SSTL2_II	2.5	–	–

Notes:
1. See Table 10 for a listing of the differential DCI standards.

The need to supply V_{REF} and V_{CCO} imposes constraints on which standards can be used in the same bank. See The Organization of IOBs into Banks section for additional guidelines concerning the use of the V_{CCO} and V_{REF} lines.

Digitally Controlled Impedance (DCI)

When the round-trip delay of an output signal—i.e., from output to input and back again—exceeds rise and fall times, it is common practice to add termination resistors to the line carrying the signal. These resistors effectively match the impedance of a device's I/O to the characteristic impedance of the transmission line, thereby preventing reflections that adversely affect signal integrity. However, with the high I/O counts supported by modern devices, adding resistors requires significantly more components and board area. Furthermore, for some packages—e.g., ball grid arrays—it may not always be possible to place resistors close to pins.

DCI answers these concerns by providing two kinds of on-chip terminations: Parallel terminations make use of an integrated resistor network. Series terminations result from controlling the impedance of output drivers. DCI actively adjusts both parallel and series terminations to accurately match the characteristic impedance of the transmission line. This adjustment process compensates for differences in I/O impedance that can result from normal variation in the ambient temperature, the supply voltage and the manufacturing process. When the output driver turns off, the series termination, by definition, approaches a very high impedance; in contrast, parallel termination resistors remain at the targeted values.

DCI is available only for certain I/O standards, as listed in Table 10. DCI is selected by applying the appropriate I/O standard extensions to symbols or components. There are five basic ways to configure terminations, as shown in Table 11. The DCI I/O standard determines which of these terminations is put into effect.

HSTL_I_DCI-, HSTL_III_DCI-, and SSTL2_I_DCI-type outputs do not require the VRN and VRP reference resistors. Likewise, LVDCI-type inputs do not require the VRN and VRP reference resistors. In a bank without any DCI I/O or a bank containing non-DCI I/O and purely HSTL_I_DCI- or HSTL_III_DCI-type outputs, or SSTL2_I_DCI-type outputs or LVDCI-type inputs, the associated VRN and VRP pins can be used as general-purpose I/O pins.

The HSLVDCI (High-Speed LVDCI) standard is intended for bidirectional use. The driver is identical to LVDCI, while the input is identical to HSTL. By using a V_{REF}-referenced input, HSLVDCI allows greater input sensitivity at the receiver than when using a single-ended LVCMOS-type receiver.

Table 34: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical[(1)]	Commercial Maximum[(1)]	Industrial Maximum[(1)]	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50	5	24	31	mA
		XC3S200	10	54	80	mA
		XC3S400	15	110	157	mA
		XC3S1000	35	160	262	mA
		XC3S1500	45	260	332	mA
		XC3S2000	60	360	470	mA
		XC3S4000	100	450	810	mA
		XC3S5000	120	600	870	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50	1.5	2.0	2.5	mA
		XC3S200	1.5	3.0	3.5	mA
		XC3S400	1.5	3.0	3.5	mA
		XC3S1000	2.0	4.0	5.0	mA
		XC3S1500	2.5	4.0	5.0	mA
		XC3S2000	3.0	5.0	6.0	mA
		XC3S4000	3.5	5.0	6.0	mA
		XC3S5000	3.5	5.0	6.0	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50	7	20	22	mA
		XC3S200	10	30	33	mA
		XC3S400	15	40	44	mA
		XC3S1000	20	50	55	mA
		XC3S1500	35	75	85	mA
		XC3S2000	45	90	100	mA
		XC3S4000	55	110	125	mA
		XC3S5000	70	130	145	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using devices with typical processing at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). Maximum values are the production test limits measured for each device at the maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.465V, and V_{CCAUX} = 2.625V. The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements, the use of DCI standards, etc.), measured quiescent current levels may be different than the values in the table. Use the XPower Estimator or XPower Analyzer for more accurate estimates. See Note 2.
2. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3 XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer, part of the Xilinx ISE development software, uses the FPGA netlist as input to provide more accurate maximum and typical estimates.
3. The maximum numbers in this table also indicate the minimum current each power rail requires in order for the FPGA to power-on successfully, once all three rails are supplied. If V_{CCINT} is applied before V_{CCAUX}, there may be temporary additional I_{CCINT} current until V_{CCAUX} is applied. See Surplus I_{CCINT} if V_{CCINT} Applied before V_{CCAUX}, page 54

Simultaneously Switching Output Guidelines

This section provides guidelines for the maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins, of a given output signal standard, that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 49 and Table 50 provide the essential SSO guidelines. For each device/package combination, Table 49 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and will possibly not match the physical number of pairs. For each output signal standard and drive strength, Table 50 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The Table 50 guidelines are categorized by package style. Multiply the appropriate numbers from Table 49 and Table 50 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines may result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 49 x Table 50

The recommended maximum SSO values assume that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The number of SSOs allowed for quad-flat packages (VQ, TQ, PQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 49: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	VQ100	CP132 (1)(2)	TQ144 (1)	PQ208	FT256	FG320	FG456	FG676	FG900	FG1156 (2)
XC3S50	1	1.5	1.5	2	–	–	–	–	–	–
XC3S200	1	–	1.5	2	3	–	–	–	–	–
XC3S400	–	–	1.5	2	3	3	5	–	–	–
XC3S1000	–	–	–	–	3	3	5	5	–	–
XC3S1500	–	–	–	–	–	3	5	6	–	–
XC3S2000	–	–	–	–	–	–	5	6	9	–
XC3S4000	–	–	–	–	–	–	–	6	10	12
XC3S5000	–	–	–	–	–	–	–	6	10	12

Notes:

1. The V_{CCO} lines for the pair of banks on each side of the CP132 and TQ144 packages are internally tied together. Each pair of interconnected banks shares three V_{CCO}/GND pairs. Consequently, the per bank number is 1.5.
2. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.
3. The information in this table also applies to Pb-free packages.

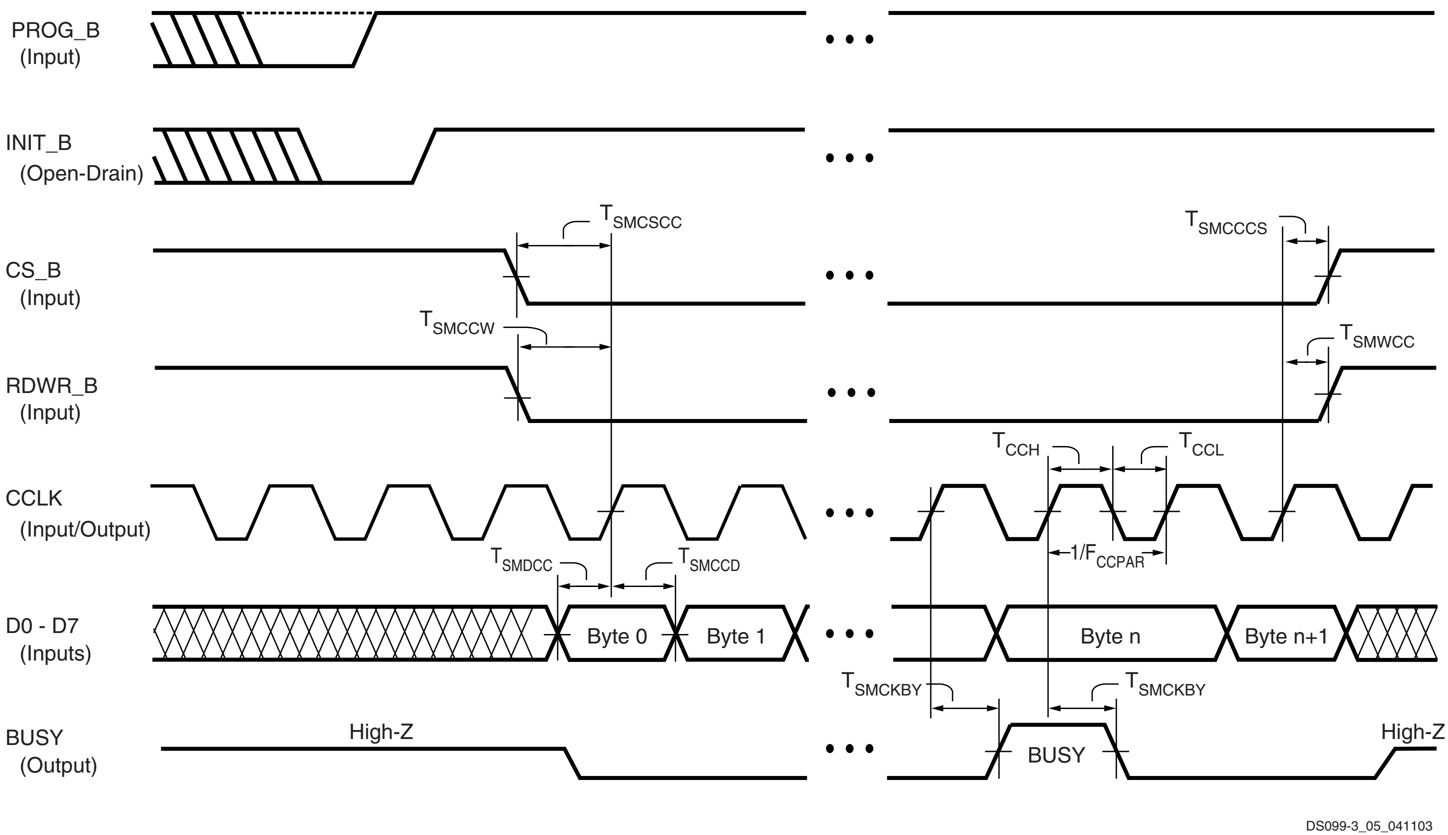

Figure 38: **Waveforms for Master and Slave Parallel Configuration**

Table 67: **Timing for the Master and Slave Parallel Configuration Modes**

Symbol	Description	Slave/ Master	All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin	Slave	–	12.0	ns
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	Both	10.0	–	ns
T_{SMCSCC}	The time from the setup of a logic level at the CS_B pin to the rising transition at the CCLK pin		10.0	–	ns
T_{SMCCW}(3)	The time from the setup of a logic level at the RDWR_B pin to the rising transition at the CCLK pin		10.0	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins	Both	0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CS_B pin		0	–	ns
T_{SMWCC}(3)	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns

CCLK: Configuration Clock

The configuration clock signal on this pin synchronizes the reading or writing of configuration data. The CCLK pin is an input-only pin for the Slave Serial and Slave Parallel configuration modes. In the Master Serial and Master Parallel configuration modes, the FPGA drives the CCLK pin and CCLK should be treated as a full bidirectional I/O pin for signal integrity analysis.

Although the CCLK frequency is relatively low, Spartan-3 FPGA output edge rates are fast. Any potential signal integrity problems on the CCLK board trace can cause FPGA configuration to fail. Therefore, pay careful attention to the CCLK signal integrity on the printed circuit board. Signal integrity simulation with IBIS is recommended. For all configuration modes except JTAG, consider the signal integrity at every CCLK trace destination, including the FPGA's CCLK pin. For more details on CCLK design considerations, see Chapter 2 of UG332, *Spartan-3 Generation Configuration User Guide*.

During configuration, the CCLK pin has a pull-up resistor to VCCAUX, regardless of the HSWAP_EN pin. After configuration, the CCLK pin is pulled High to VCCAUX by default as defined by the ***CclkPin*** bitstream selection, although this behavior is programmable. Any clocks applied to CCLK after configuration are ignored unless the bitstream option ***Persist*** is set to ***Yes***, which retains the configuration interface. ***Persist*** is set to ***No*** by default. However, if ***Persist*** is set to ***Yes***, then all clock edges are potentially active events, depending on the other configuration control signals.

The bitstream generator option ***ConfigRate*** determines the frequency of the internally-generated CCLK oscillator required for the Master configuration modes. The actual frequency is approximate due to the characteristics of the silicon oscillator and varies by up to 50% over the temperature and voltage range. By default, CCLK operates at approximately 6 MHz. Via the ***ConfigRate*** option, the oscillator frequency is set at approximately 3, 6, 12, 25, or 50 MHz. At power-on, CCLK always starts operation at its lowest frequency. The device does not start operating at the higher frequency until the ConfigRate control bits are loaded during the configuration process.

PROG_B: Program/Configure Device

This asynchronous pin initiates the configuration or re-configuration processes. A Low-going pulse resets the configuration logic, initializing the configuration memory. This initialization process cannot finish until PROG_B returns High. Asserting PROG_B Low for an extended period delays the configuration process. At power-up, there is always a pull-up resistor to VCCAUX on this pin, regardless of the HSWAP_EN input. After configuration, the bitstream generator option ***ProgPin*** determines whether or not the pull-up resistor is present. By default, the ***ProgPin*** option retains the pull-up resistor.

After configuration, hold the PROG_B input High. Any Low-going pulse on PROG_B lasting 300 ns or longer restarts the configuration process.

Table 73: **PROG_B Operation**

PROG_B Input	Response
Power-up	Automatically initiates configuration process.
Low-going pulse	Initiate (re-)configuration process and continue to completion.
Extended Low	Initiate (re-)configuration process and stall process at step where configuration memory is cleared. Process is stalled until PROG_B returns High.
1	If the configuration process is started, continue to completion. If configuration process is complete, stay in User mode.

DONE: Configuration Done, Delay Start-Up Sequence

The FPGA produces a Low-to-High transition on this pin indicating that the configuration process is complete. The bitstream generator option ***DriveDone*** determines whether this pin functions as a totem-pole output that can drive High or as an open-drain output. If configured as an open-drain output—which is the default behavior—then a pull-up resistor is required to produce a High logic level. There is a bitstream option that provides an internal pull-up resistor, otherwise an external pull-up resistor is required.

The open-drain option permits the DONE lines of multiple FPGAs to be tied together, so that the common node transitions High only after all of the FPGAs have completed configuration. Externally holding the open-drain DONE pin Low delays the start-up sequence, which marks the transition to user mode.

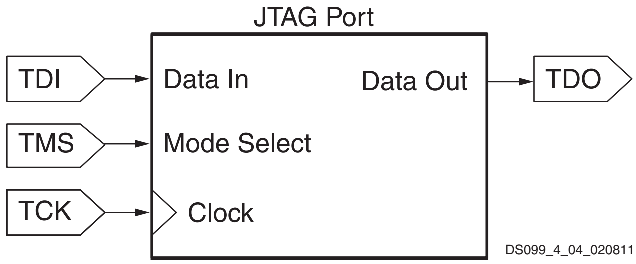

Figure 43: **JTAG Port**

IDCODE Register

Spartan-3 FPGAs contain a 32-bit identification register called the IDCODE register, as defined in the IEEE 1149.1 JTAG standard. The fixed value electrically identifies the manufacture (Xilinx) and the type of device being addressed over a JTAG chain. This register allows the JTAG host to identify the device being tested or programmed via JTAG. See Table 78.

Using JTAG Port After Configuration

The JTAG port is always active and available before, during, and after FPGA configuration. Add the BSCAN_SPARTAN3 primitive to the design to create user-defined JTAG instructions and JTAG chains to communicate with internal logic.

Furthermore, the contents of the User ID register within the JTAG port can be specified as a Bitstream Generation option. By default, the 32-bit User ID register contains `0xFFFFFFFF`.

Table 78: **Spartan-3 JTAG IDCODE Register Values (hexadecimal)**

Part Number	IDCODE Register
XC3S50	0x0140C093
XC3S200	0x01414093
XC3S400	0x0141C093
XC3S1000	0x01428093
XC3S1500	0x01434093
XC3S2000	0x01440093
XC3S4000	0x01448093
XC3S5000	0x01450093

Precautions When Using the JTAG Port in 3.3V Environments

The JTAG port is powered by the +2.5V VCCAUX power supply. When connecting to a 3.3V interface, the JTAG input pins must be current-limited using a series resistor. Similarly, the TDO pin is a CMOS output powered from +2.5V. The TDO output can directly drive a 3.3V input but with reduced noise immunity. See 3.3V-Tolerant Configuration Interface, page 47. See also XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional details.

The following interface precautions are recommended when connecting the JTAG port to a 3.3V interface.

- Avoid actively driving the JTAG input signals High with 3.3V signal levels. If required in the application, use series current-limiting resistors to keep the current below 10 mA per pin.
- If possible, drive the FPGA JTAG inputs with drivers that can be placed in high-impedance (Hi-Z) after using the JTAG port. Alternatively, drive the FPGA JTAG inputs with open-drain outputs, which only drive Low. In both cases, pull-up resistors are required. The FPGA JTAG pins have pull-up resistors to VCCAUX before configuration and optional pull-up resistors after configuration, controlled by Bitstream Options, page 125.

Table 80: **Bitstream Options Affecting Spartan-3 Device Pins *(Cont'd)***

Affected Pin Name(s)	Bitstream Generation Function	Option Variable Name	Values (Default)
CCLK	After configuration, this bitstream option either pulls CCLK to VCCAUX via a pull-up resistor, or allows CCLK to float.	CclkPin	• **Pullup** • Pullnone
CCLK	For Master configuration modes, this option sets the approximate frequency, in MHz, for the internal silicon oscillator.	ConfigRate	• 3, **6**, 12, 25, 50
PROG_B	A pull-up resistor to VCCAUX exists on PROG_B during configuration. After configuration, this bitstream option either pulls PROG_B to VCCAUX via a pull-up resistor, or allows PROG_B to float.	ProgPin	• **Pullup** • Pullnone
DONE	After configuration, this bitstream option either pulls DONE to VCCAUX via a pull-up resistor, or allows DONE to float. See also DriveDone option.	DonePin	• **Pullup** • Pullnone
DONE	If set to Yes, this option allows the FPGA's DONE pin to drive High when configuration completes. By default, the DONE is an open-drain output and can only drive Low. Only single FPGAs and the last FPGA in a multi-FPGA daisy-chain should use this option.	DriveDone	• **No** • Yes
M2	After configuration, this bitstream option either pulls M2 to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows M2 to float.	M2Pin	• **Pullup** • Pulldown • Pullnone
M1	After configuration, this bitstream option either pulls M1 to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows M1 to float.	M1Pin	• **Pullup** • Pulldown • Pullnone
M0	After configuration, this bitstream option either pulls M0 to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows M0 to float.	M0Pin	• **Pullup** • Pulldown • Pullnone
HSWAP_EN	After configuration, this bitstream option either pulls HSWAP_EN to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows HSWAP_EN to float.	HswapenPin	• **Pullup** • Pulldown • Pullnone
TDI	After configuration, this bitstream option either pulls TDI to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows TDI to float.	TdiPin	• **Pullup** • Pulldown • Pullnone
TMS	After configuration, this bitstream option either pulls TMS to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows TMS to float.	TmsPin	• **Pullup** • Pulldown • Pullnone
TCK	After configuration, this bitstream option either pulls TCK to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows TCK to float.	TckPin	• **Pullup** • Pulldown • Pullnone
TDO	After configuration, this bitstream option either pulls TDO to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows TDO to float.	TdoPin	• **Pullup** • Pulldown • Pullnone

Setting Bitstream Generator Options

Refer to the "BitGen" chapter in the Xilinx ISE® software documentation.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx website at the specified location in Table 83.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx website for each package.

Table 83: **Xilinx Package Mechanical Drawings**

Package	Web Link (URL)
VQ100 and VQG100	http://www.xilinx.com/support/documentation/package_specs/vq100.pdf
CP132 and CPG132[(1)]	http://www.xilinx.com/support/documentation/package_specs/cp132.pdf
TQ144 and TQG144	http://www.xilinx.com/support/documentation/package_specs/tq144.pdf
PQ208 and PQG208	http://www.xilinx.com/support/documentation/package_specs/pq208.pdf
FT256 and FTG256	http://www.xilinx.com/support/documentation/package_specs/ft256.pdf
FG320 and FGG320	http://www.xilinx.com/support/documentation/package_specs/fg320.pdf
FG456 and FGG456	http://www.xilinx.com/support/documentation/package_specs/fg456.pdf
FG676 and FGG676	http://www.xilinx.com/support/documentation/package_specs/fg676.pdf
FG900 and FGG900	http://www.xilinx.com/support/documentation/package_specs/fg900.pdf
FG1156 and FGG1156[(1)]	http://www.xilinx.com/support/documentation/package_specs/fg1156.pdf

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Power, Ground, and I/O by Package

Each package has three separate voltage supply inputs—VCCINT, VCCAUX, and VCCO—and a common ground return, GND. The numbers of pins dedicated to these functions varies by package, as shown in Table 84.

Table 84: **Power and Ground Supply Pins by Package**

Package	VCCINT	VCCAUX	VCCO	GND
VQ100	4	4	8	10
CP132[(1)]	4	4	12	12
TQ144	4	4	12	16
PQ208	4	8	12	28
FT256	8	8	24	32
FG320	12	8	28	40
FG456	12	8	40	52
FG676	20	16	64	76
FG900	32	24	80	120
FG1156[(1)]	40	32	104	184

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

A majority of package pins are user-defined I/O pins. However, the numbers and characteristics of these I/O depends on the device type and the package in which it is available, as shown in Table 85. The table shows the maximum number of single-ended I/O pins available, assuming that all I/O-, DUAL-, DCI-, VREF-, and GCLK-type pins are used as general-purpose I/O. Likewise, the table shows the maximum number of differential pin-pairs available on the package. Finally, the table shows how the total maximum user I/Os are distributed by pin type, including the number of unconnected—i.e., N.C.—pins on the device.

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
7	IO_L24P_7	G4	I/O
7	IO_L39N_7	H3	I/O
7	IO_L39P_7	H4	I/O
7	IO_L40N_7/VREF_7	H1	VREF
7	IO_L40P_7	G1	I/O
7	VCCO_7	G6	VCCO
7	VCCO_7	H5	VCCO
7	VCCO_7	H6	VCCO
N/A	GND	A1	GND
N/A	GND	A16	GND
N/A	GND	B2	GND
N/A	GND	B9	GND
N/A	GND	B15	GND
N/A	GND	F6	GND
N/A	GND	F11	GND
N/A	GND	G7	GND
N/A	GND	G8	GND
N/A	GND	G9	GND
N/A	GND	G10	GND
N/A	GND	H2	GND
N/A	GND	H7	GND
N/A	GND	H8	GND
N/A	GND	H9	GND
N/A	GND	H10	GND
N/A	GND	J7	GND
N/A	GND	J8	GND
N/A	GND	J9	GND
N/A	GND	J10	GND
N/A	GND	J15	GND
N/A	GND	K7	GND
N/A	GND	K8	GND
N/A	GND	K9	GND
N/A	GND	K10	GND
N/A	GND	L6	GND
N/A	GND	L11	GND
N/A	GND	R2	GND
N/A	GND	R8	GND
N/A	GND	R15	GND
N/A	GND	T1	GND

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
N/A	VCCINT	N6	VCCINT
N/A	VCCINT	N7	VCCINT
VCCAUX	CCLK	T15	CONFIG
VCCAUX	DONE	R15	CONFIG
VCCAUX	HSWAP_EN	E6	CONFIG
VCCAUX	M0	P5	CONFIG
VCCAUX	M1	U3	CONFIG
VCCAUX	M2	R4	CONFIG
VCCAUX	PROG_B	E5	CONFIG
VCCAUX	TCK	E14	JTAG
VCCAUX	TDI	D4	JTAG
VCCAUX	TDO	D15	JTAG
VCCAUX	TMS	B16	JTAG

User I/Os by Bank

Table 99 indicates how the available user-I/O pins are distributed between the eight I/O banks on the FG320 package.

Table 99: **User I/Os Per Bank in FG320 Package**

Package Edge	I/O Bank	Maximum I/O	Maximum LVDS Pairs	All Possible I/O Pins by Type				
				I/O	DUAL	DCI	VREF	GCLK
Top	0	26	11	19	0	2	3	2
	1	26	11	19	0	2	3	2
Right	2	29	14	23	0	2	4	0
	3	29	14	23	0	2	4	0
Bottom	4	27	11	13	6	2	4	2
	5	26	11	13	6	2	3	2
Left	6	29	14	23	0	2	4	0
	7	29	14	23	0	2	4	0

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
1	IO_L15P_1	IO_L15P_1	E17	I/O
1	IO_L16N_1	IO_L16N_1	B17	I/O
1	IO_L16P_1	IO_L16P_1	C17	I/O
1	N.C. (◆)	IO_L19N_1	C16	I/O
1	N.C. (◆)	IO_L19P_1	D16	I/O
1	N.C. (◆)	IO_L22N_1	A16	I/O
1	N.C. (◆)	IO_L22P_1	B16	I/O
1	IO_L24N_1	IO_L24N_1	D15	I/O
1	IO_L24P_1	IO_L24P_1	E15	I/O
1	IO_L25N_1	IO_L25N_1	B15	I/O
1	IO_L25P_1	IO_L25P_1	A15	I/O
1	IO_L27N_1	IO_L27N_1	D14	I/O
1	IO_L27P_1	IO_L27P_1	E14	I/O
1	IO_L28N_1	IO_L28N_1	A14	I/O
1	IO_L28P_1	IO_L28P_1	B14	I/O
1	IO_L29N_1	IO_L29N_1	C13	I/O
1	IO_L29P_1	IO_L29P_1	D13	I/O
1	IO_L30N_1	IO_L30N_1	A13	I/O
1	IO_L30P_1	IO_L30P_1	B13	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D12	VREF
1	IO_L31P_1	IO_L31P_1	E12	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B12	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C12	GCLK
1	VCCO_1	VCCO_1	C15	VCCO
1	VCCO_1	VCCO_1	F15	VCCO
1	VCCO_1	VCCO_1	G12	VCCO
1	VCCO_1	VCCO_1	G13	VCCO
1	VCCO_1	VCCO_1	G14	VCCO
2	IO	IO	C22	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C20	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C21	DCI
2	IO_L16N_2	IO_L16N_2	D20	I/O
2	IO_L16P_2	IO_L16P_2	D19	I/O
2	IO_L17N_2	IO_L17N_2	D21	I/O
2	IO_L17P_2/VREF_2	IO_L17P_2/VREF_2	D22	VREF
2	IO_L19N_2	IO_L19N_2	E18	I/O
2	IO_L19P_2	IO_L19P_2	F18	I/O
2	IO_L20N_2	IO_L20N_2	E19	I/O
2	IO_L20P_2	IO_L20P_2	E20	I/O
2	IO_L21N_2	IO_L21N_2	E21	I/O

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
6	N.C. (◆)	IO_L28N_6	R5	I/O
6	N.C. (◆)	IO_L28P_6	P6	I/O
6	N.C. (◆)	IO_L29N_6	R2	I/O
6	N.C. (◆)	IO_L29P_6	R1	I/O
6	N.C. (◆)	IO_L31N_6	P5	I/O
6	N.C. (◆)	IO_L31P_6	P4	I/O
6	N.C. (◆)	IO_L32N_6	P2	I/O
6	N.C. (◆)	IO_L32P_6	P1	I/O
6	N.C. (◆)	IO_L33N_6	N6	I/O
6	N.C. (◆)	IO_L33P_6	N5	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	N4	VREF
6	IO_L34P_6	IO_L34P_6	N3	I/O
6	IO_L35N_6	IO_L35N_6	N2	I/O
6	IO_L35P_6	IO_L35P_6	N1	I/O
6	IO_L38N_6	IO_L38N_6	M6	I/O
6	IO_L38P_6	IO_L38P_6	M5	I/O
6	IO_L39N_6	IO_L39N_6	M4	I/O
6	IO_L39P_6	IO_L39P_6	M3	I/O
6	IO_L40N_6	IO_L40N_6	M2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	M1	VREF
6	VCCO_6	VCCO_6	M7	VCCO
6	VCCO_6	VCCO_6	N7	VCCO
6	VCCO_6	VCCO_6	P7	VCCO
6	VCCO_6	VCCO_6	R3	VCCO
6	VCCO_6	VCCO_6	R6	VCCO
7	IO	IO	C2	I/O
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	C3	DCI
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	C4	DCI
7	IO_L16N_7	IO_L16N_7	D1	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	C1	VREF
7	IO_L17N_7	IO_L17N_7	E4	I/O
7	IO_L17P_7	IO_L17P_7	D4	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	D3	VREF
7	IO_L19P_7	IO_L19P_7	D2	I/O
7	IO_L20N_7	IO_L20N_7	F4	I/O
7	IO_L20P_7	IO_L20P_7	E3	I/O
7	IO_L21N_7	IO_L21N_7	E1	I/O
7	IO_L21P_7	IO_L21P_7	E2	I/O
7	IO_L22N_7	IO_L22N_7	G6	I/O
7	IO_L22P_7	IO_L22P_7	F5	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	GND	GND	R17	GND
N/A	GND	GND	T17	GND
N/A	GND	GND	U17	GND
N/A	GND	GND	V17	GND
N/A	GND	GND	AC17	GND
N/A	GND	GND	AF17	GND
N/A	GND	GND	AK17	GND
N/A	GND	GND	N18	GND
N/A	GND	GND	P18	GND
N/A	GND	GND	R18	GND
N/A	GND	GND	T18	GND
N/A	GND	GND	U18	GND
N/A	GND	GND	V18	GND
N/A	GND	GND	R19	GND
N/A	GND	GND	T19	GND
N/A	GND	GND	A21	GND
N/A	GND	GND	E21	GND
N/A	GND	GND	H21	GND
N/A	GND	GND	AC21	GND
N/A	GND	GND	AF21	GND
N/A	GND	GND	AK21	GND
N/A	GND	GND	K23	GND
N/A	GND	GND	P23	GND
N/A	GND	GND	U23	GND
N/A	GND	GND	AA23	GND
N/A	GND	GND	A25	GND
N/A	GND	GND	AK25	GND
N/A	GND	GND	E26	GND
N/A	GND	GND	K26	GND
N/A	GND	GND	P26	GND
N/A	GND	GND	U26	GND
N/A	GND	GND	AA26	GND
N/A	GND	GND	AF26	GND
N/A	GND	GND	A29	GND
N/A	GND	GND	B29	GND
N/A	GND	GND	AJ29	GND
N/A	GND	GND	AK29	GND
N/A	GND	GND	A30	GND
N/A	GND	GND	B30	GND
N/A	GND	GND	F30	GND

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
0	IO_L03P_0	IO_L03P_0	B5	I/O
0	IO_L04N_0	IO_L04N_0	D6	I/O
0	IO_L04P_0	IO_L04P_0	C6	I/O
0	IO_L05N_0	IO_L05N_0	B6	I/O
0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	A6	VREF
0	IO_L06N_0	IO_L06N_0	F7	I/O
0	IO_L06P_0	IO_L06P_0	E7	I/O
0	IO_L07N_0	IO_L07N_0	G9	I/O
0	IO_L07P_0	IO_L07P_0	F9	I/O
0	IO_L08N_0	IO_L08N_0	D9	I/O
0	IO_L08P_0	IO_L08P_0	C9	I/O
0	IO_L09N_0	IO_L09N_0	J10	I/O
0	IO_L09P_0	IO_L09P_0	H10	I/O
0	IO_L10N_0	IO_L10N_0	G10	I/O
0	IO_L10P_0	IO_L10P_0	F10	I/O
0	IO_L11N_0	IO_L11N_0	L12	I/O
0	IO_L11P_0	IO_L11P_0	K12	I/O
0	IO_L12N_0	IO_L12N_0	J12	I/O
0	IO_L12P_0	IO_L12P_0	H12	I/O
0	IO_L13N_0	IO_L13N_0	F12	I/O
0	IO_L13P_0	IO_L13P_0	E12	I/O
0	IO_L14N_0	IO_L14N_0	D12	I/O
0	IO_L14P_0	IO_L14P_0	C12	I/O
0	IO_L15N_0	IO_L15N_0	B12	I/O
0	IO_L15P_0	IO_L15P_0	A12	I/O
0	IO_L16N_0	IO_L16N_0	H13	I/O
0	IO_L16P_0	IO_L16P_0	G13	I/O
0	IO_L17N_0	IO_L17N_0	D13	I/O
0	IO_L17P_0	IO_L17P_0	C13	I/O
0	IO_L18N_0	IO_L18N_0	L14	I/O
0	IO_L18P_0	IO_L18P_0	K14	I/O
0	IO_L19N_0	IO_L19N_0	H14	I/O
0	IO_L19P_0	IO_L19P_0	G14	I/O
0	IO_L20N_0	IO_L20N_0	F14	I/O
0	IO_L20P_0	IO_L20P_0	E14	I/O
0	IO_L21N_0	IO_L21N_0	D14	I/O
0	IO_L21P_0	IO_L21P_0	C14	I/O
0	IO_L22N_0	IO_L22N_0	B14	I/O
0	IO_L22P_0	IO_L22P_0	A14	I/O
0	IO_L23N_0	IO_L23N_0	K15	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
1	IO_L27N_1	IO_L27N_1	F19	I/O
1	IO_L27P_1	IO_L27P_1	G19	I/O
1	IO_L28N_1	IO_L28N_1	B19	I/O
1	IO_L28P_1	IO_L28P_1	C19	I/O
1	IO_L29N_1	IO_L29N_1	J18	I/O
1	IO_L29P_1	IO_L29P_1	K18	I/O
1	IO_L30N_1	IO_L30N_1	G18	I/O
1	IO_L30P_1	IO_L30P_1	H18	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D18	VREF
1	IO_L31P_1	IO_L31P_1	E18	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B18	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C18	GCLK
1	N.C. (◆)	IO_L33N_1	C28	I/O
1	N.C. (◆)	IO_L33P_1	D28	I/O
1	N.C. (◆)	IO_L34N_1	A28	I/O
1	N.C. (◆)	IO_L34P_1	B28	I/O
1	N.C. (◆)	IO_L35N_1	J24	I/O
1	N.C. (◆)	IO_L35P_1	K24	I/O
1	N.C. (◆)	IO_L36N_1	F24	I/O
1	N.C. (◆)	IO_L36P_1	G24	I/O
1	IO_L37N_1	IO_L37N_1	J20	I/O
1	IO_L37P_1	IO_L37P_1	K20	I/O
1	IO_L38N_1	IO_L38N_1	F20	I/O
1	IO_L38P_1	IO_L38P_1	G20	I/O
1	IO_L39N_1	IO_L39N_1	C20	I/O
1	IO_L39P_1	IO_L39P_1	D20	I/O
1	IO_L40N_1	IO_L40N_1	A20	I/O
1	IO_L40P_1	IO_L40P_1	B20	I/O
1	VCCO_1	VCCO_1	B22	VCCO
1	VCCO_1	VCCO_1	C27	VCCO
1	VCCO_1	VCCO_1	C31	VCCO
1	VCCO_1	VCCO_1	D19	VCCO
1	VCCO_1	VCCO_1	D24	VCCO
1	VCCO_1	VCCO_1	F22	VCCO
1	VCCO_1	VCCO_1	G27	VCCO
1	VCCO_1	VCCO_1	H20	VCCO
1	VCCO_1	VCCO_1	H24	VCCO
1	VCCO_1	VCCO_1	M19	VCCO
1	VCCO_1	VCCO_1	M20	VCCO
1	VCCO_1	VCCO_1	M21	VCCO

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
5	VCCO_5	VCCO_5	AJ13	VCCO
5	VCCO_5	VCCO_5	AL11	VCCO
5	VCCO_5	VCCO_5	AL16	VCCO
5	VCCO_5	VCCO_5	AM4	VCCO
5	VCCO_5	VCCO_5	AM8	VCCO
5	VCCO_5	VCCO_5	AN13	VCCO
6	IO	IO	AH1	I/O
6	IO	IO	AH2	I/O
6	IO	IO	V9	I/O
6	IO	IO	V10	I/O
6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	AM2	DCI
6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	AM1	DCI
6	IO_L02N_6	IO_L02N_6	AL2	I/O
6	IO_L02P_6	IO_L02P_6	AL1	I/O
6	IO_L03N_6/VREF_6	IO_L03N_6/VREF_6	AK3	VREF
6	IO_L03P_6	IO_L03P_6	AK2	I/O
6	IO_L04N_6	IO_L04N_6	AJ4	I/O
6	IO_L04P_6	IO_L04P_6	AJ3	I/O
6	IO_L05N_6	IO_L05N_6	AJ2	I/O
6	IO_L05P_6	IO_L05P_6	AJ1	I/O
6	IO_L06N_6	IO_L06N_6	AH6	I/O
6	IO_L06P_6	IO_L06P_6	AH5	I/O
6	IO_L07N_6	IO_L07N_6	AG6	I/O
6	IO_L07P_6	IO_L07P_6	AG5	I/O
6	IO_L08N_6	IO_L08N_6	AG2	I/O
6	IO_L08P_6	IO_L08P_6	AG1	I/O
6	IO_L09N_6/VREF_6	IO_L09N_6/VREF_6	AF7	VREF
6	IO_L09P_6	IO_L09P_6	AF6	I/O
6	IO_L10N_6	IO_L10N_6	AG4	I/O
6	IO_L10P_6	IO_L10P_6	AF4	I/O
6	IO_L11N_6	IO_L11N_6	AF3	I/O
6	IO_L11P_6	IO_L11P_6	AF2	I/O
6	IO_L12N_6	IO_L12N_6	AF8	I/O
6	IO_L12P_6	IO_L12P_6	AE9	I/O
6	IO_L13N_6	IO_L13N_6	AE8	I/O
6	IO_L13P_6/VREF_6	IO_L13P_6/VREF_6	AE7	VREF
6	IO_L14N_6	IO_L14N_6	AE6	I/O
6	IO_L14P_6	IO_L14P_6	AE5	I/O
6	IO_L15N_6	IO_L15N_6	AE4	I/O
6	IO_L15P_6	IO_L15P_6	AE3	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
7	IO_L45P_7	IO_L45P_7	M2	I/O
7	IO_L46N_7	IO_L46N_7	N7	I/O
7	IO_L46P_7	IO_L46P_7	N8	I/O
7	N.C. (◆)	IO_L47N_7	P9	I/O
7	N.C. (◆)	IO_L47P_7	P10	I/O
7	IO_L49N_7	IO_L49N_7	P1	I/O
7	IO_L49P_7	IO_L49P_7	P2	I/O
7	IO_L50N_7	IO_L50N_7	R10	I/O
7	IO_L50P_7	IO_L50P_7	R11	I/O
7	N.C. (◆)	IO_L51N_7	U11	I/O
7	N.C. (◆)	IO_L51P_7	T11	I/O
7	VCCO_7	VCCO_7	D3	VCCO
7	VCCO_7	VCCO_7	H3	VCCO
7	VCCO_7	VCCO_7	H7	VCCO
7	VCCO_7	VCCO_7	L4	VCCO
7	VCCO_7	VCCO_7	L8	VCCO
7	VCCO_7	VCCO_7	N12	VCCO
7	VCCO_7	VCCO_7	N2	VCCO
7	VCCO_7	VCCO_7	N6	VCCO
7	VCCO_7	VCCO_7	P12	VCCO
7	VCCO_7	VCCO_7	R12	VCCO
7	VCCO_7	VCCO_7	R8	VCCO
7	VCCO_7	VCCO_7	T12	VCCO
7	VCCO_7	VCCO_7	T4	VCCO
N/A	GND	GND	A1	GND
N/A	GND	GND	A13	GND
N/A	GND	GND	A16	GND
N/A	GND	GND	A19	GND
N/A	GND	GND	A2	GND
N/A	GND	GND	A22	GND
N/A	GND	GND	A26	GND
N/A	GND	GND	A30	GND
N/A	GND	GND	A33	GND
N/A	GND	GND	A34	GND
N/A	GND	GND	A5	GND
N/A	GND	GND	A9	GND
N/A	GND	GND	AA14	GND
N/A	GND	GND	AA15	GND
N/A	GND	GND	AA16	GND
N/A	GND	GND	AA17	GND

Date	Version	Description
11/30/07	2.3	Added XC3S5000 FG(G)676 package. Noted that the FG(G)1156 package is being discontinued. Updated Table 86 with latest thermal characteristics data.
06/25/08	2.4	Updated formatting and links.
12/04/09	2.5	Added link to UG332 in CCLK: Configuration Clock. Noted that the CP132, CPG132, FG1156, and FGG1156 packages are being discontinued in Table 81, Table 83, Table 84, Table 85, and Table 86. Updated CP132: 132-Ball Chip-Scale Package to indicate that the CP132 and CPG132 packages are being discontinued.
10/29/12	3.0	Added Notice of Disclaimer. Per XCN07022, updated the FG1156 and FGG1156 package discussion throughout document including in Table 81, Table 83, Table 84, Table 85, and Table 86. Per XCN08011, updated CP132 and CPG132 package discussion throughout document including in Table 81, Table 83, Table 84, Table 85, and Table 86. This product is not recommended for new designs.

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