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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	3328
Number of Logic Elements/Cells	29952
Total RAM Bits	589824
Number of I/O	333
Number of Gates	1500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1500-5fg456c

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Table 3 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

	Available User I/Os and Differential (Diff) I/O Pairs by Package Type																			
Package	VQ1 VQG	100 100	CP1 CPC	32 <mark>(1)</mark> 132	TQ1 TQG	44 144	PQ2 PQG	208 208	FT2 FTG	256 256	FG3 FGG	320 320	FG4 FGG	156 456	FG6 FGG	676 676	FG9 FGG	900 900	FG11 FGG	56 <mark>(1)</mark> 1156
Footprint (mm)	16 x	16	8 >	c 8	22 x	22	30.6 x	30.6	17 x	17	19 x	19	23 x	23	27 x	27	31 x	31	35 >	c 35
Device	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff
XC3S50	63	29	89 ⁽¹⁾	44 ⁽¹⁾	97	46	124	56	-	-	-	-	-	-	-	-	-	-	-	-
XC3S200	63	29	-	-	97	46	141	62	173	76	-	_	-	_	-	_	-	-	-	-
XC3S400	-	_	-	-	97	46	141	62	173	76	221	100	264	116	-	-	-	-	-	-
XC3S1000	-	-	-	-	-	-	-	-	173	76	221	100	333	149	391	175	-	-	-	-
XC3S1500	-	-	-	-	-	-	-	-	-	-	221	100	333	149	487	221	-	-	-	-
XC3S2000	-	-	-	-	-	-	-	-	-	-	-	-	333	149	489	221	565	270	-	-
XC3S4000	-	-	-	-	-	-	-	-	-	-	-	-	-	-	489	221	633	300	712 <mark>(1)</mark>	312 <mark>(1)</mark>
XC3S5000	_	-	_	_	_	_	_	_	_	_	1	_	_	_	489	221	633	300	784 <mark>(1)</mark>	344 <mark>(1)</mark>

Table 3: Spartan-3 Device I/O Chart

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

2. All device options listed in a given package column are pin-compatible.

3. User = Single-ended user I/O pins. Diff = Differential I/O pairs.

Package Marking

Figure 2 shows the top marking for Spartan-3 FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3 FPGAs in BGA packages except the 132-ball chip-scale package (CP132 and CPG132). The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for Spartan-3 FPGAs in the CP132 and CPG132 packages.

The "5c" and "41" part combinations may be dual marked as "5c/41". Devices with the dual mark can be used as either -5C or -4I devices. Devices with a single mark are only guaranteed for the marked speed grade and temperature range. Some specifications vary according to mask revision. Mask revision E devices are errata-free. All shipments since 2006 have been mask revision E.



Figure 2: Spartan-3 FPGA QFP Package Marking Example for Part Number XC3S400-4PQ208C

ESD Protection

Clamp diodes protect all device pads against damage from Electro-Static Discharge (ESD) as well as excessive voltage transients. Each I/O has two clamp diodes: One diode extends P-to-N from the pad to V_{CCO} and a second diode extends N-to-P from the pad to GND. During operation, these diodes are normally biased in the off state. These clamp diodes are always connected to the pad, regardless of the signal standard selected. The presence of diodes limits the ability of Spartan-3 FPGA I/Os to tolerate high signal voltages. The V_{IN} absolute maximum rating in Table 28, page 58 specifies the voltage range that I/Os can tolerate.

Slew Rate Control and Drive Strength

Two options, FAST and SLOW, control the output slew rate. The FAST option supports output switching at a high rate. The SLOW option reduces bus transients. These options are only available when using one of the LVCMOS or LVTTL standards, which also provide up to seven different levels of current drive strength: 2, 4, 6, 8, 12, 16, and 24 mA. Choosing the appropriate drive strength level is yet another means to minimize bus transients.

Table 7 shows the drive strengths that the LVCMOS and LVTTL standards support.

Signal Standard	Current Drive (mA)										
(IOSTANDARD)	2	4	6	8	12	16	24				
LVTTL	1	1	1	1	1	1	1				
LVCMOS33	~	1	1	1	1	1	1				
LVCMOS25	~	1	1	1	1	1	1				
LVCMOS18	1	1	1	1	1	1	-				
LVCMOS15	1	1	1	1	1	-	-				
LVCMOS12	1	1	1	-	-	-	-				

Table 7: Programmable Output Drive Current

Boundary-Scan Capability

All Spartan-3 FPGA IOBs support boundary-scan testing compatible with IEEE 1149.1 standards. During boundary- scan operations such as EXTEST and HIGHZ the I/O pull-down resistor is active. For more information, see Boundary-Scan (JTAG) Mode, page 50, and refer to the "Using Boundary-Scan and BSDL Files" chapter in <u>UG331</u>.

SelectIO Interface Signal Standards

The IOBs support 18 different single-ended signal standards, as listed in Table 8. Furthermore, the majority of IOBs can be used in specific pairs supporting any of eight differential signal standards, as shown in Table 9.

To define the SelectIO[™] interface signaling standard in a design, set the IOSTANDARD attribute to the appropriate setting. Xilinx provides a variety of different methods for applying the IOSTANDARD for maximum flexibility. For a full description of different methods of applying attributes to control IOSTANDARD, refer to the "Using I/O Resources" chapter in <u>UG331</u>.

Together with placing the appropriate I/O symbol, two externally applied voltage levels, V_{CCO} and V_{REF} , select the desired signal standard. The V_{CCO} lines provide current to the output driver. The voltage on these lines determines the output voltage swing for all standards except GTL and GTLP.

All single-ended standards except the LVCMOS, LVTTL, and PCI varieties require a Reference Voltage (V_{REF}) to bias the input-switching threshold. Once a configuration data file is loaded into the FPGA that calls for the I/Os of a given bank to use such a signal standard, a few specifically reserved I/O pins on the same bank automatically convert to V_{REF} inputs. When using one of the LVCMOS standards, these pins remain I/Os because the V_{CCO} voltage biases the input-switching threshold, so there is no need for V_{REF} . Select the V_{CCO} and V_{REF} levels to suit the desired single-ended standard according to Table 8.

The output frequency (f_{CLKEX}) can be expressed as a function of the incoming clock frequency (f_{CLKIN}) as follows:

Regarding the two attributes, it is possible to assign any combination of integer values, provided that two conditions are met:

- The two values fall within their corresponding ranges, as specified in Table 18.
- The f_{CLKFX} frequency calculated from the above expression accords with the DCM's operating frequency specifications.

For example, if CLKFX_MULTIPLY = 5 and CLKFX_DIVIDE = 3, then the frequency of the output clock signal would be 5/3 that of the input clock signal.

DFS Frequency Modes

The DFS supports two operating modes, High Frequency and Low Frequency, with each specified over a different clock frequency range. The DFS_FREQUENCY_MODE attribute chooses between the two modes. When the attribute is set to LOW, the Low Frequency mode permits the two DFS outputs to operate over a low-to-moderate frequency range. When the attribute is set to HIGH, the High Frequency mode allows both these outputs to operate at the highest possible frequencies.

DFS With or Without the DLL

The DFS component can be used with or without the DLL component:

Without the DLL, the DFS component multiplies or divides the CLKIN signal frequency according to the respective CLKFX_MULTIPLY and CLKFX_DIVIDE values, generating a clock with the new target frequency on the CLKFX and CLKFX180 outputs. Though classified as belonging to the DLL component, the CLKIN input is shared with the DFS component. This case does not employ feedback loop; therefore, it cannot correct for clock distribution delay.

With the DLL, the DFS operates as described in the preceding case, only with the additional benefit of eliminating the clock distribution delay. In this case, a feedback loop from the CLK0 output to the CLKFB input must be present.

The DLL and DFS components work together to achieve this phase correction as follows: Given values for the CLKFX_MULTIPLY and CLKFX_DIVIDE attributes, the DLL selects the delay element for which the output clock edge coincides with the input clock edge whenever mathematically possible. For example, when CLKFX_MULTIPLY = 5 and CLKFX_DIVIDE = 3, the input and output clock edges will coincide every three input periods, which is equivalent in time to five output periods.

Smaller CLKFX_MULTIPLY and CLKFX_DIVIDE values achieve faster lock times. With no factors common to the two attributes, alignment will occur once with every number of cycles equal to the CLKFX_DIVIDE value. Therefore, it is recommended that the user reduce these values by factoring wherever possible. For example, given CLKFX_MULTIPLY = 9 and CLKFX_DIVIDE = 6, removing a factor of three yields CLKFX_MULTIPLY = 3 and CLKFX_DIVIDE = 2. While both value-pairs will result in the multiplication of clock frequency by 3/2, the latter value-pair will enable the DLL to lock more quickly.

Table 18: DFS Attributes

Attribute	Description	Values
DFS_FREQUENCY_MODE	Chooses between High Frequency and Low Frequency modes	Low, High
CLKFX_MULTIPLY	Frequency multiplier constant	Integer from 2 to 32
CLKFX_DIVIDE	Frequency divisor constant	Integer from 1 to 32

Table 19: DFS Signals

Signal	Direction	Description
CLKFX	Output	Multiplies the CLKIN frequency by the attribute-value ratio (CLKFX_MULTIPLY/CLKFX_DIVIDE) to generate a clock signal with a new target frequency.
CLKFX180	Output	Generates a clock signal with same frequency as CLKFX, only shifted 180° out-of-phase.

Configuration

Spartan-3 devices are configured by loading application specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are "Dedicated" to one function only, while others, indicated by the term "Dual-Purpose", can be re-used as general-purpose User I/Os once configuration is complete.

Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M0, M1, and M2 are Dedicated pins. The mode pin settings are shown in Table 26.

Configuration Mode ⁽¹⁾	MO	M1	M2	Synchronizing Clock	Data Width	Serial DOUT ⁽²⁾
Master Serial	0	0	0	CCLK Output	1	Yes
Slave Serial	1	1	1	CCLK Input	1	Yes
Master Parallel	1	1	0	CCLK Output	8	No
Slave Parallel	0	1	1	CCLK Input	8	No
JTAG	1	0	1	TCK Input	1	No

Table 26: Spartan-3 FPGAs Configuration Mode Pin Settings

Notes:

1. The voltage levels on the M0, M1, and M2 pins select the configuration mode.

2. The daisy chain is possible only in the Serial modes when DOUT is used.

The HSWAP_EN input pin defines whether the I/O pins that are not actively used during configuration have pull-up resistors during configuration. By default, HSWAP_EN is tied High (via an internal pull-up resistor if left floating) which shuts off the pull-up resistors on the user I/O pins during configuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration. The Dedicated configuration pins (CCLK, DONE, PROG_B, M2, M1, M0, HSWAP_EN) and the JTAG pins (TDI, TMS, TCK, and TDO) always have a pull-up resistor to VCCAUX during configuration, regardless of the value on the HSWAP_EN pin. Similarly, the dual-purpose INIT_B pin has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM, depending on the package style.

Depending on the chosen configuration mode, the FPGA either generates a CCLK output, or CCLK is an input accepting an externally generated clock.

A persist option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected then the configuration pins with the exception of CCLK, PROG_B, and DONE can be used as user I/O in normal operation. The persist option does not apply to the boundary-scan related pins. The persist feature is valuable in applications that readback configuration data after entering the User mode.

Device		Xilinx Platform Flash PROM						
	File Sizes	Serial Configuration	Parallel Configuration					
XC3S50	439,264	XCF01S	XCF08P					
XC3S200	1,047,616	XCF01S	XCF08P					
XC3S400	1,699,136	XCF02S	XCF08P					
XC3S1000	3,223,488	XCF04S	XCF08P					
XC3S1500	5,214,784	XCF08P	XCF08P					
XC3S2000	7,673,024	XCF08P	XCF08P					
XC3S4000	11,316,864	XCF16P	XCF16P					
XC3S5000	13,271,936	XCF16P	XCF16P					

The maximum bitstream length that Spartan-3 FPGAs support in serial daisy-chains is 4,294,967,264 bits (4 Gbits), roughly equivalent to a daisy-chain with 323 XC3S5000 FPGAs. This is a limit only for serial daisy-chains where configuration data is passed via the FPGA's DOUT pin. There is no such limit for JTAG chains.



Spartan-3 FPGA Family: DC and Switching Characteristics

DS099 (v3.0) October 29, 2012

Product Specification

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

- <u>Advance</u>: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur. Use as estimates, not for production.
- <u>Preliminary</u>: Based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reported delays is greatly reduced compared to Advance data. Use as estimates, not for production.
- <u>Production</u>: These specifications are approved only after silicon has been characterized over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Parameter values are considered stable with no future changes expected.

Production-quality systems must only use FPGA designs compiled with a Production status speed file. FPGA designs using a less mature speed file designation should only be used during system prototyping or preproduction qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the <u>latest Xilinx ISE®</u> software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. The following applies unless otherwise noted: The parameter values published in this module apply to all Spartan®-3 devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades. All parameters representing voltages are measured with respect to GND.

Mask and Fab Revisions

Some specifications list different values for one or more mask or fab revisions, indicated by the device top marking (see Package Marking, page 5). The revision differences involve the power ramp rates, differential DC specifications, and DCM characteristics. The most recent revision (mask rev E and GQ fab/geometry code) is errata-free with improved specifications than earlier revisions.

Mask rev E with fab rev GQ has been shipping since 2005 (see <u>XCN05009</u>) and has been 100% of Xilinx Spartan-3 device shipments since 2006. SCD 0974 was provided to ensure the receipt of the rev E silicon, but it is no longer needed. Parts ordered under the SCD appended "0974" to the standard part number. For example, "XC3S50-4VQ100C" became "XC3S50-4VQ100C0974".

Symbol	Description	Description Conditions			Max	Units
V _{CCINT}	Internal supply voltage relative to GND			-0.5	1.32	V
V _{CCAUX}	Auxiliary supply voltage relative to GND			-0.5	3.00	V
V _{CCO}	Output driver supply voltage relative to GND			-0.5	3.75	V
V _{REF}	Input reference voltage relative to GND			-0.5	V _{CCO} +0.5	V
V _{IN}	Voltage applied to all User I/O pins and	Driver in a	Commercial	-0.95	4.4	V
	Dual-Purpose pins relative to GND ^(2,4)	high-impedance state	Industrial	-0.85	4.3	
	Voltage applied to all Dedicated pins relative to $\mathrm{GND}^{(3)}$		All temp. ranges	-0.5	V _{CCAUX} + 0.5	V

Table 28: Absolute Maximum Ratings

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Table 36: DC Characteristics of User I/Os Using Single-Ended Standards

Signal Standard		Test Co	nditions	Logic Level Characteristics			
(IOSTANDARD) a Drive Attribu	nd Current te (mA)	l _{OL} (mA)	I _{ОН} (mA)	V _{OL} Max (V)	V _{OH} Min (V)		
GTL		32	_	0.4	-		
GTL_DCI		Note 3	Note 3				
GTLP		36	_	0.6	-		
GTLP_DCI		Note 3	Note 3				
HSLVDCI_15		Note 3	Note 3	0.4	V _{CCO} – 0.4		
HSLVDCI_18							
HSLVDCI_25							
HSLVDCI_33							
HSTL_I		8	-8	0.4	V _{CCO} – 0.4		
HSTL_I_DCI		Note 3	Note 3				
HSTL_III		24	-8	0.4	V _{CCO} – 0.4		
HSTL_III_DCI		Note 3	Note 3				
HSTL_I_18		8	-8	0.4	V _{CCO} – 0.4		
HSTL_I_DCI_18		Note 3	Note 3				
HSTL_II_18		16	–16	0.4	V _{CCO} – 0.4		
HSTL_II_DCI_18		Note 3	Note 3				
HSTL_III_18	HSTL_III_18		-8	0.4	V _{CCO} – 0.4		
HSTL_III_DCI_18		Note 3	Note 3				
LVCMOS12 ⁽⁴⁾	2	2	-2	0.4	V _{CCO} – 0.4		
	4	4	-4	_			
	6	6	-6				
LVCMOS15 ⁽⁴⁾	2	2	-2	0.4	V _{CCO} – 0.4		
	4	4	-4	_			
	6	6	-6	_			
	8	8	-8	_			
	12	12	-12	-			
LVDCI_15, LVDCI_DV2_15		Note 3	Note 3				
LVCMOS18 ⁽⁴⁾	2	2	-2	0.4	V _{CCO} – 0.4		
	4	4	-4				
	6	6	-6				
	8	8	-8				
	12	12	–12				
	16	16	–16				
LVDCI_18, LVDCI_DV2_18		Note 3	Note 3				
LVCMOS25 ^(4,5)	2	2	-2	0.4	V _{CCO} – 0.4		
	4	4	-4	-			
	6	6	-6	-			
	8	8	-8				
	12	12	-12				
	16	16	-16				
	24	24	-24	1			
LVDCI_25, LVDCI_DV2_25		Note 3	Note 3				

Switching Characteristics

All Spartan-3 devices are available in two speed grades: -4 and the higher performance -5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production. Each category is defined as follows:

<u>Advance</u>: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reported delays may still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Production-quality systems must use FPGA designs compiled using a Production status speed file. FPGAs designs using a less mature speed file designation may only be used during system prototyping or preproduction qualification. FPGA designs using Advance or Preliminary status speed files should never be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

Xilinx ISE Software Updates: http://www.xilinx.com/support/download/index.htm

All specified limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the following applies: Parameter values apply to all Spartan-3 devices. All parameters representing voltages are measured with respect to GND.

Selected timing parameters and their representative values are included below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3 FPGA v1.38 speed files are the original source for many but not all of the values. The v1.38 speed files are available in Xilinx Integrated Software Environment (ISE) software version 8.2i.

The speed grade designations for these files are shown in Table 39. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Device	Advance	Preliminary	Production
XC3S50			-4, -5 (v1.37 and later)
XC3S200			
XC3S400			
XC3S1000			
XC3S1500			
XC3S2000			
XC3S4000			
XC3S5000			-4, -5 (v1.38 and later)

Table 39: Spartan-3 FPGA Speed Grade Designations (ISE v8.2i or Later)

Table 41: System-Synchronous Pin-to-Pin Setup and Hold Times for the IOB Input Path (Cont'd)

	Description			Speed		
Symbol		Conditions	Device	-5	-4	Units
				Min	Min	
T _{PHFD}	T _{PHFD} When writing to IFF, the time from the active transition at the Global Clock pin to the point when data	LVCMOS25 ⁽³⁾ ,	XC3S50	-0.98	-0.93	ns
		IOBDELAY = IFD, without DCM	XC3S200	-0.40	-0.35	ns
	must be held at the Input pin. The		XC3S400	-0.27	-0.22	ns
	DCM is not in use. The Input Delay is programmed.		XC3S1000	-1.19	-1.14	ns
			XC3S1500	-1.43	-1.38	ns
			XC3S2000	-2.33	-2.28	ns
			XC3S4000	-2.47	-2.42	ns
			XC3S5000	-2.66	-2.61	ns

Notes:

- 1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
- 2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *subtract* the appropriate adjustment from Table 44. If this is true of the data Input, *add* the appropriate Input adjustment from the same table.
- 3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *add* the appropriate Input adjustment from Table 44. If this is true of the data Input, *subtract* the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
- 4. DCM output jitter is included in all measurements.

Table 42: Setup and Hold Times for the IOB Input Path

	Description	Conditions		Speed Grade		
Symbol			Device	-5	-4	Units
				Min	Min	
Setup Times						
T _{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25 ⁽²⁾ ,	XC3S50	1.65	1.89	ns
		IOBDELAY = NONE	XC3S200	1.37	1.57	ns
			XC3S400	1.37	1.57	ns
			XC3S1000	1.65	1.89	ns
			XC3S1500	1.65	1.89	ns
			XC3S2000	1.65	1.89	ns
			XC3S4000	1.73	1.99	ns
			XC3S5000	1.82	2.09	ns
T _{IOPICKD}	Time from the setup of data at the Input pin	LVCMOS25 ⁽²⁾ , IOBDELAY = IFD	XC3S50	4.39	5.04	ns
	input. The Input Delay is programmed.		XC3S200	4.76	5.47	ns
			XC3S400	4.63	5.32	ns
			XC3S1000	5.02	5.76	ns
			XC3S1500	5.40	6.20	ns
			XC3S2000	6.68	7.68	ns
			XC3S4000	7.16	8.24	ns
			XC3S5000	7.33	8.42	ns

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Table 45: Timing for the IOB Output Path

				Speed	Grade	
Symbol	Description	Conditions	Device	-5	-5 -4	Units
				Max ⁽³⁾	Max ⁽³⁾	
Clock-to-Output	Times					
T _{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OTCLK input to data appearing at the Output pin	LVCMOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Propagation Tim	les					
T _{IOOP}	T _{IOOP} The time it takes for data to travel from the IOB's O input to the Output pin T _{IOOLP} The time it takes for data to travel from the O input through the OFF latch to the Output pin	LVCMOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.46	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.94	2.23	ns
T _{IOOLP}			XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Set/Reset Times						
T _{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the	LVCMOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate	XC3S200 XC3S400	2.10	2.41	ns
	Output pin		XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	2.77	3.18	ns
T _{IOGSRQ}	Time from asserting the Global Set Reset (GSR) net to setting/resetting data at the Output pin		All	8.07	9.28	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.

2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 47.

3. For minimums, use the values reported by the Xilinx timing analyzer.

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 58 and Table 59) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 60 through Table 63) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 58 and Table 59.

Period jitter and cycle-cycle jitter are two (of many) different ways of characterizing clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the average clock period of all clock cycles in the collection of clock periods sampled (usually from 100,000 to more than a million samples for specification purposes). In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Delay-Locked Loop (DLL)

Table 58: Recommended Operating Conditions for the DLL

Symbol				Speed Grade				
		Description	Frequency Mode/	-5		-4		Units
			CERIN CONSC	Min	Max	Min	Max	
Input Fr	requency Ranges							
F _{CLKIN}	CLKIN_FREQ_DLL_LF	Frequency for the CLKIN input	Low	18 <mark>(2)</mark>	167 <mark>(3)</mark>	18 <mark>(2)</mark>	167 <mark>(3)</mark>	MHz
	CLKIN_FREQ_DLL_HF		High	48	280 ⁽³⁾	48	280 ⁽³⁾⁽⁴⁾	MHz
Input P	ulse Requirements							
CLKIN_	PULSE	CLKIN pulse width as a	$F_{CLKIN} \le 100 \text{ MHz}$	40%	60%	40%	60%	-
		percentage of the CLKIN period	F _{CLKIN} > 100 MHz	45%	55%	45%	55%	-
Input C	lock Jitter Tolerance and	Delay Path Variation ⁽⁵⁾						
CLKIN_	CYC_JITT_DLL_LF	Cycle-to-cycle jitter at the CLKIN	Low	-	±300	-	±300	ps
CLKIN_	CYC_JITT_DLL_HF	input	High	-	±150	-	±150	ps
CLKIN_	PER_JITT_DLL_LF	Period jitter at the CLKIN input	All	-	±1	-	±1	ns
CLKIN_PER_JITT_DLL_HF				-		-		
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input	All	-	±1	-	±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.

2. The DFS, when operating independently of the DLL, supports lower F_{CLKIN} frequencies. See Table 60.

 The CLKIN_DIVIDE_BY_2 attribute can be used to increase the effective input frequency range up to F_{BUFG}. When set to TRUE, CLKIN_DIVIDE_BY_2 divides the incoming clock frequency by two as it enters the DCM.

4. Industrial temperature range devices have additional requirements for continuous clocking, as specified in Table 64.

5. CLKIN input jitter beyond these limits may cause the DCM to lose lock. See UG331 for more details.



Spartan-3 FPGA Family: Pinout Descriptions

DS099 (v3.0) October 29, 2012

Product Specification

Introduction

This data sheet module describes the various pins on a Spartan®-3 FPGA and how they connect to the supported component packages.

- The Pin Types section categorizes all of the FPGA pins by their function type.
- The Pin Definitions section provides a top-level description for each pin on the device.
- The Detailed, Functional Pin Descriptions section offers significantly more detail about each pin, especially for the dualor special-function pins used during device configuration.
- Some pins have associated behavior that is controlled by settings in the configuration bitstream. These options are described in the Bitstream Options section.
- The Package Overview section describes the various packaging options available for Spartan-3 FPGAs. Detailed pin list tables and footprint diagrams are provided for each package solution.

Pin Descriptions

Pin Types

A majority of the pins on a Spartan-3 FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3 device packages, as outlined in Table 69. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Pin Type/ Color Code	Description	Pin Name
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO, IO_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. There are 12 dual-purpose configuration pins on every package. The INIT_B pin has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM during configuration.	IO_Lxxy_#/DIN/D0, IO_Lxxy_#/D1, IO_Lxxy_#/D2, IO_Lxxy_#/D3, IO_Lxxy_#/D4, IO_Lxxy_#/D5, IO_Lxxy_#/D6, IO_Lxxy_#/D7, IO_Lxxy_#/CS_B, IO_Lxxy_#/RDWR_B, IO_Lxxy_#/BUSY/DOUT, IO_Lxxy_#/INIT_B
CONFIG	Dedicated configuration pin. Not available as a user-I/O pin. Every package has seven dedicated configuration pins. These pins are powered by VCCAUX and have a dedicated internal pull-up resistor to VCCAUX during configuration.	CCLK, DONE, M2, M1, M0, PROG_B, HSWAP_EN
JTAG	Dedicated JTAG pin. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX and have a dedicated internal pull-up resistor to VCCAUX during configuration.	TDI, TMS, TCK, TDO
DCI	Dual-purpose pin that is either a user-I/O pin or used to calibrate output buffer impedance for a specific bank using Digital Controlled Impedance (DCI). There are two DCI pins per I/O bank.	IO/VRN_# IO_Lxxy_#/VRN_# IO/VRP_# IO_Lxxy_#/VRP_#

Table 09. Types of Fills on Spartan-31 FGAs	Table	69:	Types	of P	Pins	on	Spartan-3	FPGAs
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Table 69: Types of Pins on Spartan-3 FPGAs (Cont'd)

Pin Type/ Color Code	Description	Pin Name
VREF	Dual-purpose pin that is either a user-I/O pin or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IO/VREF_# IO_Lxxy_#/VREF_#
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. All must be connected to +2.5V.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V.	VCCINT
VCCO	Dedicated I/O bank, output buffer power supply pin. Along with other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards.	VCCO_# CP132 and TQ144 Packages Only: VCCO_LEFT, VCCO_TOP, VCCO_RIGHT, VCCO_BOTTOM
GCLK	Dual-purpose pin that is either a user-I/O pin or an input to a specific global buffer input. Every package has eight dedicated GCLK pins.	IO_Lxxy_#/GCLK0, IO_Lxxy_#/GCLK1, IO_Lxxy_#/GCLK2, IO_Lxxy_#/GCLK3, IO_Lxxy_#/GCLK4, IO_Lxxy_#/GCLK5, IO_Lxxy_#/GCLK6, IO_Lxxy_#/GCLK7
N.C.	This package pin is not connected in this specific device/package combination but may be connected in larger devices in the same package.	N.C.

Notes:

1. # = I/O bank number, an integer between 0 and 7.

I/Os with Lxxy_# are part of a differential output pair. 'L' indicates differential output capability. The "xx" field is a two-digit integer, unique to each bank that identifies a differential pin-pair. The 'y' field is either 'P' for the true signal or 'N' for the inverted signal in the differential pair. The '#' field is the I/O bank number.

Pin Definitions

Table 70 provides a brief description of each pin listed in the Spartan-3 FPGA pinout tables and package footprint diagrams. Pins are categorized by their pin type, as listed in Table 69. See Detailed, Functional Pin Descriptions for more information.

Table 89: CP132 Package Pinout (Cont'd)

Bank	XC3S50 Pin Name	CP132 Ball	Туре
2	IO_L24P_2	G13	I/O
2	IO_L40N_2	G14	I/O
2	IO_L40P_2/VREF_2	H12	VREF
3	IO_L01N_3/VRP_3	N13	DCI
3	IO_L01P_3/VRN_3	N14	DCI
3	IO_L20N_3	L12	I/O
3	IO_L20P_3	M14	I/O
3	IO_L22N_3	L14	I/O
3	IO_L22P_3	L13	I/O
3	IO_L23N_3	K13	I/O
3	IO_L23P_3/VREF_3	K12	VREF
3	IO_L24N_3	J12	I/O
3	IO_L24P_3	K14	I/O
3	IO_L40N_3/VREF_3	H14	VREF
3	IO_L40P_3	J13	I/O
4	IO/VREF_4	N12	VREF
4	IO_L01N_4/VRP_4	P12	DCI
4	IO_L01P_4/VRN_4	M11	DCI
4	IO_L27N_4/DIN/D0	M10	DUAL
4	IO_L27P_4/D1	N10	DUAL
4	IO_L30N_4/D2	N9	DUAL
4	IO_L30P_4/D3	P9	DUAL
4	IO_L31N_4/INIT_B	M8	DUAL
4	IO_L31P_4/DOUT/BUSY	N8	DUAL
4	IO_L32N_4/GCLK1	P8	GCLK
4	IO_L32P_4/GCLK0	M7	GCLK
5	IO_L01N_5/RDWR_B	P2	DUAL
5	IO_L01P_5/CS_B	N2	DUAL
5	IO_L27N_5/VREF_5	M4	VREF
5	IO_L27P_5	P3	I/O
5	IO_L28N_5/D6	P4	DUAL
5	IO_L28P_5/D7	N4	DUAL
5	IO_L31N_5/D4	M6	DUAL
5	IO_L31P_5/D5	P5	DUAL
5	IO_L32N_5/GCLK3	P7	GCLK
5	IO_L32P_5/GCLK2	P6	GCLK
6	IO_L01N_6/VRP_6	L3	DCI
6	IO_L01P_6/VRN_6	M1	DCI
6	IO_L20N_6	K3	I/O
6	IO_L20P_6	K2	I/O

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User I/Os by Bank

Table 92 indicates how the available user-I/O pins are distributed between the eight I/O banks on the TQ144 package.

Table 92: User I/Os Per Bank in TQ144 Package

Package Edge I/O Bank Maximum I/O All Possible I/O Pins by Type					ns by Type		
Fackage Luge	I/O Dallk		I/O	DUAL	DCI	VREF	GCLK
Тор	0	10	5	0	2	1	2
	1	9	4	0	2	1	2
Diaht	2	14	10	0	2	2	0
nigiii	3	15	11	0	2	2	0
Bottom	4	11	0	6	2	1	2
Bollom	5	9	0	6	0	1	2
Left	6	14	10	0	2	2	0
	7	15	11	0	2	2	0

Table 103: FG676 Package Pinout (Cont'd)

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Туре
6	IO_L20N_6	IO_L20N_6	IO_L20N_6	IO_L20N_6	IO_L20N_6	V7	I/O
6	IO_L20P_6	IO_L20P_6	IO_L20P_6	IO_L20P_6	IO_L20P_6	U7	I/O
6	IO_L21N_6	IO_L21N_6	IO_L21N_6	IO_L21N_6	IO_L21N_6	V5	I/O
6	IO_L21P_6	IO_L21P_6	IO_L21P_6	IO_L21P_6	IO_L21P_6	V4	I/O
6	IO_L22N_6	IO_L22N_6	IO_L22N_6	IO_L22N_6	IO_L22N_6	V3	I/O
6	IO_L22P_6	IO_L22P_6	IO_L22P_6	IO_L22P_6	IO_L22P_6	V2	I/O
6	IO_L23N_6	IO_L23N_6	IO_L23N_6	IO_L23N_6	IO_L23N_6	U6	I/O
6	IO_L23P_6	IO_L23P_6	IO_L23P_6	IO_L23P_6	IO_L23P_6	U5	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	U4	VREF
6	IO_L24P_6	IO_L24P_6	IO_L24P_6	IO_L24P_6	IO_L24P_6	U3	I/O
6	IO_L26N_6	IO_L26N_6	IO_L26N_6	IO_L26N_6	IO_L26N_6	U2	I/O
6	IO_L26P_6	IO_L26P_6	IO_L26P_6	IO_L26P_6	IO_L26P_6	U1	I/O
6	IO_L27N_6	IO_L27N_6	IO_L27N_6	IO_L27N_6	IO_L27N_6	Т8	I/O
6	IO_L27P_6	IO_L27P_6	IO_L27P_6	IO_L27P_6	IO_L27P_6	T7	I/O
6	IO_L28N_6	IO_L28N_6	IO_L28N_6	IO_L28N_6	IO_L28N_6	Т6	I/O
6	IO_L28P_6	IO_L28P_6	IO_L28P_6	IO_L28P_6	IO_L28P_6	T5	I/O
6	IO_L29N_6	IO_L29N_6	IO_L29N_6	IO_L29N_6	IO_L29N_6	T2	I/O
6	IO_L29P_6	IO_L29P_6	IO_L29P_6	IO_L29P_6	IO_L29P_6	T1	I/O
6	IO_L31N_6	IO_L31N_6	IO_L31N_6	IO_L31N_6	IO_L31N_6	R8	I/O
6	IO_L31P_6	IO_L31P_6	IO_L31P_6	IO_L31P_6	IO_L31P_6	R7	I/O
6	IO_L32N_6	IO_L32N_6	IO_L32N_6	IO_L32N_6	IO_L32N_6	R6	I/O
6	IO_L32P_6	IO_L32P_6	IO_L32P_6	IO_L32P_6	IO_L32P_6	R5	I/O
6	IO_L33N_6	IO_L33N_6	IO_L33N_6	IO_L33N_6	IO_L33N_6	T4	I/O
6	IO_L33P_6	IO_L33P_6	IO_L33P_6	IO_L33P_6	IO_L33P_6	R3	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	R2	VREF
6	IO_L34P_6	IO_L34P_6	IO_L34P_6	IO_L34P_6	IO_L34P_6	R1	I/O
6	IO_L35N_6	IO_L35N_6	IO_L35N_6	IO_L35N_6	IO_L35N_6	P8	I/O
6	IO_L35P_6	IO_L35P_6	IO_L35P_6	IO_L35P_6	IO_L35P_6	P7	I/O
6	IO_L38N_6	IO_L38N_6	IO_L38N_6	IO_L38N_6	IO_L38N_6	P6	I/O
6	IO_L38P_6	IO_L38P_6	IO_L38P_6	IO_L38P_6	IO_L38P_6	P5	I/O
6	IO_L39N_6	IO_L39N_6	IO_L39N_6	IO_L39N_6	IO_L39N_6	P4	I/O
6	IO_L39P_6	IO_L39P_6	IO_L39P_6	IO_L39P_6	IO_L39P_6	P3	I/O
6	IO_L40N_6	IO_L40N_6	IO_L40N_6	IO_L40N_6	IO_L40N_6	P2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	P1	VREF
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	P9	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	P10	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	R9	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	Т3	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	Т9	vcco
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	U8	vcco
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	V8	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	Y3	vcco
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	F5	DCI

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Туре
2	VCCO_2	VCCO_2	J28	VCCO
2	VCCO_2	VCCO_2	N28	VCCO
3	IO	IO	AB25	I/O
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	AH30	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	AH29	DCI
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	AG28	VREF
3	IO_L02P_3	IO_L02P_3	AG27	I/O
3	IO_L03N_3	IO_L03N_3	AG30	I/O
3	IO_L03P_3	IO_L03P_3	AG29	I/O
3	IO_L04N_3	IO_L04N_3	AF30	I/O
3	IO_L04P_3	IO_L04P_3	AF29	I/O
3	IO_L05N_3	IO_L05N_3	AE26	I/O
3	IO_L05P_3	IO_L05P_3	AF27	I/O
3	IO_L06N_3	IO_L06N_3	AE29	I/O
3	IO_L06P_3	IO_L06P_3	AE28	I/O
3	IO_L07N_3	IO_L07N_3	AD28	I/O
3	IO_L07P_3	IO_L07P_3	AD27	I/O
3	IO_L08N_3	IO_L08N_3	AD30	I/O
3	IO_L08P_3	IO_L08P_3	AD29	I/O
3	IO_L09N_3	IO_L09N_3	AC24	I/O
3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	AD25	VREF
3	IO_L10N_3	IO_L10N_3	AC26	I/O
3	IO_L10P_3	IO_L10P_3	AC25	I/O
3	IO_L11N_3	IO_L11N_3	AC28	I/O
3	IO_L11P_3	IO_L11P_3	AC27	I/O
3	IO_L13N_3/VREF_3	IO_L13N_3/VREF_3	AC30	VREF
3	IO_L13P_3	IO_L13P_3	AC29	I/O
3	IO_L14N_3	IO_L14N_3	AB27	I/O
3	IO_L14P_3	IO_L14P_3	AB26	I/O
3	IO_L15N_3	IO_L15N_3	AB30	I/O
3	IO_L15P_3	IO_L15P_3	AB29	I/O
3	IO_L16N_3	IO_L16N_3	AA22	I/O
3	IO_L16P_3	IO_L16P_3	AB23	I/O
3	IO_L17N_3	IO_L17N_3	AA25	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	AA24	VREF
3	IO_L19N_3	IO_L19N_3	AA29	I/O
3	IO_L19P_3	IO_L19P_3	AA28	I/O
3	IO_L20N_3	IO_L20N_3	Y21	I/O
3	IO_L20P_3	IO_L20P_3	AA21	I/O
3	IO_L21N_3	IO_L21N_3	Y24	I/O

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Туре
3	N.C. (♠)	IO_L50P_3	V26	I/O
3	VCCO_3	VCCO_3	U20	VCCO
3	VCCO_3	VCCO_3	V20	VCCO
3	VCCO_3	VCCO_3	W20	VCCO
3	VCCO_3	VCCO_3	Y22	VCCO
3	VCCO_3	VCCO_3	V24	VCCO
3	VCCO_3	VCCO_3	AB24	VCCO
3	VCCO_3	VCCO_3	AD26	VCCO
3	VCCO_3	VCCO_3	V28	VCCO
3	VCCO_3	VCCO_3	AB28	VCCO
3	VCCO_3	VCCO_3	AF28	VCCO
4	IO	IO	AA16	I/O
4	IO	IO	AG18	I/O
4	IO	IO	AA18	I/O
4	IO	IO	AE22	I/O
4	IO	IO	AD23	I/O
4	IO	IO	AH27	I/O
4	IO/VREF_4	IO/VREF_4	AF16	VREF
4	IO/VREF_4	IO/VREF_4	AK28	VREF
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	AJ27	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	AK27	DCI
4	IO_L02N_4	IO_L02N_4	AJ26	I/O
4	IO_L02P_4	IO_L02P_4	AK26	I/O
4	IO_L03N_4	IO_L03N_4	AG26	I/O
4	IO_L03P_4	IO_L03P_4	AF25	I/O
4	IO_L04N_4	IO_L04N_4	AD24	I/O
4	IO_L04P_4	IO_L04P_4	AC23	I/O
4	IO_L05N_4	IO_L05N_4	AE23	I/O
4	IO_L05P_4	IO_L05P_4	AF23	I/O
4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	AG23	VREF
4	IO_L06P_4	IO_L06P_4	AH23	I/O
4	IO_L07N_4	IO_L07N_4	AJ23	I/O
4	IO_L07P_4	IO_L07P_4	AK23	I/O
4	IO_L08N_4	IO_L08N_4	AB22	I/O
4	IO_L08P_4	IO_L08P_4	AC22	I/O
4	IO_L09N_4	IO_L09N_4	AF22	I/O
4	IO_L09P_4	IO_L09P_4	AG22	I/O
4	IO_L10N_4	IO_L10N_4	AJ22	I/O
4	IO_L10P_4	IO_L10P_4	AK22	I/O
4	IO_L11N_4	IO_L11N_4	AD21	I/O

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Туре
2	IO_L19N_2	IO_L19N_2	M29	I/O
2	IO_L19P_2	IO_L19P_2	M30	I/O
2	IO_L20N_2	IO_L20N_2	M31	I/O
2	IO_L20P_2	IO_L20P_2	M32	I/O
2	IO_L21N_2	IO_L21N_2	M26	I/O
2	IO_L21P_2	IO_L21P_2	N25	I/O
2	IO_L22N_2	IO_L22N_2	N27	I/O
2	IO_L22P_2	IO_L22P_2	N28	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2VREF_2	N31	VREF
2	IO_L23P_2	IO_L23P_2	N32	I/O
2	IO_L24N_2	IO_L24N_2	N24	I/O
2	IO_L24P_2	IO_L24P_2	P24	I/O
2	IO_L26N_2	IO_L26N_2	P29	I/O
2	IO_L26P_2	IO_L26P_2	P30	I/O
2	IO_L27N_2	IO_L27N_2	P31	I/O
2	IO_L27P_2	IO_L27P_2	P32	I/O
2	IO_L28N_2	IO_L28N_2	P33	I/O
2	IO_L28P_2	IO_L28P_2	P34	I/O
2	IO_L29N_2	IO_L29N_2	R24	I/O
2	IO_L29P_2	IO_L29P_2	R25	I/O
2	IO_L30N_2	IO_L30N_2	R28	I/O
2	IO_L30P_2	IO_L30P_2	R29	I/O
2	IO_L31N_2	IO_L31N_2	R31	I/O
2	IO_L31P_2	IO_L31P_2	R32	I/O
2	IO_L32N_2	IO_L32N_2	R33	I/O
2	IO_L32P_2	IO_L32P_2	R34	I/O
2	IO_L33N_2	IO_L33N_2	R26	I/O
2	IO_L33P_2	IO_L33P_2	T25	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	T28	VREF
2	IO_L34P_2	IO_L34P_2	T29	I/O
2	IO_L35N_2	IO_L35N_2	T32	I/O
2	IO_L35P_2	IO_L35P_2	T33	I/O
2	IO_L37N_2	IO_L37N_2	U27	I/O
2	IO_L37P_2	IO_L37P_2	U28	I/O
2	IO_L38N_2	IO_L38N_2	U29	I/O
2	IO_L38P_2	IO_L38P_2	U30	I/O
2	IO_L39N_2	IO_L39N_2	U31	I/O
2	IO_L39P_2	IO_L39P_2	U32	I/O
2	IO_L40N_2	IO_L40N_2	U33	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	U34	VREF

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Туре
N/A	GND	GND	AA18	GND
N/A	GND	GND	AA19	GND
N/A	GND	GND	AA20	GND
N/A	GND	GND	AA21	GND
N/A	GND	GND	AB1	GND
N/A	GND	GND	AB17	GND
N/A	GND	GND	AB18	GND
N/A	GND	GND	AB26	GND
N/A	GND	GND	AB30	GND
N/A	GND	GND	AB34	GND
N/A	GND	GND	AB5	GND
N/A	GND	GND	AB9	GND
N/A	GND	GND	AD3	GND
N/A	GND	GND	AD32	GND
N/A	GND	GND	AE10	GND
N/A	GND	GND	AE25	GND
N/A	GND	GND	AF1	GND
N/A	GND	GND	AF13	GND
N/A	GND	GND	AF16	GND
N/A	GND	GND	AF19	GND
N/A	GND	GND	AF22	GND
N/A	GND	GND	AF30	GND
N/A	GND	GND	AF34	GND
N/A	GND	GND	AF5	GND
N/A	GND	GND	AH28	GND
N/A	GND	GND	AH7	GND
N/A	GND	GND	AK1	GND
N/A	GND	GND	AK13	GND
N/A	GND	GND	AK16	GND
N/A	GND	GND	AK19	GND
N/A	GND	GND	AK22	GND
N/A	GND	GND	AK26	GND
N/A	GND	GND	AK30	GND
N/A	GND	GND	AK34	GND
N/A	GND	GND	AK5	GND
N/A	GND	GND	AK9	GND
N/A	GND	GND	AM11	GND
N/A	GND	GND	AM24	GND
N/A	GND	GND	AM3	GND
N/A	GND	GND	AM32	GND

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Туре
N/A	VCCINT	VCCINT	Y22	VCCINT
VCCAUX	CCLK	CCLK	AL31	CONFIG
VCCAUX	DONE	DONE	AD24	CONFIG
VCCAUX	HSWAP_EN	HSWAP_EN	L11	CONFIG
VCCAUX	MO	MO	AL4	CONFIG
VCCAUX	M1	M1	AK4	CONFIG
VCCAUX	M2	M2	AG8	CONFIG
VCCAUX	PROG_B	PROG_B	D4	CONFIG
VCCAUX	ТСК	ТСК	D31	JTAG
VCCAUX	TDI	TDI	E4	JTAG
VCCAUX	TDO	TDO	E31	JTAG
VCCAUX	TMS	TMS	H27	JTAG