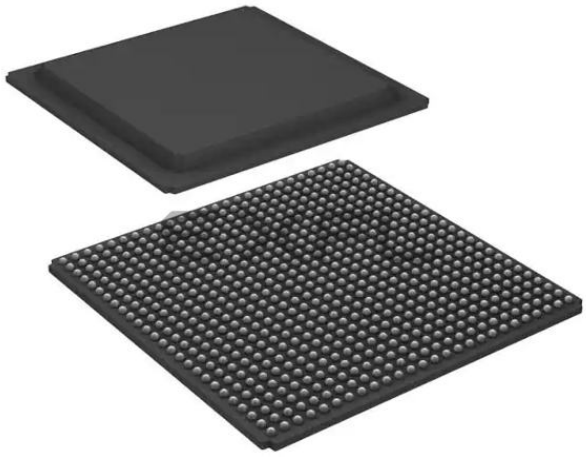

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3328
Number of Logic Elements/Cells	29952
Total RAM Bits	589824
Number of I/O	487
Number of Gates	1500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1500-5fg676c

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Table 10: **DCI I/O Standards**

Category of Signal Standard	Signal Standard (IOSTANDARD)	V_{CCO} (V)		V_{REF} for Inputs (V)	Termination Type	
		For Outputs	For Inputs		At Output	At Input
Single-Ended						
Gunning Transceiver Logic	GTL_DCI	1.2	1.2	0.8	Single	Single
	GTLP_DCI	1.5	1.5	1.0		
High-Speed Transceiver Logic	HSTL_I_DCI	1.5	1.5	0.75	None	Split
	HSTL_III_DCI	1.5	1.5	0.9	None	Single
	HSTL_I_DCI_18	1.8	1.8	0.9	None	Split
	HSTL_II_DCI_18 DIFF_HSTL_II_18_DCI	1.8	1.8	0.9	Split	
	HSTL_III_DCI_18	1.8	1.8	1.1	None	Single
Low-Voltage CMOS	LVDCI_15	1.5	1.5	–	Controlled impedance driver	None
	LVDCI_18	1.8	1.8	–		
	LVDCI_25	2.5	2.5	–		
	LVDCI_33(2)	3.3	3.3	–		
	LVDCI_DV2_15	1.5	1.5	–	Controlled driver with half-impedance	
	LVDCI_DV2_18	1.8	1.8	–		
	LVDCI_DV2_25	2.5	2.5	–		
	LVDCI_DV2_33	3.3	3.3	–		
Hybrid HSTL Input and LVCMOS Output	HSLVDCI_15	1.5	1.5	0.75	Controlled impedance driver	None
	HSLVDCI_18	1.8	1.8	0.9		
	HSLVDCI_25	2.5	2.5	1.25		
	HSLVDCI_33	3.3	3.3	1.65		
Stub Series Terminated Logic(3)	SSTL18_I_DCI	1.8	1.8	0.9	25Ω driver	Split
	SSTL2_I_DCI	2.5	2.5	1.25	25Ω driver	
	SSTL2_II_DCI DIFF_SSTL2_II_DCI	2.5	2.5	1.25	Split with 25Ω driver	
Differential						
Low-Voltage Differential Signaling	LVDS_25_DCI	N/A	2.5	–	None	Split on each line of pair
	LVDSEXT_25_DCI	N/A	2.5	–		

Notes:

1. DCI signal standards are not supported in Bank 5 of any Spartan-3 FPGA packaged in a VQ100, CP132, or TQ144 package.
2. Equivalent to LVTTL DCI.
3. The SSTL18_II signal standard does not have a DCI equivalent.

Supply Voltages for the IOBs

Three different supplies power the IOBs:

- The V_{CCO} supplies, one for each of the FPGA's I/O banks, power the output drivers, except when using the GTL and GTLP signal standards. The voltage on the V_{CCO} pins determines the voltage swing of the output signal.
- V_{CCINT} is the main power supply for the FPGA's internal logic.
- The V_{CCAUX} is an auxiliary source of power, primarily to optimize the performance of various FPGA functions such as I/O switching.

The I/Os During Power-On, Configuration, and User Mode

With no power applied to the FPGA, all I/Os are in a high-impedance state. The V_{CCINT} (1.2V), V_{CCAUX} (2.5V), and V_{CCO} supplies may be applied in any order. Before power-on can finish, V_{CCINT}, V_{CCO} Bank 4, and V_{CCAUX} must have reached their respective minimum recommended operating levels (see Table 29, page 59). At this time, all I/O drivers also will be in a high-impedance state. V_{CCO} Bank 4, V_{CCINT}, and V_{CCAUX} serve as inputs to the internal Power-On Reset circuit (POR).

A Low level applied to the HSWAP_EN input enables pull-up resistors on User I/Os from power-on throughout configuration. A High level on HSWAP_EN disables the pull-up resistors, allowing the I/Os to float. If the HSWAP_EN pin is floating, then an internal pull-up resistor pulls HSWAP_EN High. As soon as power is applied, the FPGA begins initializing its configuration memory. At the same time, the FPGA internally asserts the Global Set-Reset (GSR), which asynchronously resets all IOB storage elements to a Low state.

Upon the completion of initialization, INIT_B goes High, sampling the M0, M1, and M2 inputs to determine the configuration mode. At this point, the configuration data is loaded into the FPGA. The I/O drivers remain in a high-impedance state (with or without pull-up resistors, as determined by the HSWAP_EN input) throughout configuration.

The Global Three State (GTS) net is released during Start-Up, marking the end of configuration and the beginning of design operation in the User mode. At this point, those I/Os to which signals have been assigned go active while all unused I/Os remain in a high-impedance state. The release of the GSR net, also part of Start-up, leaves the IOB registers in a Low state by default, unless the loaded design reverses the polarity of their respective RS inputs.

In User mode, all internal pull-up resistors on the I/Os are disabled and HSWAP_EN becomes a "don't care" input. If it is desirable to have pull-up or pull-down resistors on I/Os carrying signals, the appropriate symbol—e.g., PULLUP, PULLDOWN—must be placed at the appropriate pads in the design. The Bitstream Generator (Bitgen) option UnusedPin available in the Xilinx development software determines whether unused I/Os collectively have pull-up resistors, pull-down resistors, or no resistors in User mode.

CLB Overview

For more details on the CLBs, refer to the chapter entitled "Using Configurable Logic Blocks" in UG331.

The Configurable Logic Blocks (CLBs) constitute the main logic resource for implementing synchronous as well as combinatorial circuits. Each CLB comprises four interconnected slices, as shown in Figure 11. These slices are grouped in pairs. Each pair is organized as a column with an independent carry chain.

The nomenclature that the FPGA Editor—part of the Xilinx development software—uses to designate slices is as follows: The letter 'X' followed by a number identifies columns of slices. The 'X' number counts up in sequence from the left side of the die to the right. The letter 'Y' followed by a number identifies the position of each slice in a pair as well as indicating the CLB row. The 'Y' number counts slices starting from the bottom of the die according to the sequence: 0, 1, 0, 1 (the first CLB row); 2, 3, 2, 3 (the second CLB row); etc. Figure 11 shows the CLB located in the lower left-hand corner of the die. Slices X0Y0 and X0Y1 make up the column-pair on the left where as slices X1Y0 and X1Y1 make up the column-pair on the right. For each CLB, the term "left-hand" (or SLICEM) indicates the pair of slices labeled with an even 'X' number, such as X0, and the term "right-hand" (or SLICEL) designates the pair of slices with an odd 'X' number, e.g., X1.

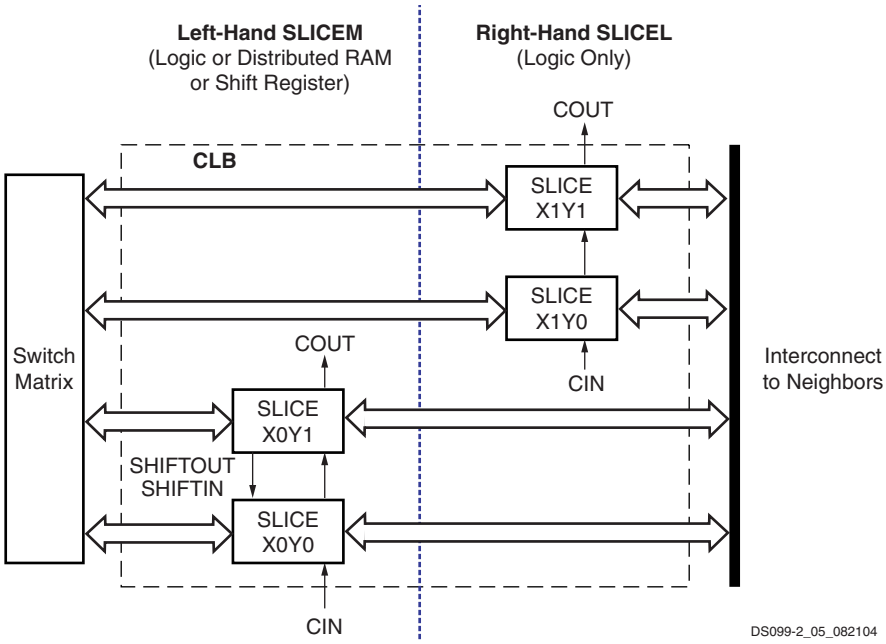


Figure 11: **Arrangement of Slices within the CLB**

Elements Within a Slice

All four slices have the following elements in common: two logic function generators, two storage elements, wide-function multiplexers, carry logic, and arithmetic gates, as shown in Figure 12, page 24. Both the left-hand and right-hand slice pairs use these elements to provide logic, arithmetic, and ROM functions. Besides these, the left-hand pair supports two additional functions: storing data using Distributed RAM and shifting data with 16-bit registers. Figure 12 is a diagram of the left-hand slice; therefore, it represents a superset of the elements and connections to be found in all slices. See Function Generator, page 25 for more information.

The RAM-based function generator—also known as a Look-Up Table or LUT—is the main resource for implementing logic functions. Furthermore, the LUTs in each left-hand slice pair can be configured as Distributed RAM or a 16-bit shift register. For information on the former, refer to the chapter entitled “Using Look-Up Tables as Distributed RAM” in UG331; for information on the latter, refer to the chapter entitled “Using Look-Up Tables as Shift Registers” in UG331. The function generators located in the upper and lower portions of the slice are referred to as the "G" and "F", respectively.

The storage element, which is programmable as either a D-type flip-flop or a level-sensitive latch, provides a means for synchronizing data to a clock signal, among other uses. The storage elements in the upper and lower portions of the slice are called FFY and FFX, respectively.

Wide-function multiplexers effectively combine LUTs in order to permit more complex logic operations. Each slice has two of these multiplexers with F5MUX in the lower portion of the slice and FiMUX in the upper portion. Depending on the slice, FiMUX takes on the name F6MUX, F7MUX, or F8MUX. For more details on the multiplexers, refer to the chapter entitled “Using Dedicated Multiplexers” in UG331.

The carry chain, together with various dedicated arithmetic logic gates, support fast and efficient implementations of math operations. The carry chain enters the slice as CIN and exits as COUT. Five multiplexers control the chain: CYINIT, CY0F, and CYMUXF in the lower portion as well as CY0G and CYMUXG in the upper portion. The dedicated arithmetic logic includes the exclusive-OR gates XORG and XORF (upper and lower portions of the slice, respectively) as well as the AND gates GAND and FAND (upper and lower portions, respectively). For more details on the carry logic, refer to the chapter entitled “Using Carry and Arithmetic Logic” in UG331.

Main Logic Paths

Central to the operation of each slice are two nearly identical data paths, distinguished using the terms *top* and *bottom*. The description that follows uses names associated with the bottom path. (The top path names appear in parentheses.) The basic path originates at an interconnect-switch matrix outside the CLB. Four lines, F1 through F4 (or G1 through G4 on the

Function Generator

Each of the two LUTs (F and G) in a slice have four logic inputs (A1-A4) and a single output (D). This permits any four-variable Boolean logic operation to be programmed into them. Furthermore, wide function multiplexers can be used to effectively combine LUTs within the same CLB or across different CLBs, making logic functions with still more input variables possible.

The LUTs in both the right-hand and left-hand slice-pairs not only support the logic functions described above, but also can function as ROM that is initialized with data at the time of configuration.

The LUTs in the left-hand slice-pair (even-numbered columns such as X0 in Figure 11) of each CLB support two additional functions that the right-hand slice-pair (odd-numbered columns such as X1) do not.

First, it is possible to program the “left-hand LUTs” as distributed RAM. This type of memory affords moderate amounts of data buffering anywhere along a data path. One left-hand LUT stores 16 bits. Multiple left-hand LUTs can be combined in various ways to store larger amounts of data. A dual port option combines two LUTs so that memory access is possible from two independent data lines. A Distributed ROM option permits pre-loading the memory with data during FPGA configuration.

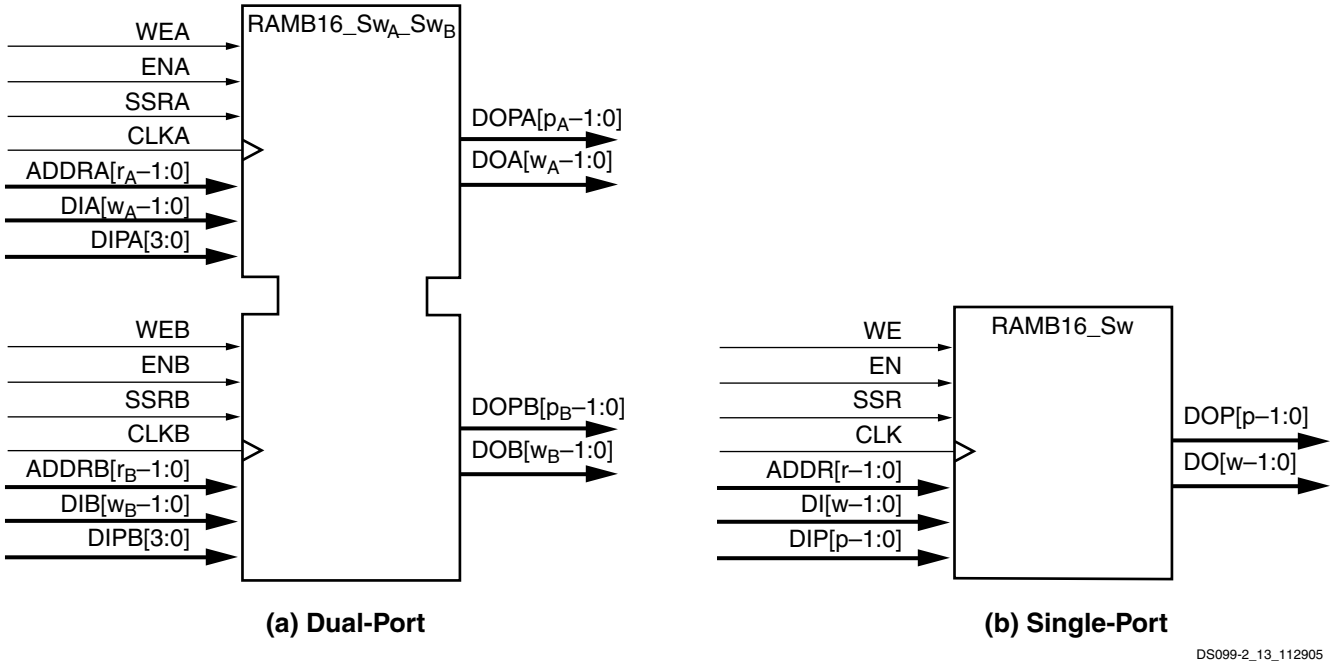
Second, it is possible to program each left-hand LUT as a 16-bit shift register. Used in this way, each LUT can delay serial data anywhere from one to 16 clock cycles. The four left-hand LUTs of a single CLB can be combined to produce delays up to 64 clock cycles. The SHIFTIN and SHIFTOUT lines cascade LUTs to form larger shift registers. It is also possible to combine shift registers across more than one CLB. The resulting programmable delays can be used to balance the timing of data pipelines.

Block RAM Overview

All Spartan-3 devices support block RAM, which is organized as configurable, synchronous 18Kbit blocks. Block RAM stores relatively large amounts of data more efficiently than the distributed RAM feature described earlier. (The latter is better suited for buffering small amounts of data anywhere along signal paths.) This section describes basic Block RAM functions. For more information, refer to the chapter entitled “Using Block RAM” in UG331.

The aspect ratio—i.e., width vs. depth—of each block RAM is configurable. Furthermore, multiple blocks can be cascaded to create still wider and/or deeper memories.

A choice among primitives determines whether the block RAM functions as dual- or single-port memory. A name of the form RAMB16_S[w_A]_S[w_B] calls out the dual-port primitive, where the integers w_A and w_B specify the total data path width at ports w_A and w_B, respectively. Thus, a RAMB16_S9_S18 is a dual-port RAM with a 9-bit-wide Port A and an 18-bit-wide Port B. A name of the form RAMB16_S[w] identifies the single-port primitive, where the integer w specifies the total data path width of the lone port. A RAMB16_S18 is a single-port RAM with an 18-bit-wide port. Other memory functions—e.g., FIFOs, data path width conversion, ROM, etc.—are readily available using the CORE Generator™ software, part of the Xilinx development software.



Notes:

1. w_A and w_B are integers representing the total data path width (i.e., data bits plus parity bits) at ports A and B, respectively.
2. p_A and p_B are integers that indicate the number of data path lines serving as parity bits.
3. r_A and r_B are integers representing the address bus width at ports A and B, respectively.
4. The control signals CLK, WE, EN, and SSR on both ports have the option of inverted polarity.

Figure 14: **Block RAM Primitives**

Table 13: **Block RAM Port Signals**

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Address Bus	ADDRA	ADDRB	Input	The Address Bus selects a memory location for read or write operations. The width (w) of the port's associated data path determines the number of available address lines (r). Whenever a port is enabled (ENA or ENB = High), address transitions must meet the data sheet setup and hold times with respect to the port clock (CLKA or CLKB). This requirement must be met, even if the RAM read output is of no interest.
Data Input Bus	DIA	DIB	Input	Data at the DI input bus is written to the addressed memory location addressed on an enabled active CLK edge. It is possible to configure a port's total data path width (w) to be 1, 2, 4, 9, 18, or 36 bits. This selection applies to both the DI and DO paths of a given port. Each port is independent. For a port assigned a width (w), the number of addressable locations is 16,384/(w-p) where "p" is the number of parity bits. Each memory location has a width of "w" (including parity bits). See the DIP signal description for more information of parity.
Parity Data Input(s)	DIPA	DIPB	Input	Parity inputs represent additional bits included in the data input path to support error detection. The number of parity bits "p" included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 14.

The product of w and n yields the total block RAM capacity. Equation 1 and Equation 2 show that as the data bus width increases, the number of address lines along with the number of addressable memory locations decreases. Using the permissible DI/DO bus widths as inputs to these equations provides the bus width and memory capacity measures shown in Table 14.

Table 14: **Port Aspect Ratios for Port A or B**

DI/DO Bus Width (w – p Bits)	DIP/DOP Bus Width (p Bits)	Total Data Path Width (w Bits)	ADDR Bus Width (r Bits)	No. of Addressable Locations (n)	Block RAM Capacity (Bits)
1	0	1	14	16,384	16,384
2	0	2	13	8,192	16,384
4	0	4	12	4,096	16,384
8	1	9	11	2,048	18,432
16	2	18	10	1,024	18,432
32	4	36	9	512	18,432

Block RAM Data Operations

Writing data to and accessing data from the block RAM are synchronous operations that take place independently on each of the two ports.

The waveforms for the write operation are shown in the top half of the Figure 15, Figure 16, and Figure 17. When the WE and EN signals enable the active edge of CLK, data at the DI input bus is written to the block RAM location addressed by the ADDR lines.

There are a number of different conditions under which data can be accessed at the DO outputs. Basic data access always occurs when the WE input is inactive. Under this condition, data stored in the memory location addressed by the ADDR lines passes through a transparent output latch to the DO outputs. The timing for basic data access is shown in the portions of Figure 15, Figure 16, and Figure 17 during which WE is Low.

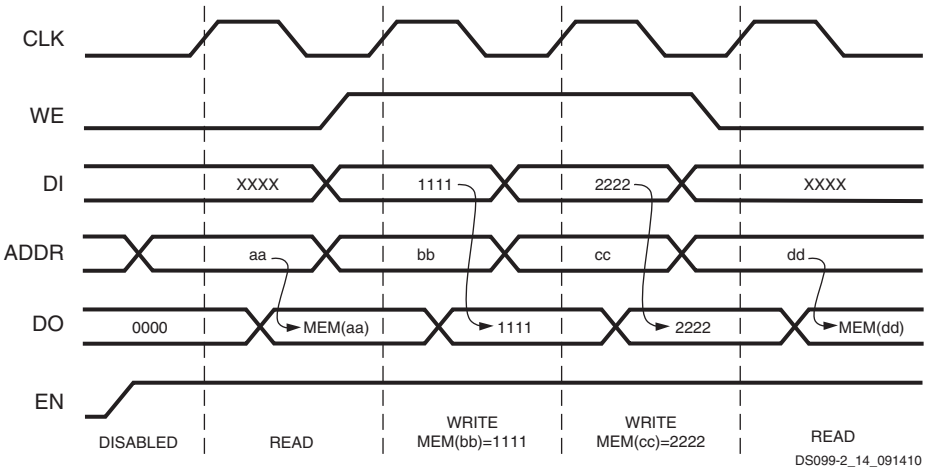


Figure 15: **Waveforms of Block RAM Data Operations with WRITE_FIRST Selected**

Data can also be accessed on the DO outputs when asserting the WE input. This is accomplished using two different attributes:

Choosing the WRITE_FIRST attribute, data is written to the addressed memory location on an enabled active CLK edge and is also passed to the DO outputs. WRITE_FIRST timing is shown in the portion of Figure 15 during which WE is High.

Choosing the READ_FIRST attribute, data already stored in the addressed location pass to the DO outputs before that location is overwritten with new data from the DI inputs on an enabled active CLK edge. READ_FIRST timing is shown in the portion of Figure 16 during which WE is High.

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Table 35: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

Signal Standard (IOSTANDARD)	V_{CCO}			V_{REF}			V_{IL}	V_{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
GTL[3]	–	–	–	0.74	0.8	0.86	V_{REF} – 0.05	V_{REF} + 0.05
GTL_DCI	–	1.2	–	0.74	0.8	0.86	V_{REF} – 0.05	V_{REF} + 0.05
GTLP[3]	–	–	–	0.88	1	1.12	V_{REF} – 0.1	V_{REF} + 0.1
GTLP_DCI	–	1.5	–	0.88	1	1.12	V_{REF} – 0.1	V_{REF} + 0.1
HSLVDCI_15	1.4	1.5	1.6	–	0.75	–	V_{REF} – 0.1	V_{REF} + 0.1
HSLVDCI_18	1.7	1.8	1.9	–	0.9	–	V_{REF} – 0.1	V_{REF} + 0.1
HSLVDCI_25	2.3	2.5	2.7	–	1.25	–	V_{REF} – 0.1	V_{REF} + 0.1
HSLVDCI_33	3.0	3.3	3.465	–	1.65	–	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_I, HSTL_I_DCI	1.4	1.5	1.6	0.68	0.75	0.9	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_III, HSTL_III_DCI	1.4	1.5	1.6	–	0.9	–	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_I_18, HSTL_I_DCI_18	1.7	1.8	1.9	0.8	0.9	1.1	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_II_18, HSTL_II_DCI_18	1.7	1.8	1.9	–	0.9	–	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_III_18, HSTL_III_DCI_18	1.7	1.8	1.9	–	1.1	–	V_{REF} – 0.1	V_{REF} + 0.1
LVCMOS12	1.14	1.2	1.3	–	–	–	$0.37V_{CCO}$	$0.58V_{CCO}$
LVCMOS15, LVDCI_15, LVDCI_DV2_15	1.4	1.5	1.6	–	–	–	$0.30V_{CCO}$	$0.70V_{CCO}$
LVCMOS18, LVDCI_18, LVDCI_DV2_18	1.7	1.8	1.9	–	–	–	$0.30V_{CCO}$	$0.70V_{CCO}$
LVCMOS25[4,5], LVDCI_25, LVDCI_DV2_25[4]	2.3	2.5	2.7	–	–	–	0.7	1.7
LVCMOS33, LVDCI_33, LVDCI_DV2_33[4]	3.0	3.3	3.465	–	–	–	0.8	2.0
LVTTL	3.0	3.3	3.465	–	–	–	0.8	2.0
PCI33_3[7]	3.0	3.3	3.465	–	–	–	$0.30V_{CCO}$	$0.50V_{CCO}$
SSTL18_I, SSTL18_I_DCI	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} – 0.125	V_{REF} + 0.125
SSTL18_II	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} – 0.125	V_{REF} + 0.125
SSTL2_I, SSTL2_I_DCI	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} – 0.15	V_{REF} + 0.15
SSTL2_II, SSTL2_II_DCI	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} – 0.15	V_{REF} + 0.15

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} – the supply voltage for output drivers as well as LVCMOS, LVTTL, and PCI inputs
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
2. For device operation, the maximum signal voltage (V_{IH} max) may be as high as V_{IN} max. See Table 28.
3. Because the GTL and GTLP standards employ open-drain output buffers, V_{CCO} lines do not supply current to the I/O circuit, rather this current is provided using an external pull-up resistor connected from the I/O pin to a termination voltage (V_{TT}). Nevertheless, the voltage applied to the associated V_{CCO} lines must always be at or above V_{TT} and I/O pad voltages.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS25 or LVCMOS33 standards.
5. All dedicated pins (M0-M2, CCLK, PROG_B, DONE, HSWAP_EN, TCK, TDI, TDO, and TMS) use the LVCMOS standard and draw power from the V_{CCAUX} rail (2.5V). The dual-purpose configuration pins (DIN/D0, D1-D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B) use the LVCMOS standard before the user mode. For these pins, apply 2.5V to the V_{CCO} Bank 4 and V_{CCO} Bank 5 rails at power-on and throughout configuration. For information concerning the use of 3.3V signals, see 3.3V-Tolerant Configuration Interface, page 47.
6. The Global Clock Inputs (GCLK0-GCLK7) are dual-purpose pins to which any signal standard can be assigned.
7. For more information, see XAPP457.

Table 42: **Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Hold Times						
T_{IOICKP}	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(3), IOBDELAY = NONE	XC3S50	-0.55	-0.55	ns
			XC3S200	-0.29	-0.29	ns
			XC3S400	-0.29	-0.29	ns
			XC3S1000	-0.55	-0.55	ns
			XC3S1500	-0.55	-0.55	ns
			XC3S2000	-0.55	-0.55	ns
			XC3S4000	-0.61	-0.61	ns
			XC3S5000	-0.68	-0.68	ns
$T_{IOICKPD}$	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(3), IOBDELAY = IFD	XC3S50	-2.74	-2.74	ns
			XC3S200	-3.00	-3.00	ns
			XC3S400	-2.90	-2.90	ns
			XC3S1000	-3.24	-3.24	ns
			XC3S1500	-3.55	-3.55	ns
			XC3S2000	-4.57	-4.57	ns
			XC3S4000	-4.96	-4.96	ns
			XC3S5000	-5.09	-5.09	ns
Set/Reset Pulse Width						
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB		All	0.66	0.76	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 44.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 44. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
HSLVDCI_25			0.27	0.31	ns
HSLVDCI_33			0.28	0.32	ns
HSTL_I			0.60	0.69	ns
HSTL_I_DCI			0.59	0.68	ns
HSTL_III			0.19	0.22	ns
HSTL_III_DCI			0.20	0.23	ns
HSTL_I_18			0.18	0.21	ns
HSTL_I_DCI_18			0.17	0.19	ns
HSTL_II_18			–0.02	–0.01	ns
HSTL_II_DCI_18			0.75	0.86	ns
HSTL_III_18			0.28	0.32	ns
HSTL_III_DCI_18			0.28	0.32	ns
LVCMOS12	Slow	2 mA	7.60	8.73	ns
		4 mA	7.42	8.53	ns
		6 mA	6.67	7.67	ns
	Fast	2 mA	3.16	3.63	ns
		4 mA	2.70	3.10	ns
		6 mA	2.41	2.77	ns
LVCMOS15	Slow	2 mA	4.55	5.23	ns
		4 mA	3.76	4.32	ns
		6 mA	3.57	4.11	ns
		8 mA	3.55	4.09	ns
		12 mA	3.00	3.45	ns
	Fast	2 mA	3.11	3.57	ns
		4 mA	1.71	1.96	ns
		6 mA	1.44	1.66	ns
		8 mA	1.26	1.44	ns
		12 mA	1.11	1.27	ns
LVDCI_15			1.51	1.74	ns
LVDCI_DV2_15			1.32	1.52	ns

Table 61: **Switching Characteristics for the DFS**

Symbol	Description	Frequency Mode	Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_FX_LF	Frequency for the CLKFX and CLKFX180 outputs	Low	All	18	210	18	210	MHz
CLKOUT_FREQ_FX_HF		High	All	210	326(2)	210	307(2)	MHz
Output Clock Jitter								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs	All	All	Note 3	Note 3	Note 3	Note 3	ps
Duty Cycle(4)								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs	All	XC3S50	–	±100	–	±100	ps
			XC3S200	–	±100	–	±100	ps
			XC3S400	–	±250	–	±250	ps
			XC3S1000	–	±400	–	±400	ps
			XC3S1500	–	±400	–	±400	ps
			XC3S2000	–	±400	–	±400	ps
			XC3S4000	–	±400	–	±400	ps
			XC3S5000	–	±400	–	±400	ps
Phase Alignment								
CLKOUT_PHASE	Phase offset between the DFS output and the CLK0 output	All	All	–	±300	–	±300	ps
Lock Time								
LOCK_DLL_FX	When using the DFS in conjunction with the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.	All	All	–	10.0	–	10.0	ms
LOCK_FX	When using the DFS without the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. By asserting the LOCKED signal, the DFS indicates valid CLKFX and CLKFX180 signals.	All	All	–	10.0	–	10.0	ms

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32 and Table 60.
2. Mask revisions prior to the E mask revision have a CLKOUT_FREQ_FX_HF max of 280 MHz. See Mask and Fab Revisions, page 58.
3. Use the DCM Clocking Wizard in the ISE software for a Spartan-3 device specific number. Jitter number assumes 150 ps of input clock jitter.
4. The CLKFX and CLKFX180 outputs always approximate 50% duty cycles.
5. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) is in use.

Revision History

Date	Version	Description
04/11/03	1.0	Initial Xilinx release.
07/11/03	1.1	Extended Absolute Maximum Rating for junction temperature in Table 28. Added numbers for typical quiescent supply current (Table 34) and DLL timing.
02/06/04	1.2	Revised V_{IN} maximum rating (Table 28). Added power-on requirements (Table 30), leakage current number (Table 33), and differential output voltage levels (Table 38) for Rev. 0. Published new quiescent current numbers (Table 34). Updated pull-up and pull-down resistor strengths (Table 33). Added LVDCI_DV2 and LVPECL standards (Table 37 and Table 38). Changed CCLK setup time (Table 66 and Table 67).
03/04/04	1.3	Added timing numbers from v1.29 speed files as well as DCM timing (Table 58 through Table 63).
08/24/04	1.4	Added reference to errata documents on page 49. Clarified Absolute Maximum Ratings and added ESD information (Table 28). Explained V_{CCO} ramp time measurement (Table 30). Clarified I_L specification (Table 33). Updated quiescent current numbers and added information on power-on and surplus current (Table 34). Adjusted V_{REF} range for HSTL_III and HSTL_I_18 and changed V_{IH} min for LVCMOS12 (Table 35). Added note limiting V_{TT} range for SSTL2_II signal standards (Table 36). Calculated V_{OH} and V_{OL} levels for differential standards (Table 38). Updated Switching Characteristics with speed file v1.32 (Table 40 through Table 48 and Table 51 through Table 56). Corrected IOB test conditions (Table 41). Updated DCM timing with latest characterization data (Table 58 through Table 62). Improved DCM CLKIN pulse width specification (Table 58). Recommended use of Virtex-II FPGA Jitter calculator (Table 61). Improved DCM PSCLK pulse width specification (Table 62). Changed Phase Shifter lock time parameter (Table 63). Because the BitGen option Centered_x#_y# is not necessary for Variable Phase Shift mode, removed BitGen command table and referring text. Adjusted maximum CCLK frequency for the slave serial and parallel configuration modes (Table 66). Inverted CCLK waveform (Figure 37). Adjusted JTAG setup times (Table 68).
12/17/04	1.5	Updated timing parameters to match v1.35 speed file. Improved V_{CCO} ramp time specification (Table 30). Added a note limiting the rate of change of V_{CCAUX} (Table 32). Added typical quiescent current values for the XC3S2000, XC3S4000, and XC3S5000 (Table 34). Increased I_{OH} and I_{OL} for SSTL2-I and SSTL2-II standards (Table 36). Added SSO guidelines for the VQ, TQ, and PQ packages as well as edited SSO guidelines for the FT and FG packages (Table 50). Added maximum CCLK frequencies for configuration using compressed bitstreams (Table 66 and Table 67). Added specifications for the HSLVDCI standards (Table 35, Table 36, Table 44, Table 47, Table 48, and Table 50).
08/19/05	1.6	Updated timing parameters to match v1.37 speed file. All Spartan-3 FPGA part types, except XC3S5000, promoted to Production status. Removed V_{CCO} ramp rate restriction from all mask revision 'E' and later devices (Table 30). Added equivalent resistance values for internal pull-up and pull-down resistors (Table 33). Added worst-case quiescent current values for XC3S2000, XC3S4000, XC3S5000 (Table 34). Added industrial temperature range specification and improved typical quiescent current values (Table 34). Improved the DLL minimum clock input frequency specification from 24 MHz down to 18 MHz (Table 58). Improved the DFS minimum and maximum clock output frequency specifications (Table 60, Table 61). Added new miscellaneous DCM specifications (Table 64), primarily affecting Industrial temperature range applications. Updated Simultaneously Switching Output Guidelines and Table 50 for QFP packages. Added information on SSTL18_II I/O standard and timing to support DDR2 SDRAM interfaces. Added differential (or complementary single-ended) DIFF_HSTL_II_18 and DIFF_SSTL2_II I/O standards, including DCI terminated versions. Added electro-static discharge (ESD) data for the XC3S2000 and larger FPGAs (Table 28). Added link to Spartan-3 FPGA errata notices and how to receive automatic notifications of data sheet or errata changes.
04/03/06	2.0	Upgraded Module 3, removing Preliminary status. Moved XC3S5000 to Production status in Table 39. Finalized I/O timing on XC3S5000 for v1.38 speed files. Added minimum timing values for various logic and I/O paths. Corrected labels for R_{PU} and R_{PD} and updated R_{PD} conditions for in Table 33. Added final mask revision 'E' specifications for LVDS_25, RSDS_25, LVDSEXT_25 differential outputs to Table 38. Added BLVDS termination requirements to Figure 34. Improved recommended Simultaneous Switching Outputs (SSOs) limits in Table 50 for quad-flat packaged based on silicon testing using devices soldered on a printed circuit board. Updated Note 2 in Table 63. Updated Note 6 in Table 30. Added INIT_B minimum pulse width specification, T_{INIT}, to Table 65.
04/26/06	2.1	Updated document links.

Table 79: **Pin Behavior After Power-Up, During Configuration *(Cont'd)***

Pin Name	Configuration Mode Settings <M2:M1:M0>					Bitstream Configuration Option
	Serial Modes		SelectMap Parallel Modes		JTAG Mode <1:0:1>	
	Master <0:0:0>	Slave <1:1:1>	Master <0:1:1>	Slave <1:1:0>		
IO_Lxxy_#/ D5			D5 (I/O)	D5 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D6			D6 (I/O)	D6 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D7			D7 (I/O)	D7 (I/O)		Persist UnusedPin
IO_Lxxy_#/ CS_B			CS_B (I)	CS_B (I)		Persist UnusedPin
IO_Lxxy_#/ RDWR_B			RDWR_B (I)	RDWR_B (I)		Persist UnusedPin
IO_Lxxy_#/ BUSY/DOUT	DOUT (O)	DOUT (O)	BUSY (O)	BUSY (O)		Persist UnusedPin
DUAL: Dual-purpose configuration pins (INIT_B has a pull-up resistor to VCCO_4 or VCCO_BOTTOM always active during configuration, regardless of HSWAP_EN pin)						
IO_Lxxy_#/ INIT_B	INIT_B (I/OD)	INIT_B (I/OD)	INIT_B (I/OD)	INIT_B (I/OD)		UnusedPin
DCI: Digitally Controlled Impedance reference resistor input pins						
IO_Lxxy_#/ VRN_#						UnusedPin
IO/VRN_#						UnusedPin
IO_Lxxy_#/ VRP_#						UnusedPin
IO/VRP_#						UnusedPin
GCLK: Global clock buffer inputs						
IO_Lxxy_#/ GCLK0 through GCLK7						UnusedPin
VREF: I/O bank input reference voltage pins						
IO_Lxxy_#/ VREF_#						UnusedPin
IO/VREF_#						UnusedPin
CONFIG: Dedicated configuration pins (pull-up resistor to VCCAUX always active during configuration, regardless of HSWAP_EN pin)						
CCLK	CCLK (I/O)	CCLK (I)	CCLK (I/O)	CCLK (I)		CclkPin ConfigRate
PROG_B	PROG_B (I) (pull-up)	PROG_B (I) (pull-up)	PROG_B (I) (pull-up)	PROG_B (I) (pull-up)	PROG_B (I), Via JPROG_B instruction	ProgPin
DONE	DONE (I/OD)	DONE (I/OD)	DONE (I/OD)	DONE (I/OD)	DONE (I/OD)	DriveDone DonePin DonePipe
M2	M2=0 (I)	M2=1 (I)	M2=0 (I)	M2=1 (I)	M2=1 (I)	M2Pin
M1	M1=0 (I)	M1=1 (I)	M1=1 (I)	M1=1 (I)	M1=0 (I)	M1Pin
M0	M0=0 (I)	M0=1 (I)	M0=1 (I)	M0=0 (I)	M0=1 (I)	M0Pin
HSWAP_EN	HSWAP_EN (I)	HSWAP_EN (I)	HSWAP_EN (I)	HSWAP_EN (I)	HSWAP_EN (I)	HswapenPin

Right Half of Package (Top View)

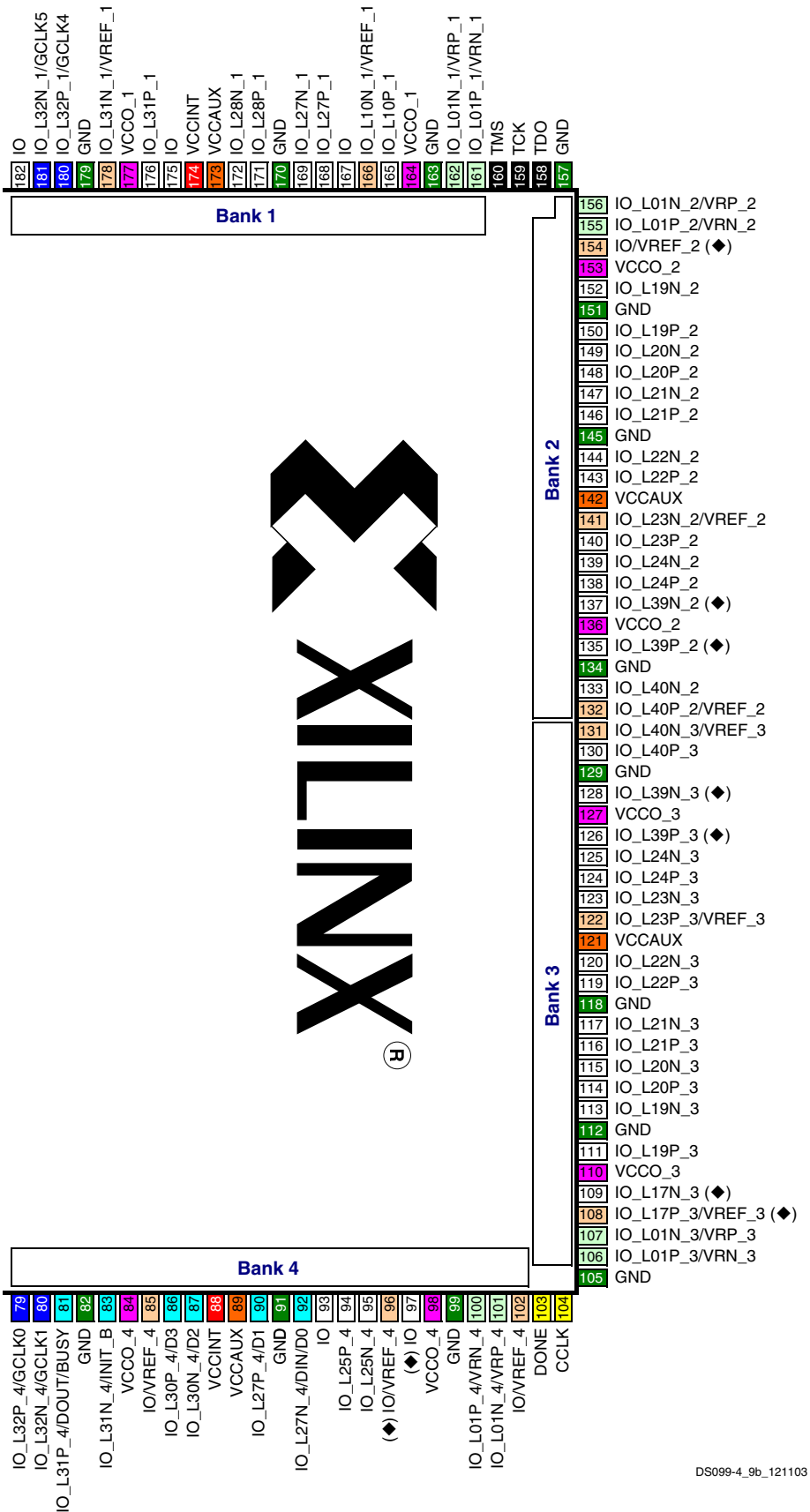

Figure 48: PQ208 Package Footprint (Top View) Continued

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
0	VCCO_0	G9	VCCO
1	IO	A11	I/O
1	IO	B13	I/O
1	IO	D10	I/O
1	IO/VREF_1	A12	VREF
1	IO_L01N_1/VRP_1	A16	DCI
1	IO_L01P_1/VRN_1	A17	DCI
1	IO_L10N_1/VREF_1	A15	VREF
1	IO_L10P_1	B15	I/O
1	IO_L15N_1	C14	I/O
1	IO_L15P_1	C15	I/O
1	IO_L16N_1	A14	I/O
1	IO_L16P_1	B14	I/O
1	IO_L24N_1	D14	I/O
1	IO_L24P_1	D13	I/O
1	IO_L27N_1	E13	I/O
1	IO_L27P_1	E12	I/O
1	IO_L28N_1	C12	I/O
1	IO_L28P_1	D12	I/O
1	IO_L29N_1	F11	I/O
1	IO_L29P_1	E11	I/O
1	IO_L30N_1	C11	I/O
1	IO_L30P_1	D11	I/O
1	IO_L31N_1/VREF_1	A10	VREF
1	IO_L31P_1	B10	I/O
1	IO_L32N_1/GCLK5	E10	GCLK
1	IO_L32P_1/GCLK4	F10	GCLK
1	VCCO_1	B11	VCCO
1	VCCO_1	C13	VCCO
1	VCCO_1	G10	VCCO
1	VCCO_1	G11	VCCO
2	IO	J13	I/O
2	IO_L01N_2/VRP_2	C16	DCI
2	IO_L01P_2/VRN_2	C17	DCI
2	IO_L16N_2	B18	I/O
2	IO_L16P_2	C18	I/O
2	IO_L17N_2	D17	I/O
2	IO_L17P_2/VREF_2	D18	VREF
2	IO_L19N_2	D16	I/O
2	IO_L19P_2	E16	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
0	IO_L09N_0	IO_L09N_0	IO_L09N_0	IO_L09N_0	IO_L09N_0	E7	I/O
0	IO_L09P_0	IO_L09P_0	IO_L09P_0	IO_L09P_0	IO_L09P_0	D7	I/O
0	IO_L10N_0	IO_L10N_0	IO_L10N_0	IO_L10N_0	IO_L10N_0	B7	I/O
0	IO_L10P_0	IO_L10P_0	IO_L10P_0	IO_L10P_0	IO_L10P_0	A7	I/O
0	N.C. (◆)	IO_L11N_0	IO_L11N_0	IO_L11N_0	IO_L11N_0	G8	I/O
0	N.C. (◆)	IO_L11P_0	IO_L11P_0	IO_L11P_0	IO_L11P_0	F8	I/O
0	N.C. (◆)	IO_L12N_0	IO_L12N_0	IO_L12N_0	IO(3)	E8	I/O
0	N.C. (◆)	IO_L12P_0	IO_L12P_0	IO_L12P_0	IO(3)	D8	I/O
0	IO_L15N_0	IO_L15N_0	IO_L15N_0	IO_L15N_0	IO_L13P_0(3)	B8	I/O
0	IO_L15P_0	IO_L15P_0	IO_L15P_0	IO_L15P_0	IO(3)	A8	I/O
0	IO_L16N_0	IO_L16N_0	IO_L16N_0	IO_L16N_0	IO_L16N_0	G9	I/O
0	IO_L16P_0	IO_L16P_0	IO_L16P_0	IO_L16P_0	IO_L16P_0	F9	I/O
0	N.C. (◆)	IO_L17N_0	IO_L17N_0	IO_L17N_0	IO_L17N_0	E9	I/O
0	N.C. (◆)	IO_L17P_0	IO_L17P_0	IO_L17P_0	IO_L17P_0	D9	I/O
0	N.C. (◆)	IO_L18N_0	IO_L18N_0	IO_L18N_0	IO_L18N_0	C9	I/O
0	N.C. (◆)	IO_L18P_0	IO_L18P_0	IO_L18P_0	IO_L18P_0	B9	I/O
0	IO_L19N_0	IO_L19N_0	IO_L19N_0	IO_L19N_0	IO_L19N_0	F10	I/O
0	IO_L19P_0	IO_L19P_0	IO_L19P_0	IO_L19P_0	IO_L19P_0	E10	I/O
0	IO_L22N_0	IO_L22N_0	IO_L22N_0	IO_L22N_0	IO_L22N_0	D10	I/O
0	IO_L22P_0	IO_L22P_0	IO_L22P_0	IO_L22P_0	IO_L22P_0	C10	I/O
0	N.C. (◆)	IO_L23N_0	IO_L23N_0	IO_L23N_0	IO_L23N_0	B10	I/O
0	N.C. (◆)	IO_L23P_0	IO_L23P_0	IO_L23P_0	IO_L23P_0	A10	I/O
0	IO_L24N_0	IO_L24N_0	IO_L24N_0	IO_L24N_0	IO_L24N_0	G11	I/O
0	IO_L24P_0	IO_L24P_0	IO_L24P_0	IO_L24P_0	IO_L24P_0	F11	I/O
0	IO_L25N_0	IO_L25N_0	IO_L25N_0	IO_L25N_0	IO_L25N_0	E11	I/O
0	IO_L25P_0	IO_L25P_0	IO_L25P_0	IO_L25P_0	IO_L25P_0	D11	I/O
0	N.C. (◆)	IO_L26N_0	IO_L26N_0	IO_L26N_0	IO_L26N_0	B11	I/O
0	N.C. (◆)	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	A11	VREF
0	IO_L27N_0	IO_L27N_0	IO_L27N_0	IO_L27N_0	IO_L27N_0	G12	I/O
0	IO_L27P_0	IO_L27P_0	IO_L27P_0	IO_L27P_0	IO_L27P_0	H13	I/O
0	IO_L28N_0	IO_L28N_0	IO_L28N_0	IO_L28N_0	IO_L28N_0	F12	I/O
0	IO_L28P_0	IO_L28P_0	IO_L28P_0	IO_L28P_0	IO_L28P_0	E12	I/O
0	IO_L29N_0	IO_L29N_0	IO_L29N_0	IO_L29N_0	IO_L29N_0	B12	I/O
0	IO_L29P_0	IO_L29P_0	IO_L29P_0	IO_L29P_0	IO_L29P_0	A12	I/O
0	IO_L30N_0	IO_L30N_0	IO_L30N_0	IO_L30N_0	IO_L30N_0	G13	I/O
0	IO_L30P_0	IO_L30P_0	IO_L30P_0	IO_L30P_0	IO_L30P_0	F13	I/O
0	IO_L31N_0	IO_L31N_0	IO_L31N_0	IO_L31N_0	IO_L31N_0	D13	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C13	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B13	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A13	GCLK
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	C7	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	C11	VCCO

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	C1	DCI
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	C2	DCI
7	IO_L02N_7	IO_L02N_7	D3	I/O
7	IO_L02P_7	IO_L02P_7	D4	I/O
7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	D1	VREF
7	IO_L03P_7	IO_L03P_7	D2	I/O
7	IO_L04N_7	IO_L04N_7	E1	I/O
7	IO_L04P_7	IO_L04P_7	E2	I/O
7	IO_L05N_7	IO_L05N_7	F5	I/O
7	IO_L05P_7	IO_L05P_7	E4	I/O
7	IO_L06N_7	IO_L06N_7	F2	I/O
7	IO_L06P_7	IO_L06P_7	F3	I/O
7	IO_L07N_7	IO_L07N_7	G3	I/O
7	IO_L07P_7	IO_L07P_7	G4	I/O
7	IO_L08N_7	IO_L08N_7	G1	I/O
7	IO_L08P_7	IO_L08P_7	G2	I/O
7	IO_L09N_7	IO_L09N_7	H7	I/O
7	IO_L09P_7	IO_L09P_7	G6	I/O
7	IO_L10N_7	IO_L10N_7	H5	I/O
7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	H6	VREF
7	IO_L11N_7	IO_L11N_7	H3	I/O
7	IO_L11P_7	IO_L11P_7	H4	I/O
7	IO_L13N_7	IO_L13N_7	H1	I/O
7	IO_L13P_7	IO_L13P_7	H2	I/O
7	IO_L14N_7	IO_L14N_7	J4	I/O
7	IO_L14P_7	IO_L14P_7	J5	I/O
7	IO_L15N_7	IO_L15N_7	J1	I/O
7	IO_L15P_7	IO_L15P_7	J2	I/O
7	IO_L16N_7	IO_L16N_7	K9	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	J8	VREF
7	IO_L17N_7	IO_L17N_7	K6	I/O
7	IO_L17P_7	IO_L17P_7	K7	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	K2	VREF
7	IO_L19P_7	IO_L19P_7	K3	I/O
7	IO_L20N_7	IO_L20N_7	L10	I/O
7	IO_L20P_7	IO_L20P_7	K10	I/O
7	IO_L21N_7	IO_L21N_7	L7	I/O
7	IO_L21P_7	IO_L21P_7	L8	I/O
7	IO_L22N_7	IO_L22N_7	L5	I/O
7	IO_L22P_7	IO_L22P_7	L6	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
7	VCCO_7	VCCO_7	N3	VCCO
7	VCCO_7	VCCO_7	G5	VCCO
7	VCCO_7	VCCO_7	J7	VCCO
7	VCCO_7	VCCO_7	N7	VCCO
7	VCCO_7	VCCO_7	L9	VCCO
7	VCCO_7	VCCO_7	M11	VCCO
7	VCCO_7	VCCO_7	N11	VCCO
7	VCCO_7	VCCO_7	P11	VCCO
N/A	GND	GND	A1	GND
N/A	GND	GND	B1	GND
N/A	GND	GND	F1	GND
N/A	GND	GND	K1	GND
N/A	GND	GND	P1	GND
N/A	GND	GND	U1	GND
N/A	GND	GND	AA1	GND
N/A	GND	GND	AE1	GND
N/A	GND	GND	AJ1	GND
N/A	GND	GND	AK1	GND
N/A	GND	GND	A2	GND
N/A	GND	GND	B2	GND
N/A	GND	GND	AJ2	GND
N/A	GND	GND	E5	GND
N/A	GND	GND	K5	GND
N/A	GND	GND	P5	GND
N/A	GND	GND	U5	GND
N/A	GND	GND	AA5	GND
N/A	GND	GND	AF5	GND
N/A	GND	GND	A6	GND
N/A	GND	GND	AK6	GND
N/A	GND	GND	K8	GND
N/A	GND	GND	P8	GND
N/A	GND	GND	U8	GND
N/A	GND	GND	AA8	GND
N/A	GND	GND	A10	GND
N/A	GND	GND	E10	GND
N/A	GND	GND	H10	GND
N/A	GND	GND	AC10	GND
N/A	GND	GND	AF10	GND
N/A	GND	GND	AK10	GND
N/A	GND	GND	R12	GND

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	VCCAUX	VCCAUX	Y5	VCCAUX
N/A	VCCINT	VCCINT	AA13	VCCINT
N/A	VCCINT	VCCINT	AA22	VCCINT
N/A	VCCINT	VCCINT	AB13	VCCINT
N/A	VCCINT	VCCINT	AB14	VCCINT
N/A	VCCINT	VCCINT	AB15	VCCINT
N/A	VCCINT	VCCINT	AB16	VCCINT
N/A	VCCINT	VCCINT	AB19	VCCINT
N/A	VCCINT	VCCINT	AB20	VCCINT
N/A	VCCINT	VCCINT	AB21	VCCINT
N/A	VCCINT	VCCINT	AB22	VCCINT
N/A	VCCINT	VCCINT	AC12	VCCINT
N/A	VCCINT	VCCINT	AC17	VCCINT
N/A	VCCINT	VCCINT	AC18	VCCINT
N/A	VCCINT	VCCINT	AC23	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	M23	VCCINT
N/A	VCCINT	VCCINT	N13	VCCINT
N/A	VCCINT	VCCINT	N14	VCCINT
N/A	VCCINT	VCCINT	N15	VCCINT
N/A	VCCINT	VCCINT	N16	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	N20	VCCINT
N/A	VCCINT	VCCINT	N21	VCCINT
N/A	VCCINT	VCCINT	N22	VCCINT
N/A	VCCINT	VCCINT	P13	VCCINT
N/A	VCCINT	VCCINT	P22	VCCINT
N/A	VCCINT	VCCINT	R13	VCCINT
N/A	VCCINT	VCCINT	R22	VCCINT
N/A	VCCINT	VCCINT	T13	VCCINT
N/A	VCCINT	VCCINT	T22	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT
N/A	VCCINT	VCCINT	U23	VCCINT
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	V23	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	W22	VCCINT
N/A	VCCINT	VCCINT	Y13	VCCINT