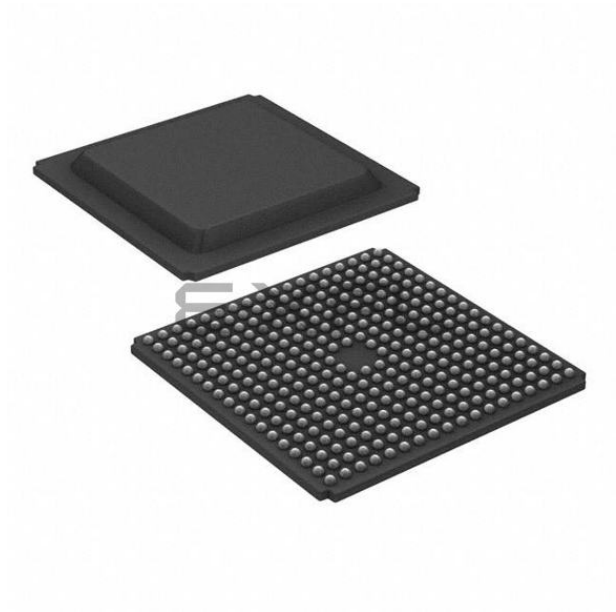

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 3328 |
| Number of Logic Elements/Cells | 29952 |
| Total RAM Bits | 589824 |
| Number of I/O | 221 |
| Number of Gates | 1500000 |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 320-BGA |
| Supplier Device Package | 320-FBGA (19x19) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc3s1500-5fgg320c |

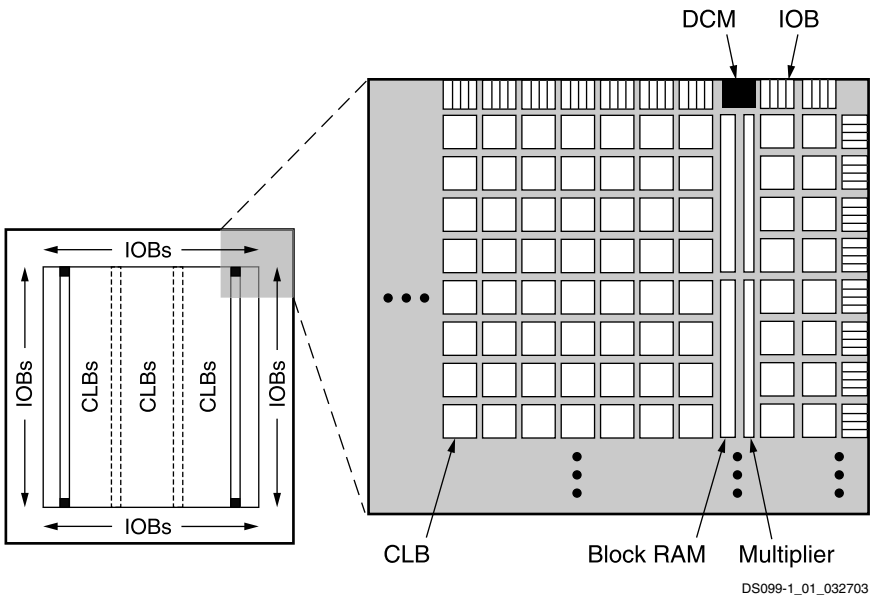
## Architectural Overview

The Spartan-3 family architecture consists of five fundamental programmable functional elements:

- Configurable Logic Blocks (CLBs) contain RAM-based Look-Up Tables (LUTs) to implement logic and storage elements that can be used as flip-flops or latches. CLBs can be programmed to perform a wide variety of logical functions as well as to store data.
- Input/Output Blocks (IOBs) control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Twenty-six different signal standards, including eight high-performance differential standards, are available as shown in Table 2. Double Data-Rate (DDR) registers are included. The Digitally Controlled Impedance (DCI) feature provides automatic on-chip terminations, simplifying board designs.
- Block RAM provides data storage in the form of 18-Kbit dual-port blocks.
- Multiplier blocks accept two 18-bit binary numbers as inputs and calculate the product.
- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. The XC3S50 has a single column of block RAM embedded in the array. Those devices ranging from the XC3S200 to the XC3S2000 have two columns of block RAM. The XC3S4000 and XC3S5000 devices have four RAM columns. Each column is made up of several 18-Kbit RAM blocks; each block is associated with a dedicated multiplier. The DCMs are positioned at the ends of the outer block RAM columns.

The Spartan-3 family features a rich network of traces and switches that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.




**Notes:**

1. The two additional block RAM columns of the XC3S4000 and XC3S5000 devices are shown with dashed lines. The XC3S50 has only the block RAM column on the far left.

*Figure 1:* **Spartan-3 Family Architecture**

## Configuration

Spartan-3 FPGAs are programmed by loading configuration data into robust reprogrammable static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. Before powering on the FPGA, configuration data is stored externally in a PROM or some other nonvolatile medium either on or off the board. After applying

*Table 8:* **Single-Ended I/O Standards**

| Signal Standard (IOSTANDARD) | $V_{CCO}$ (Volts) | | $V_{REF}$ for Inputs (Volts)(1) | Board Termination Voltage ($V_{TT}$) in Volts |
|---|---|---|---|---|
| | For Outputs | For Inputs | | |
| GTL | Note 2 | Note 2 | 0.8 | 1.2 |
| GTLP | Note 2 | Note 2 | 1 | 1.5 |
| HSTL_I | 1.5 | – | 0.75 | 0.75 |
| HSTL_III | 1.5 | – | 0.9 | 1.5 |
| HSTL_I_18 | 1.8 | – | 0.9 | 0.9 |
| HSTL_II_18 | 1.8 | – | 0.9 | 0.9 |
| HSTL_III_18 | 1.8 | – | 1.1 | 1.8 |
| LVCMOS12 | 1.2 | 1.2 | – | – |
| LVCMOS15 | 1.5 | 1.5 | – | – |
| LVCMOS18 | 1.8 | 1.8 | – | – |
| LVCMOS25 | 2.5 | 2.5 | – | – |
| LVCMOS33 | 3.3 | 3.3 | – | – |
| LVTTL | 3.3 | 3.3 | – | – |
| PCI33_3 | 3.0 | 3.0 | – | – |
| SSTL18_I | 1.8 | – | 0.9 | 0.9 |
| SSTL18_II | 1.8 | – | 0.9 | 0.9 |
| SSTL2_I | 2.5 | – | 1.25 | 1.25 |
| SSTL2_II | 2.5 | – | 1.25 | 1.25 |

**Notes:**

1. Banks 4 and 5 of any Spartan-3 device in a VQ100 package do not support signal standards using $V_{REF}$.
2. The $V_{CCO}$ level used for the GTL and GTLP standards must be no lower than the termination voltage ($V_{TT}$), nor can it be lower than the voltage at the I/O pad.
3. See Table 10 for a listing of the single-ended DCI standards.

Differential standards employ a pair of signals, one the opposite polarity of the other. The noise canceling (e.g., Common-Mode Rejection) properties of these standards permit exceptionally high data transfer rates. This section introduces the differential signaling capabilities of Spartan-3 devices.

Each device-package combination designates specific I/O pairs that are specially optimized to support differential standards. A unique “L-number”, part of the pin name, identifies the line-pairs associated with each bank (see Figure 40, page 112). For each pair, the letters ‘P’ and ‘N’ designate the true and inverted lines, respectively. For example, the pin names IO_L43P_7 and IO_L43N_7 indicate the true and inverted lines comprising the line pair L43 on Bank 7. The $V_{CCO}$ lines provide current to the outputs. The $V_{CCAUX}$ lines supply power to the differential inputs, making them independent of the $V_{CCO}$ voltage for an I/O bank. The $V_{REF}$ lines are not used. Select the $V_{CCO}$ level to suit the desired differential standard according to Table 9.

upper path), enter the slice and connect directly to the LUT. Once inside the slice, the lower 4-bit path passes through a function generator ‘F’ (or ‘G’) that performs logic operations. The function generator’s Data output, ‘D’, offers five possible paths:

- Exit the slice via line ‘X’ (or ‘Y’) and return to interconnect.
- Inside the slice, ‘X’ (or ‘Y’) serves as an input to the DXMUX (DYMUX) which feeds the data input, ‘D’, of the FFX (FFY) storage element. The ‘Q’ output of the storage element drives the line XQ (or YQ) which exits the slice.
- Control the CYMUXF (or CYMUXG) multiplexer on the carry chain.
- With the carry chain, serve as an input to the XORF (or XORG) exclusive-OR gate that performs arithmetic operations, producing a result on ‘X’ (or ‘Y’).
- Drive the multiplexer F5MUX to implement logic functions wider than four bits. The ‘D’ outputs of both the F-LUT and G-LUT serve as data inputs to this multiplexer.

In addition to the main logic paths described above, there are two bypass paths that enter the slice as BX and BY. Once inside the FPGA, BX in the bottom half of the slice (or BY in the top half) can take any of several possible branches:

- Bypass both the LUT and the storage element, then exit the slice as BXOUT (or BYOUT) and return to interconnect.
- Bypass the LUT, then pass through a storage element via the D input before exiting as XQ (or YQ).
- Control the wide function multiplexer F5MUX (or F6MUX).
- Via multiplexers, serve as an input to the carry chain.
- Drives the DI input of the LUT.
- BY can control the REV inputs of both the FFY and FFX storage elements.
- Finally, the DIG_MUX multiplexer can switch BY onto the DIG line, which exits the slice.

Other slice signals shown in Figure 12 are discussed in the sections that follow.

*Table 41:* **System-Synchronous Pin-to-Pin Setup and Hold Times for the IOB Input Path**

| Symbol | Description | Conditions | Device | Speed Grade | | Units |
|---|---|---|---|---|---|---|
| | | | | -5 | -4 | |
| | | | | Min | Min | |
| **Setup Times** | | | | | | |
| $T_{PSDCM}$ | When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed. | LVCMOS25(2), IOBDELAY = NONE, with DCM(4) | XC3S50 | 2.37 | 2.71 | ns |
| | | | XC3S200 | 2.13 | 2.35 | ns |
| | | | XC3S400 | 2.15 | 2.36 | ns |
| | | | XC3S1000 | 2.58 | 2.95 | ns |
| | | | XC3S1500 | 2.55 | 2.91 | ns |
| | | | XC3S2000 | 2.59 | 2.96 | ns |
| | | | XC3S4000 | 2.76 | 3.15 | ns |
| | | | XC3S5000 | 2.69 | 3.08 | ns |
| $T_{PSFD}$ | When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed. | LVCMOS25(2), IOBDELAY = IFD, without DCM | XC3S50 | 3.00 | 3.46 | ns |
| | | | XC3S200 | 2.63 | 3.02 | ns |
| | | | XC3S400 | 2.50 | 2.87 | ns |
| | | | XC3S1000 | 3.50 | 4.03 | ns |
| | | | XC3S1500 | 3.78 | 4.35 | ns |
| | | | XC3S2000 | 4.98 | 5.73 | ns |
| | | | XC3S4000 | 5.25 | 6.05 | ns |
| | | | XC3S5000 | 5.37 | 6.18 | ns |
| **Hold Times** | | | | | | |
| $T_{PHDCM}$ | When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed. | LVCMOS25(3), IOBDELAY = NONE, with DCM(4) | XC3S50 | –0.45 | –0.40 | ns |
| | | | XC3S200 | –0.12 | –0.05 | ns |
| | | | XC3S400 | –0.12 | –0.05 | ns |
| | | | XC3S1000 | –0.43 | –0.38 | ns |
| | | | XC3S1500 | –0.45 | –0.40 | ns |
| | | | XC3S2000 | –0.47 | –0.42 | ns |
| | | | XC3S4000 | –0.61 | –0.56 | ns |
| | | | XC3S5000 | –0.62 | –0.57 | ns |

*Table 46:* **Timing for the IOB Three-State Path**

| Symbol | Description | Conditions | Device | Speed Grade | | Units |
|---|---|---|---|---|---|---|
| | | | | -5 | -4 | |
| | | | | Max[3] | Max[3] | |
| **Synchronous Output Enable/Disable Times** | | | | | | |
| $T_{IOCKHZ}$ | Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state | LVCMOS25, 12 mA output drive, Fast slew rate | All | 0.74 | 0.85 | ns |
| $T_{IOCKON}$[2] | Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data | | All | 0.72 | 0.82 | ns |
| **Asynchronous Output Enable/Disable Times** | | | | | | |
| $T_{GTS}$ | Time from asserting the Global Three State (GTS) net to when the Output pin enters the high-impedance state | LVCMOS25, 12 mA output drive, Fast slew rate | XC3S200<br>XC3S400 | 7.71 | 8.87 | ns |
| | | | XC3S50<br>XC3S1000<br>XC3S1500<br>XC3S2000<br>XC3S4000<br>XC3S5000 | 8.38 | 9.63 | ns |
| **Set/Reset Times** | | | | | | |
| $T_{IOSRHZ}$ | Time from asserting TFF's SR input to when the Output pin enters a high-impedance state | LVCMOS25, 12 mA output drive, Fast slew rate | All | 1.55 | 1.78 | ns |
| $T_{IOSRON}$[2] | Time from asserting TFF's SR input at TFF to when the Output pin drives valid data | | XC3S200<br>XC3S400 | 2.24 | 2.57 | ns |
| | | | XC3S50<br>XC3S1000<br>XC3S1500<br>XC3S2000<br>XC3S4000<br>XC3S5000 | 2.91 | 3.34 | ns |

**Notes:**

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 47.
3. For minimums, use the values reported by the Xilinx timing analyzer.

*Table 47:* **Output Timing Adjustments for IOB**

| Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD) | Add the Adjustment Below | | Units |
|---|---|---|---|
| | Speed Grade | | |
| | -5 | -4 | |
| **Single-Ended Standards** | | | |
| GTL | 0 | 0.02 | ns |
| GTL_DCI | 0.13 | 0.15 | ns |
| GTLP | 0.03 | 0.04 | ns |
| GTLP_DCI | 0.23 | 0.27 | ns |
| HSLVDCI_15 | 1.51 | 1.74 | ns |
| HSLVDCI_18 | 0.81 | 0.94 | ns |

## Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 58 and Table 59) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 60 through Table 63) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 58 and Table 59.

Period jitter and cycle-cycle jitter are two (of many) different ways of characterizing clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the average clock period of all clock cycles in the collection of clock periods sampled (usually from 100,000 to more than a million samples for specification purposes). In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

### Delay-Locked Loop (DLL)

*Table 58:* **Recommended Operating Conditions for the DLL**

| Symbol | | Description | Frequency Mode/ $F_{CLKIN}$ Range | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | -5 | | -4 | | |
| | | | | Min | Max | Min | Max | |
| **Input Frequency Ranges** | | | | | | | | |
| $F_{CLKIN}$ | CLKIN_FREQ_DLL_LF | Frequency for the CLKIN input | Low | 18(2) | 167(3) | 18(2) | 167(3) | MHz |
| | CLKIN_FREQ_DLL_HF | | High | 48 | 280(3) | 48 | 280(3)(4) | MHz |
| **Input Pulse Requirements** | | | | | | | | |
| CLKIN_PULSE | | CLKIN pulse width as a percentage of the CLKIN period | $F_{CLKIN} \leq 100$ MHz | 40% | 60% | 40% | 60% | - |
| | | | $F_{CLKIN} > 100$ MHz | 45% | 55% | 45% | 55% | - |
| **Input Clock Jitter Tolerance and Delay Path Variation**(5) | | | | | | | | |
| CLKIN_CYC_JITT_DLL_LF | | Cycle-to-cycle jitter at the CLKIN input | Low | – | ±300 | – | ±300 | ps |
| CLKIN_CYC_JITT_DLL_HF | | | High | – | ±150 | – | ±150 | ps |
| CLKIN_PER_JITT_DLL_LF | | Period jitter at the CLKIN input | All | – | ±1 | – | ±1 | ns |
| CLKIN_PER_JITT_DLL_HF | | | | – | | – | | |
| CLKFB_DELAY_VAR_EXT | | Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input | All | – | ±1 | – | ±1 | ns |

**Notes:**

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower $F_{CLKIN}$ frequencies. See Table 60.
3. The CLKIN_DIVIDE_BY_2 attribute can be used to increase the effective input frequency range up to $F_{BUFG}$. When set to TRUE, CLKIN_DIVIDE_BY_2 divides the incoming clock frequency by two as it enters the DCM.
4. Industrial temperature range devices have additional requirements for continuous clocking, as specified in Table 64.
5. CLKIN input jitter beyond these limits may cause the DCM to lose lock. See UG331 for more details.

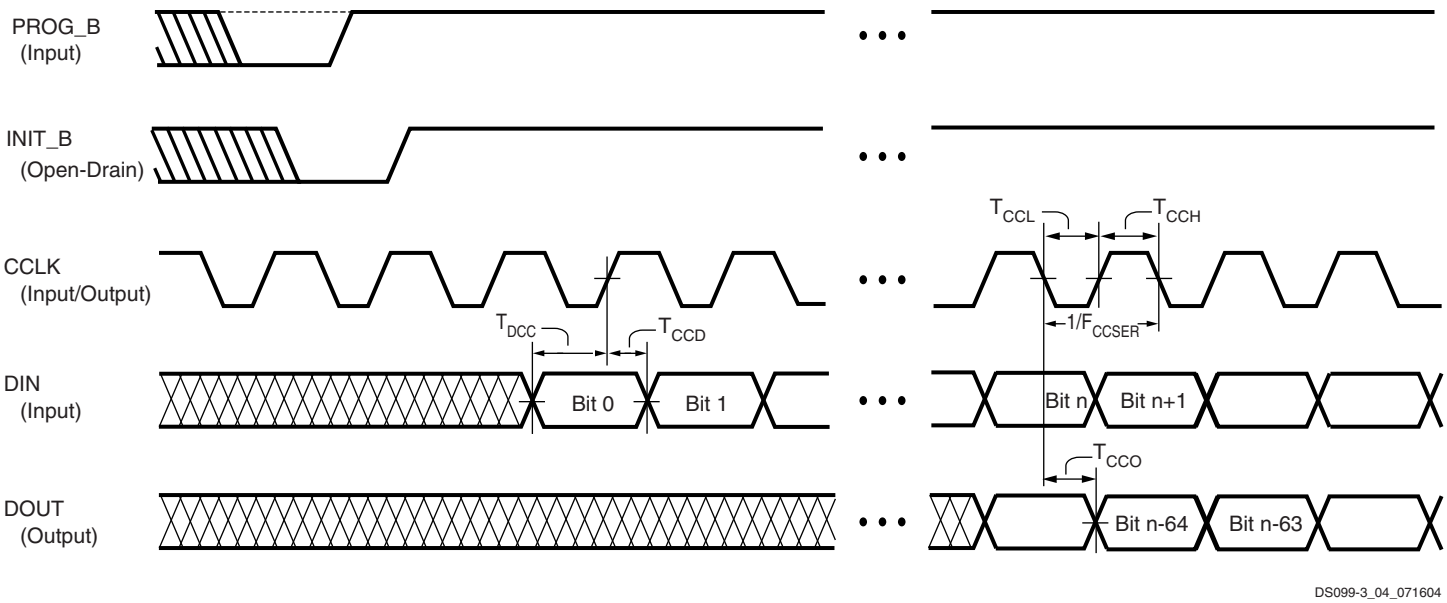



*Figure 37:* **Waveforms for Master and Slave Serial Configuration**

*Table 66:* **Timing for the Master and Slave Serial Configuration Modes**

| Symbol | Description | | Slave/ Master | All Speed Grades | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| **Clock-to-Output Times** | | | | | | |
| $T_{CCO}$ | The time from the falling transition on the CCLK pin to data appearing at the DOUT pin | | Both | 1.5 | 12.0 | ns |
| **Setup Times** | | | | | | |
| $T_{DCC}$ | The time from the setup of data at the DIN pin to the rising transition at the CCLK pin | | Both | 10.0 | – | ns |
| **Hold Times** | | | | | | |
| $T_{CCD}$ | The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin | | Both | 0 | – | ns |
| **Clock Timing** | | | | | | |
| $T_{CCH}$ | CCLK input pin High pulse width | | Slave | 5.0 | ∞ | ns |
| $T_{CCL}$ | CCLK input pin Low pulse width | | | 5.0 | ∞ | ns |
| $F_{CCSER}$ | Frequency of the clock signal at the CCLK input pin | No bitstream compression | | 0 | 66(2) | MHz |
| | | With bitstream compression | | 0 | 20 | MHz |
| | | During STARTUP phase | | 0 | 50 | MHz |
| $\Delta F_{CCSER}$ | Variation from the CCLK output frequency set using the ConfigRate BitGen option | | Master | –50% | +50% | – |

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

*Table 69:* **Types of Pins on Spartan-3 FPGAs *(Cont'd)***

| Pin Type/ Color Code | Description | Pin Name |
|---|---|---|
| VREF | Dual-purpose pin that is either a user-I/O pin or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected. | IO/VREF_#<br>IO_Lxxy_#/VREF_# |
| GND | Dedicated ground pin. The number of GND pins depends on the package used. All must be connected. | GND |
| VCCAUX | Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. All must be connected to +2.5V. | VCCAUX |
| VCCINT | Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V. | VCCINT |
| VCCO | Dedicated I/O bank, output buffer power supply pin. Along with other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. | VCCO_#<br>**CP132 and TQ144 Packages Only:**<br>VCCO_LEFT, VCCO_TOP,<br>VCCO_RIGHT, VCCO_BOTTOM |
| GCLK | Dual-purpose pin that is either a user-I/O pin or an input to a specific global buffer input. Every package has eight dedicated GCLK pins. | IO_Lxxy_#/GCLK0,<br>IO_Lxxy_#/GCLK1,<br>IO_Lxxy_#/GCLK2,<br>IO_Lxxy_#/GCLK3,<br>IO_Lxxy_#/GCLK4,<br>IO_Lxxy_#/GCLK5,<br>IO_Lxxy_#/GCLK6,<br>IO_Lxxy_#/GCLK7 |
| N.C. | This package pin is not connected in this specific device/package combination but may be connected in larger devices in the same package. | N.C. |

**Notes:**

1. # = I/O bank number, an integer between 0 and 7.

I/Os with Lxxy_# are part of a differential output pair. 'L' indicates differential output capability. The "xx" field is a two-digit integer, unique to each bank that identifies a differential pin-pair. The 'y' field is either 'P' for the true signal or 'N' for the inverted signal in the differential pair. The '#' field is the I/O bank number.

## Pin Definitions

Table 70 provides a brief description of each pin listed in the Spartan-3 FPGA pinout tables and package footprint diagrams. Pins are categorized by their pin type, as listed in Table 69. See Detailed, Functional Pin Descriptions for more information.

*Table 79:* **Pin Behavior After Power-Up, During Configuration *(Cont'd)***

| Pin Name | Configuration Mode Settings <M2:M1:M0> | | | | | Bitstream Configuration Option |
|---|---|---|---|---|---|---|
| | Serial Modes | | SelectMap Parallel Modes | | JTAG Mode <1:0:1> | |
| | Master <0:0:0> | Slave <1:1:1> | Master <0:1:1> | Slave <1:1:0> | | |
| **JTAG: JTAG interface pins (pull-up resistor to VCCAUX always active during configuration, regardless of HSWAP_EN pin)** | | | | | | |
| TDI | TDI (I) | TDI (I) | TDI (I) | TDI (I) | TDI (I) | TdiPin |
| TMS | TMS (I) | TMS (I) | TMS (I) | TMS (I) | TMS (I) | TmsPin |
| TCK | TCK (I) | TCK (I) | TCK (I) | TCK (I) | TCK (I) | TckPin |
| TDO | TDO (O) | TDO (O) | TDO (O) | TDO (O) | TDO (O) | TdoPin |

## Package Overview

Table 81 shows the 10 low-cost, space-saving production package styles for the Spartan-3 family. Each package style is available as a standard and an environmentally-friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "VQ100" package becomes "VQG100" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 83.

Not all Spartan-3 device densities are available in all packages. However, for a specific package there is a common footprint that supports the various devices available in that package. See the footprint diagrams that follow.

*Table 81:* **Spartan-3 Family Package Options**

| Package | Leads | Type | Maximum I/O | Pitch (mm) | Footprint (mm) | Height (mm) |
|---|---|---|---|---|---|---|
| VQ100 / VQG100 | 100 | Very-thin Quad Flat Pack | 63 | 0.5 | 16 x 16 | 1.20 |
| CP132 / CPG132(1) | 132 | Chip-Scale Package | 89 | 0.5 | 8 x 8 | 1.10 |
| TQ144 / TQG144 | 144 | Thin Quad Flat Pack | 97 | 0.5 | 22 x 22 | 1.60 |
| PQ208 / PQG208 | 208 | Quad Flat Pack | 141 | 0.5 | 30.6 x 30.6 | 4.10 |
| FT256 / FTG256 | 256 | Fine-pitch, Thin Ball Grid Array | 173 | 1.0 | 17 x 17 | 1.55 |
| FG320 / FGG320 | 320 | Fine-pitch Ball Grid Array | 221 | 1.0 | 19 x 19 | 2.00 |
| FG456 / FGG456 | 456 | Fine-pitch Ball Grid Array | 333 | 1.0 | 23 x 23 | 2.60 |
| FG676 / FGG676 | 676 | Fine-pitch Ball Grid Array | 489 | 1.0 | 27 x 27 | 2.60 |
| FG900 / FGG900 | 900 | Fine-pitch Ball Grid Array | 633 | 1.0 | 31 x 31 | 2.60 |
| FG1156 / FGG1156(1) | 1156 | Fine-pitch Ball Grid Array | 784 | 1.0 | 35 x 35 | 2.60 |

**Notes:**

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

## Selecting the Right Package Option

Spartan-3 FPGAs are available in both quad-flat pack (QFP) and ball grid array (BGA) packaging options. While QFP packaging offers the lowest absolute cost, the BGA packages are superior in almost every other aspect, as summarized in Table 82. Consequently, Xilinx recommends using BGA packaging whenever possible.

*Table 82:* **Comparing Spartan-3 Device Packaging Options**

| Characteristic | Quad Flat-Pack (QFP) | Ball Grid Array (BGA) |
|---|---|---|
| Maximum User I/O | 141 | 633 |
| Packing Density (Logic/Area) | Good | Better |
| Signal Integrity | Fair | Better |
| Simultaneous Switching Output (SSO) Support | Limited | Better |
| Thermal Dissipation | Fair | Better |
| Minimum Printed Circuit Board (PCB) Layers | 4 | 6 |
| Hand Assembly/Rework | Possible | Very Difficult |

## Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3 FPGA is reported using either the XPower Estimator (XPE) or the XPower Analyzer integrated in the Xilinx ISE development software. Table 86 provides the thermal characteristics for the various Spartan-3 device/package offerings.

The junction-to-case thermal resistance ($\theta_{JC}$) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board ($\theta_{JB}$) value similarly reports the difference between the board and junction temperature. The junction-to-ambient ($\theta_{JA}$) value reports the temperature difference per watt between the ambient environment and the junction temperature. The $\theta_{JA}$ value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the $\theta_{JA}$ value in a system without a fan. The thermal resistance drops with increasing air flow.

*Table 86:* **Spartan-3 FPGA Package Thermal Characteristics**

| Package | Device | Junction-to-Case ($\theta_{JC}$) | Junction-to-Board ($\theta_{JB}$) | Junction-to-Ambient ($\theta_{JA}$) at Different Air Flows | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Still Air (0 LFM) | 250 LFM | 500 LFM | 750 LFM | |
| VQ(G)100 | XC3S50 | 12.0 | – | 46.2 | 38.4 | 35.8 | 34.9 | °C/Watt |
| | XC3S200 | 10.0 | – | 40.5 | 33.7 | 31.3 | 30.5 | °C/Watt |
| CP(G)132(1) | XC3S50 | 14.5 | 32.8 | 53.0 | 46.4 | 44.0 | 42.5 | °C/Watt |
| TQ(G)144 | XC3S50 | 7.6 | – | 41.0 | 31.9 | 27.2 | 25.6 | °C/Watt |
| | XC3S200 | 6.6 | – | 34.5 | 26.9 | 23.0 | 21.6 | °C/Watt |
| | XC3S400 | 6.1 | – | 32.8 | 25.5 | 21.8 | 20.4 | °C/Watt |
| PQ(G)208 | XC3S50 | 10.6 | – | 37.4 | 27.6 | 24.4 | 22.6 | °C/Watt |
| | XC3S200 | 8.6 | – | 36.2 | 26.7 | 23.6 | 21.9 | °C/Watt |
| | XC3S400 | 7.5 | – | 35.4 | 26.1 | 23.1 | 21.4 | °C/Watt |
| FT(G)256 | XC3S200 | 9.9 | 22.9 | 31.7 | 25.6 | 24.5 | 24.2 | °C/Watt |
| | XC3S400 | 7.9 | 19.0 | 28.4 | 22.8 | 21.5 | 21.0 | °C/Watt |
| | XC3S1000 | 5.6 | 14.7 | 24.8 | 19.2 | 18.0 | 17.5 | °C/Watt |
| FG(G)320 | XC3S400 | 8.9 | 13.9 | 24.4 | 19.0 | 17.8 | 17.0 | °C/Watt |
| | XC3S1000 | 7.8 | 11.8 | 22.3 | 17.0 | 15.8 | 15.0 | °C/Watt |
| | XC3S1500 | 6.7 | 9.8 | 20.3 | 15.18 | 13.8 | 13.1 | °C/Watt |
| FG(G)456 | XC3S400 | 8.4 | 13.6 | 20.8 | 15.1 | 13.9 | 13.4 | °C/Watt |
| | XC3S1000 | 6.4 | 10.6 | 19.3 | 13.4 | 12.3 | 11.7 | °C/Watt |
| | XC3S1500 | 4.9 | 8.3 | 18.3 | 12.4 | 11.2 | 10.7 | °C/Watt |
| | XC3S2000 | 3.7 | 6.5 | 17.7 | 11.7 | 10.5 | 10.0 | °C/Watt |
| FG(G)676 | XC3S1000 | 6.0 | 10.4 | 17.9 | 13.7 | 12.6 | 12.0 | °C/Watt |
| | XC3S1500 | 4.9 | 8.8 | 16.8 | 12.4 | 11.3 | 10.7 | °C/Watt |
| | XC3S2000 | 4.1 | 7.9 | 15.6 | 11.1 | 9.9 | 9.3 | °C/Watt |
| | XC3S4000 | 3.6 | 7.0 | 15.0 | 10.5 | 9.3 | 8.7 | °C/Watt |
| | XC3S5000 | 3.4 | 6.3 | 14.7 | 10.3 | 9.1 | 8.5 | °C/Watt |
| FG(G)900 | XC3S2000 | 3.7 | 7.0 | 14.3 | 10.3 | 9.3 | 8.8 | °C/Watt |
| | XC3S4000 | 3.3 | 6.4 | 13.6 | 9.7 | 8.7 | 8.2 | °C/Watt |
| | XC3S5000 | 2.9 | 5.9 | 13.1 | 9.2 | 8.1 | 7.6 | °C/Watt |

*Table 89:* **CP132 Package Pinout *(Cont'd)***

| Bank | XC3S50 Pin Name | CP132 Ball | Type |
|---|---|---|---|
| N/A | GND | M3 | GND |
| N/A | GND | M13 | GND |
| N/A | GND | N6 | GND |
| N/A | GND | N11 | GND |
| N/A | VCCAUX | A5 | VCCAUX |
| N/A | VCCAUX | C10 | VCCAUX |
| N/A | VCCAUX | M5 | VCCAUX |
| N/A | VCCAUX | P10 | VCCAUX |
| N/A | VCCINT | B10 | VCCINT |
| N/A | VCCINT | C6 | VCCINT |
| N/A | VCCINT | M9 | VCCINT |
| N/A | VCCINT | N5 | VCCINT |
| VCCAUX | CCLK | P14 | CONFIG |
| VCCAUX | DONE | P13 | CONFIG |
| VCCAUX | HSWAP_EN | B3 | CONFIG |
| VCCAUX | M0 | N1 | CONFIG |
| VCCAUX | M1 | M2 | CONFIG |
| VCCAUX | M2 | P1 | CONFIG |
| VCCAUX | PROG_B | A2 | CONFIG |
| VCCAUX | TCK | B14 | JTAG |
| VCCAUX | TDI | A1 | JTAG |
| VCCAUX | TDO | C13 | JTAG |
| VCCAUX | TMS | A14 | JTAG |

## User I/Os by Bank

Table 90 indicates how the 89 available user-I/O pins are distributed between the eight I/O banks on the CP132 package. There are only four output banks, each with its own VCCO voltage input.

*Table 90:* **User I/Os Per Bank for XC3S50 in CP132 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | DUAL | DCI | VREF | GCLK |
| Top | 0 | 10 | 5 | 0 | 2 | 1 | 2 |
| | 1 | 10 | 5 | 0 | 2 | 1 | 2 |
| Right | 2 | 12 | 8 | 0 | 2 | 2 | 0 |
| | 3 | 12 | 8 | 0 | 2 | 2 | 0 |
| Bottom | 4 | 11 | 0 | 6 | 2 | 1 | 2 |
| | 5 | 10 | 1 | 6 | 0 | 1 | 2 |
| Left | 6 | 12 | 8 | 0 | 2 | 2 | 0 |
| | 7 | 12 | 9 | 0 | 2 | 1 | 0 |

**Notes:**

1. The CP132 and CPG132 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

*Table 100:* **FG456 Package Pinout *(Cont'd)***

| Bank | 3S400 Pin Name | 3S1000, 3S1500, 3S2000 Pin Name | FG456 Pin Number | Type |
|---|---|---|---|---|
| 4 | IO_L30N_4/D2 | IO_L30N_4/D2 | U12 | DUAL |
| 4 | IO_L30P_4/D3 | IO_L30P_4/D3 | V12 | DUAL |
| 4 | IO_L31N_4/INIT_B | IO_L31N_4/INIT_B | W12 | DUAL |
| 4 | IO_L31P_4/DOUT/BUSY | IO_L31P_4/DOUT/BUSY | Y12 | DUAL |
| 4 | IO_L32N_4/GCLK1 | IO_L32N_4/GCLK1 | AA12 | GCLK |
| 4 | IO_L32P_4/GCLK0 | IO_L32P_4/GCLK0 | AB12 | GCLK |
| 4 | VCCO_4 | VCCO_4 | T12 | VCCO |
| 4 | VCCO_4 | VCCO_4 | T13 | VCCO |
| 4 | VCCO_4 | VCCO_4 | T14 | VCCO |
| 4 | VCCO_4 | VCCO_4 | U15 | VCCO |
| 4 | VCCO_4 | VCCO_4 | Y15 | VCCO |
| 5 | IO | IO | U7 | I/O |
| 5 | N.C. (◆) | IO | U9 | I/O |
| 5 | IO | IO | U10 | I/O |
| 5 | IO | IO | U11 | I/O |
| 5 | IO | IO | V7 | I/O |
| 5 | IO | IO | V10 | I/O |
| 5 | IO/VREF_5 | IO/VREF_5 | AB11 | VREF |
| 5 | IO/VREF_5 | IO/VREF_5 | U6 | VREF |
| 5 | IO_L01N_5/RDWR_B | IO_L01N_5/RDWR_B | Y4 | DUAL |
| 5 | IO_L01P_5/CS_B | IO_L01P_5/CS_B | AA3 | DUAL |
| 5 | IO_L06N_5 | IO_L06N_5 | AB4 | I/O |
| 5 | IO_L06P_5 | IO_L06P_5 | AA4 | I/O |
| 5 | IO_L09N_5 | IO_L09N_5 | Y5 | I/O |
| 5 | IO_L09P_5 | IO_L09P_5 | W5 | I/O |
| 5 | IO_L10N_5/VRP_5 | IO_L10N_5/VRP_5 | AB5 | DCI |
| 5 | IO_L10P_5/VRN_5 | IO_L10P_5/VRN_5 | AA5 | DCI |
| 5 | IO_L15N_5 | IO_L15N_5 | W6 | I/O |
| 5 | IO_L15P_5 | IO_L15P_5 | V6 | I/O |
| 5 | IO_L16N_5 | IO_L16N_5 | AA6 | I/O |
| 5 | IO_L16P_5 | IO_L16P_5 | Y6 | I/O |
| 5 | N.C. (◆) | IO_L19N_5 | Y7 | I/O |
| 5 | N.C. (◆) | IO_L19P_5/ VREF_5 | W7 | VREF |
| 5 | N.C. (◆) | IO_L22N_5 | AB7 | I/O |
| 5 | N.C. (◆) | IO_L22P_5 | AA7 | I/O |
| 5 | IO_L24N_5 | IO_L24N_5 | W8 | I/O |
| 5 | IO_L24P_5 | IO_L24P_5 | V8 | I/O |
| 5 | IO_L25N_5 | IO_L25N_5 | AB8 | I/O |
| 5 | IO_L25P_5 | IO_L25P_5 | AA8 | I/O |

*Table 103:* **FG676 Package Pinout *(Cont'd)***

| Bank | XC3S1000 Pin Name | XC3S1500 Pin Name | XC3S2000 Pin Name | XC3S4000 Pin Name | XC3S5000 Pin Name | FG676 Pin Number | Type |
|---|---|---|---|---|---|---|---|
| 4 | IO_L22N_4/VREF_4 | IO_L22N_4/VREF_4 | IO_L22N_4/VREF_4 | IO_L22N_4/VREF_4 | IO_L22N_4/VREF_4 | AD17 | VREF |
| 4 | IO_L22P_4 | IO_L22P_4 | IO_L22P_4 | IO_L22P_4 | IO_L22P_4 | AB17 | I/O |
| 4 | N.C. (◆) | IO_L23N_4 | IO_L23N_4 | IO_L23N_4 | IO_L23N_4 | AE17 | I/O |
| 4 | N.C. (◆) | IO_L23P_4 | IO_L23P_4 | IO_L23P_4 | IO_L23P_4 | AF17 | I/O |
| 4 | IO_L24N_4 | IO_L24N_4 | IO_L24N_4 | IO_L24N_4 | IO_L24N_4 | Y16 | I/O |
| 4 | IO_L24P_4 | IO_L24P_4 | IO_L24P_4 | IO_L24P_4 | IO_L24P_4 | AA16 | I/O |
| 4 | IO_L25N_4 | IO_L25N_4 | IO_L25N_4 | IO_L25N_4 | IO_L25N_4 | AB16 | I/O |
| 4 | IO_L25P_4 | IO_L25P_4 | IO_L25P_4 | IO_L25P_4 | IO_L25P_4 | AC16 | I/O |
| 4 | N.C. (◆) | IO_L26N_4 | IO_L26N_4 | IO_L26N_4 | IO_L26N_4 | AE16 | I/O |
| 4 | N.C. (◆) | IO_L26P_4/VREF_4 | IO_L26P_4/VREF_4 | IO_L26P_4/VREF_4 | IO_L26P_4/VREF_4 | AF16 | VREF |
| 4 | IO_L27N_4/DIN/D0 | IO_L27N_4/DIN/D0 | IO_L27N_4/DIN/D0 | IO_L27N_4/DIN/D0 | IO_L27N_4/DIN/D0 | Y15 | DUAL |
| 4 | IO_L27P_4/D1 | IO_L27P_4/D1 | IO_L27P_4/D1 | IO_L27P_4/D1 | IO_L27P_4/D1 | W14 | DUAL |
| 4 | IO_L28N_4 | IO_L28N_4 | IO_L28N_4 | IO_L28N_4 | IO_L28N_4 | AA15 | I/O |
| 4 | IO_L28P_4 | IO_L28P_4 | IO_L28P_4 | IO_L28P_4 | IO_L28P_4 | AB15 | I/O |
| 4 | IO_L29N_4 | IO_L29N_4 | IO_L29N_4 | IO_L29N_4 | IO_L29N_4 | AE15 | I/O |
| 4 | IO_L29P_4 | IO_L29P_4 | IO_L29P_4 | IO_L29P_4 | IO_L29P_4 | AF15 | I/O |
| 4 | IO_L30N_4/D2 | IO_L30N_4/D2 | IO_L30N_4/D2 | IO_L30N_4/D2 | IO_L30N_4/D2 | Y14 | DUAL |
| 4 | IO_L30P_4/D3 | IO_L30P_4/D3 | IO_L30P_4/D3 | IO_L30P_4/D3 | IO_L30P_4/D3 | AA14 | DUAL |
| 4 | IO_L31N_4/INIT_B | IO_L31N_4/INIT_B | IO_L31N_4/INIT_B | IO_L31N_4/INIT_B | IO_L31N_4/INIT_B | AC14 | DUAL |
| 4 | IO_L31P_4/ DOUT/BUSY | IO_L31P_4/ DOUT/BUSY | IO_L31P_4/ DOUT/BUSY | IO_L31P_4/ DOUT/BUSY | IO_L31P_4/ DOUT/BUSY | AD14 | DUAL |
| 4 | IO_L32N_4/GCLK1 | IO_L32N_4/GCLK1 | IO_L32N_4/GCLK1 | IO_L32N_4/GCLK1 | IO_L32N_4/GCLK1 | AE14 | GCLK |
| 4 | IO_L32P_4/GCLK0 | IO_L32P_4/GCLK0 | IO_L32P_4/GCLK0 | IO_L32P_4/GCLK0 | IO_L32P_4/GCLK0 | AF14 | GCLK |
| 4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | AD16 | VCCO |
| 4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | AD20 | VCCO |
| 4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | U14 | VCCO |
| 4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | V14 | VCCO |
| 4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | V15 | VCCO |
| 4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | V16 | VCCO |
| 4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | W17 | VCCO |
| 4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | W18 | VCCO |
| 5 | IO | IO | IO | IO | IO | AA7 | I/O |
| 5 | IO | IO | IO | IO | IO | AA13 | I/O |
| 5 | IO | IO | IO | IO | IO_L17P_5[3] | AB9 | I/O |
| 5 | N.C. (◆) | IO | IO | IO | IO_L17N_5[3] | AC9 | I/O |
| 5 | IO | IO | IO | IO | IO | AC11 | I/O |
| 5 | IO | IO | IO | IO | IO | AD10 | I/O |
| 5 | IO | IO | IO | IO | IO | AD12 | I/O |
| 5 | IO | IO | IO | IO | IO | AF4 | I/O |
| 5 | IO | IO | IO | IO | IO | Y8 | I/O |
| 5 | IO/VREF_5 | IO/VREF_5 | IO/VREF_5 | IO/VREF_5 | IO/VREF_5 | AF5 | VREF |
| 5 | IO/VREF_5 | IO/VREF_5 | IO/VREF_5 | IO/VREF_5 | IO/VREF_5 | AF13 | VREF |
| 5 | IO_L01N_5/RDWR_B | IO_L01N_5/RDWR_B | IO_L01N_5/RDWR_B | IO_L01N_5/RDWR_B | IO_L01N_5/RDWR_B | AC5 | DUAL |

## FG676 Footprint

### *Left Half of Package (Top View)*

**XC3S1000 (391 max. user I/O)**

315 **I/O:** Unrestricted, general-purpose user I/O

40 **VREF:** User I/O or input voltage reference for bank

98 **N.C.:** Unconnected pins for XC3S1000 (◆)

**XC3S1500 (487 max user I/O)**

403 **I/O:** Unrestricted, general-purpose user I/O

48 **VREF:** User I/O or input voltage reference for bank

2 **N.C.:** Unconnected pins for XC3S1500 (■)

**XC3S2000, XC3S4000, XC3S5000 (489 max user I/O)**

405 **I/O:** Unrestricted, general-purpose user I/O

48 **VREF:** User I/O or input voltage reference for bank

0 **N.C.:** No unconnected pins

**All devices**

12 **DUAL:** Configuration pin, then possible user I/O

8 **GCLK:** User I/O or global clock buffer input

16 **DCI:** User I/O or reference resistor input for bank

7 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

20 **VCCINT:** Internal core voltage supply (+1.2V)

64 **VCCO:** Output voltage supply for bank

16 **VCCAUX:** Auxiliary voltage supply (+2.5V)

76 **GND:** Ground

| | Bank 0 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
| A | GND | VCCAUX | I/O | I/O L05P_0 VREF_0 | I/O | I/O | I/O L10P_0 | I/O L15P_0 | VCCAUX | I/O L23P_0 ◆ | I/O L26P_0 VREF_0 ◆ | I/O L29P_0 | I/O L32P_0 GCLK6 |
| B | VCCAUX | GND | I/O VREF_0 | I/O L05N_0 | I/O L06P_0 | I/O L08P_0 | I/O L10N_0 | I/O L15N_0 | I/O L18P_0 ◆ | I/O L23N_0 ◆ | I/O L26N_0 ◆ | I/O L29N_0 | I/O L32N_0 GCLK7 |
| C | TDI | HSWAP_EN | GND | I/O | I/O L06N_0 | I/O L08N_0 | VCCO_0 | I/O ◆ | I/O L18N_0 ◆ | I/O L22P_0 | VCCO_0 | I/O | I/O L31P_0 VREF_0 |
| D | I/O L03N_7 VREF_7 | I/O L03P_7 | PROG_B | GND | I/O L01P_0 VRN_0 | I/O L07P_0 | I/O L09P_0 | I/O L12P_0 ◆ | I/O L17P_0 ◆ | I/O L22N_0 | I/O L25P_0 | GND | I/O L31N_0 |
| E | I/O L06N_7 ◆ | I/O L06P_7 ◆ | I/O L02N_7 | I/O L02P_7 | I/O L01N_0 VRP_0 | I/O L07N_0 | I/O L09N_0 | I/O L12N_0 ◆ | I/O L17N_0 ◆ | I/O L19P_0 | I/O L25N_0 | I/O L28P_0 | I/O |
| F | I/O L09N_7 ◆ | I/O L09P_7 ◆ | I/O L07N_7 ◆ | I/O L07P_7 ◆ | I/O L01N_7 VRP_7 | I/O L01P_7 VRN_7 | I/O VREF_0 | I/O L11P_0 ◆ | I/O L16P_0 | I/O L19N_0 | I/O L24P_0 | I/O L28N_0 | I/O L30P_0 |
| G | I/O L14N_7 | I/O L14P_7 | VCCO_7 | I/O L08N_7 ◆ | I/O L08P_7 ◆ | I/O L05N_7 ◆ | I/O L05P_7 ◆ | I/O L11N_0 ◆ | I/O L16N_0 | I/O VREF_0 | I/O L24N_0 | I/O L27N_0 | I/O L30N_0 |
| H | I/O L19N_7 VREF_7 | I/O L19P_7 | I/O L17N_7 | I/O L17P_7 | I/O L16P_7 VREF_7 | I/O L10N_7 ◆ | I/O L10P_7 VREF_7 ◆ | VCCINT | VCCO_0 | VCCO_0 | I/O | I/O | I/O L27P_0 |
| J | VCCAUX | I/O L22N_7 | I/O L22P_7 | I/O L21N_7 | I/O L21P_7 | I/O L16N_7 | I/O L20P_7 | VCCO_7 | VCCINT | VCCINT | VCCO_0 | VCCO_0 | VCCO_0 |
| K | I/O L26N_7 | I/O L26P_7 | I/O L24N_7 | I/O L24P_7 | I/O L23N_7 | I/O L23P_7 | I/O L20N_7 | VCCO_7 | VCCINT | VCCINT | GND | GND | VCCO_0 |
| L | I/O L29N_7 | I/O L29P_7 | VCCO_7 | I/O L33P_7 | I/O L28N_7 | I/O L28P_7 | I/O L27N_7 | I/O L27P_7 VREF_7 | VCCO_7 | GND | GND | GND | GND |
| M | I/O L34N_7 | I/O L34P_7 | I/O L33N_7 | GND | I/O L32P_7 | I/O L32N_7 | I/O L31N_7 | I/O L31P_7 | VCCO_7 | GND | GND | GND | GND |
| N | I/O L40N_7 VREF_7 | I/O L40P_7 | I/O L39N_7 | I/O L39P_7 | I/O L38N_7 | I/O L38P_7 | I/O L35N_7 | I/O L35P_7 | VCCO_7 | VCCO_7 | GND | GND | GND |
| P | I/O L40P_6 VREF_6 | I/O L40N_6 | I/O L39P_6 | I/O L39N_6 | I/O L38P_6 | I/O L38N_6 | I/O L35P_6 | I/O L35N_6 | VCCO_6 | VCCO_6 | GND | GND | GND |
| R | I/O L34P_6 | I/O L34N_6 VREF_6 | I/O L33P_6 | GND | I/O L32P_6 | I/O L32N_6 | I/O L31P_6 | I/O L31N_6 | VCCO_6 | GND | GND | GND | GND |
| T | I/O L29P_6 | I/O L29N_6 | VCCO_6 | I/O L33N_6 | I/O L28P_6 | I/O L28N_6 | I/O L27P_6 | I/O L27N_6 | VCCO_6 | GND | GND | GND | GND |
| U | I/O L26P_6 | I/O L26N_6 | I/O L24P_6 | I/O L24N_6 VREF_6 | I/O L23P_6 | I/O L23N_6 | I/O L20P_6 | VCCO_6 | VCCINT | VCCINT | GND | GND | VCCO_5 |
| V | VCCAUX | I/O L22P_6 | I/O L22N_6 | I/O L21P_6 | I/O L21N_6 | I/O L16N_6 | I/O L20N_6 | VCCO_6 | VCCINT | VCCINT | VCCO_5 | VCCO_5 | VCCO_5 |
| W | I/O L19P_6 | I/O L19N_6 | I/O L17P_6 VREF_6 | I/O L17N_6 | I/O L16P_6 | I/O L14P_6 | I/O L14N_6 | VCCINT | VCCO_5 | VCCO_5 | I/O L24P_5 | I/O L27P_5 | I/O L30P_5 |
| Y | I/O L10P_6 ◆ | I/O L10N_6 ◆ | VCCO_6 | I/O L08P_6 ◆ | I/O L08N_6 ◆ | I/O L06P_6 ◆ | I/O L06N_6 ◆ | I/O | I/O L16P_5 | I/O L19P_5 VREF_5 | I/O L24N_5 | I/O L27N_5 VREF_5 | I/O L30N_5 |
| AA | I/O L09P_6 ◆ | I/O L09N_6 VREF_6 ◆ | I/O L07P_6 ◆ | I/O L07N_6 ◆ | I/O ◆■ | I/O L05P_5 | I/O | I/O L11P_5 ◆ | I/O L16N_5 | I/O L19N_5 | I/O L25P_5 | I/O L28P_5 D7 | I/O |
| AB | I/O L05P_6 ◆ | I/O L05N_6 ◆ | I/O L02P_6 | I/O L02N_6 | I/O L01P_5 CS_B | I/O L05N_5 | I/O L09P_5 | I/O L11N_5 VREF_5 ◆ | I/O | I/O L22P_5 | I/O L25N_5 | I/O L28N_5 D6 | I/O L31P_5 D5 |
| AC | I/O L03P_6 | I/O L03N_6 VREF_6 | M1 | GND | I/O L01N_5 RDWR_B | I/O L07P_5 | I/O L09N_5 | I/O L12P_5 ◆ | I/O ◆ | I/O L22N_5 | I/O | GND | I/O L31N_5 D4 |
| AD | I/O L01P_6 VRN_6 | I/O L01N_6 VRP_6 | GND | I/O L04P_5 | I/O L06P_5 | I/O L07N_5 | VCCO_5 | I/O L12N_5 ◆ | I/O L18P_5 ◆ | I/O | VCCO_5 | I/O | I/O L32P_5 GCLK2 |
| AE | VCCAUX | GND | M0 | I/O L04N_5 | I/O L06N_5 | I/O L08P_5 | I/O L10P_5 VRN_5 | I/O L15P_5 | I/O L18N_5 ◆ | I/O L23P_5 ◆ | I/O L26P_5 ◆ | I/O L29P_5 VREF_5 | I/O L32N_5 GCLK3 |
| AF | GND | VCCAUX | M2 | I/O | I/O VREF_5 | I/O L08N_5 | I/O L10N_5 VRP_5 | I/O L15N_5 | VCCAUX | I/O L23N_5 ◆ | I/O L26N_5 ◆ | I/O L29N_5 | I/O VREF_5 |

Bank 7 (rows H–N) · Bank 6 (rows P–AF) · Bank 5

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*Figure 53:* **FG676 Package Footprint (Top View)**

*Table 107:* **FG900 Package Pinout *(Cont'd)***

| Bank | XC3S2000 Pin Name | XC3S4000, XC3S5000 Pin Name | FG900 Pin Number | Type |
|---|---|---|---|---|
| 0 | IO_L10N_0 | IO_L10N_0 | J9 | I/O |
| 0 | IO_L10P_0 | IO_L10P_0 | H9 | I/O |
| 0 | IO_L11N_0 | IO_L11N_0 | G10 | I/O |
| 0 | IO_L11P_0 | IO_L11P_0 | F10 | I/O |
| 0 | IO_L12N_0 | IO_L12N_0 | C10 | I/O |
| 0 | IO_L12P_0 | IO_L12P_0 | B10 | I/O |
| 0 | IO_L13N_0 | IO_L13N_0 | J10 | I/O |
| 0 | IO_L13P_0 | IO_L13P_0 | K11 | I/O |
| 0 | IO_L14N_0 | IO_L14N_0 | H11 | I/O |
| 0 | IO_L14P_0 | IO_L14P_0 | G11 | I/O |
| 0 | IO_L15N_0 | IO_L15N_0 | F11 | I/O |
| 0 | IO_L15P_0 | IO_L15P_0 | E11 | I/O |
| 0 | IO_L16N_0 | IO_L16N_0 | D11 | I/O |
| 0 | IO_L16P_0 | IO_L16P_0 | C11 | I/O |
| 0 | IO_L17N_0 | IO_L17N_0 | B11 | I/O |
| 0 | IO_L17P_0 | IO_L17P_0 | A11 | I/O |
| 0 | IO_L18N_0 | IO_L18N_0 | K12 | I/O |
| 0 | IO_L18P_0 | IO_L18P_0 | J12 | I/O |
| 0 | IO_L19N_0 | IO_L19N_0 | H12 | I/O |
| 0 | IO_L19P_0 | IO_L19P_0 | G12 | I/O |
| 0 | IO_L20N_0 | IO_L20N_0 | F12 | I/O |
| 0 | IO_L20P_0 | IO_L20P_0 | E12 | I/O |
| 0 | IO_L21N_0 | IO_L21N_0 | D12 | I/O |
| 0 | IO_L21P_0 | IO_L21P_0 | C12 | I/O |
| 0 | IO_L22N_0 | IO_L22N_0 | B12 | I/O |
| 0 | IO_L22P_0 | IO_L22P_0 | A12 | I/O |
| 0 | IO_L23N_0 | IO_L23N_0 | J13 | I/O |
| 0 | IO_L23P_0 | IO_L23P_0 | H13 | I/O |
| 0 | IO_L24N_0 | IO_L24N_0 | F13 | I/O |
| 0 | IO_L24P_0 | IO_L24P_0 | E13 | I/O |
| 0 | IO_L25N_0 | IO_L25N_0 | B13 | I/O |
| 0 | IO_L25P_0 | IO_L25P_0 | A13 | I/O |
| 0 | IO_L26N_0 | IO_L26N_0 | K14 | I/O |
| 0 | IO_L26P_0/VREF_0 | IO_L26P_0/VREF_0 | J14 | VREF |
| 0 | IO_L27N_0 | IO_L27N_0 | G14 | I/O |
| 0 | IO_L27P_0 | IO_L27P_0 | F14 | I/O |
| 0 | IO_L28N_0 | IO_L28N_0 | C14 | I/O |
| 0 | IO_L28P_0 | IO_L28P_0 | B14 | I/O |
| 0 | IO_L29N_0 | IO_L29N_0 | J15 | I/O |
| 0 | IO_L29P_0 | IO_L29P_0 | H15 | I/O |

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| 5 | IO_L04P_5 | IO_L04P_5 | AL6 | I/O |
| 5 | IO_L05N_5 | IO_L05N_5 | AP6 | I/O |
| 5 | IO_L05P_5 | IO_L05P_5 | AN6 | I/O |
| 5 | IO_L06N_5 | IO_L06N_5 | AK7 | I/O |
| 5 | IO_L06P_5 | IO_L06P_5 | AJ7 | I/O |
| 5 | IO_L07N_5 | IO_L07N_5 | AG10 | I/O |
| 5 | IO_L07P_5 | IO_L07P_5 | AF10 | I/O |
| 5 | IO_L08N_5 | IO_L08N_5 | AJ10 | I/O |
| 5 | IO_L08P_5 | IO_L08P_5 | AH10 | I/O |
| 5 | IO_L09N_5 | IO_L09N_5 | AM10 | I/O |
| 5 | IO_L09P_5 | IO_L09P_5 | AL10 | I/O |
| 5 | IO_L10N_5/VRP_5 | IO_L10N_5/VRP_5 | AP10 | DCI |
| 5 | IO_L10P_5/VRN_5 | IO_L10P_5/VRN_5 | AN10 | DCI |
| 5 | IO_L11N_5/VREF_5 | IO_L11N_5/VREF_5 | AP11 | VREF |
| 5 | IO_L11P_5 | IO_L11P_5 | AN11 | I/O |
| 5 | IO_L12N_5 | IO_L12N_5 | AF12 | I/O |
| 5 | IO_L12P_5 | IO_L12P_5 | AE12 | I/O |
| 5 | IO_L13N_5 | IO_L13N_5 | AJ12 | I/O |
| 5 | IO_L13P_5 | IO_L13P_5 | AH12 | I/O |
| 5 | IO_L14N_5 | IO_L14N_5 | AL12 | I/O |
| 5 | IO_L14P_5 | IO_L14P_5 | AK12 | I/O |
| 5 | IO_L15N_5 | IO_L15N_5 | AP12 | I/O |
| 5 | IO_L15P_5 | IO_L15P_5 | AN12 | I/O |
| 5 | IO_L16N_5 | IO_L16N_5 | AE13 | I/O |
| 5 | IO_L16P_5 | IO_L16P_5 | AD13 | I/O |
| 5 | IO_L17N_5 | IO_L17N_5 | AH13 | I/O |
| 5 | IO_L17P_5 | IO_L17P_5 | AG13 | I/O |
| 5 | IO_L18N_5 | IO_L18N_5 | AM13 | I/O |
| 5 | IO_L18P_5 | IO_L18P_5 | AL13 | I/O |
| 5 | IO_L19N_5 | IO_L19N_5 | AG14 | I/O |
| 5 | IO_L19P_5/VREF_5 | IO_L19P_5/VREF_5 | AF14 | VREF |
| 5 | IO_L20N_5 | IO_L20N_5 | AJ14 | I/O |
| 5 | IO_L20P_5 | IO_L20P_5 | AH14 | I/O |
| 5 | IO_L21N_5 | IO_L21N_5 | AM14 | I/O |
| 5 | IO_L21P_5 | IO_L21P_5 | AL14 | I/O |
| 5 | IO_L22N_5 | IO_L22N_5 | AP14 | I/O |
| 5 | IO_L22P_5 | IO_L22P_5 | AN14 | I/O |
| 5 | IO_L23N_5 | IO_L23N_5 | AF15 | I/O |
| 5 | IO_L23P_5 | IO_L23P_5 | AE15 | I/O |
| 5 | IO_L24N_5 | IO_L24N_5 | AJ15 | I/O |

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| N/A | GND | GND | J22 | GND |
| N/A | GND | GND | J30 | GND |
| N/A | GND | GND | J34 | GND |
| N/A | GND | GND | J5 | GND |
| N/A | GND | GND | K10 | GND |
| N/A | GND | GND | K25 | GND |
| N/A | GND | GND | L3 | GND |
| N/A | GND | GND | L32 | GND |
| N/A | GND | GND | N1 | GND |
| N/A | GND | GND | N17 | GND |
| N/A | GND | GND | N18 | GND |
| N/A | GND | GND | N26 | GND |
| N/A | GND | GND | N30 | GND |
| N/A | GND | GND | N34 | GND |
| N/A | GND | GND | N5 | GND |
| N/A | GND | GND | N9 | GND |
| N/A | GND | GND | P14 | GND |
| N/A | GND | GND | P15 | GND |
| N/A | GND | GND | P16 | GND |
| N/A | GND | GND | P17 | GND |
| N/A | GND | GND | P18 | GND |
| N/A | GND | GND | P19 | GND |
| N/A | GND | GND | P20 | GND |
| N/A | GND | GND | P21 | GND |
| N/A | GND | GND | R14 | GND |
| N/A | GND | GND | R15 | GND |
| N/A | GND | GND | R16 | GND |
| N/A | GND | GND | R17 | GND |
| N/A | GND | GND | R18 | GND |
| N/A | GND | GND | R19 | GND |
| N/A | GND | GND | R20 | GND |
| N/A | GND | GND | R21 | GND |
| N/A | GND | GND | T1 | GND |
| N/A | GND | GND | T14 | GND |
| N/A | GND | GND | T15 | GND |
| N/A | GND | GND | T16 | GND |
| N/A | GND | GND | T17 | GND |
| N/A | GND | GND | T18 | GND |
| N/A | GND | GND | T19 | GND |
| N/A | GND | GND | T20 | GND |

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| N/A | GND | GND | Y14 | GND |
| N/A | GND | GND | Y15 | GND |
| N/A | GND | GND | Y16 | GND |
| N/A | GND | GND | Y17 | GND |
| N/A | GND | GND | Y18 | GND |
| N/A | GND | GND | Y19 | GND |
| N/A | GND | GND | Y20 | GND |
| N/A | GND | GND | Y21 | GND |
| N/A | N.C. (◆) | N.C. (■) | AK31 | N.C. |
| N/A | VCCAUX | VCCAUX | AD30 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AD5 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AG16 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AG19 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AJ30 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AJ5 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AK11 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AK15 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AK20 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AK24 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AK29 | VCCAUX |
| N/A | VCCAUX | VCCAUX | AK6 | VCCAUX |
| N/A | VCCAUX | VCCAUX | E11 | VCCAUX |
| N/A | VCCAUX | VCCAUX | E15 | VCCAUX |
| N/A | VCCAUX | VCCAUX | E20 | VCCAUX |
| N/A | VCCAUX | VCCAUX | E24 | VCCAUX |
| N/A | VCCAUX | VCCAUX | E29 | VCCAUX |
| N/A | VCCAUX | VCCAUX | E6 | VCCAUX |
| N/A | VCCAUX | VCCAUX | F30 | VCCAUX |
| N/A | VCCAUX | VCCAUX | F5 | VCCAUX |
| N/A | VCCAUX | VCCAUX | H16 | VCCAUX |
| N/A | VCCAUX | VCCAUX | H19 | VCCAUX |
| N/A | VCCAUX | VCCAUX | L30 | VCCAUX |
| N/A | VCCAUX | VCCAUX | L5 | VCCAUX |
| N/A | VCCAUX | VCCAUX | R30 | VCCAUX |
| N/A | VCCAUX | VCCAUX | R5 | VCCAUX |
| N/A | VCCAUX | VCCAUX | T27 | VCCAUX |
| N/A | VCCAUX | VCCAUX | T8 | VCCAUX |
| N/A | VCCAUX | VCCAUX | W27 | VCCAUX |
| N/A | VCCAUX | VCCAUX | W8 | VCCAUX |
| N/A | VCCAUX | VCCAUX | Y30 | VCCAUX |

| 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | GND | GND | GND | GND | VCCINT | I/O L51N_3 ◆ | I/O | I/O | I/O L37P_3 | I/O L37N_3 | I/O L38P_3 | I/O L38N_3 | I/O L39P_3 | I/O L39N_3 | I/O L40P_3 | I/O L40N_3 VREF_3 | V |
| GND | GND | GND | GND | VCCINT | VCCO_3 | I/O L51P_3 ◆ | I/O L33N_3 | GND | VCCAUX | I/O L34P_3 VREF_3 | I/O L34N_3 | GND | VCCO_3 | I/O L35P_3 | I/O L35N_3 | GND | W |
| GND | GND | GND | GND | VCCINT | VCCO_3 | I/O L50P_3 | I/O L50N_3 | I/O L33P_3 | VCCO_3 | I/O L30P_3 | I/O L30N_3 | VCCAUX | I/O L31P_3 | I/O L31N_3 | I/O L32P_3 | I/O L32N_3 | Y |
| GND | GND | GND | GND | VCCINT | VCCO_3 | I/O L48N_3 | I/O L49P_3 ◆ | I/O L49N_3 ◆ | I/O L26P_3 | I/O L26N_3 | I/O L27P_3 | I/O L27N_3 | I/O L28P_3 | I/O L28N_3 | I/O L29P_3 | I/O L29N_3 | AA |
| GND | VCCINT | VCCINT | VCCINT | VCCINT | VCCO_3 | I/O L48P_3 | I/O L24N_3 | GND | I/O L46P_3 | I/O L46N_3 | VCCO_3 | GND | I/O L47P_3 | I/O L47N_3 | VCCO_3 | GND | AB |
| VCCINT | VCCO_4 | VCCO_4 | VCCO_4 | VCCO_4 | VCCINT | I/O L20P_3 | I/O L20N_3 | I/O L24P_3 | I/O L21P_3 | I/O L21N_3 | I/O L22P_3 | I/O L22N_3 | I/O L23P_3 VREF_3 | I/O L23N_3 | I/O L45P_3 | I/O L45N_3 | AC |
| I/O | I/O | I/O | I/O L18N_4 | I/O | I/O L11N_4 | DONE | I/O L17P_3 VREF_3 | I/O L17N_3 | VCCO_3 | I/O L44P_3 ◆ | I/O L44N_3 ◆ | VCCAUX | VCCO_3 | GND | I/O L19P_3 | I/O L19N_3 | AD |
| I/O | I/O | I/O L23N_4 | I/O L18P_4 | I/O | I/O L11P_4 | I/O ◆ | GND | I/O L12N_3 | I/O L13P_3 | I/O L13N_3 VREF_3 | I/O L14P_3 | I/O L14N_3 | I/O L15P_3 | I/O L15N_3 | I/O L16P_3 | I/O L16N_3 | AE |
| I/O L29N_4 | GND | I/O L23P_4 | IO VREF_4 | GND | I/O L12N_4 | I/O | I/O L07N_4 | I/O ◆ | I/O L12P_3 | I/O L09P_3 VREF_3 | I/O L09N_3 | GND | I/O L10N_3 | I/O L11P_3 | I/O L11N_3 | GND | AF |
| I/O L29P_4 | VCCAUX | VCCO_4 | I/O L19N_4 | I/O L16N_4 | I/O L12P_4 | VCCO_4 | I/O L07P_4 | I/O | I/O | VCCO_3 | I/O L07P_3 | I/O L07N_3 | I/O L10P_3 | VCCO_3 | I/O L08P_3 | I/O L08N_3 | AG |
| I/O L30N_4 D2 | I/O L27N_4 DIN D0 | I/O L24N_4 | I/O L19P_4 | I/O L16P_4 | IO VREF_4 | I/O L39N_4 ◆ | I/O L08N_4 | I/O L05N_4 | VCCO_4 | GND | I/O L06P_3 | I/O L06N_3 | I/O L41P_3 ◆ | I/O L41N_3 ◆ | I/O | I/O | AH |
| I/O L30P_4 D3 | I/O L27P_4 D1 | I/O L24P_4 | I/O L20N_4 | VCCO_4 | I/O L13N_4 | I/O L39P_4 ◆ | I/O L08P_4 | I/O L05P_4 | I/O | I/O L35N_4 | I/O | VCCAUX | I/O L04P_3 | I/O L04N_3 | I/O L05P_3 | I/O L05N_3 | AJ |
| IO VREF_4 | GND | VCCAUX | I/O L20P_4 | GND | I/O L13P_4 | VCCAUX | I/O | GND | I/O L38N_4 | I/O L35P_4 | VCCAUX | GND | N.C. ◆ ■ | I/O L03P_3 | I/O L03N_3 | GND | AK |
| I/O L31N_4 INIT_B | VCCO_4 | I/O L25N_4 | I/O L21N_4 | I/O L17N_4 | I/O L14N_4 | VCCO_4 | I/O L09N_4 | I/O L06N_4 VREF_4 | I/O L38P_4 | I/O L36N_4 ◆ | I/O L33N_4 | IO VREF_4 | CCLK | VCCO_3 | I/O L02P_3 | I/O L02N_3 VREF_3 | AL |
| I/O L31P_4 DOUT BUSY | I/O L28N_4 | I/O L25P_4 | I/O L21P_4 | I/O L17P_4 | I/O L14P_4 | GND | I/O L09P_4 | I/O L06P_4 | VCCO_4 | I/O L36P_4 ◆ | I/O L33P_4 | I/O L03N_4 | VCCO_4 | GND | I/O L01P_3 VRN_3 | I/O L01N_3 VRP_3 | AM |
| I/O L32N_4 GCLK1 | I/O L28P_4 | I/O L26N_4 | I/O L22N_4 VREF_4 | VCCO_4 | I/O L15N_4 | I/O L40N_4 ◆ | I/O L10N_4 | I/O | I/O L04N_4 | I/O L37N_4 ◆ | I/O L34N_4 | I/O L03P_4 | I/O L02N_4 | I/O L01N_4 VRP_4 | GND | GND | AN |
| I/O L32P_4 GCLK0 | GND | I/O L26P_4 VREF_4 | I/O L22P_4 | GND | I/O L15P_4 | I/O L40P_4 ◆ | I/O L10P_4 | GND | I/O L04P_4 | I/O L37P_4 ◆ | I/O L34P_4 | GND | I/O L02P_4 | I/O L01P_4 VRN_4 | GND | GND | AP |

Bank 3

Bank 4

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***Bottom Right Corner of FG1156 Package (Top View)***

**Figure 60: FG1156 Package Footprint (Top View) Continued**