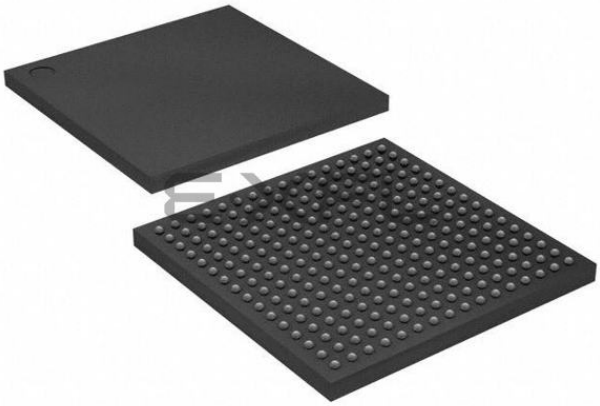
AMD Xilinx - XC3S200-4FT256C Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	480
Number of Logic Elements/Cells	4320
Total RAM Bits	221184
Number of I/O	173
Number of Gates	200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s200-4ft256c

The DCI feature operates independently for each of the device's eight banks. Each bank has an 'N' reference pin (VRN) and a 'P' reference pin, (VRP), to calibrate driver and termination resistance. Only when using a DCI standard on a given bank do these two pins function as VRN and VRP. When not using a DCI standard, the two pins function as user I/Os. As shown in Figure 9, add an external reference resistor to pull the VRN pin up to V_{CCO} and another reference resistor to pull the VRP pin down to GND. Also see Figure 42, page 116. Both resistors have the same value—commonly 50Ω—with one-percent tolerance, which is either the characteristic impedance of the line or twice that, depending on the DCI standard in use. Standards having a symbol name that contains the letters "DV2" use a reference resistor value that is twice the line impedance. DCI adjusts the output driver impedance to match the reference resistors' value or half that, according to the standard. DCI always adjusts the on-chip termination resistors to directly match the reference resistors' value.

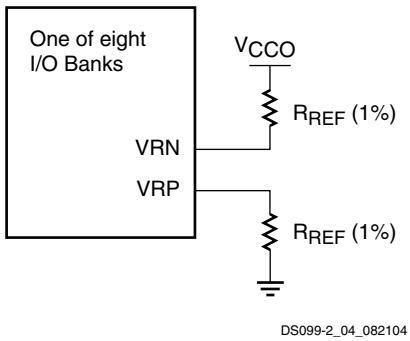

Figure 9: **Connection of Reference Resistors (R_{REF})**

The rules guiding the use of DCI standards on banks are as follows:

- No more than one DCI I/O standard with a Single Termination is allowed per bank.
- No more than one DCI I/O standard with a Split Termination is allowed per bank.
- Single Termination, Split Termination, Controlled- Impedance Driver, and Controlled-Impedance Driver with Half Impedance can co-exist in the same bank.

See also The Organization of IOBs into Banks, immediately below, and DCI: User I/O or Digitally Controlled Impedance Resistor Reference Input, page 115.

The Organization of IOBs into Banks

IOBs are allocated among eight banks, so that each side of the device has two banks, as shown in Figure 10. For all packages, each bank has independent V_{REF} lines. For example, V_{REF} Bank 3 lines are separate from the V_{REF} lines going to all other banks.

For the Very Thin Quad Flat Pack (VQ), Plastic Quad Flat Pack (PQ), Fine Pitch Thin Ball Grid Array (FT), and Fine Pitch Ball Grid Array (FG) packages, each bank has dedicated V_{CCO} lines. For example, the V_{CCO} Bank 7 lines are separate from the V_{CCO} lines going to all other banks. Thus, Spartan-3 devices in these packages support eight independent V_{CCO} supplies.

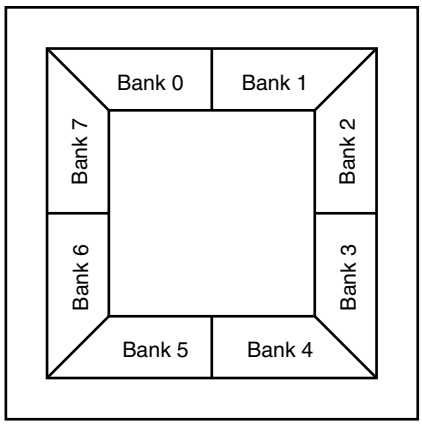

Figure 10: **Spartan-3 FPGA I/O Banks (Top View)**

I/O Timing

Table 40: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max(2)	Max(2)	
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(3), 12 mA output drive, Fast slew rate, with DCM(4)	XC3S50	2.04	2.35	ns
			XC3S200	1.45	1.75	ns
			XC3S400	1.45	1.75	ns
			XC3S1000	2.07	2.39	ns
			XC3S1500	2.05	2.36	ns
			XC3S2000	2.03	2.34	ns
			XC3S4000	1.94	2.24	ns
			XC3S5000	2.00	2.30	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(3), 12 mA output drive, Fast slew rate, without DCM	XC3S50	3.70	4.24	ns
			XC3S200	3.89	4.46	ns
			XC3S400	3.91	4.48	ns
			XC3S1000	4.00	4.59	ns
			XC3S1500	4.07	4.66	ns
			XC3S2000	4.19	4.80	ns
			XC3S4000	4.44	5.09	ns
			XC3S5000	4.38	5.02	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. For minimums, use the values reported by the Xilinx timing analyzer.
3. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 44. If the latter is true, *add* the appropriate Output adjustment from Table 47.
4. DCM output jitter is included in all measurements.

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package				
			VQ100	TQ144	PQ208	CP132	FT256, FG320, FG456, FG676, FG900, FG1156
LVCMOS33	Slow	2	34	24	24	52	76
		4	17	14	14	26	46
		6	17	11	11	26	27
		8	10	10	10	13	20
		12	9	9	9	13	13
		16	8	8	8	8	10
		24	8	8	8	8	9
	Fast	2	20	20	20	26	44
		4	15	15	15	15	26
		6	11	11	11	13	16
		8	10	10	10	10	12
		12	8	8	8	8	10
		16	8	8	8	8	8
		24	7	7	7	7	7
LVDCI_33			10	10	10	10	10
LVDCI_DV2_33			10	10	10	10	10
HSLVDCI_33			10	10	10	10	10
LVTTL	Slow	2	34	25	25	52	60
		4	17	16	16	26	41
		6	17	15	15	26	29
		8	12	12	12	13	22
		12	10	10	10	13	13
		16	10	10	10	10	11
		24	8	8	8	8	9
	Fast	2	20	20	20	26	34
		4	13	13	13	13	20
		6	11	11	11	13	15
		8	10	10	10	10	12
		12	9	9	9	9	10
		16	8	8	8	8	9
		24	7	7	7	7	7

Miscellaneous DCM Timing

Table 64: **Miscellaneous DCM Timing**

Symbol	Description	DLL Frequency Mode	Temperature Range		Units
			Commercial	Industrial	
DCM_INPUT_CLOCK_STOP	Maximum duration that the CLKIN and CLKFB signals can be stopped(1,2)	Any	100	100	ms
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	Any	3	3	CLKIN cycles
DCM_RST_PW_MAX(3)	Maximum duration of a RST pulse width(1,2)	Low	N/A	N/A	seconds
		High	N/A	10	seconds
DCM_CONFIG_LAG_TIME(4)	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL(1,2)	Low	N/A	N/A	minutes
		High	N/A	10	minutes

Notes:

1. These limits only apply to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected. Required due to effects of device cooling: see “Momentarily Stopping CLKIN” in Chapter 3 of UG331.
2. Industrial-temperature applications that use the DLL in High-Frequency mode must use a continuous or increasing operating frequency. The DLL under these conditions does not support reducing the operating frequency once establishing an initial operating frequency.
3. This specification is equivalent to the Virtex-4 FPGA DCM_RESET specification.
4. This specification is equivalent to the Virtex-4 FPGA TCONFIG specification.

Differential Pair Labeling

A pin supports differential standards if the pin is labeled in the format “Lxxy_#”. The pin name suffix has the following significance. Figure 40 provides a specific example showing a differential input to and a differential output from Bank 2.

- ‘L’ indicates differential capability.
- "xx" is a two-digit integer, unique for each bank, that identifies a differential pin-pair.
- ‘y’ is replaced by ‘P’ for the true signal or ‘N’ for the inverted. These two pins form one differential pin-pair.
- ‘#’ is an integer, 0 through 7, indicating the associated I/O bank.

If unused, these pins are in a high impedance state. The Bitstream generator option UnusedPin enables a pull-up or pull-down resistor on all unused I/O pins.

Behavior from Power-On through End of Configuration

During the configuration process, all pins that are not actively involved in the configuration process are in a high-impedance state. The CONFIG- and JTAG-type pins have an internal pull-up resistor to VCCAUX during configuration. For all other I/O pins, the HSWAP_EN input determines whether or not pull-up resistors are activated during configuration. HSWAP_EN = 0 enables the pull-up resistors. HSWAP_EN = 1 disables the pull-up resistors allowing the pins to float, which is the desired state for hot-swap applications.

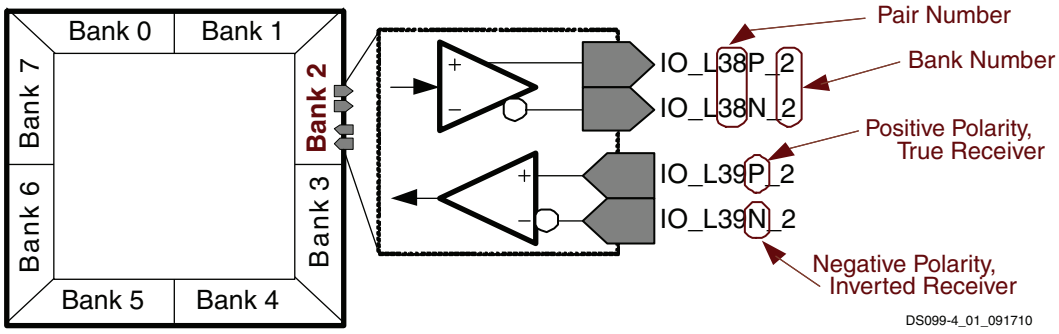

Figure 40: **Differential Pair Labelling**

DUAL Type: Dual-Purpose Configuration and I/O Pins

These pins serve dual purposes. The user-I/O pins are temporarily borrowed during the configuration process to load configuration data into the FPGA. After configuration, these pins are then usually available as a user I/O in the application. If a pin is not applicable to the specific configuration mode—controlled by the mode select pins M2, M1, and M0—then the pin behaves as an I/O-type pin.

There are 12 dual-purpose configuration pins on every package, six of which are part of I/O Bank 4, the other six part of I/O Bank 5. Only a few of the pins in Bank 4 are used in the Serial configuration modes.

See Pin Behavior During Configuration, page 122.

Serial Configuration Modes

This section describes the dual-purpose pins used during either Master or Slave Serial mode. See Table 75 for Mode Select pin settings required for Serial modes. All such pins are in Bank 4 and powered by VCCO_4.

In both the Master and Slave Serial modes, DIN is the serial configuration data input. The D1-D7 inputs are unused in serial mode and behave like general-purpose I/O pins.

In all the cases, the configuration data is synchronized to the rising edge of the CCLK clock signal.

The DIN, DOUT, and INIT_B pins can be retained in the application to support reconfiguration by setting the Persist bitstream generation option. However, the serial modes do not support device readback.

User I/Os by Bank

Table 92 indicates how the available user-I/O pins are distributed between the eight I/O banks on the TQ144 package.

Table 92: **User I/Os Per Bank in TQ144 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	10	5	0	2	1	2
	1	9	4	0	2	1	2
Right	2	14	10	0	2	2	0
	3	15	11	0	2	2	0
Bottom	4	11	0	6	2	1	2
	5	9	0	6	0	1	2
Left	6	14	10	0	2	2	0
	7	15	11	0	2	2	0

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	AD17	VREF
4	IO_L22P_4	IO_L22P_4	IO_L22P_4	IO_L22P_4	IO_L22P_4	AB17	I/O
4	N.C. (◆)	IO_L23N_4	IO_L23N_4	IO_L23N_4	IO_L23N_4	AE17	I/O
4	N.C. (◆)	IO_L23P_4	IO_L23P_4	IO_L23P_4	IO_L23P_4	AF17	I/O
4	IO_L24N_4	IO_L24N_4	IO_L24N_4	IO_L24N_4	IO_L24N_4	Y16	I/O
4	IO_L24P_4	IO_L24P_4	IO_L24P_4	IO_L24P_4	IO_L24P_4	AA16	I/O
4	IO_L25N_4	IO_L25N_4	IO_L25N_4	IO_L25N_4	IO_L25N_4	AB16	I/O
4	IO_L25P_4	IO_L25P_4	IO_L25P_4	IO_L25P_4	IO_L25P_4	AC16	I/O
4	N.C. (◆)	IO_L26N_4	IO_L26N_4	IO_L26N_4	IO_L26N_4	AE16	I/O
4	N.C. (◆)	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	AF16	VREF
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	Y15	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	IO_L27P_4/D1	IO_L27P_4/D1	IO_L27P_4/D1	W14	DUAL
4	IO_L28N_4	IO_L28N_4	IO_L28N_4	IO_L28N_4	IO_L28N_4	AA15	I/O
4	IO_L28P_4	IO_L28P_4	IO_L28P_4	IO_L28P_4	IO_L28P_4	AB15	I/O
4	IO_L29N_4	IO_L29N_4	IO_L29N_4	IO_L29N_4	IO_L29N_4	AE15	I/O
4	IO_L29P_4	IO_L29P_4	IO_L29P_4	IO_L29P_4	IO_L29P_4	AF15	I/O
4	IO_L30N_4/D2	IO_L30N_4/D2	IO_L30N_4/D2	IO_L30N_4/D2	IO_L30N_4/D2	Y14	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	IO_L30P_4/D3	IO_L30P_4/D3	IO_L30P_4/D3	AA14	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	AC14	DUAL
4	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	AD14	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	AE14	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	AF14	GCLK
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	AD16	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	AD20	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	U14	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	V14	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	V15	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	V16	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	W17	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	W18	VCCO
5	IO	IO	IO	IO	IO	AA7	I/O
5	IO	IO	IO	IO	IO	AA13	I/O
5	IO	IO	IO	IO	IO_L17P_5(3)	AB9	I/O
5	N.C. (◆)	IO	IO	IO	IO_L17N_5(3)	AC9	I/O
5	IO	IO	IO	IO	IO	AC11	I/O
5	IO	IO	IO	IO	IO	AD10	I/O
5	IO	IO	IO	IO	IO	AD12	I/O
5	IO	IO	IO	IO	IO	AF4	I/O
5	IO	IO	IO	IO	IO	Y8	I/O
5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	AF5	VREF
5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	AF13	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	AC5	DUAL

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
6	IO_L20N_6	IO_L20N_6	IO_L20N_6	IO_L20N_6	IO_L20N_6	V7	I/O
6	IO_L20P_6	IO_L20P_6	IO_L20P_6	IO_L20P_6	IO_L20P_6	U7	I/O
6	IO_L21N_6	IO_L21N_6	IO_L21N_6	IO_L21N_6	IO_L21N_6	V5	I/O
6	IO_L21P_6	IO_L21P_6	IO_L21P_6	IO_L21P_6	IO_L21P_6	V4	I/O
6	IO_L22N_6	IO_L22N_6	IO_L22N_6	IO_L22N_6	IO_L22N_6	V3	I/O
6	IO_L22P_6	IO_L22P_6	IO_L22P_6	IO_L22P_6	IO_L22P_6	V2	I/O
6	IO_L23N_6	IO_L23N_6	IO_L23N_6	IO_L23N_6	IO_L23N_6	U6	I/O
6	IO_L23P_6	IO_L23P_6	IO_L23P_6	IO_L23P_6	IO_L23P_6	U5	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	U4	VREF
6	IO_L24P_6	IO_L24P_6	IO_L24P_6	IO_L24P_6	IO_L24P_6	U3	I/O
6	IO_L26N_6	IO_L26N_6	IO_L26N_6	IO_L26N_6	IO_L26N_6	U2	I/O
6	IO_L26P_6	IO_L26P_6	IO_L26P_6	IO_L26P_6	IO_L26P_6	U1	I/O
6	IO_L27N_6	IO_L27N_6	IO_L27N_6	IO_L27N_6	IO_L27N_6	T8	I/O
6	IO_L27P_6	IO_L27P_6	IO_L27P_6	IO_L27P_6	IO_L27P_6	T7	I/O
6	IO_L28N_6	IO_L28N_6	IO_L28N_6	IO_L28N_6	IO_L28N_6	T6	I/O
6	IO_L28P_6	IO_L28P_6	IO_L28P_6	IO_L28P_6	IO_L28P_6	T5	I/O
6	IO_L29N_6	IO_L29N_6	IO_L29N_6	IO_L29N_6	IO_L29N_6	T2	I/O
6	IO_L29P_6	IO_L29P_6	IO_L29P_6	IO_L29P_6	IO_L29P_6	T1	I/O
6	IO_L31N_6	IO_L31N_6	IO_L31N_6	IO_L31N_6	IO_L31N_6	R8	I/O
6	IO_L31P_6	IO_L31P_6	IO_L31P_6	IO_L31P_6	IO_L31P_6	R7	I/O
6	IO_L32N_6	IO_L32N_6	IO_L32N_6	IO_L32N_6	IO_L32N_6	R6	I/O
6	IO_L32P_6	IO_L32P_6	IO_L32P_6	IO_L32P_6	IO_L32P_6	R5	I/O
6	IO_L33N_6	IO_L33N_6	IO_L33N_6	IO_L33N_6	IO_L33N_6	T4	I/O
6	IO_L33P_6	IO_L33P_6	IO_L33P_6	IO_L33P_6	IO_L33P_6	R3	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	R2	VREF
6	IO_L34P_6	IO_L34P_6	IO_L34P_6	IO_L34P_6	IO_L34P_6	R1	I/O
6	IO_L35N_6	IO_L35N_6	IO_L35N_6	IO_L35N_6	IO_L35N_6	P8	I/O
6	IO_L35P_6	IO_L35P_6	IO_L35P_6	IO_L35P_6	IO_L35P_6	P7	I/O
6	IO_L38N_6	IO_L38N_6	IO_L38N_6	IO_L38N_6	IO_L38N_6	P6	I/O
6	IO_L38P_6	IO_L38P_6	IO_L38P_6	IO_L38P_6	IO_L38P_6	P5	I/O
6	IO_L39N_6	IO_L39N_6	IO_L39N_6	IO_L39N_6	IO_L39N_6	P4	I/O
6	IO_L39P_6	IO_L39P_6	IO_L39P_6	IO_L39P_6	IO_L39P_6	P3	I/O
6	IO_L40N_6	IO_L40N_6	IO_L40N_6	IO_L40N_6	IO_L40N_6	P2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	P1	VREF
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	P9	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	P10	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	R9	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	T3	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	T9	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	U8	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	V8	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	Y3	VCCO
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	F5	DCI

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	U17	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	U18	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V9	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V10	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V17	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V18	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	W8	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	W19	VCCINT
VCC AUX	CCLK	CCLK	CCLK	CCLK	CCLK	AD26	CONFIG
VCC AUX	DONE	DONE	DONE	DONE	DONE	AC24	CONFIG
VCC AUX	HSWAP_EN	HSWAP_EN	HSWAP_EN	HSWAP_EN	HSWAP_EN	C2	CONFIG
VCC AUX	M0	M0	M0	M0	M0	AE3	CONFIG
VCC AUX	M1	M1	M1	M1	M1	AC3	CONFIG
VCC AUX	M2	M2	M2	M2	M2	AF3	CONFIG
VCC AUX	PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	D3	CONFIG
VCC AUX	TCK	TCK	TCK	TCK	TCK	B24	JTAG
VCC AUX	TDI	TDI	TDI	TDI	TDI	C1	JTAG
VCC AUX	TDO	TDO	TDO	TDO	TDO	D24	JTAG
VCC AUX	TMS	TMS	TMS	TMS	TMS	A24	JTAG

Notes:
1. XC3S1500 balls D25 and F25 are not VREF pins although they are designated as such. If a design uses an IOSTANDARD requiring VREF in bank 2 then apply the workaround in Answer Record 20519.
2. XC3S4000 is pin compatible with XC3S2000 but uses alternate differential pair labeling on six package balls (H20, H21, H22, H23, H24, J21).
3. XC3S5000 is pin compatible with XC3S4000 but uses alternate differential pair functionality on fifteen package balls (A3, A8, B8, B18, C4, C8, C18, D8, D18, E8, E18, H23, H24, AB9, and AC9).

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	IO_L04N_2	IO_L04N_2	E29	I/O
2	IO_L04P_2	IO_L04P_2	E30	I/O
2	IO_L05N_2	IO_L05N_2	F28	I/O
2	IO_L05P_2	IO_L05P_2	F29	I/O
2	IO_L06N_2	IO_L06N_2	G27	I/O
2	IO_L06P_2	IO_L06P_2	G28	I/O
2	IO_L07N_2	IO_L07N_2	G29	I/O
2	IO_L07P_2	IO_L07P_2	G30	I/O
2	IO_L08N_2	IO_L08N_2	G25	I/O
2	IO_L08P_2	IO_L08P_2	H24	I/O
2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	H25	VREF
2	IO_L09P_2	IO_L09P_2	H26	I/O
2	IO_L10N_2	IO_L10N_2	H27	I/O
2	IO_L10P_2	IO_L10P_2	H28	I/O
2	IO_L12N_2	IO_L12N_2	H29	I/O
2	IO_L12P_2	IO_L12P_2	H30	I/O
2	IO_L13N_2	IO_L13N_2	J26	I/O
2	IO_L13P_2/VREF_2	IO_L13P_2/VREF_2	J27	VREF
2	IO_L14N_2	IO_L14N_2	J29	I/O
2	IO_L14P_2	IO_L14P_2	J30	I/O
2	IO_L15N_2	IO_L15N_2	J23	I/O
2	IO_L15P_2	IO_L15P_2	K22	I/O
2	IO_L16N_2	IO_L16N_2	K24	I/O
2	IO_L16P_2	IO_L16P_2	K25	I/O
2	IO_L19N_2	IO_L19N_2	L25	I/O
2	IO_L19P_2	IO_L19P_2	L26	I/O
2	IO_L20N_2	IO_L20N_2	L27	I/O
2	IO_L20P_2	IO_L20P_2	L28	I/O
2	IO_L21N_2	IO_L21N_2	L29	I/O
2	IO_L21P_2	IO_L21P_2	L30	I/O
2	IO_L22N_2	IO_L22N_2	M22	I/O
2	IO_L22P_2	IO_L22P_2	M23	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	M24	VREF
2	IO_L23P_2	IO_L23P_2	M25	I/O
2	IO_L24N_2	IO_L24N_2	M27	I/O
2	IO_L24P_2	IO_L24P_2	M28	I/O
2	IO_L26N_2	IO_L26N_2	M21	I/O
2	IO_L26P_2	IO_L26P_2	N21	I/O
2	IO_L27N_2	IO_L27N_2	N22	I/O
2	IO_L27P_2	IO_L27P_2	N23	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	VCCO_2	VCCO_2	J28	VCCO
2	VCCO_2	VCCO_2	N28	VCCO
3	IO	IO	AB25	I/O
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	AH30	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	AH29	DCI
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	AG28	VREF
3	IO_L02P_3	IO_L02P_3	AG27	I/O
3	IO_L03N_3	IO_L03N_3	AG30	I/O
3	IO_L03P_3	IO_L03P_3	AG29	I/O
3	IO_L04N_3	IO_L04N_3	AF30	I/O
3	IO_L04P_3	IO_L04P_3	AF29	I/O
3	IO_L05N_3	IO_L05N_3	AE26	I/O
3	IO_L05P_3	IO_L05P_3	AF27	I/O
3	IO_L06N_3	IO_L06N_3	AE29	I/O
3	IO_L06P_3	IO_L06P_3	AE28	I/O
3	IO_L07N_3	IO_L07N_3	AD28	I/O
3	IO_L07P_3	IO_L07P_3	AD27	I/O
3	IO_L08N_3	IO_L08N_3	AD30	I/O
3	IO_L08P_3	IO_L08P_3	AD29	I/O
3	IO_L09N_3	IO_L09N_3	AC24	I/O
3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	AD25	VREF
3	IO_L10N_3	IO_L10N_3	AC26	I/O
3	IO_L10P_3	IO_L10P_3	AC25	I/O
3	IO_L11N_3	IO_L11N_3	AC28	I/O
3	IO_L11P_3	IO_L11P_3	AC27	I/O
3	IO_L13N_3/VREF_3	IO_L13N_3/VREF_3	AC30	VREF
3	IO_L13P_3	IO_L13P_3	AC29	I/O
3	IO_L14N_3	IO_L14N_3	AB27	I/O
3	IO_L14P_3	IO_L14P_3	AB26	I/O
3	IO_L15N_3	IO_L15N_3	AB30	I/O
3	IO_L15P_3	IO_L15P_3	AB29	I/O
3	IO_L16N_3	IO_L16N_3	AA22	I/O
3	IO_L16P_3	IO_L16P_3	AB23	I/O
3	IO_L17N_3	IO_L17N_3	AA25	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	AA24	VREF
3	IO_L19N_3	IO_L19N_3	AA29	I/O
3	IO_L19P_3	IO_L19P_3	AA28	I/O
3	IO_L20N_3	IO_L20N_3	Y21	I/O
3	IO_L20P_3	IO_L20P_3	AA21	I/O
3	IO_L21N_3	IO_L21N_3	Y24	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
3	IO_L21P_3	IO_L21P_3	Y23	I/O
3	IO_L22N_3	IO_L22N_3	Y26	I/O
3	IO_L22P_3	IO_L22P_3	Y25	I/O
3	IO_L23N_3	IO_L23N_3	Y28	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	Y27	VREF
3	IO_L24N_3	IO_L24N_3	Y30	I/O
3	IO_L24P_3	IO_L24P_3	Y29	I/O
3	IO_L26N_3	IO_L26N_3	W30	I/O
3	IO_L26P_3	IO_L26P_3	W29	I/O
3	IO_L27N_3	IO_L27N_3	V21	I/O
3	IO_L27P_3	IO_L27P_3	W21	I/O
3	IO_L28N_3	IO_L28N_3	V23	I/O
3	IO_L28P_3	IO_L28P_3	V22	I/O
3	IO_L29N_3	IO_L29N_3	V25	I/O
3	IO_L29P_3	IO_L29P_3	W26	I/O
3	IO_L31N_3	IO_L31N_3	V30	I/O
3	IO_L31P_3	IO_L31P_3	V29	I/O
3	IO_L32N_3	IO_L32N_3	U22	I/O
3	IO_L32P_3	IO_L32P_3	U21	I/O
3	IO_L33N_3	IO_L33N_3	U25	I/O
3	IO_L33P_3	IO_L33P_3	U24	I/O
3	IO_L34N_3	IO_L34N_3	U29	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	U28	VREF
3	IO_L35N_3	IO_L35N_3	T22	I/O
3	IO_L35P_3	IO_L35P_3	T21	I/O
3	IO_L37N_3	IO_L37N_3	T24	I/O
3	IO_L37P_3	IO_L37P_3	T23	I/O
3	IO_L38N_3	IO_L38N_3	T26	I/O
3	IO_L38P_3	IO_L38P_3	T25	I/O
3	IO_L39N_3	IO_L39N_3	T28	I/O
3	IO_L39P_3	IO_L39P_3	T27	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	T30	VREF
3	IO_L40P_3	IO_L40P_3	T29	I/O
3	N.C. (◆)	IO_L46N_3	W23	I/O
3	N.C. (◆)	IO_L46P_3	W22	I/O
3	N.C. (◆)	IO_L47N_3	W25	I/O
3	N.C. (◆)	IO_L47P_3	W24	I/O
3	N.C. (◆)	IO_L48N_3	W28	I/O
3	N.C. (◆)	IO_L48P_3	W27	I/O
3	N.C. (◆)	IO_L50N_3	V27	I/O

FG900 Footprint

Left Half of FG900 Package (Top View)

XC3S2000
(565 max. user I/O)

481 **I/O:** Unrestricted, general-purpose user I/O

48 **VREF:** User I/O or input voltage reference for bank

68 **N.C.:** Unconnected pins for XC3S2000 (◆)

XC3S4000, XC3S5000
(633 max user I/O)

549 **I/O:** Unrestricted, general-purpose user I/O

48 **VREF:** User I/O or input voltage reference for bank

0 **N.C.:** No unconnected pins in this package

All devices

12 **DUAL:** Configuration pin, then possible user I/O

8 **GCLK:** User I/O or global clock buffer input

16 **DCI:** User I/O or reference resistor input for bank

7 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

32 **VCCINT:** Internal core voltage supply (+1.2V)

80 **VCCO:** Output voltage supply for bank

24 **VCCAUX:** Auxiliary voltage supply (+2.5V)

120 **GND:** Ground

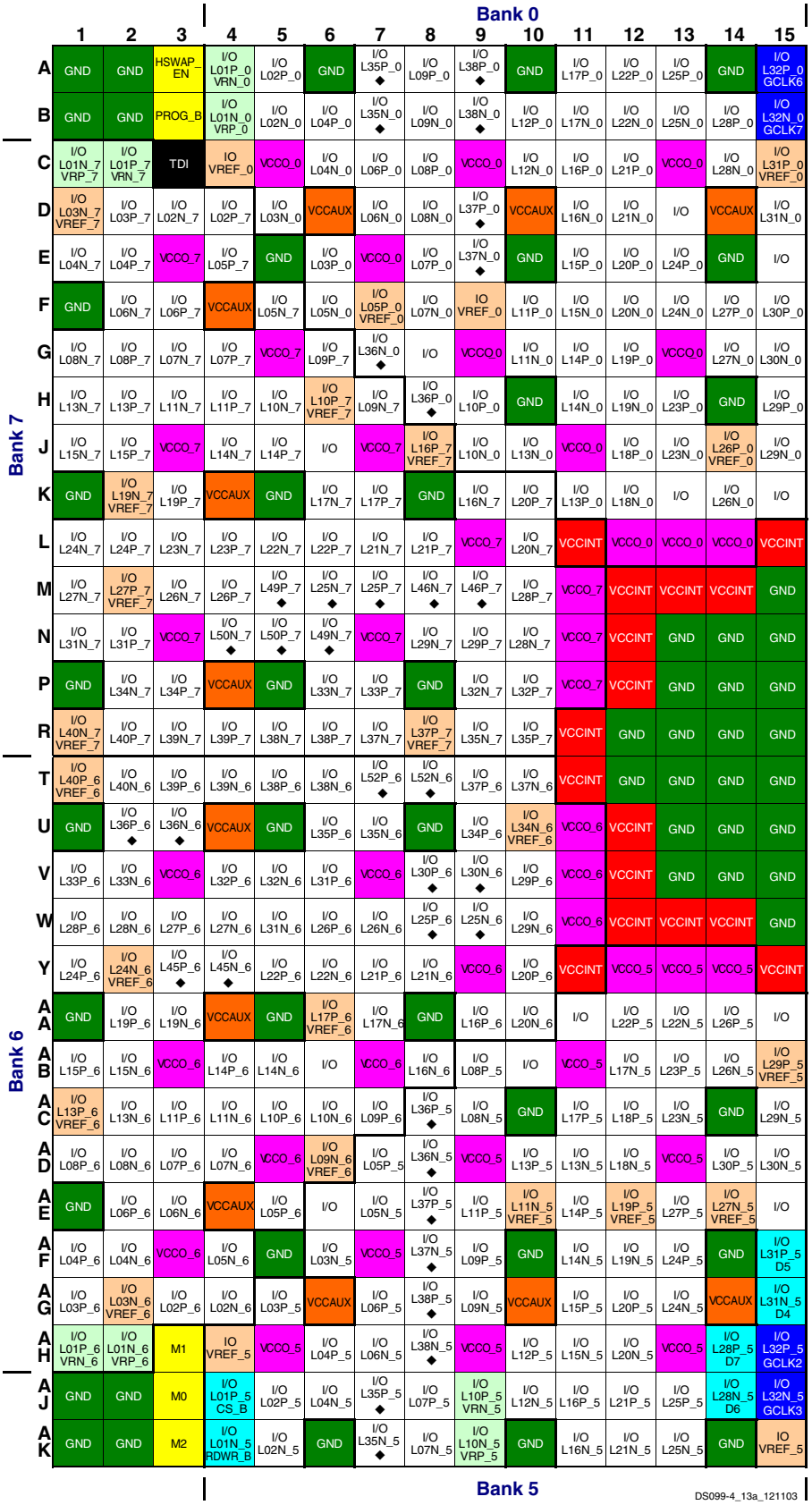

Figure 55: **FG900 Package Footprint (Top View)**

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
1	IO_L27N_1	IO_L27N_1	F19	I/O
1	IO_L27P_1	IO_L27P_1	G19	I/O
1	IO_L28N_1	IO_L28N_1	B19	I/O
1	IO_L28P_1	IO_L28P_1	C19	I/O
1	IO_L29N_1	IO_L29N_1	J18	I/O
1	IO_L29P_1	IO_L29P_1	K18	I/O
1	IO_L30N_1	IO_L30N_1	G18	I/O
1	IO_L30P_1	IO_L30P_1	H18	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D18	VREF
1	IO_L31P_1	IO_L31P_1	E18	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B18	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C18	GCLK
1	N.C. (◆)	IO_L33N_1	C28	I/O
1	N.C. (◆)	IO_L33P_1	D28	I/O
1	N.C. (◆)	IO_L34N_1	A28	I/O
1	N.C. (◆)	IO_L34P_1	B28	I/O
1	N.C. (◆)	IO_L35N_1	J24	I/O
1	N.C. (◆)	IO_L35P_1	K24	I/O
1	N.C. (◆)	IO_L36N_1	F24	I/O
1	N.C. (◆)	IO_L36P_1	G24	I/O
1	IO_L37N_1	IO_L37N_1	J20	I/O
1	IO_L37P_1	IO_L37P_1	K20	I/O
1	IO_L38N_1	IO_L38N_1	F20	I/O
1	IO_L38P_1	IO_L38P_1	G20	I/O
1	IO_L39N_1	IO_L39N_1	C20	I/O
1	IO_L39P_1	IO_L39P_1	D20	I/O
1	IO_L40N_1	IO_L40N_1	A20	I/O
1	IO_L40P_1	IO_L40P_1	B20	I/O
1	VCCO_1	VCCO_1	B22	VCCO
1	VCCO_1	VCCO_1	C27	VCCO
1	VCCO_1	VCCO_1	C31	VCCO
1	VCCO_1	VCCO_1	D19	VCCO
1	VCCO_1	VCCO_1	D24	VCCO
1	VCCO_1	VCCO_1	F22	VCCO
1	VCCO_1	VCCO_1	G27	VCCO
1	VCCO_1	VCCO_1	H20	VCCO
1	VCCO_1	VCCO_1	H24	VCCO
1	VCCO_1	VCCO_1	M19	VCCO
1	VCCO_1	VCCO_1	M20	VCCO
1	VCCO_1	VCCO_1	M21	VCCO

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
2	IO_L19N_2	IO_L19N_2	M29	I/O
2	IO_L19P_2	IO_L19P_2	M30	I/O
2	IO_L20N_2	IO_L20N_2	M31	I/O
2	IO_L20P_2	IO_L20P_2	M32	I/O
2	IO_L21N_2	IO_L21N_2	M26	I/O
2	IO_L21P_2	IO_L21P_2	N25	I/O
2	IO_L22N_2	IO_L22N_2	N27	I/O
2	IO_L22P_2	IO_L22P_2	N28	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2VREF_2	N31	VREF
2	IO_L23P_2	IO_L23P_2	N32	I/O
2	IO_L24N_2	IO_L24N_2	N24	I/O
2	IO_L24P_2	IO_L24P_2	P24	I/O
2	IO_L26N_2	IO_L26N_2	P29	I/O
2	IO_L26P_2	IO_L26P_2	P30	I/O
2	IO_L27N_2	IO_L27N_2	P31	I/O
2	IO_L27P_2	IO_L27P_2	P32	I/O
2	IO_L28N_2	IO_L28N_2	P33	I/O
2	IO_L28P_2	IO_L28P_2	P34	I/O
2	IO_L29N_2	IO_L29N_2	R24	I/O
2	IO_L29P_2	IO_L29P_2	R25	I/O
2	IO_L30N_2	IO_L30N_2	R28	I/O
2	IO_L30P_2	IO_L30P_2	R29	I/O
2	IO_L31N_2	IO_L31N_2	R31	I/O
2	IO_L31P_2	IO_L31P_2	R32	I/O
2	IO_L32N_2	IO_L32N_2	R33	I/O
2	IO_L32P_2	IO_L32P_2	R34	I/O
2	IO_L33N_2	IO_L33N_2	R26	I/O
2	IO_L33P_2	IO_L33P_2	T25	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	T28	VREF
2	IO_L34P_2	IO_L34P_2	T29	I/O
2	IO_L35N_2	IO_L35N_2	T32	I/O
2	IO_L35P_2	IO_L35P_2	T33	I/O
2	IO_L37N_2	IO_L37N_2	U27	I/O
2	IO_L37P_2	IO_L37P_2	U28	I/O
2	IO_L38N_2	IO_L38N_2	U29	I/O
2	IO_L38P_2	IO_L38P_2	U30	I/O
2	IO_L39N_2	IO_L39N_2	U31	I/O
2	IO_L39P_2	IO_L39P_2	U32	I/O
2	IO_L40N_2	IO_L40N_2	U33	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	U34	VREF

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L24P_3	IO_L24P_3	AC26	I/O
3	IO_L26N_3	IO_L26N_3	AA28	I/O
3	IO_L26P_3	IO_L26P_3	AA27	I/O
3	IO_L27N_3	IO_L27N_3	AA30	I/O
3	IO_L27P_3	IO_L27P_3	AA29	I/O
3	IO_L28N_3	IO_L28N_3	AA32	I/O
3	IO_L28P_3	IO_L28P_3	AA31	I/O
3	IO_L29N_3	IO_L29N_3	AA34	I/O
3	IO_L29P_3	IO_L29P_3	AA33	I/O
3	IO_L30N_3	IO_L30N_3	Y29	I/O
3	IO_L30P_3	IO_L30P_3	Y28	I/O
3	IO_L31N_3	IO_L31N_3	Y32	I/O
3	IO_L31P_3	IO_L31P_3	Y31	I/O
3	IO_L32N_3	IO_L32N_3	Y34	I/O
3	IO_L32P_3	IO_L32P_3	Y33	I/O
3	IO_L33N_3	IO_L33N_3	W25	I/O
3	IO_L33P_3	IO_L33P_3	Y26	I/O
3	IO_L34N_3	IO_L34N_3	W29	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	W28	VREF
3	IO_L35N_3	IO_L35N_3	W33	I/O
3	IO_L35P_3	IO_L35P_3	W32	I/O
3	IO_L37N_3	IO_L37N_3	V28	I/O
3	IO_L37P_3	IO_L37P_3	V27	I/O
3	IO_L38N_3	IO_L38N_3	V30	I/O
3	IO_L38P_3	IO_L38P_3	V29	I/O
3	IO_L39N_3	IO_L39N_3	V32	I/O
3	IO_L39P_3	IO_L39P_3	V31	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	V34	VREF
3	IO_L40P_3	IO_L40P_3	V33	I/O
3	N.C. (◆)	IO_L41N_3	AH32	I/O
3	N.C. (◆)	IO_L41P_3	AH31	I/O
3	N.C. (◆)	IO_L44N_3	AD29	I/O
3	N.C. (◆)	IO_L44P_3	AD28	I/O
3	IO_L45N_3	IO_L45N_3	AC34	I/O
3	IO_L45P_3	IO_L45P_3	AC33	I/O
3	IO_L46N_3	IO_L46N_3	AB28	I/O
3	IO_L46P_3	IO_L46P_3	AB27	I/O
3	IO_L47N_3	IO_L47N_3	AB32	I/O
3	IO_L47P_3	IO_L47P_3	AB31	I/O
3	IO_L48N_3	IO_L48N_3	AA24	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
5	IO_L24P_5	IO_L24P_5	AH15	I/O
5	IO_L25N_5	IO_L25N_5	AM15	I/O
5	IO_L25P_5	IO_L25P_5	AL15	I/O
5	IO_L26N_5	IO_L26N_5	AP15	I/O
5	IO_L26P_5	IO_L26P_5	AN15	I/O
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	AJ16	VREF
5	IO_L27P_5	IO_L27P_5	AH16	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	AN16	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	AM16	DUAL
5	IO_L29N_5	IO_L29N_5	AF17	I/O
5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	AE17	VREF
5	IO_L30N_5	IO_L30N_5	AH17	I/O
5	IO_L30P_5	IO_L30P_5	AG17	I/O
5	IO_L31N_5/D4	IO_L31N_5/D4	AL17	DUAL
5	IO_L31P_5/D5	IO_L31P_5/D5	AK17	DUAL
5	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	AN17	GCLK
5	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	AM17	GCLK
5	N.C. (◆)	IO_L33N_5	AM7	I/O
5	N.C. (◆)	IO_L33P_5	AL7	I/O
5	N.C. (◆)	IO_L34N_5	AP7	I/O
5	N.C. (◆)	IO_L34P_5	AN7	I/O
5	IO_L35N_5	IO_L35N_5	AL8	I/O
5	IO_L35P_5	IO_L35P_5	AK8	I/O
5	IO_L36N_5	IO_L36N_5	AP8	I/O
5	IO_L36P_5	IO_L36P_5	AN8	I/O
5	IO_L37N_5	IO_L37N_5	AJ9	I/O
5	IO_L37P_5	IO_L37P_5	AH9	I/O
5	IO_L38N_5	IO_L38N_5	AM9	I/O
5	IO_L38P_5	IO_L38P_5	AL9	I/O
5	N.C. (◆)	IO_L39N_5	AF11	I/O
5	N.C. (◆)	IO_L39P_5	AE11	I/O
5	N.C. (◆)	IO_L40N_5	AJ11	I/O
5	N.C. (◆)	IO_L40P_5	AH11	I/O
5	VCCO_5	VCCO_5	AC13	VCCO
5	VCCO_5	VCCO_5	AC14	VCCO
5	VCCO_5	VCCO_5	AC15	VCCO
5	VCCO_5	VCCO_5	AC16	VCCO
5	VCCO_5	VCCO_5	AG11	VCCO
5	VCCO_5	VCCO_5	AG15	VCCO
5	VCCO_5	VCCO_5	AH8	VCCO

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
6	IO_L37N_6	IO_L37N_6	W3	I/O
6	IO_L37P_6	IO_L37P_6	W2	I/O
6	IO_L38N_6	IO_L38N_6	V6	I/O
6	IO_L38P_6	IO_L38P_6	V5	I/O
6	IO_L39N_6	IO_L39N_6	V4	I/O
6	IO_L39P_6	IO_L39P_6	V3	I/O
6	IO_L40N_6	IO_L40N_6	V2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	V1	VREF
6	N.C. (◆)	IO_L41N_6	AH4	I/O
6	N.C. (◆)	IO_L41P_6	AH3	I/O
6	N.C. (◆)	IO_L44N_6	AD7	I/O
6	N.C. (◆)	IO_L44P_6	AD6	I/O
6	IO_L45N_6	IO_L45N_6	AC4	I/O
6	IO_L45P_6	IO_L45P_6	AC3	I/O
6	N.C. (◆)	IO_L46N_6	AA10	I/O
6	N.C. (◆)	IO_L46P_6	AA9	I/O
6	IO_L48N_6	IO_L48N_6	Y7	I/O
6	IO_L48P_6	IO_L48P_6	Y6	I/O
6	N.C. (◆)	IO_L49N_6	W11	I/O
6	N.C. (◆)	IO_L49P_6	V11	I/O
6	IO_L52N_6	IO_L52N_6	V8	I/O
6	IO_L52P_6	IO_L52P_6	V7	I/O
6	VCCO_6	VCCO_6	AA12	VCCO
6	VCCO_6	VCCO_6	AB12	VCCO
6	VCCO_6	VCCO_6	AB2	VCCO
6	VCCO_6	VCCO_6	AB6	VCCO
6	VCCO_6	VCCO_6	AD4	VCCO
6	VCCO_6	VCCO_6	AD8	VCCO
6	VCCO_6	VCCO_6	AG3	VCCO
6	VCCO_6	VCCO_6	AG7	VCCO
6	VCCO_6	VCCO_6	AL3	VCCO
6	VCCO_6	VCCO_6	W12	VCCO
6	VCCO_6	VCCO_6	W4	VCCO
6	VCCO_6	VCCO_6	Y12	VCCO
6	VCCO_6	VCCO_6	Y8	VCCO
7	IO	IO	G1	I/O
7	IO	IO	G2	I/O
7	IO	IO	U10	I/O
7	IO	IO	U9	I/O
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	C1	DCI

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	GND	GND	AA18	GND
N/A	GND	GND	AA19	GND
N/A	GND	GND	AA20	GND
N/A	GND	GND	AA21	GND
N/A	GND	GND	AB1	GND
N/A	GND	GND	AB17	GND
N/A	GND	GND	AB18	GND
N/A	GND	GND	AB26	GND
N/A	GND	GND	AB30	GND
N/A	GND	GND	AB34	GND
N/A	GND	GND	AB5	GND
N/A	GND	GND	AB9	GND
N/A	GND	GND	AD3	GND
N/A	GND	GND	AD32	GND
N/A	GND	GND	AE10	GND
N/A	GND	GND	AE25	GND
N/A	GND	GND	AF1	GND
N/A	GND	GND	AF13	GND
N/A	GND	GND	AF16	GND
N/A	GND	GND	AF19	GND
N/A	GND	GND	AF22	GND
N/A	GND	GND	AF30	GND
N/A	GND	GND	AF34	GND
N/A	GND	GND	AF5	GND
N/A	GND	GND	AH28	GND
N/A	GND	GND	AH7	GND
N/A	GND	GND	AK1	GND
N/A	GND	GND	AK13	GND
N/A	GND	GND	AK16	GND
N/A	GND	GND	AK19	GND
N/A	GND	GND	AK22	GND
N/A	GND	GND	AK26	GND
N/A	GND	GND	AK30	GND
N/A	GND	GND	AK34	GND
N/A	GND	GND	AK5	GND
N/A	GND	GND	AK9	GND
N/A	GND	GND	AM11	GND
N/A	GND	GND	AM24	GND
N/A	GND	GND	AM3	GND
N/A	GND	GND	AM32	GND

FG1156 Footprint

Top Left Corner of FG1156 Package (Top View)

XC3S4000 (712 max. user I/O)

621 **I/O:** Unrestricted, general-purpose user I/O

55 **VREF:** User I/O or input voltage reference for bank

73 **N.C.:** Unconnected pins for XC3S4000 (◆)

XC3S5000 (784 max. user I/O)

692 **I/O:** Unrestricted, general-purpose user I/O

56 **VREF:** User I/O or input voltage reference for bank

1 **N.C.:** Unconnected pins for XC3S5000 (■)

Bank 0

Bank 7

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	GND	GND	I/O L01P_0 VRN_0	I/O L02P_0	GND	I/O L05P_0 VREF_0	I/O L34P_0 ◆	I/O L36P_0	GND	I/O L38P_0	I/O L40P_0 ◆	I/O L15P_0	GND	I/O L22P_0	I/O L26P_0 VREF_0	GND	I/O L32P_0 GCLK6
B	GND	GND	I/O L01N_0 VRP_0	I/O L02N_0	I/O L03P_0	I/O L05N_0	I/O L34N_0 ◆	I/O L36N_0	I/O	I/O L38N_0	I/O L40N_0 ◆	I/O L15N_0	VCCO_0	I/O L22N_0	I/O L26N_0	I/O L28P_0	I/O L32N_0 GCLK7
C	I/O L01N_7 VRP_7	I/O L01P_7 VRN_7	GND	VCCO_0	I/O L03N_0	I/O L04P_0	I/O L33P_0 ◆	VCCO_0	I/O L08P_0	I/O L37P_0	GND	I/O L14P_0	I/O L17P_0	I/O L21P_0	I/O L25P_0	I/O L28N_0	I/O L31P_0 VREF_0
D	I/O L02N_7	I/O L02P_7	VCCO_7	PROG_B	IO VREF_0	I/O L04N_0	I/O L33N_0 ◆	I/O L35P_0	I/O L08N_0	I/O L37N_0	VCCO_0	I/O L14N_0	I/O L17N_0	I/O L21N_0	I/O L25N_0	VCCO_0	I/O L31N_0
E	GND	I/O L03N_7 VREF_7	I/O L03P_7	TDI	GND	VCCAUX	I/O L06P_0	I/O L35N_0	GND	IO VREF_0	VCCAUX	I/O L13P_0	GND	I/O L20P_0	VCCAUX	GND	I/O
F	I/O L05N_7	I/O L05P_7	I/O L04N_7	I/O L04P_7	VCCAUX	I/O	I/O L06N_0	I/O	I/O L07P_0	I/O L10P_0	I/O L39P_0 ◆	I/O L13N_0	VCCO_0	I/O L20N_0	I/O L24P_0	I/O L27P_0	I/O L30P_0
G	I/O	I/O	I/O L41N_7 ◆	I/O L41P_7 ◆	I/O L06N_7	I/O L06P_7	GND	VCCO_0	I/O L07N_0	I/O L10N_0	I/O L39N_0 ◆	I/O	I/O L16P_0	I/O L19P_0	I/O L24N_0	I/O L27N_0	I/O L30N_0
H	I/O L08N_7	I/O L08P_7	VCCO_7	I/O L10P_7 VREF_7	I/O L07N_7	I/O L07P_7	VCCO_7	I/O	I/O	I/O L09P_0	VCCO_0	I/O L12P_0	I/O L16N_0	I/O L19N_0	VCCO_0	VCCAUX	I/O L29P_0
J	GND	I/O L11N_7	I/O L11P_7	I/O L10N_7	GND	I/O L09N_7	I/O L09P_7	I/O L12P_7	I/O ◆	I/O L09N_0	I/O	I/O L12N_0	GND	IO VREF_0	I/O L23P_0	GND	I/O L29N_0
K	I/O L16N_7	I/O L16P_7 VREF_7	I/O L15N_7	I/O L15P_7	I/O L14N_7	I/O L14P_7	I/O L13N_7	I/O L13P_7	I/O L12N_7	GND	I/O ◆	I/O L11P_0	I/O	I/O L18P_0	I/O L23N_0	I/O	I/O
L	I/O L19N_7 VREF_7	I/O L19P_7	GND	VCCO_7	VCCAUX	I/O L44N_7 ◆	I/O L44P_7 ◆	VCCO_7	I/O L17N_7	I/O L17P_7	HSWAP_ EN	I/O L11N_0	I/O	I/O L18N_0	IO VREF_0	I/O	I/O
M	I/O L45N_7	I/O L45P_7	I/O L23N_7	I/O L23P_7	I/O L22N_7	I/O L22P_7	I/O L21N_7	I/O L21P_7	I/O L24P_7	I/O L20N_7	I/O L20P_7	VCCINT	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCINT
N	GND	VCCO_7	I/O L25N_7	I/O L25P_7	GND	VCCO_7	I/O L46N_7	I/O L46P_7	GND	I/O L24N_7	I/O L26P_7	VCCO_7	VCCINT	VCCINT	VCCINT	VCCINT	GND
P	I/O L49N_7	I/O L49P_7	I/O L29N_7	I/O L29P_7	I/O L28N_7	I/O L28P_7	I/O L27N_7	I/O L27P_7 VREF_7	I/O L47N_7 ◆	I/O L47P_7 ◆	I/O L26N_7	VCCO_7	VCCINT	GND	GND	GND	GND
R	I/O L32N_7	I/O L32P_7	I/O L31N_7	I/O L31P_7	VCCAUX	I/O L30N_7	I/O L30P_7	VCCO_7	I/O L33P_7	I/O L50N_7	I/O L50P_7	VCCO_7	VCCINT	GND	GND	GND	GND
T	GND	I/O L35N_7	I/O L35P_7	VCCO_7	GND	I/O L34N_7	I/O L34P_7	VCCAUX	GND	I/O L33N_7	I/O L51P_7 ◆	VCCO_7	VCCINT	GND	GND	GND	GND
U	I/O L40N_7 VREF_7	I/O L40P_7	I/O L39N_7	I/O L39P_7	I/O L38N_7	I/O L38P_7	I/O L37N_7	I/O L37P_7 VREF_7	I/O	I/O	I/O L51N_7 ◆	VCCINT	GND	GND	GND	GND	GND

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Figure 57: **FG1156 Package Footprint (Top View)**