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### Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### Details

Product Status	Active
Number of LABs/CLBs	480
Number of Logic Elements/Cells	4320
Total RAM Bits	221184
Number of I/O	173
Number of Gates	200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xc3s200-4ftg256i">https://www.e-xfl.com/product-detail/xilinx/xc3s200-4ftg256i</a>

## Interconnect

Interconnect (or routing) passes signals among the various functional elements of Spartan-3 devices. There are four kinds of interconnect: Long lines, Hex lines, Double lines, and Direct lines.

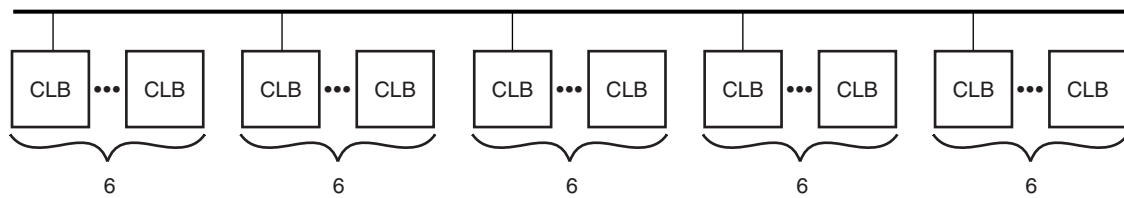
Long lines connect to one out of every six CLBs (see section [a] of Figure 25). Because of their low capacitance, these lines are well-suited for carrying high-frequency signals with minimal loading effects (e.g. skew). If all eight Global Clock Inputs are already committed and there remain additional clock signals to be assigned, Long lines serve as a good alternative.

Hex lines connect one out of every three CLBs (see section [b] of Figure 25). These lines fall between Long lines and Double lines in terms of capability: Hex lines approach the high-frequency characteristics of Long lines at the same time, offering greater connectivity.

Double lines connect to every other CLB (see section [c] of Figure 25). Compared to the types of lines already discussed, Double lines provide a higher degree of flexibility when making connections.

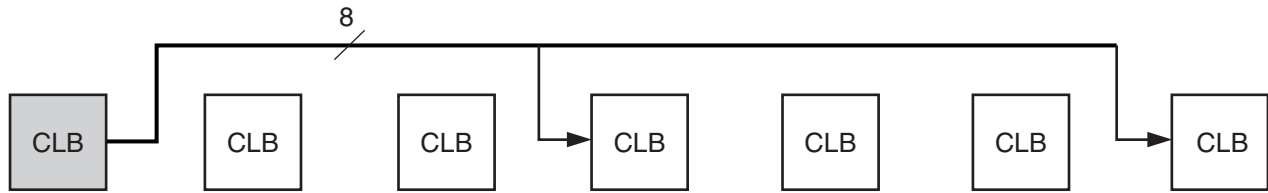
Direct lines afford any CLB direct access to neighboring CLBs (see section [d] of Figure 25). These lines are most often used to conduct a signal from a "source" CLB to a Double, Hex, or Long line and then from the longer interconnect back to a Direct line accessing a "destination" CLB.

For more details, refer to the "Using Interconnect" chapter in [UG331](#).



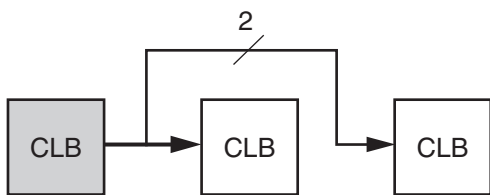
DS099-2\_19\_040103

(a) Long Lines



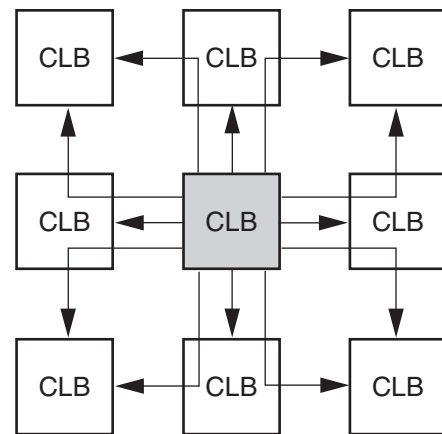
DS099-2\_20\_040103

(b) Hex Lines



DS099-2\_21\_040103

(c) Double Lines



DS099-2\_22\_040103

(d) Direct Lines

Figure 25: Types of Interconnect

**Table 30: Power Voltage Ramp Time Requirements**

Symbol	Description	Device	Package	Min	Max	Units
$T_{CCO}$	$V_{CCO}$ ramp time for all eight banks	All	All	No limit <sup>(4)</sup>	–	N/A
$T_{CCINT}$	$V_{CCINT}$ ramp time, only if $V_{CCINT}$ is last in three-rail power-on sequence	All	All	No limit	No limit <sup>(5)</sup>	N/A

**Notes:**

1. If a limit exists, this specification is based on characterization.
2. The ramp time is measured from 10% to 90% of the full nominal voltage swing for all I/O standards.
3. For information on power-on current needs, see [Power-On Behavior, page 54](#)
4. For mask revisions earlier than revision E (see [Mask and Fab Revisions, page 58](#)),  $T_{CCO}$  min is limited to 2.0 ms for the XC3S200 and XC3S400 devices in QFP packages, and limited to 0.6 ms for the XC3S200, XC3S400, XC3S1500, and XC3S4000 devices in the FT and FG packages.
5. For earlier device versions with the FQ fabrication/process code (see [Mask and Fab Revisions, page 58](#)),  $T_{CCINT}$  max is limited to 500  $\mu$ s.

**Table 31: Power Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
$V_{DRINT}$	$V_{CCINT}$ level required to retain RAM data	1.0	V
$V_{DRAUX}$	$V_{CCAUX}$ level required to retain RAM data	2.0	V

**Notes:**

1. RAM contents include data stored in CMOS configuration latches.
2. The level of the  $V_{CCO}$  supply has no effect on data retention.
3. If a brown-out condition occurs where  $V_{CCAUX}$  or  $V_{CCINT}$  drops below the retention voltage, then  $V_{CCAUX}$  or  $V_{CCINT}$  must drop below the minimum power-on reset voltage indicated in [Table 29](#) in order to clear out the device configuration content.

**Table 32: General Recommended Operating Conditions**

Symbol	Description	Min	Nom	Max	Units	
$T_J$	Junction temperature	Commercial	0	25	85	$^{\circ}$ C
		Industrial	–40	25	100	$^{\circ}$ C
$V_{CCINT}$	Internal supply voltage	1.140	1.200	1.260	V	
$V_{CCO}$ <sup>(1)</sup>	Output driver supply voltage	1.140	–	3.465	V	
$V_{CCAUX}$	Auxiliary supply voltage	2.375	2.500	2.625	V	
$\Delta V_{CCAUX}$ <sup>(2)</sup>	Voltage variance on $V_{CCAUX}$ when using a DCM	–	–	10	mV/ms	
$V_{IN}$ <sup>(3)</sup>	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND <sup>(4)(6)</sup>	$V_{CCO} = 3.3V$ , IO	–0.3	–	3.75	V
		$V_{CCO} = 3.3V$ , IO_Lxxy <sup>(7)</sup>	–0.3	–	3.75	V
		$V_{CCO} \leq 2.5V$ , IO	–0.3	–	$V_{CCO} + 0.3$ <sup>(4)</sup>	V
		$V_{CCO} \leq 2.5V$ , IO_Lxxy <sup>(7)</sup>	–0.3	–	$V_{CCO} + 0.3$ <sup>(4)</sup>	V
	Voltage applied to all Dedicated pins relative to GND <sup>(5)</sup>	–0.3	–	$V_{CCAUX} + 0.3$ <sup>(5)</sup>	V	

**Notes:**

1. The  $V_{CCO}$  range given here spans the lowest and highest operating voltages of all supported I/O standards. The recommended  $V_{CCO}$  range specific to each of the single-ended I/O standards is given in [Table 35](#), and that specific to the differential standards is given in [Table 37](#).
2. Only during DCM operation is it recommended that the rate of change of  $V_{CCAUX}$  not exceed 10 mV/ms.
3. Input voltages outside the recommended range are permissible provided that the  $I_{IK}$  input diode clamp diode rating is met. Refer to [Table 28](#).
4. Each of the User I/O and Dual-Purpose pins is associated with one of the  $V_{CCO}$  rails. Meeting the  $V_{IN}$  limit ensures that the internal diode junctions that exist between these pins and their associated  $V_{CCO}$  and GND rails do not turn on. The absolute maximum rating is provided in [Table 28](#).
5. All Dedicated pins (PROG\_B, DONE, TCK, TDI, TDO, and TMS) draw power from the  $V_{CCAUX}$  rail (2.5V). Meeting the  $V_{IN}$  max limit ensures that the internal diode junctions that exist between each of these pins and the  $V_{CCAUX}$  and GND rails do not turn on.
6. See [XAPP459, Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Generation FPGAs](#).
7. For single-ended signals that are placed on a differential-capable I/O,  $V_{IN}$  of –0.2V to –0.3V is supported but can cause increased leakage between the two pins. See the *Parasitic Leakage* section in [UG331, Spartan-3 Generation FPGA User Guide](#).

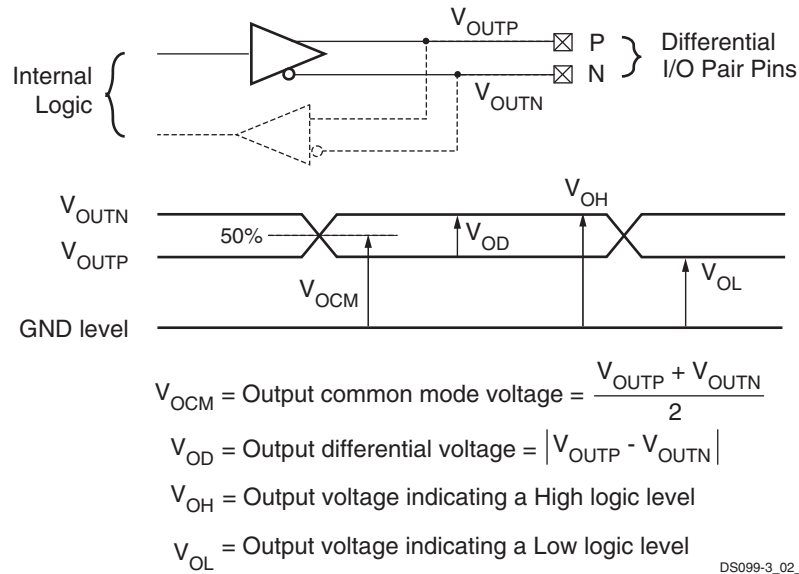


Figure 33: Differential Output Voltages

Table 38: DC Characteristics of User I/Os Using Differential Signal Standards

Signal Standard	Mask <sup>(3)</sup> Revision	$V_{OD}$			$V_{OCM}$			$V_{OH}$	$V_{OL}$
		Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LDT_25 (ULVDS_25)	All	430 <sup>(4)</sup>	600	670	0.495	0.600	0.715	0.71	0.50
LVDS_25	All	100	–	600	0.80	–	1.6	0.85	1.55
	'E'	200	–	500	1.0	–	1.5	1.10	1.40
BLVDS_25 <sup>(5)</sup>	All	250	350	450	–	1.20	–	–	–
LVDSEXT_25	All	100	–	600	0.80	–	1.6	0.85	1.55
	'E'	300	–	700	1.0	–	1.5	1.15	1.35
LVPECL_25 <sup>(5)</sup>	All	–	–	–	–	–	–	1.35	1.005
RSDS_25 <sup>(6)</sup>	All	100	–	600	0.80	–	1.6	0.85	1.55
	'E'	200	–	500	1.0	–	1.5	1.10	1.40
DIFF_HSTL_II_18	All	–	–	–	–	–	–	$V_{CC0} - 0.40$	0.40
DIFF_SSTL2_II	All	–	–	–	–	–	–	$V_{TT} + 0.80$	$V_{TT} - 0.80$

Notes:

- The numbers in this table are based on the conditions set forth in Table 32 and Table 37.
- Output voltage measurements for all differential standards are made with a termination resistor ( $R_T$ ) of 100Ω across the N and P pins of the differential signal pair.
- Mask revision E devices have tighter output ranges but can be used in any design that was in a previous revision. See Mask and Fab Revisions, page 58.
- This value must be compatible with the receiver to which the FPGA's output pair is connected.
- Each LVPECL\_25 or BLVDS\_25 output-pair requires three external resistors for proper output operation as shown in Figure 34. Each LVPECL\_25 or BLVDS\_25 input-pair uses a 100Ω termination resistor at the receiver.
- Only one of the differential standards RSDS\_25, LDT\_25, LVDS\_25, and LVDSEXT\_25 may be used for outputs within a bank. Each differential standard input-pair requires an external 100Ω termination resistor.

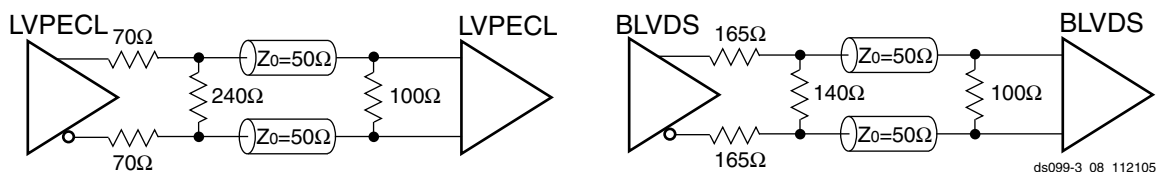


Figure 34: External Termination Required for LVPECL and BLVDS Output and Input

## Internal Logic Timing

Table 51: CLB Timing

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
<b>Clock-to-Output Times</b>						
$T_{CKO}$	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	–	0.63	–	0.72	ns
<b>Setup Times</b>						
$T_{AS}$	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.46	–	0.53	–	ns
$T_{DICK}$	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.27	–	1.57	–	ns
<b>Hold Times</b>						
$T_{AH}$	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	–	0	–	ns
$T_{CKDI}$	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0.25	–	0.29	–	ns
<b>Clock Timing</b>						
$T_{CH}$	CLB CLK signal High pulse width	0.69	$\infty$	0.79	$\infty$	ns
$T_{CL}$	CLB CLK signal Low pulse width	0.69	$\infty$	0.79	$\infty$	ns
$F_{TOG}$	Maximum toggle frequency (for export control)	–	725	–	630	MHz
<b>Propagation Times</b>						
$T_{ILO}$	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	–	0.53	–	0.61	ns
<b>Set/Reset Pulse Width</b>						
$T_{RPW\_CLB}$	The minimum allowable pulse width, High or Low, to the CLB's SR input	0.76	–	0.87	–	ns

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in [Table 32](#).
2. The timing shown is for SLICEM.
3. For minimums, use the values reported by the Xilinx timing analyzer.



Once the FPGA enters User mode after completing configuration, the DONE pin no longer drives the DONE pin Low. The bitstream generator option DonePin determines whether or not a pull-up resistor is present on the DONE pin to pull the pin to VCCAUX. If the pull-up resistor is eliminated, then the DONE pin must be pulled High using an external pull-up resistor or one of the FPGAs in the design must actively drive the DONE pin High via the DriveDone bitstream generator option.

The bitstream generator option DriveDone causes the FPGA to actively drive the DONE output High after configuration. This option should only be used in single-FPGA designs or on the last FPGA in a multi-FPGA daisy-chain.

By default, the bitstream generator software retains the pull-up resistor and does not actively drive the DONE pin as highlighted in Table 74, which shows the interaction of these bitstream options in single- and multi-FPGA designs.

**Table 74: DonePin and DriveDone Bitstream Option Interaction**

DonePin	DriveDone	Single- or Multi-FPGA Design	Comments
Pullnone	No	Single	External pull-up resistor, with value between 330Ω to 3.3kΩ, required on DONE.
Pullnone	No	Multi	External pull-up resistor, with value between 330Ω to 3.3kΩ, required on common node connecting to all DONE pins.
Pullnone	Yes	Single	OK, no external requirements.
Pullnone	Yes	Multi	DriveDone on last device in daisy-chain only. No external requirements.
Pullup	No	Single	OK, but pull-up on DONE pin has slow rise time. May require 330Ω pull-up resistor for high CCLK frequencies.
Pullup	No	Multi	External pull-up resistor, with value between 330Ω to 3.3kΩ, required on common node connecting to all DONE pins.
Pullup	Yes	Single	OK, no external requirements.
Pullup	Yes	Multi	DriveDone on last device in daisy-chain only. No external requirements.

**M2, M1, M0: Configuration Mode Selection**

The M2, M1, and M0 inputs select the FPGA configuration mode, as described in Table 75. The logic levels applied to the mode pins are sampled on the rising edge of INIT\_B.

**Table 75: Spartan-3 FPGA Mode Select Settings**

Configuration Mode	M2	M1	M0
Master Serial	0	0	0
Slave Serial	1	1	1
Master Parallel	0	1	1
Slave Parallel	1	1	0
JTAG	1	0	1
Reserved	0	0	1
Reserved	0	1	0
Reserved	1	0	0
After Configuration	X	X	X

**Notes:**

- 1. X = don't care, either 0 or 1.

Before and during configuration, the mode pins have an internal pull-up resistor to VCCAUX, regardless of the HSWAP\_EN pin. If the mode pins are unconnected, then the FPGA defaults to the Slave Serial configuration mode. After configuration successfully completes, any levels applied to these input are ignored. Furthermore, the bitstream generator options M0Pin, M1Pin, and M2Pin determines whether a pull-up resistor, pull-down resistor, or no resistor is present on its respective mode pin, M0, M1, or M2.

Table 79: Pin Behavior After Power-Up, During Configuration (Cont'd)

Pin Name	Configuration Mode Settings <M2:M1:M0>					Bitstream Configuration Option
	Serial Modes		SelectMap Parallel Modes		JTAG Mode <1:0:1>	
	Master <0:0:0>	Slave <1:1:1>	Master <0:1:1>	Slave <1:1:0>		
IO_Lxxy_#/D5			D5 (I/O)	D5 (I/O)		Persist UnusedPin
IO_Lxxy_#/D6			D6 (I/O)	D6 (I/O)		Persist UnusedPin
IO_Lxxy_#/D7			D7 (I/O)	D7 (I/O)		Persist UnusedPin
IO_Lxxy_#/CS_B			CS_B (I)	CS_B (I)		Persist UnusedPin
IO_Lxxy_#/RDWR_B			RDWR_B (I)	RDWR_B (I)		Persist UnusedPin
IO_Lxxy_#/BUSY/DOUT	DOUT (O)	DOUT (O)	BUSY (O)	BUSY (O)		Persist UnusedPin
<b>DUAL: Dual-purpose configuration pins (INIT_B has a pull-up resistor to VCCO_4 or VCCO_BOTTOM always active during configuration, regardless of HSWAP_EN pin)</b>						
IO_Lxxy_#/INIT_B	INIT_B (I/OD)	INIT_B (I/OD)	INIT_B (I/OD)	INIT_B (I/OD)		UnusedPin
<b>DCI: Digitally Controlled Impedance reference resistor input pins</b>						
IO_Lxxy_#/VRN_#						UnusedPin
IO/VRN_#						UnusedPin
IO_Lxxy_#/VRP_#						UnusedPin
IO/VRP_#						UnusedPin
<b>GCLK: Global clock buffer inputs</b>						
IO_Lxxy_#/GCLK0 through GCLK7						UnusedPin
<b>VREF: I/O bank input reference voltage pins</b>						
IO_Lxxy_#/VREF_#						UnusedPin
IO/VREF_#						UnusedPin
<b>CONFIG: Dedicated configuration pins (pull-up resistor to VCCAUX always active during configuration, regardless of HSWAP_EN pin)</b>						
CCLK	CCLK (I/O)	CCLK (I)	CCLK (I/O)	CCLK (I)		CclkPin ConfigRate
PROG_B	PROG_B (I) (pull-up)	PROG_B (I) (pull-up)	PROG_B (I) (pull-up)	PROG_B (I) (pull-up)	PROG_B (I), Via JPROG_B instruction	ProgPin
DONE	DONE (I/OD)	DONE (I/OD)	DONE (I/OD)	DONE (I/OD)	DONE (I/OD)	DriveDone DonePin DonePipe
M2	M2=0 (I)	M2=1 (I)	M2=0 (I)	M2=1 (I)	M2=1 (I)	M2Pin
M1	M1=0 (I)	M1=1 (I)	M1=1 (I)	M1=1 (I)	M1=0 (I)	M1Pin
M0	M0=0 (I)	M0=1 (I)	M0=1 (I)	M0=0 (I)	M0=1 (I)	M0Pin
HSWAP_EN	HSWAP_EN (I)	HSWAP_EN (I)	HSWAP_EN (I)	HSWAP_EN (I)	HSWAP_EN (I)	HswapenPin



Table 87: VQ100 Package Pinout (Cont'd)

Bank	XC3S50 XC3S200 Pin Name	VQ100 Pin Number	Type
VCCAUX	TDO	P76	JTAG
VCCAUX	TMS	P78	JTAG

### User I/Os by Bank

Table 88 indicates how the available user-I/O pins are distributed between the eight I/O banks on the VQ100 package.

Table 88: User I/Os Per Bank in VQ100 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	6	1	0	2	1	2
	1	7	2	0	2	1	2
Right	2	8	5	0	2	1	0
	3	8	5	0	2	1	0
Bottom	4	10	0	6	2	0	2
	5	8	0	6	0	0	2
Left	6	8	4	0	2	2	0
	7	8	5	0	2	1	0

## PQ208: 208-lead Plastic Quad Flat Pack

The 208-lead plastic quad flat package, PQ208, supports three different Spartan-3 devices, including the XC3S50, the XC3S200, and the XC3S400. The footprints for the XC3S200 and XC3S400 are identical, as shown in [Table 93](#) and [Figure 47](#). The XC3S50, however, has fewer I/O pins resulting in 17 unconnected pins on the PQ208 package, labeled as “N.C.” In [Table 93](#) and [Figure 47](#), these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in [Table 93](#) and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S50 pinout and the pinout for the XC3S200 and XC3S400, then that difference is highlighted in [Table 93](#). If the table entry is shaded grey, then there is an unconnected pin on the XC3S50 that maps to a user-I/O pin on the XC3S200 and XC3S400. If the table entry is shaded tan, then the unconnected pin on the XC3S50 maps to a VREF-type pin on the XC3S200 and XC3S400. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S50 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S50 device to an XC3S200 or XC3S400 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at [http://www.xilinx.com/support/documentation/data\\_sheets/s3\\_pin.zip](http://www.xilinx.com/support/documentation/data_sheets/s3_pin.zip)

### Pinout Table

Table 93: PQ208 Package Pinout

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
0	IO	IO	P189	I/O
0	IO	IO	P197	I/O
0	N.C. (◆)	IO/VREF_0	P200	VREF
0	IO/VREF_0	IO/VREF_0	P205	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	P204	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	P203	DCI
0	IO_L25N_0	IO_L25N_0	P199	I/O
0	IO_L25P_0	IO_L25P_0	P198	I/O
0	IO_L27N_0	IO_L27N_0	P196	I/O
0	IO_L27P_0	IO_L27P_0	P194	I/O
0	IO_L30N_0	IO_L30N_0	P191	I/O
0	IO_L30P_0	IO_L30P_0	P190	I/O
0	IO_L31N_0	IO_L31N_0	P187	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	P185	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	P184	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	P183	GCLK
0	VCCO_0	VCCO_0	P188	VCCO
0	VCCO_0	VCCO_0	P201	VCCO
1	IO	IO	P167	I/O
1	IO	IO	P175	I/O
1	IO	IO	P182	I/O
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	P162	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	P161	DCI

Table 93: PQ208 Package Pinout (Cont'd)

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
7	IO_L21N_7	IO_L21N_7	P13	I/O
7	IO_L21P_7	IO_L21P_7	P12	I/O
7	IO_L22N_7	IO_L22N_7	P16	I/O
7	IO_L22P_7	IO_L22P_7	P15	I/O
7	IO_L23N_7	IO_L23N_7	P19	I/O
7	IO_L23P_7	IO_L23P_7	P18	I/O
7	IO_L24N_7	IO_L24N_7	P21	I/O
7	IO_L24P_7	IO_L24P_7	P20	I/O
7	N.C. (◆)	IO_L39N_7	P24	I/O
7	N.C. (◆)	IO_L39P_7	P22	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	P27	VREF
7	IO_L40P_7	IO_L40P_7	P26	I/O
7	VCCO_7	VCCO_7	P6	VCCO
7	VCCO_7	VCCO_7	P23	VCCO
N/A	GND	GND	P1	GND
N/A	GND	GND	P186	GND
N/A	GND	GND	P195	GND
N/A	GND	GND	P202	GND
N/A	GND	GND	P163	GND
N/A	GND	GND	P170	GND
N/A	GND	GND	P179	GND
N/A	GND	GND	P134	GND
N/A	GND	GND	P145	GND
N/A	GND	GND	P151	GND
N/A	GND	GND	P157	GND
N/A	GND	GND	P112	GND
N/A	GND	GND	P118	GND
N/A	GND	GND	P129	GND
N/A	GND	GND	P82	GND
N/A	GND	GND	P91	GND
N/A	GND	GND	P99	GND
N/A	GND	GND	P105	GND
N/A	GND	GND	P53	GND
N/A	GND	GND	P59	GND
N/A	GND	GND	P66	GND
N/A	GND	GND	P75	GND
N/A	GND	GND	P30	GND
N/A	GND	GND	P41	GND
N/A	GND	GND	P47	GND
N/A	GND	GND	P8	GND

PQ208 Footprint

Left Half of Package (Top View)

XC3S50

(124 max. user I/O)

72 I/O: Unrestricted, general-purpose user I/O

16 VREF: User I/O or input voltage reference for bank

17 N.C.: Unconnected pins for XC3S50 (◆)

XC3S200, XC3S400

(141 max user I/O)

83 I/O: Unrestricted, general-purpose user I/O

22 VREF: User I/O or input voltage reference for bank

0 N.C.: No unconnected pins in this package

All devices

12 DUAL: Configuration pin, then possible user I/O

8 GCLK: User I/O or global clock buffer input

16 DCI: User I/O or reference resistor input for bank

7 CONFIG: Dedicated configuration pins

4 JTAG: Dedicated JTAG port pins

4 VCCINT: Internal core voltage supply (+1.2V)

12 VCCO: Output voltage supply for bank

8 VCCAUX: Auxiliary voltage supply (+2.5V)

28 GND: Ground

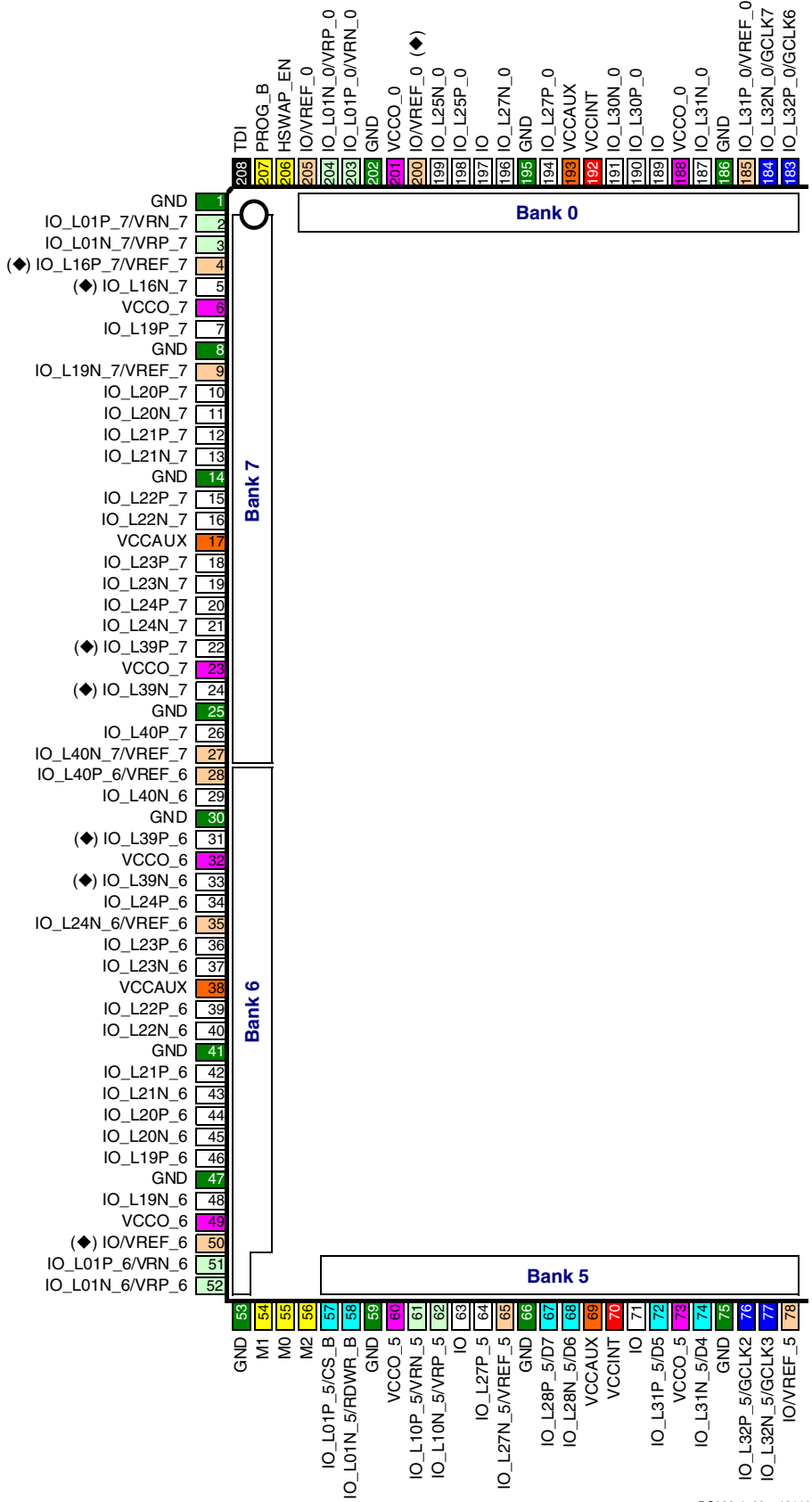


Figure 47: PQ208 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.

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Table 96: FT256 Package Pinout (Cont'd)

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
7	IO_L24P_7	G4	I/O
7	IO_L39N_7	H3	I/O
7	IO_L39P_7	H4	I/O
7	IO_L40N_7/VREF_7	H1	VREF
7	IO_L40P_7	G1	I/O
7	VCCO_7	G6	VCCO
7	VCCO_7	H5	VCCO
7	VCCO_7	H6	VCCO
N/A	GND	A1	GND
N/A	GND	A16	GND
N/A	GND	B2	GND
N/A	GND	B9	GND
N/A	GND	B15	GND
N/A	GND	F6	GND
N/A	GND	F11	GND
N/A	GND	G7	GND
N/A	GND	G8	GND
N/A	GND	G9	GND
N/A	GND	G10	GND
N/A	GND	H2	GND
N/A	GND	H7	GND
N/A	GND	H8	GND
N/A	GND	H9	GND
N/A	GND	H10	GND
N/A	GND	J7	GND
N/A	GND	J8	GND
N/A	GND	J9	GND
N/A	GND	J10	GND
N/A	GND	J15	GND
N/A	GND	K7	GND
N/A	GND	K8	GND
N/A	GND	K9	GND
N/A	GND	K10	GND
N/A	GND	L6	GND
N/A	GND	L11	GND
N/A	GND	R2	GND
N/A	GND	R8	GND
N/A	GND	R15	GND
N/A	GND	T1	GND

Table 100: FG456 Package Pinout (Cont'd)

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
0	N.C. (◆)	IO_L22N_0	E8	I/O
0	N.C. (◆)	IO_L22P_0	D8	I/O
0	IO_L24N_0	IO_L24N_0	B8	I/O
0	IO_L24P_0	IO_L24P_0	A8	I/O
0	IO_L25N_0	IO_L25N_0	F9	I/O
0	IO_L25P_0	IO_L25P_0	E9	I/O
0	IO_L27N_0	IO_L27N_0	B9	I/O
0	IO_L27P_0	IO_L27P_0	A9	I/O
0	IO_L28N_0	IO_L28N_0	F10	I/O
0	IO_L28P_0	IO_L28P_0	E10	I/O
0	IO_L29N_0	IO_L29N_0	C10	I/O
0	IO_L29P_0	IO_L29P_0	B10	I/O
0	IO_L30N_0	IO_L30N_0	F11	I/O
0	IO_L30P_0	IO_L30P_0	E11	I/O
0	IO_L31N_0	IO_L31N_0	D11	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C11	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B11	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A11	GCLK
0	VCCO_0	VCCO_0	C8	VCCO
0	VCCO_0	VCCO_0	F8	VCCO
0	VCCO_0	VCCO_0	G9	VCCO
0	VCCO_0	VCCO_0	G10	VCCO
0	VCCO_0	VCCO_0	G11	VCCO
1	IO	IO	A12	I/O
1	IO	IO	E16	I/O
1	IO	IO	F12	I/O
1	IO	IO	F13	I/O
1	IO	IO	F16	I/O
1	IO	IO	F17	I/O
1	IO/VREF_1	IO/VREF_1	E13	VREF
1	N.C. (◆)	IO/VREF_1	F14	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	C19	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B20	DCI
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	A19	VREF
1	IO_L06P_1	IO_L06P_1	B19	I/O
1	IO_L09N_1	IO_L09N_1	C18	I/O
1	IO_L09P_1	IO_L09P_1	D18	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	A18	VREF
1	IO_L10P_1	IO_L10P_1	B18	I/O
1	IO_L15N_1	IO_L15N_1	D17	I/O

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO_L30N_0	IO_L30N_0	G15	I/O
0	IO_L30P_0	IO_L30P_0	F15	I/O
0	IO_L31N_0	IO_L31N_0	D15	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C15	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B15	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A15	GCLK
0	N.C. (◆)	IO_L35N_0	B7	I/O
0	N.C. (◆)	IO_L35P_0	A7	I/O
0	N.C. (◆)	IO_L36N_0	G7	I/O
0	N.C. (◆)	IO_L36P_0	H8	I/O
0	N.C. (◆)	IO_L37N_0	E9	I/O
0	N.C. (◆)	IO_L37P_0	D9	I/O
0	N.C. (◆)	IO_L38N_0	B9	I/O
0	N.C. (◆)	IO_L38P_0	A9	I/O
0	VCCO_0	VCCO_0	C5	VCCO
0	VCCO_0	VCCO_0	E7	VCCO
0	VCCO_0	VCCO_0	C9	VCCO
0	VCCO_0	VCCO_0	G9	VCCO
0	VCCO_0	VCCO_0	J11	VCCO
0	VCCO_0	VCCO_0	L12	VCCO
0	VCCO_0	VCCO_0	C13	VCCO
0	VCCO_0	VCCO_0	G13	VCCO
0	VCCO_0	VCCO_0	L13	VCCO
0	VCCO_0	VCCO_0	L14	VCCO
1	IO	IO	E25	I/O
1	IO	IO	J21	I/O
1	IO	IO	K20	I/O
1	IO	IO	F18	I/O
1	IO	IO	F16	I/O
1	IO	IO	A16	I/O
1	IO/VREF_1	IO/VREF_1	J17	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	A27	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B27	DCI
1	IO_L02N_1	IO_L02N_1	D26	I/O
1	IO_L02P_1	IO_L02P_1	C27	I/O
1	IO_L03N_1	IO_L03N_1	A26	I/O
1	IO_L03P_1	IO_L03P_1	B26	I/O
1	IO_L04N_1	IO_L04N_1	B25	I/O
1	IO_L04P_1	IO_L04P_1	C25	I/O
1	IO_L05N_1	IO_L05N_1	F24	I/O

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
7	VCCO_7	VCCO_7	N3	VCCO
7	VCCO_7	VCCO_7	G5	VCCO
7	VCCO_7	VCCO_7	J7	VCCO
7	VCCO_7	VCCO_7	N7	VCCO
7	VCCO_7	VCCO_7	L9	VCCO
7	VCCO_7	VCCO_7	M11	VCCO
7	VCCO_7	VCCO_7	N11	VCCO
7	VCCO_7	VCCO_7	P11	VCCO
N/A	GND	GND	A1	GND
N/A	GND	GND	B1	GND
N/A	GND	GND	F1	GND
N/A	GND	GND	K1	GND
N/A	GND	GND	P1	GND
N/A	GND	GND	U1	GND
N/A	GND	GND	AA1	GND
N/A	GND	GND	AE1	GND
N/A	GND	GND	AJ1	GND
N/A	GND	GND	AK1	GND
N/A	GND	GND	A2	GND
N/A	GND	GND	B2	GND
N/A	GND	GND	AJ2	GND
N/A	GND	GND	E5	GND
N/A	GND	GND	K5	GND
N/A	GND	GND	P5	GND
N/A	GND	GND	U5	GND
N/A	GND	GND	AA5	GND
N/A	GND	GND	AF5	GND
N/A	GND	GND	A6	GND
N/A	GND	GND	AK6	GND
N/A	GND	GND	K8	GND
N/A	GND	GND	P8	GND
N/A	GND	GND	U8	GND
N/A	GND	GND	AA8	GND
N/A	GND	GND	A10	GND
N/A	GND	GND	E10	GND
N/A	GND	GND	H10	GND
N/A	GND	GND	AC10	GND
N/A	GND	GND	AF10	GND
N/A	GND	GND	AK10	GND
N/A	GND	GND	R12	GND



**Table 110: FG1156 Package Pinout (Cont'd)**

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
4	IO_L21N_4	IO_L21N_4	AL21	I/O
4	IO_L21P_4	IO_L21P_4	AM21	I/O
4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	AN21	VREF
4	IO_L22P_4	IO_L22P_4	AP21	I/O
4	IO_L23N_4	IO_L23N_4	AE20	I/O
4	IO_L23P_4	IO_L23P_4	AF20	I/O
4	IO_L24N_4	IO_L24N_4	AH20	I/O
4	IO_L24P_4	IO_L24P_4	AJ20	I/O
4	IO_L25N_4	IO_L25N_4	AL20	I/O
4	IO_L25P_4	IO_L25P_4	AM20	I/O
4	IO_L26N_4	IO_L26N_4	AN20	I/O
4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	AP20	VREF
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	AH19	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	AJ19	DUAL
4	IO_L28N_4	IO_L28N_4	AM19	I/O
4	IO_L28P_4	IO_L28P_4	AN19	I/O
4	IO_L29N_4	IO_L29N_4	AF18	I/O
4	IO_L29P_4	IO_L29P_4	AG18	I/O
4	IO_L30N_4/D2	IO_L30N_4/D2	AH18	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	AJ18	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	AL18	DUAL
4	IO_L31P_4/DOUT/BUSY	IO_L31P_4/DOUT/BUSY	AM18	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	AN18	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	AP18	GCLK
4	IO_L33N_4	IO_L33N_4	AL29	I/O
4	IO_L33P_4	IO_L33P_4	AM29	I/O
4	IO_L34N_4	IO_L34N_4	AN29	I/O
4	IO_L34P_4	IO_L34P_4	AP29	I/O
4	IO_L35N_4	IO_L35N_4	AJ28	I/O
4	IO_L35P_4	IO_L35P_4	AK28	I/O
4	N.C. (◆)	IO_L36N_4	AL28	I/O
4	N.C. (◆)	IO_L36P_4	AM28	I/O
4	N.C. (◆)	IO_L37N_4	AN28	I/O
4	N.C. (◆)	IO_L37P_4	AP28	I/O
4	IO_L38N_4	IO_L38N_4	AK27	I/O
4	IO_L38P_4	IO_L38P_4	AL27	I/O
4	N.C. (◆)	IO_L39N_4	AH24	I/O
4	N.C. (◆)	IO_L39P_4	AJ24	I/O
4	N.C. (◆)	IO_L40N_4	AN24	I/O
4	N.C. (◆)	IO_L40P_4	AP24	I/O

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
5	IO_L24P_5	IO_L24P_5	AH15	I/O
5	IO_L25N_5	IO_L25N_5	AM15	I/O
5	IO_L25P_5	IO_L25P_5	AL15	I/O
5	IO_L26N_5	IO_L26N_5	AP15	I/O
5	IO_L26P_5	IO_L26P_5	AN15	I/O
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	AJ16	VREF
5	IO_L27P_5	IO_L27P_5	AH16	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	AN16	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	AM16	DUAL
5	IO_L29N_5	IO_L29N_5	AF17	I/O
5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	AE17	VREF
5	IO_L30N_5	IO_L30N_5	AH17	I/O
5	IO_L30P_5	IO_L30P_5	AG17	I/O
5	IO_L31N_5/D4	IO_L31N_5/D4	AL17	DUAL
5	IO_L31P_5/D5	IO_L31P_5/D5	AK17	DUAL
5	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	AN17	GCLK
5	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	AM17	GCLK
5	N.C. (◆)	IO_L33N_5	AM7	I/O
5	N.C. (◆)	IO_L33P_5	AL7	I/O
5	N.C. (◆)	IO_L34N_5	AP7	I/O
5	N.C. (◆)	IO_L34P_5	AN7	I/O
5	IO_L35N_5	IO_L35N_5	AL8	I/O
5	IO_L35P_5	IO_L35P_5	AK8	I/O
5	IO_L36N_5	IO_L36N_5	AP8	I/O
5	IO_L36P_5	IO_L36P_5	AN8	I/O
5	IO_L37N_5	IO_L37N_5	AJ9	I/O
5	IO_L37P_5	IO_L37P_5	AH9	I/O
5	IO_L38N_5	IO_L38N_5	AM9	I/O
5	IO_L38P_5	IO_L38P_5	AL9	I/O
5	N.C. (◆)	IO_L39N_5	AF11	I/O
5	N.C. (◆)	IO_L39P_5	AE11	I/O
5	N.C. (◆)	IO_L40N_5	AJ11	I/O
5	N.C. (◆)	IO_L40P_5	AH11	I/O
5	VCCO_5	VCCO_5	AC13	VCCO
5	VCCO_5	VCCO_5	AC14	VCCO
5	VCCO_5	VCCO_5	AC15	VCCO
5	VCCO_5	VCCO_5	AC16	VCCO
5	VCCO_5	VCCO_5	AG11	VCCO
5	VCCO_5	VCCO_5	AG15	VCCO
5	VCCO_5	VCCO_5	AH8	VCCO

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
5	VCCO_5	VCCO_5	AJ13	VCCO
5	VCCO_5	VCCO_5	AL11	VCCO
5	VCCO_5	VCCO_5	AL16	VCCO
5	VCCO_5	VCCO_5	AM4	VCCO
5	VCCO_5	VCCO_5	AM8	VCCO
5	VCCO_5	VCCO_5	AN13	VCCO
6	IO	IO	AH1	I/O
6	IO	IO	AH2	I/O
6	IO	IO	V9	I/O
6	IO	IO	V10	I/O
6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	AM2	DCI
6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	AM1	DCI
6	IO_L02N_6	IO_L02N_6	AL2	I/O
6	IO_L02P_6	IO_L02P_6	AL1	I/O
6	IO_L03N_6/VREF_6	IO_L03N_6/VREF_6	AK3	VREF
6	IO_L03P_6	IO_L03P_6	AK2	I/O
6	IO_L04N_6	IO_L04N_6	AJ4	I/O
6	IO_L04P_6	IO_L04P_6	AJ3	I/O
6	IO_L05N_6	IO_L05N_6	AJ2	I/O
6	IO_L05P_6	IO_L05P_6	AJ1	I/O
6	IO_L06N_6	IO_L06N_6	AH6	I/O
6	IO_L06P_6	IO_L06P_6	AH5	I/O
6	IO_L07N_6	IO_L07N_6	AG6	I/O
6	IO_L07P_6	IO_L07P_6	AG5	I/O
6	IO_L08N_6	IO_L08N_6	AG2	I/O
6	IO_L08P_6	IO_L08P_6	AG1	I/O
6	IO_L09N_6/VREF_6	IO_L09N_6/VREF_6	AF7	VREF
6	IO_L09P_6	IO_L09P_6	AF6	I/O
6	IO_L10N_6	IO_L10N_6	AG4	I/O
6	IO_L10P_6	IO_L10P_6	AF4	I/O
6	IO_L11N_6	IO_L11N_6	AF3	I/O
6	IO_L11P_6	IO_L11P_6	AF2	I/O
6	IO_L12N_6	IO_L12N_6	AF8	I/O
6	IO_L12P_6	IO_L12P_6	AE9	I/O
6	IO_L13N_6	IO_L13N_6	AE8	I/O
6	IO_L13P_6/VREF_6	IO_L13P_6/VREF_6	AE7	VREF
6	IO_L14N_6	IO_L14N_6	AE6	I/O
6	IO_L14P_6	IO_L14P_6	AE5	I/O
6	IO_L15N_6	IO_L15N_6	AE4	I/O
6	IO_L15P_6	IO_L15P_6	AE3	I/O

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
6	IO_L16N_6	IO_L16N_6	AE2	I/O
6	IO_L16P_6	IO_L16P_6	AE1	I/O
6	IO_L17N_6	IO_L17N_6	AD10	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	AD9	VREF
6	IO_L19N_6	IO_L19N_6	AD2	I/O
6	IO_L19P_6	IO_L19P_6	AD1	I/O
6	IO_L20N_6	IO_L20N_6	AC11	I/O
6	IO_L20P_6	IO_L20P_6	AC10	I/O
6	IO_L21N_6	IO_L21N_6	AC8	I/O
6	IO_L21P_6	IO_L21P_6	AC7	I/O
6	IO_L22N_6	IO_L22N_6	AC6	I/O
6	IO_L22P_6	IO_L22P_6	AC5	I/O
6	IO_L23N_6	IO_L23N_6	AC2	I/O
6	IO_L23P_6	IO_L23P_6	AC1	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	AC9	VREF
6	IO_L24P_6	IO_L24P_6	AB10	I/O
6	IO_L25N_6	IO_L25N_6	AB8	I/O
6	IO_L25P_6	IO_L25P_6	AB7	I/O
6	IO_L26N_6	IO_L26N_6	AB4	I/O
6	IO_L26P_6	IO_L26P_6	AB3	I/O
6	IO_L27N_6	IO_L27N_6	AB11	I/O
6	IO_L27P_6	IO_L27P_6	AA11	I/O
6	IO_L28N_6	IO_L28N_6	AA8	I/O
6	IO_L28P_6	IO_L28P_6	AA7	I/O
6	IO_L29N_6	IO_L29N_6	AA6	I/O
6	IO_L29P_6	IO_L29P_6	AA5	I/O
6	IO_L30N_6	IO_L30N_6	AA4	I/O
6	IO_L30P_6	IO_L30P_6	AA3	I/O
6	IO_L31N_6	IO_L31N_6	AA2	I/O
6	IO_L31P_6	IO_L31P_6	AA1	I/O
6	IO_L32N_6	IO_L32N_6	Y11	I/O
6	IO_L32P_6	IO_L32P_6	Y10	I/O
6	IO_L33N_6	IO_L33N_6	Y4	I/O
6	IO_L33P_6	IO_L33P_6	Y3	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	Y2	VREF
6	IO_L34P_6	IO_L34P_6	Y1	I/O
6	IO_L35N_6	IO_L35N_6	Y9	I/O
6	IO_L35P_6	IO_L35P_6	W10	I/O
6	IO_L36N_6	IO_L36N_6	W7	I/O
6	IO_L36P_6	IO_L36P_6	W6	I/O

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	VCCINT	VCCINT	Y22	VCCINT
VCCAUX	CCLK	CCLK	AL31	CONFIG
VCCAUX	DONE	DONE	AD24	CONFIG
VCCAUX	HSWAP_EN	HSWAP_EN	L11	CONFIG
VCCAUX	M0	M0	AL4	CONFIG
VCCAUX	M1	M1	AK4	CONFIG
VCCAUX	M2	M2	AG8	CONFIG
VCCAUX	PROG_B	PROG_B	D4	CONFIG
VCCAUX	TCK	TCK	D31	JTAG
VCCAUX	TDI	TDI	E4	JTAG
VCCAUX	TDO	TDO	E31	JTAG
VCCAUX	TMS	TMS	H27	JTAG