AMD Xilinx - XC3S200-4PQ208I Datasheet

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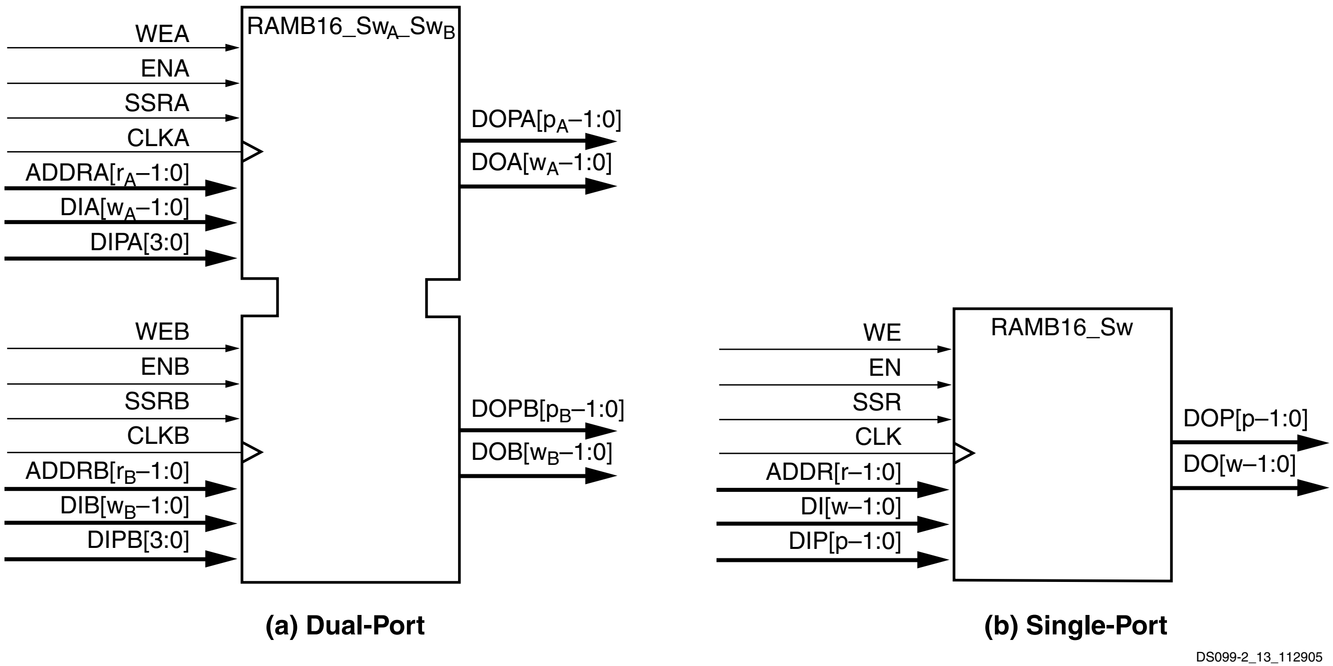
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	480
Number of Logic Elements/Cells	4320
Total RAM Bits	221184
Number of I/O	141
Number of Gates	200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s200-4pq208i



Notes:

1. w_A and w_B are integers representing the total data path width (i.e., data bits plus parity bits) at ports A and B, respectively.
2. p_A and p_B are integers that indicate the number of data path lines serving as parity bits.
3. r_A and r_B are integers representing the address bus width at ports A and B, respectively.
4. The control signals CLK, WE, EN, and SSR on both ports have the option of inverted polarity.

Figure 14: **Block RAM Primitives**

Table 13: **Block RAM Port Signals**

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Address Bus	ADDRA	ADDRB	Input	The Address Bus selects a memory location for read or write operations. The width (w) of the port's associated data path determines the number of available address lines (r). Whenever a port is enabled (ENA or ENB = High), address transitions must meet the data sheet setup and hold times with respect to the port clock (CLKA or CLKB). This requirement must be met, even if the RAM read output is of no interest.
Data Input Bus	DIA	DIB	Input	Data at the DI input bus is written to the addressed memory location addressed on an enabled active CLK edge. It is possible to configure a port's total data path width (w) to be 1, 2, 4, 9, 18, or 36 bits. This selection applies to both the DI and DO paths of a given port. Each port is independent. For a port assigned a width (w), the number of addressable locations is 16,384/(w-p) where "p" is the number of parity bits. Each memory location has a width of "w" (including parity bits). See the DIP signal description for more information of parity.
Parity Data Input(s)	DIPA	DIPB	Input	Parity inputs represent additional bits included in the data input path to support error detection. The number of parity bits "p" included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 14.

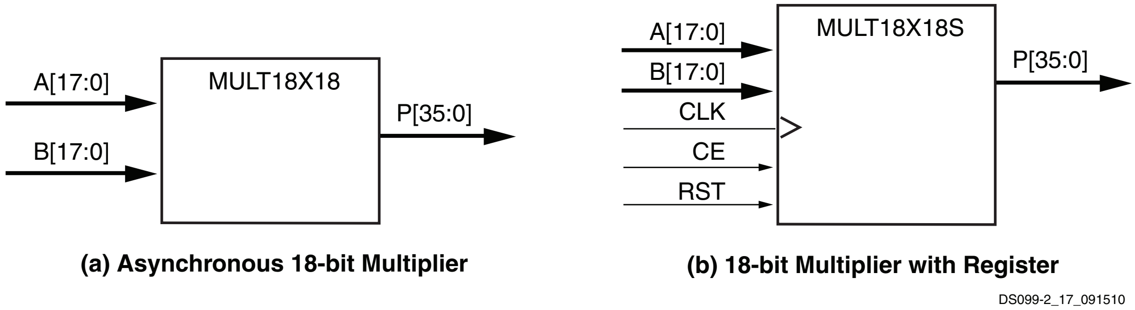


Figure 18: **Embedded Multiplier Primitives**

Table 15: **Embedded Multiplier Primitives Descriptions**

Signal Name	Direction	Function
A[17:0]	Input	Apply one 18-bit multiplicand to these inputs. The MULT18X18S primitive requires a setup time before the enabled rising edge of CLK.
B[17:0]	Input	Apply the other 18-bit multiplicand to these inputs. The MULT18X18S primitive requires a setup time before the enabled rising edge of CLK.
P[35:0]	Output	The output on the P bus is a 36-bit product of the multiplicands A and B. In the case of the MULT18X18S primitive, an enabled rising CLK edge updates the P bus.
CLK	Input(1)	CLK is only an input to the MULT18X18S primitive. The clock signal applied to this input, when enabled by CE, updates the output register that drives the P bus.
CE	Input(1)	CE is only an input to the MULT18X18S primitive. Enable for the CLK signal. Asserting this input enables the CLK signal to update the P bus.
RST	Input(1)	RST is only an input to the MULT18X18S primitive. Asserting this input resets the output register on an enabled, rising CLK edge, forcing the P bus to all zeroes.

Notes:

1. The control signals CLK, CE and RST have the option of inverted polarity.

Digital Clock Manager (DCM)

Spartan-3 devices provide flexible, complete control over clock frequency, phase shift and skew through the use of the DCM feature. To accomplish this, the DCM employs a Delay-Locked Loop (DLL), a fully digital control system that uses feedback to maintain clock signal characteristics with a high degree of precision despite normal variations in operating temperature and voltage. This section provides a fundamental description of the DCM. For further information, refer to the chapter entitled "Using Digital Clock Managers" in UG331.

Each member of the Spartan-3 family has four DCMs, except the smallest, the XC3S50, which has two DCMs. The DCMs are located at the ends of the outermost Block RAM column(s). See Figure 1, page 3. The Digital Clock Manager is placed in a design as the "DCM" primitive.

The DCM supports three major functions:

- **Clock-skew Elimination:** Clock skew describes the extent to which clock signals may, under normal circumstances, deviate from zero-phase alignment. It occurs when slight differences in path delays cause the clock signal to arrive at different points on the die at different times. This clock skew can increase set-up and hold time requirements as well as clock-to-out time, which may be undesirable in applications operating at a high frequency, when timing is critical. The DCM eliminates clock skew by aligning the output clock signal it generates with another version of the clock signal that is fed back. As a result, the two clock signals establish a zero-phase relationship. This effectively cancels out clock distribution delays that may lie in the signal path leading from the clock output of the DCM to its feedback input.
- **Frequency Synthesis:** Provided with an input clock signal, the DCM can generate a wide range of different output clock frequencies. This is accomplished by either multiplying and/or dividing the frequency of the input clock signal by any of several different factors.

DFS Clock Output Connections

There are two basic cases that determine how to connect the DFS clock outputs: on-chip and off-chip, which are illustrated in sections [a] and [c], respectively, of Figure 21. This is similar to what has already been described for the DLL component. See DLL Clock Output and Feedback Connections, page 34.

In the on-chip case, it is possible to connect either of the DFS's two output clock signals through general routing resources to the FPGA's internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. The optional feedback loop is formed in this way, routing CLK0 to a global clock net, which in turn drives the CLKFB input.

In the off-chip case, the DFS's two output clock signals, plus CLK0 for an optional feedback loop, can exit the FPGA using output buffers (OBUF) to drive a clock network plus registers on the board. The feedback loop is formed by feeding the CLK0 signal back into the FPGA using an IBUFG, which directly accesses the global clock network, or an IBUF. Then, the global clock net is connected directly to the CLKFB input.

Phase Shifter (PS)

The DCM provides two approaches to controlling the phase of a DCM clock output signal relative to the CLKIN signal: First, there are nine clock outputs that employ the DLL to achieve a desired phase relationship: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, CLKDV CLKFX, and CLKFX180. These outputs afford “coarse” phase control.

The second approach uses the PS component described in this section to provide a still finer degree of control. The PS component is only available when the DLL is operating in its low-frequency mode. The PS component phase shifts the DCM output clocks by introducing a "fine phase shift" (T_{PS}) between the CLKFB and CLKIN signals inside the DLL component. The user can control this fine phase shift down to a resolution of 1/256 of a CLKIN cycle or one tap delay (DCM_TAP), whichever is greater. When in use, the PS component shifts the phase of all nine DCM clock output signals together. If the PS component is used together with a DCM clock output such as the CLK90, CLK180, CLK270, CLK2X180 and CLKFX180, then the fine phase shift of the former gets added to the coarse phase shift of the latter.

PS Component Enabling and Mode Selection

The CLKOUT_PHASE_SHIFT attribute enables the PS component for use in addition to selecting between two operating modes. As described in Table 20, this attribute has three possible values: NONE, FIXED and VARIABLE. When CLKOUT_PHASE_SHIFT is set to NONE, the PS component is disabled and its inputs, PSEN, PSCLK, and PSINCDEC, must be tied to GND. The set of waveforms in section [a] of Figure 22 shows the disabled case, where the DLL maintains a zero-phase alignment of signals CLKFB and CLKIN upon which the PS component has no effect. The PS component is enabled by setting the attribute to either the FIXED or VARIABLE values, which select the Fixed Phase mode and the Variable Phase mode, respectively. These two modes are described in the sections that follow

Determining the Fine Phase Shift

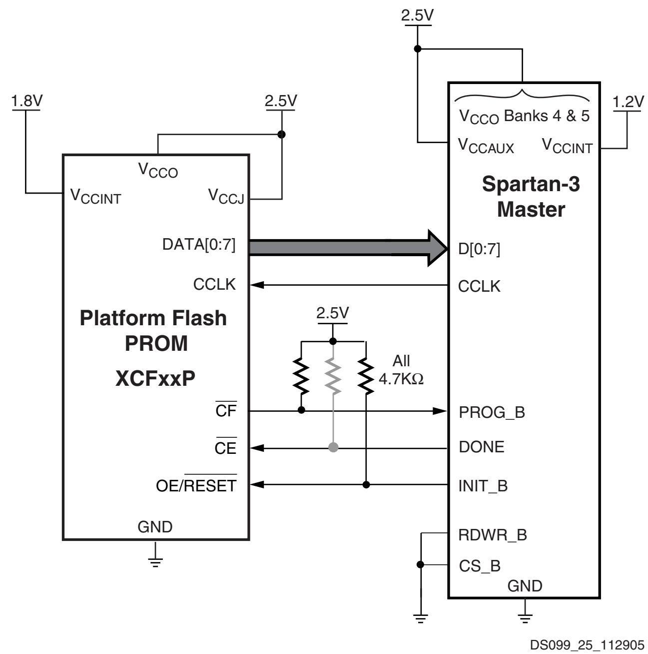
The user controls the phase shift of CLKFB relative to CLKIN by setting and/or adjusting the value of the PHASE_SHIFT attribute. This value must be an integer ranging from –255 to +255. The PS component uses this value to calculate the desired fine phase shift (T_{PS}) as a fraction of the CLKIN period (T_{CLKIN}). Given values for PHASE-SHIFT and T_{CLKIN}, it is possible to calculate T_{PS} as follows:

$$T_{PS} = T_{CLKIN}(PHASE\_SHIFT/256) \quad \textit{Equation 4}$$

Both the Fixed Phase and Variable Phase operating modes employ this calculation. If the PHASE_SHIFT value is zero, then CLKFB and CLKIN will be in phase, the same as when the PS component is disabled. When the PHASE_SHIFT value is positive, the CLKFB signal will be shifted later in time with respect to CLKIN. If the attribute value is negative, the CLKFB signal will be shifted earlier in time with respect to CLKIN.

The Fixed Phase Mode

This mode fixes the desired fine phase shift to a fraction of the T_{CLKIN}, as determined by Equation 4 and its user-selected PHASE_SHIFT value P. The set of waveforms insection [b] of Figure 22 illustrates the relationship between CLKFB and CLKIN in the Fixed Phase mode. In the Fixed Phase mode, the PSEN, PSCLK and PSINCDEC inputs are not used and must be tied to GND. Fixed phase shift requires ISE software version 10.1.03 or later.



Notes:

1. There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.

Figure 28: **Connection Diagram for Master Parallel Configuration**

Master Parallel Mode

In this mode, the FPGA configures from byte-wide data, and the FPGA supplies the CCLK configuration clock. In Master configuration modes, CCLK behaves as a bidirectional I/O pin. Timing is similar to the Slave Parallel mode except that CCLK is supplied by the FPGA. The device connections are shown in Figure 28.

Boundary-Scan (JTAG) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the FPGA. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). FPGA configuration using the Boundary-Scan mode is compatible with the IEEE Std 1149.1-1993 standard and IEEE Std 1532 for In-System Configurable (ISC) devices.

Configuration through the boundary-scan port is always available, regardless of the selected configuration mode. In some cases, however, the mode pin setting may affect proper programming of the device due to various interactions. For example, if the mode pins are set to Master Serial or Master Parallel mode, and the associated PROM is already programmed with a valid configuration image, then there is potential for configuration interference between the JTAG and PROM data. Selecting the Boundary-Scan mode disables the other modes and is the most reliable mode when programming via JTAG.

Configuration Sequence

The configuration of Spartan-3 devices is a three-stage process that occurs after Power-On Reset or the assertion of PROG_B. POR occurs after the V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 4 supplies have reached their respective maximum input threshold levels (see Table 29, page 59). After POR, the three-stage process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process. A flow diagram for the configuration sequence of the Serial and Parallel modes is shown in Figure 29. The flow diagram for the Boundary-Scan configuration sequence appears in Figure 30.

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below Speed Grade -5	-4	Units
LVCMOS18	Slow	2 mA	5.49	6.31	ns
		4 mA	3.45	3.97	ns
		6 mA	2.84	3.26	ns
		8 mA	2.62	3.01	ns
		12 mA	2.11	2.43	ns
		16 mA	2.07	2.38	ns
	Fast	2 mA	2.50	2.88	ns
		4 mA	1.15	1.32	ns
		6 mA	0.96	1.10	ns
		8 mA	0.87	1.01	ns
		12 mA	0.79	0.91	ns
		16 mA	0.76	0.87	ns
LVDCI_18			0.81	0.94	ns
LVDCI_DV2_18			0.67	0.77	ns
LVCMOS25	Slow	2 mA	6.43	7.39	ns
		4 mA	4.15	4.77	ns
		6 mA	3.38	3.89	ns
		8 mA	2.99	3.44	ns
		12 mA	2.53	2.91	ns
		16 mA	2.50	2.87	ns
		24 mA	2.22	2.55	ns
	Fast	2 mA	3.27	3.76	ns
		4 mA	1.87	2.15	ns
		6 mA	0.32	0.37	ns
		8 mA	0.19	0.22	ns
		12 mA	0	0	ns
		16 mA	–0.02	–0.01	ns
		24 mA	–0.04	–0.02	ns
LVDCI_25			0.27	0.31	ns
LVDCI_DV2_25			0.16	0.19	ns

Simultaneously Switching Output Guidelines

This section provides guidelines for the maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins, of a given output signal standard, that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 49 and Table 50 provide the essential SSO guidelines. For each device/package combination, Table 49 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and will possibly not match the physical number of pairs. For each output signal standard and drive strength, Table 50 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The Table 50 guidelines are categorized by package style. Multiply the appropriate numbers from Table 49 and Table 50 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines may result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 49 x Table 50

The recommended maximum SSO values assume that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The number of SSOs allowed for quad-flat packages (VQ, TQ, PQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 49: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	VQ100	CP132[1][2]	TQ144[1]	PQ208	FT256	FG320	FG456	FG676	FG900	FG1156[2]
XC3S50	1	1.5	1.5	2	–	–	–	–	–	–
XC3S200	1	–	1.5	2	3	–	–	–	–	–
XC3S400	–	–	1.5	2	3	3	5	–	–	–
XC3S1000	–	–	–	–	3	3	5	5	–	–
XC3S1500	–	–	–	–	–	3	5	6	–	–
XC3S2000	–	–	–	–	–	–	5	6	9	–
XC3S4000	–	–	–	–	–	–	–	6	10	12
XC3S5000	–	–	–	–	–	–	–	6	10	12

Notes:

1. The V_{CCO} lines for the pair of banks on each side of the CP132 and TQ144 packages are internally tied together. Each pair of interconnected banks shares three V_{CCO}/GND pairs. Consequently, the per bank number is 1.5.
2. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.
3. The information in this table also applies to Pb-free packages.

Table 56: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{BCKO}	When reading from the Block RAM, the time from the active transition at the CLK input to data appearing at the DOUT output	–	2.09	–	2.40	ns
Setup Times						
T_{BDCK}	Time from the setup of data at the DIN inputs to the active transition at the CLK input of the Block RAM	0.43	–	0.49	–	ns
Hold Times						
T_{BCKD}	Time from the active transition at the Block RAM's CLK input to the point where data is last held at the DIN inputs	0	–	0	–	ns
Clock Timing						
T_{BPWH}	Block RAM CLK signal High pulse width	1.19	∞	1.37	∞	ns
T_{BPWL}	Block RAM CLK signal Low pulse width	1.19	∞	1.37	∞	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. For minimums, use the values reported by the Xilinx timing analyzer.

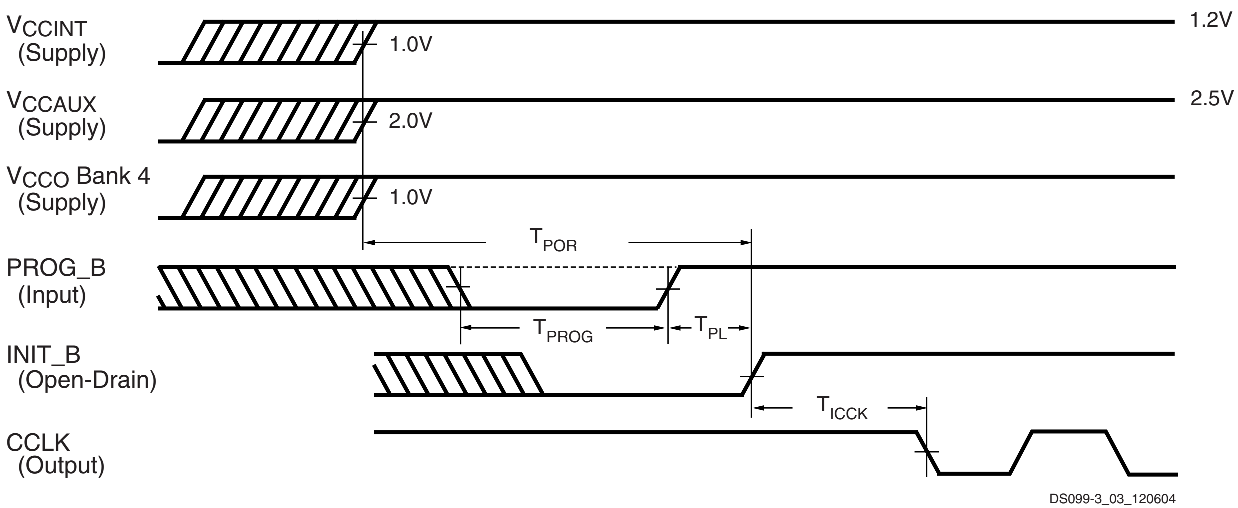
Clock Distribution Switching Characteristics

Table 57: **Clock Distribution Switching Characteristics**

Description	Symbol	Maximum		Units
		Speed Grade		
		-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I-input to O-output delay	T_{GIO}	0.36	0.41	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0- and I1-inputs. Same as BUFGCE enable CE-input	T_{GSI}	0.53	0.60	ns

Notes:
1. For minimums, use the values reported by the Xilinx timing analyzer.

Configuration and JTAG Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 36: **Waveforms for Power-On and the Beginning of Configuration**

Table 65: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 4 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XC3S50	–	5	ms
		XC3S200	–	5	ms
		XC3S400	–	5	ms
		XC3S1000	–	5	ms
		XC3S1500	–	7	ms
		XC3S2000	–	7	ms
		XC3S4000	–	7	ms
		XC3S5000	–	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.3	–	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S50	–	2	ms
		XC3S200	–	2	ms
		XC3S400	–	2	ms
		XC3S1000	–	2	ms
		XC3S1500	–	3	ms
		XC3S2000	–	3	ms
		XC3S4000	–	3	ms
		XC3S5000	–	3	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	–	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.25	4.0	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only for the Master Serial and Master Parallel modes.

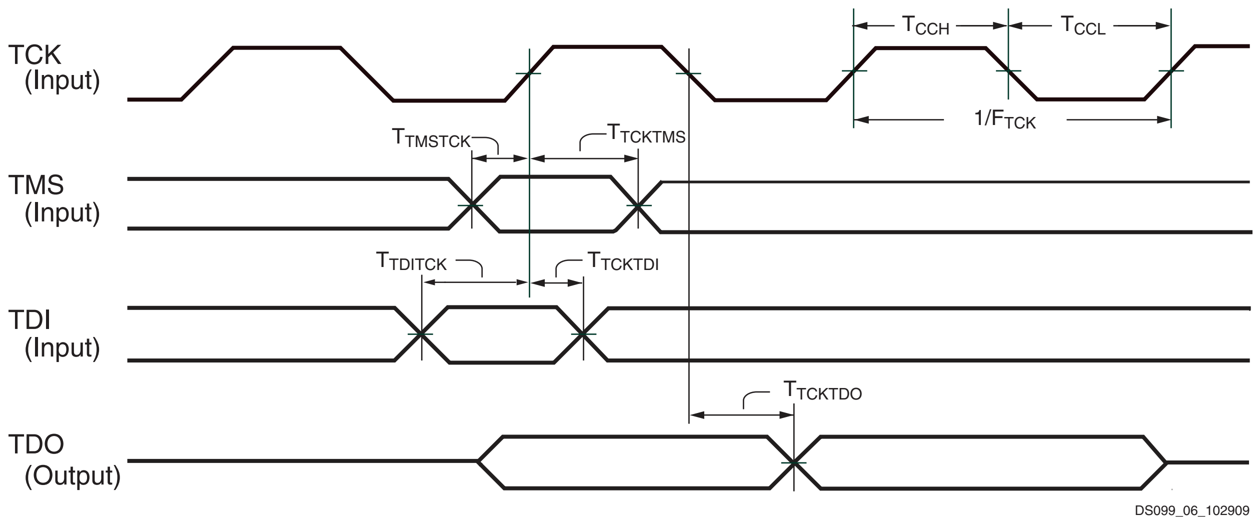


Figure 39: **JTAG Waveforms**

Table 68: **Timing for the JTAG Test Access Port**

Symbol	Description		All Speed Grades Min	All Speed Grades Max	Units
Clock-to-Output Times					
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin		1.0	11.0	ns
Setup Times					
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin		7.0	–	ns
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin		7.0	–	ns
Hold Times					
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin		0	–	ns
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin		0	–	ns
Clock Timing					
T_{TCKH}	TCK pin High pulse width		5	∞	ns
T_{TCKL}	TCK pin Low pulse width		5	∞	ns
F_{TCK}	Frequency of the TCK signal	JTAG Configuration	0	33	MHz
		Boundary-Scan	0	25	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.

Differential Pair Labeling

A pin supports differential standards if the pin is labeled in the format “Lxxy_#”. The pin name suffix has the following significance. Figure 40 provides a specific example showing a differential input to and a differential output from Bank 2.

- ‘L’ indicates differential capability.
- "xx" is a two-digit integer, unique for each bank, that identifies a differential pin-pair.
- ‘y’ is replaced by ‘P’ for the true signal or ‘N’ for the inverted. These two pins form one differential pin-pair.
- ‘#’ is an integer, 0 through 7, indicating the associated I/O bank.

If unused, these pins are in a high impedance state. The Bitstream generator option UnusedPin enables a pull-up or pull-down resistor on all unused I/O pins.

Behavior from Power-On through End of Configuration

During the configuration process, all pins that are not actively involved in the configuration process are in a high-impedance state. The CONFIG- and JTAG-type pins have an internal pull-up resistor to VCCAUX during configuration. For all other I/O pins, the HSWAP_EN input determines whether or not pull-up resistors are activated during configuration. HSWAP_EN = 0 enables the pull-up resistors. HSWAP_EN = 1 disables the pull-up resistors allowing the pins to float, which is the desired state for hot-swap applications.

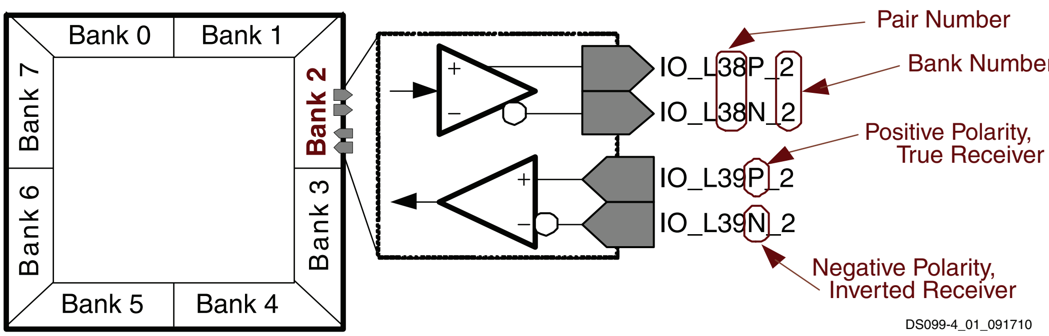


Figure 40: **Differential Pair Labelling**

DUAL Type: Dual-Purpose Configuration and I/O Pins

These pins serve dual purposes. The user-I/O pins are temporarily borrowed during the configuration process to load configuration data into the FPGA. After configuration, these pins are then usually available as a user I/O in the application. If a pin is not applicable to the specific configuration mode—controlled by the mode select pins M2, M1, and M0—then the pin behaves as an I/O-type pin.

There are 12 dual-purpose configuration pins on every package, six of which are part of I/O Bank 4, the other six part of I/O Bank 5. Only a few of the pins in Bank 4 are used in the Serial configuration modes.

See Pin Behavior During Configuration, page 122.

Serial Configuration Modes

This section describes the dual-purpose pins used during either Master or Slave Serial mode. See Table 75 for Mode Select pin settings required for Serial modes. All such pins are in Bank 4 and powered by VCCO_4.

In both the Master and Slave Serial modes, DIN is the serial configuration data input. The D1-D7 inputs are unused in serial mode and behave like general-purpose I/O pins.

In all the cases, the configuration data is synchronized to the rising edge of the CCLK clock signal.

The DIN, DOUT, and INIT_B pins can be retained in the application to support reconfiguration by setting the Persist bitstream generation option. However, the serial modes do not support device readback.

TQ144: 144-lead Thin Quad Flat Package

The XC3S50, the XC3S200, and the XC3S400 are available in the 144-lead thin quad flat package, TQ144. All devices share a common footprint for this package as shown in Table 91 and Figure 46.

The TQ144 package only has four separate VCCO inputs, unlike the BGA packages, which have eight separate VCCO inputs. The TQ144 package has a separate VCCO input for the top, bottom, left, and right. However, there are still eight separate I/O banks, as shown in Table 91 and Figure 46. Banks 0 and 1 share the VCCO_TOP input, Banks 2 and 3 share the VCCO_RIGHT input, Banks 4 and 5 share the VCCO_BOTTOM input, and Banks 6 and 7 share the VCCO_LEFT input.

All the package pins appear in Table 91 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 91: **TQ144 Package Pinout**

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
0	IO_L01N_0/VRP_0	P141	DCI
0	IO_L01P_0/VRN_0	P140	DCI
0	IO_L27N_0	P137	I/O
0	IO_L27P_0	P135	I/O
0	IO_L30N_0	P132	I/O
0	IO_L30P_0	P131	I/O
0	IO_L31N_0	P130	I/O
0	IO_L31P_0/VREF_0	P129	VREF
0	IO_L32N_0/GCLK7	P128	GCLK
0	IO_L32P_0/GCLK6	P127	GCLK
1	IO	P116	I/O
1	IO_L01N_1/VRP_1	P113	DCI
1	IO_L01P_1/VRN_1	P112	DCI
1	IO_L28N_1	P119	I/O
1	IO_L28P_1	P118	I/O
1	IO_L31N_1/VREF_1	P123	VREF
1	IO_L31P_1	P122	I/O
1	IO_L32N_1/GCLK5	P125	GCLK
1	IO_L32P_1/GCLK4	P124	GCLK
2	IO_L01N_2/VRP_2	P108	DCI
2	IO_L01P_2/VRN_2	P107	DCI
2	IO_L20N_2	P105	I/O
2	IO_L20P_2	P104	I/O
2	IO_L21N_2	P103	I/O
2	IO_L21P_2	P102	I/O
2	IO_L22N_2	P100	I/O
2	IO_L22P_2	P99	I/O

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
N/A	GND	T16	GND
N/A	VCCAUX	A6	VCCAUX
N/A	VCCAUX	A11	VCCAUX
N/A	VCCAUX	F1	VCCAUX
N/A	VCCAUX	F16	VCCAUX
N/A	VCCAUX	L1	VCCAUX
N/A	VCCAUX	L16	VCCAUX
N/A	VCCAUX	T6	VCCAUX
N/A	VCCAUX	T11	VCCAUX
N/A	VCCINT	D4	VCCINT
N/A	VCCINT	D13	VCCINT
N/A	VCCINT	E5	VCCINT
N/A	VCCINT	E12	VCCINT
N/A	VCCINT	M5	VCCINT
N/A	VCCINT	M12	VCCINT
N/A	VCCINT	N4	VCCINT
N/A	VCCINT	N13	VCCINT
VCCAUX	CCLK	T15	CONFIG
VCCAUX	DONE	R14	CONFIG
VCCAUX	HSWAP_EN	C4	CONFIG
VCCAUX	M0	P3	CONFIG
VCCAUX	M1	T2	CONFIG
VCCAUX	M2	P4	CONFIG
VCCAUX	PROG_B	B3	CONFIG
VCCAUX	TCK	C14	JTAG
VCCAUX	TDI	A2	JTAG
VCCAUX	TDO	A15	JTAG
VCCAUX	TMS	C13	JTAG

FT256 Footprint

Bank 0 (columns 3–8) | Bank 1 (columns 9–14) | Bank 7 (rows A–H, left) | Bank 2 (rows A–H, right)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	TDI	IO VREF_0	I/O L01P_0 VRN_0	I/O	VCCAUX	I/O	I/O L32P_0 GCLK6	I/O	I/O L31N_1 VREF_1	VCCAUX	I/O	I/O L10N_1 VREF_1	I/O L01N_1 VRP_1	TDO	GND
B	I/O L01P_7 VRN_7	GND	PROG_B	I/O L01N_0 VRP_0	I/O L25P_0	I/O L28P_0	I/O L30P_0	I/O L32N_0 GCLK7	GND	I/O L31P_1	I/O L29N_1	I/O L27N_1	I/O L10P_1	I/O L01P_1 VRN_1	GND	I/O L01N_2 VRP_2
C	I/O L01N_7 VRP_7	I/O L16N_7	I/O L16P_7 VREF_7	HSWAP_EN	I/O L25N_0	I/O L28N_0	I/O L30N_0	I/O L31P_0 VREF_0	I/O L32N_1 GCLK5	I/O	I/O L29P_1	I/O L27P_1	TMS	TCK	I/O L16N_2	I/O L01P_2 VRN_2
D	I/O L17N_7	I/O L17P_7	I/O L19P_7	VCCINT	IO VREF_0	I/O L27P_0	I/O L29P_0	I/O L31N_0	I/O L32P_1 GCLK4	I/O L30N_1	I/O L28N_1	IO VREF_1	VCCINT	I/O L16P_2	I/O L17N_2	I/O L17P_2 VREF_2
E	I/O L20N_7	I/O L20P_7	I/O L19N_7 VREF_7	I/O L21P_7	VCCINT	I/O L27N_0	I/O L29N_0	VCCO_0	VCCO_1	I/O L30P_1	I/O L28P_1	VCCINT	I/O L19N_2	I/O L19P_2	I/O L20N_2	I/O L20P_2
F	VCCAUX	I/O L22N_7	I/O L22P_7	I/O L21N_7	I/O L23P_7	GND	VCCO_0	VCCO_0	VCCO_1	VCCO_1	GND	I/O L21N_2	I/O L21P_2	I/O L22N_2	I/O L22P_2	VCCAUX
G	I/O L40P_7	I/O	I/O L24N_7	I/O L24P_7	I/O L23N_7	VCCO_7	GND	GND	GND	GND	VCCO_2	I/O L23N_2 VREF_2	I/O L23P_2	I/O L24N_2	I/O L24P_2	I/O
H	I/O L40N_7 VREF_7	GND	I/O L39N_7	I/O L39P_7	VCCO_7	VCCO_7	GND	GND	GND	GND	VCCO_2	VCCO_2	I/O L39N_2	I/O L39P_2	I/O L40N_2	I/O L40P_2 VREF_2
J	I/O L40P_6 VREF_6	I/O L40N_6	I/O L39P_6	I/O L39N_6	VCCO_6	VCCO_6	GND	GND	GND	GND	VCCO_3	VCCO_3	I/O L39P_3	I/O L39N_3	GND	I/O L40N_3 VREF_3
K	I/O	I/O L24P_6	I/O L24N_6 VREF_6	I/O L23P_6	I/O L23N_6	VCCO_6	GND	GND	GND	GND	VCCO_3	I/O L23N_3	I/O L24P_3	I/O L24N_3	I/O	I/O L40P_3
L	VCCAUX	I/O L22P_6	I/O L22N_6	I/O L21P_6	I/O L21N_6	GND	VCCO_5	VCCO_5	VCCO_4	VCCO_4	GND	I/O L23P_3 VREF_3	I/O L21N_3	I/O L22P_3	I/O L22N_3	VCCAUX
M	I/O L20P_6	I/O L20N_6	I/O L19P_6	I/O L19N_6	VCCINT	I/O L28P_5 D7	I/O L30P_5	VCCO_5	VCCO_4	I/O L29N_4	I/O L27N_4 DIN D0	VCCINT	I/O L21P_3	I/O L19N_3	I/O L20P_3	I/O L20N_3
N	I/O L17P_6 VREF_6	I/O L17N_6	I/O L16P_6	VCCINT	I/O	I/O L28N_5 D6	I/O L30N_5	I/O L32P_5 GCLK2	I/O L31N_4 INIT_B	I/O L29P_4	I/O L27P_4 D1	IO VREF_4	VCCINT	I/O L19P_3	I/O L17P_3 VREF_3	I/O L17N_3
P	I/O L01P_6 VRN_6	I/O L16N_6	M0	M2	I/O L27P_5	I/O L29P_5 VREF_5	I/O	I/O L32N_5 GCLK3	I/O L31P_4 DOUT BUSY	I/O L30N_4 D2	I/O L28N_4	I/O L25N_4	IO VREF_4	I/O L16P_3	I/O L16N_3	I/O L01N_3 VRP_3
R	I/O L01N_6 VRP_6	GND	I/O L01P_5 CS_B	I/O L10P_5 VRN_5	I/O L27N_5 VREF_5	I/O L29N_5	I/O L31P_5 D5	GND	I/O L32N_4 GCLK1	I/O L30P_4 D3	I/O L28P_4	I/O L25P_4	I/O L01N_4 VRP_4	DONE	GND	I/O L01P_3 VRN_3
T	GND	M1	I/O L01N_5 RDWR_B	I/O L10N_5 VRP_5	I/O	VCCAUX	I/O L31N_5 D4	IO VREF_5	I/O L32P_4 GCLK0	IO VREF_4	VCCAUX	I/O	I/O L01P_4 VRN_4	I/O	CCLK	GND

Bank 6 (rows J–R, left) | Bank 3 (rows J–R, right) | Bank 5 (columns 3–8) | Bank 4 (columns 9–14)

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Figure 49: **FT256 Package Footprint (Top View)**

113	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	24	**VREF:** User I/O or input voltage reference for bank
16	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input	24	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	8	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	32	**GND:** Ground	8	**VCCAUX:** Auxiliary voltage supply (+2.5V)

FG320: 320-lead Fine-pitch Ball Grid Array

The 320-lead fine-pitch ball grid array package, FG320, supports three different Spartan-3 devices, including the XC3S400, the XC3S1000, and the XC3S1500. The footprint for all three devices is identical, as shown in Table 98 and Figure 50.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

All the package pins appear in Table 98 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 98: **FG320 Package Pinout**

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
0	IO	D9	I/O
0	IO	E7	I/O
0	IO/VREF_0	B3	VREF
0	IO/VREF_0	D6	VREF
0	IO_L01N_0/VRP_0	A2	DCI
0	IO_L01P_0/VRN_0	A3	DCI
0	IO_L09N_0	B4	I/O
0	IO_L09P_0	C4	I/O
0	IO_L10N_0	C5	I/O
0	IO_L10P_0	D5	I/O
0	IO_L15N_0	A4	I/O
0	IO_L15P_0	A5	I/O
0	IO_L25N_0	B5	I/O
0	IO_L25P_0	B6	I/O
0	IO_L27N_0	C7	I/O
0	IO_L27P_0	D7	I/O
0	IO_L28N_0	C8	I/O
0	IO_L28P_0	D8	I/O
0	IO_L29N_0	E8	I/O
0	IO_L29P_0	F8	I/O
0	IO_L30N_0	A7	I/O
0	IO_L30P_0	A8	I/O
0	IO_L31N_0	B9	I/O
0	IO_L31P_0/VREF_0	A9	VREF
0	IO_L32N_0/GCLK7	E9	GCLK
0	IO_L32P_0/GCLK6	F9	GCLK
0	VCCO_0	B8	VCCO
0	VCCO_0	C6	VCCO
0	VCCO_0	G8	VCCO

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
2	N.C. (◆)	IO_L06N_2	IO_L06N_2	IO_L06N_2	IO_L06N_2	G20	I/O
2	N.C. (◆)	IO_L06P_2	IO_L06P_2	IO_L06P_2	IO_L06P_2	G21	I/O
2	N.C. (◆)	IO_L07N_2	IO_L07N_2	IO_L07N_2	IO_L07N_2	F23	I/O
2	N.C. (◆)	IO_L07P_2	IO_L07P_2	IO_L07P_2	IO_L07P_2	F24	I/O
2	N.C. (◆)	IO_L08N_2	IO_L08N_2	IO_L08N_2	IO_L08N_2	G22	I/O
2	N.C. (◆)	IO_L08P_2	IO_L08P_2	IO_L08P_2	IO_L08P_2	G23	I/O
2	N.C. (◆)	IO_L09N_2/VREF_2[(1)]	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	F25	VREF[(1)]
2	N.C. (◆)	IO_L09P_2	IO_L09P_2	IO_L09P_2	IO_L09P_2	F26	I/O
2	N.C. (◆)	IO_L10N_2	IO_L10N_2	IO_L10N_2	IO_L10N_2	G25	I/O
2	N.C. (◆)	IO_L10P_2	IO_L10P_2	IO_L10P_2	IO_L10P_2	G26	I/O
2	IO_L14N_2	IO_L14N_2	IO_L14N_2[(2)]	IO_L11N_2[(2)]	IO_L11N_2	H20	I/O
2	IO_L14P_2	IO_L14P_2	IO_L14P_2[(2)]	IO_L11P_2[(2)]	IO_L11P_2	H21	I/O
2	IO_L16N_2	IO_L16N_2	IO_L16N_2[(2)]	IO_L12N_2[(2)]	IO_L12N_2	H22	I/O
2	IO_L16P_2	IO_L16P_2	IO_L16P_2[(2)]	IO_L12P_2[(2)]	IO_L12P_2	J21	I/O
2	IO_L17N_2	IO_L17N_2	IO_L17N_2[(2)]	IO_L13N_2[(2)]	IO[(3)]	H23	I/O
2	IO_L17P_2/VREF_2	IO_L17P_2/VREF_2	IO_L17P_2[(2)]/VREF_2	IO_L13P_2[(2)]/VREF_2	IO/VREF_2[(3)]	H24	VREF
2	IO_L19N_2	IO_L19N_2	IO_L19N_2	IO_L19N_2	IO_L19N_2	H25	I/O
2	IO_L19P_2	IO_L19P_2	IO_L19P_2	IO_L19P_2	IO_L19P_2	H26	I/O
2	IO_L20N_2	IO_L20N_2	IO_L20N_2	IO_L20N_2	IO_L20N_2	J20	I/O
2	IO_L20P_2	IO_L20P_2	IO_L20P_2	IO_L20P_2	IO_L20P_2	K20	I/O
2	IO_L21N_2	IO_L21N_2	IO_L21N_2	IO_L21N_2	IO_L21N_2	J22	I/O
2	IO_L21P_2	IO_L21P_2	IO_L21P_2	IO_L21P_2	IO_L21P_2	J23	I/O
2	IO_L22N_2	IO_L22N_2	IO_L22N_2	IO_L22N_2	IO_L22N_2	J24	I/O
2	IO_L22P_2	IO_L22P_2	IO_L22P_2	IO_L22P_2	IO_L22P_2	J25	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	K21	VREF
2	IO_L23P_2	IO_L23P_2	IO_L23P_2	IO_L23P_2	IO_L23P_2	K22	I/O
2	IO_L24N_2	IO_L24N_2	IO_L24N_2	IO_L24N_2	IO_L24N_2	K23	I/O
2	IO_L24P_2	IO_L24P_2	IO_L24P_2	IO_L24P_2	IO_L24P_2	K24	I/O
2	IO_L26N_2	IO_L26N_2	IO_L26N_2	IO_L26N_2	IO_L26N_2	K25	I/O
2	IO_L26P_2	IO_L26P_2	IO_L26P_2	IO_L26P_2	IO_L26P_2	K26	I/O
2	IO_L27N_2	IO_L27N_2	IO_L27N_2	IO_L27N_2	IO_L27N_2	L19	I/O
2	IO_L27P_2	IO_L27P_2	IO_L27P_2	IO_L27P_2	IO_L27P_2	L20	I/O
2	IO_L28N_2	IO_L28N_2	IO_L28N_2	IO_L28N_2	IO_L28N_2	L21	I/O
2	IO_L28P_2	IO_L28P_2	IO_L28P_2	IO_L28P_2	IO_L28P_2	L22	I/O
2	IO_L29N_2	IO_L29N_2	IO_L29N_2	IO_L29N_2	IO_L29N_2	L25	I/O
2	IO_L29P_2	IO_L29P_2	IO_L29P_2	IO_L29P_2	IO_L29P_2	L26	I/O
2	IO_L31N_2	IO_L31N_2	IO_L31N_2	IO_L31N_2	IO_L31N_2	M19	I/O
2	IO_L31P_2	IO_L31P_2	IO_L31P_2	IO_L31P_2	IO_L31P_2	M20	I/O
2	IO_L32N_2	IO_L32N_2	IO_L32N_2	IO_L32N_2	IO_L32N_2	M21	I/O
2	IO_L32P_2	IO_L32P_2	IO_L32P_2	IO_L32P_2	IO_L32P_2	M22	I/O
2	IO_L33N_2	IO_L33N_2	IO_L33N_2	IO_L33N_2	IO_L33N_2	L23	I/O
2	IO_L33P_2	IO_L33P_2	IO_L33P_2	IO_L33P_2	IO_L33P_2	M24	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	AE14	VREF
5	IO_L27P_5	IO_L27P_5	AE13	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	AJ14	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	AH14	DUAL
5	IO_L29N_5	IO_L29N_5	AC15	I/O
5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	AB15	VREF
5	IO_L30N_5	IO_L30N_5	AD15	I/O
5	IO_L30P_5	IO_L30P_5	AD14	I/O
5	IO_L31N_5/D4	IO_L31N_5/D4	AG15	DUAL
5	IO_L31P_5/D5	IO_L31P_5/D5	AF15	DUAL
5	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	AJ15	GCLK
5	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	AH15	GCLK
5	N.C. (◆)	IO_L35N_5	AK7	I/O
5	N.C. (◆)	IO_L35P_5	AJ7	I/O
5	N.C. (◆)	IO_L36N_5	AD8	I/O
5	N.C. (◆)	IO_L36P_5	AC8	I/O
5	N.C. (◆)	IO_L37N_5	AF8	I/O
5	N.C. (◆)	IO_L37P_5	AE8	I/O
5	N.C. (◆)	IO_L38N_5	AH8	I/O
5	N.C. (◆)	IO_L38P_5	AG8	I/O
5	VCCO_5	VCCO_5	AH5	VCCO
5	VCCO_5	VCCO_5	AF7	VCCO
5	VCCO_5	VCCO_5	AD9	VCCO
5	VCCO_5	VCCO_5	AH9	VCCO
5	VCCO_5	VCCO_5	AB11	VCCO
5	VCCO_5	VCCO_5	Y12	VCCO
5	VCCO_5	VCCO_5	Y13	VCCO
5	VCCO_5	VCCO_5	AD13	VCCO
5	VCCO_5	VCCO_5	AH13	VCCO
5	VCCO_5	VCCO_5	Y14	VCCO
6	IO	IO	AB6	I/O
6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	AH2	DCI
6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	AH1	DCI
6	IO_L02N_6	IO_L02N_6	AG4	I/O
6	IO_L02P_6	IO_L02P_6	AG3	I/O
6	IO_L03N_6/VREF_6	IO_L03N_6/VREF_6	AG2	VREF
6	IO_L03P_6	IO_L03P_6	AG1	I/O
6	IO_L04N_6	IO_L04N_6	AF2	I/O
6	IO_L04P_6	IO_L04P_6	AF1	I/O
6	IO_L05N_6	IO_L05N_6	AF4	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
1	IO_L07N_1	IO_L07N_1	D27	I/O
1	IO_L07P_1	IO_L07P_1	E27	I/O
1	IO_L08N_1	IO_L08N_1	A27	I/O
1	IO_L08P_1	IO_L08P_1	B27	I/O
1	IO_L09N_1	IO_L09N_1	F26	I/O
1	IO_L09P_1	IO_L09P_1	G26	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	C26	VREF
1	IO_L10P_1	IO_L10P_1	D26	I/O
1	IO_L11N_1	IO_L11N_1	H25	I/O
1	IO_L11P_1	IO_L11P_1	J25	I/O
1	IO_L12N_1	IO_L12N_1	F25	I/O
1	IO_L12P_1	IO_L12P_1	G25	I/O
1	IO_L13N_1	IO_L13N_1	C25	I/O
1	IO_L13P_1	IO_L13P_1	D25	I/O
1	IO_L14N_1	IO_L14N_1	A25	I/O
1	IO_L14P_1	IO_L14P_1	B25	I/O
1	IO_L15N_1	IO_L15N_1	A24	I/O
1	IO_L15P_1	IO_L15P_1	B24	I/O
1	IO_L16N_1	IO_L16N_1	J23	I/O
1	IO_L16P_1	IO_L16P_1	K23	I/O
1	IO_L17N_1/VREF_1	IO_L17N_1/VREF_1	F23	VREF
1	IO_L17P_1	IO_L17P_1	G23	I/O
1	IO_L18N_1	IO_L18N_1	D23	I/O
1	IO_L18P_1	IO_L18P_1	E23	I/O
1	IO_L19N_1	IO_L19N_1	A23	I/O
1	IO_L19P_1	IO_L19P_1	B23	I/O
1	IO_L20N_1	IO_L20N_1	K22	I/O
1	IO_L20P_1	IO_L20P_1	L22	I/O
1	IO_L21N_1	IO_L21N_1	G22	I/O
1	IO_L21P_1	IO_L21P_1	H22	I/O
1	IO_L22N_1	IO_L22N_1	C22	I/O
1	IO_L22P_1	IO_L22P_1	D22	I/O
1	IO_L23N_1	IO_L23N_1	H21	I/O
1	IO_L23P_1	IO_L23P_1	J21	I/O
1	IO_L24N_1	IO_L24N_1	F21	I/O
1	IO_L24P_1	IO_L24P_1	G21	I/O
1	IO_L25N_1	IO_L25N_1	C21	I/O
1	IO_L25P_1	IO_L25P_1	D21	I/O
1	IO_L26N_1	IO_L26N_1	A21	I/O
1	IO_L26P_1	IO_L26P_1	B21	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
1	VCCO_1	VCCO_1	M22	VCCO
2	IO	IO	G33	I/O
2	IO	IO	G34	I/O
2	IO	IO	U25	I/O
2	IO	IO	U26	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C33	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C34	DCI
2	IO_L02N_2	IO_L02N_2	D33	I/O
2	IO_L02P_2	IO_L02P_2	D34	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	E32	VREF
2	IO_L03P_2	IO_L03P_2	E33	I/O
2	IO_L04N_2	IO_L04N_2	F31	I/O
2	IO_L04P_2	IO_L04P_2	F32	I/O
2	IO_L05N_2	IO_L05N_2	G29	I/O
2	IO_L05P_2	IO_L05P_2	G30	I/O
2	IO_L06N_2	IO_L06N_2	H29	I/O
2	IO_L06P_2	IO_L06P_2	H30	I/O
2	IO_L07N_2	IO_L07N_2	H33	I/O
2	IO_L07P_2	IO_L07P_2	H34	I/O
2	IO_L08N_2	IO_L08N_2	J28	I/O
2	IO_L08P_2	IO_L08P_2	J29	I/O
2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	H31	VREF
2	IO_L09P_2	IO_L09P_2	J31	I/O
2	IO_L10N_2	IO_L10N_2	J32	I/O
2	IO_L10P_2	IO_L10P_2	J33	I/O
2	IO_L11N_2	IO_L11N_2	J27	I/O
2	IO_L11P_2	IO_L11P_2	K26	I/O
2	IO_L12N_2	IO_L12N_2	K27	I/O
2	IO_L12P_2	IO_L12P_2	K28	I/O
2	IO_L13N_2	IO_L13N_2	K29	I/O
2	IO_L13P_2/VREF_2	IO_L13P_2/VREF_2	K30	VREF
2	IO_L14N_2	IO_L14N_2	K31	I/O
2	IO_L14P_2	IO_L14P_2	K32	I/O
2	IO_L15N_2	IO_L15N_2	K33	I/O
2	IO_L15P_2	IO_L15P_2	K34	I/O
2	IO_L16N_2	IO_L16N_2	L25	I/O
2	IO_L16P_2	IO_L16P_2	L26	I/O
2	N.C. (◆)	IO_L17N_2	L28	I/O
2	N.C. (◆)	IO_L17P_2/ VREF_2	L29	VREF

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L03P_3	IO_L03P_3	AK32	I/O
3	IO_L04N_3	IO_L04N_3	AJ32	I/O
3	IO_L04P_3	IO_L04P_3	AJ31	I/O
3	IO_L05N_3	IO_L05N_3	AJ34	I/O
3	IO_L05P_3	IO_L05P_3	AJ33	I/O
3	IO_L06N_3	IO_L06N_3	AH30	I/O
3	IO_L06P_3	IO_L06P_3	AH29	I/O
3	IO_L07N_3	IO_L07N_3	AG30	I/O
3	IO_L07P_3	IO_L07P_3	AG29	I/O
3	IO_L08N_3	IO_L08N_3	AG34	I/O
3	IO_L08P_3	IO_L08P_3	AG33	I/O
3	IO_L09N_3	IO_L09N_3	AF29	I/O
3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	AF28	VREF
3	IO_L10N_3	IO_L10N_3	AF31	I/O
3	IO_L10P_3	IO_L10P_3	AG31	I/O
3	IO_L11N_3	IO_L11N_3	AF33	I/O
3	IO_L11P_3	IO_L11P_3	AF32	I/O
3	IO_L12N_3	IO_L12N_3	AE26	I/O
3	IO_L12P_3	IO_L12P_3	AF27	I/O
3	IO_L13N_3/VREF_3	IO_L13N_3/VREF_3	AE28	VREF
3	IO_L13P_3	IO_L13P_3	AE27	I/O
3	IO_L14N_3	IO_L14N_3	AE30	I/O
3	IO_L14P_3	IO_L14P_3	AE29	I/O
3	IO_L15N_3	IO_L15N_3	AE32	I/O
3	IO_L15P_3	IO_L15P_3	AE31	I/O
3	IO_L16N_3	IO_L16N_3	AE34	I/O
3	IO_L16P_3	IO_L16P_3	AE33	I/O
3	IO_L17N_3	IO_L17N_3	AD26	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	AD25	VREF
3	IO_L19N_3	IO_L19N_3	AD34	I/O
3	IO_L19P_3	IO_L19P_3	AD33	I/O
3	IO_L20N_3	IO_L20N_3	AC25	I/O
3	IO_L20P_3	IO_L20P_3	AC24	I/O
3	IO_L21N_3	IO_L21N_3	AC28	I/O
3	IO_L21P_3	IO_L21P_3	AC27	I/O
3	IO_L22N_3	IO_L22N_3	AC30	I/O
3	IO_L22P_3	IO_L22P_3	AC29	I/O
3	IO_L23N_3	IO_L23N_3	AC32	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	AC31	VREF
3	IO_L24N_3	IO_L24N_3	AB25	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
4	IO_L21N_4	IO_L21N_4	AL21	I/O
4	IO_L21P_4	IO_L21P_4	AM21	I/O
4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	AN21	VREF
4	IO_L22P_4	IO_L22P_4	AP21	I/O
4	IO_L23N_4	IO_L23N_4	AE20	I/O
4	IO_L23P_4	IO_L23P_4	AF20	I/O
4	IO_L24N_4	IO_L24N_4	AH20	I/O
4	IO_L24P_4	IO_L24P_4	AJ20	I/O
4	IO_L25N_4	IO_L25N_4	AL20	I/O
4	IO_L25P_4	IO_L25P_4	AM20	I/O
4	IO_L26N_4	IO_L26N_4	AN20	I/O
4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	AP20	VREF
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	AH19	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	AJ19	DUAL
4	IO_L28N_4	IO_L28N_4	AM19	I/O
4	IO_L28P_4	IO_L28P_4	AN19	I/O
4	IO_L29N_4	IO_L29N_4	AF18	I/O
4	IO_L29P_4	IO_L29P_4	AG18	I/O
4	IO_L30N_4/D2	IO_L30N_4/D2	AH18	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	AJ18	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	AL18	DUAL
4	IO_L31P_4/DOUT/BUSY	IO_L31P_4/DOUT/BUSY	AM18	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	AN18	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	AP18	GCLK
4	IO_L33N_4	IO_L33N_4	AL29	I/O
4	IO_L33P_4	IO_L33P_4	AM29	I/O
4	IO_L34N_4	IO_L34N_4	AN29	I/O
4	IO_L34P_4	IO_L34P_4	AP29	I/O
4	IO_L35N_4	IO_L35N_4	AJ28	I/O
4	IO_L35P_4	IO_L35P_4	AK28	I/O
4	N.C. (◆)	IO_L36N_4	AL28	I/O
4	N.C. (◆)	IO_L36P_4	AM28	I/O
4	N.C. (◆)	IO_L37N_4	AN28	I/O
4	N.C. (◆)	IO_L37P_4	AP28	I/O
4	IO_L38N_4	IO_L38N_4	AK27	I/O
4	IO_L38P_4	IO_L38P_4	AL27	I/O
4	N.C. (◆)	IO_L39N_4	AH24	I/O
4	N.C. (◆)	IO_L39P_4	AJ24	I/O
4	N.C. (◆)	IO_L40N_4	AN24	I/O
4	N.C. (◆)	IO_L40P_4	AP24	I/O