AMD Xilinx - XC3S200-4PQG208I Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	480
Number of Logic Elements/Cells	4320
Total RAM Bits	221184
Number of I/O	141
Number of Gates	200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s200-4pqg208i

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ESD Protection

Clamp diodes protect all device pads against damage from Electro-Static Discharge (ESD) as well as excessive voltage transients. Each I/O has two clamp diodes: One diode extends P-to-N from the pad to V_{CCO} and a second diode extends N-to-P from the pad to GND. During operation, these diodes are normally biased in the off state. These clamp diodes are always connected to the pad, regardless of the signal standard selected. The presence of diodes limits the ability of Spartan-3 FPGA I/Os to tolerate high signal voltages. The V_{IN} absolute maximum rating in Table 28, page 58 specifies the voltage range that I/Os can tolerate.

Slew Rate Control and Drive Strength

Two options, FAST and SLOW, control the output slew rate. The FAST option supports output switching at a high rate. The SLOW option reduces bus transients. These options are only available when using one of the LVCMOS or LVTTL standards, which also provide up to seven different levels of current drive strength: 2, 4, 6, 8, 12, 16, and 24 mA. Choosing the appropriate drive strength level is yet another means to minimize bus transients.

Table 7 shows the drive strengths that the LVCMOS and LVTTL standards support.

Table 7: **Programmable Output Drive Current**

Signal Standard (IOSTANDARD)	Current Drive (mA)						
	2	4	6	8	12	16	24
LVTTL	✓	✓	✓	✓	✓	✓	✓
LVCMOS33	✓	✓	✓	✓	✓	✓	✓
LVCMOS25	✓	✓	✓	✓	✓	✓	✓
LVCMOS18	✓	✓	✓	✓	✓	✓	–
LVCMOS15	✓	✓	✓	✓	✓	–	–
LVCMOS12	✓	✓	✓	–	–	–	–

Boundary-Scan Capability

All Spartan-3 FPGA IOBs support boundary-scan testing compatible with IEEE 1149.1 standards. During boundary- scan operations such as EXTEST and HIGHZ the I/O pull-down resistor is active. For more information, see Boundary-Scan (JTAG) Mode, page 50, and refer to the “Using Boundary-Scan and BSDL Files” chapter in UG331.

SelectIO Interface Signal Standards

The IOBs support 18 different single-ended signal standards, as listed in Table 8. Furthermore, the majority of IOBs can be used in specific pairs supporting any of eight differential signal standards, as shown in Table 9.

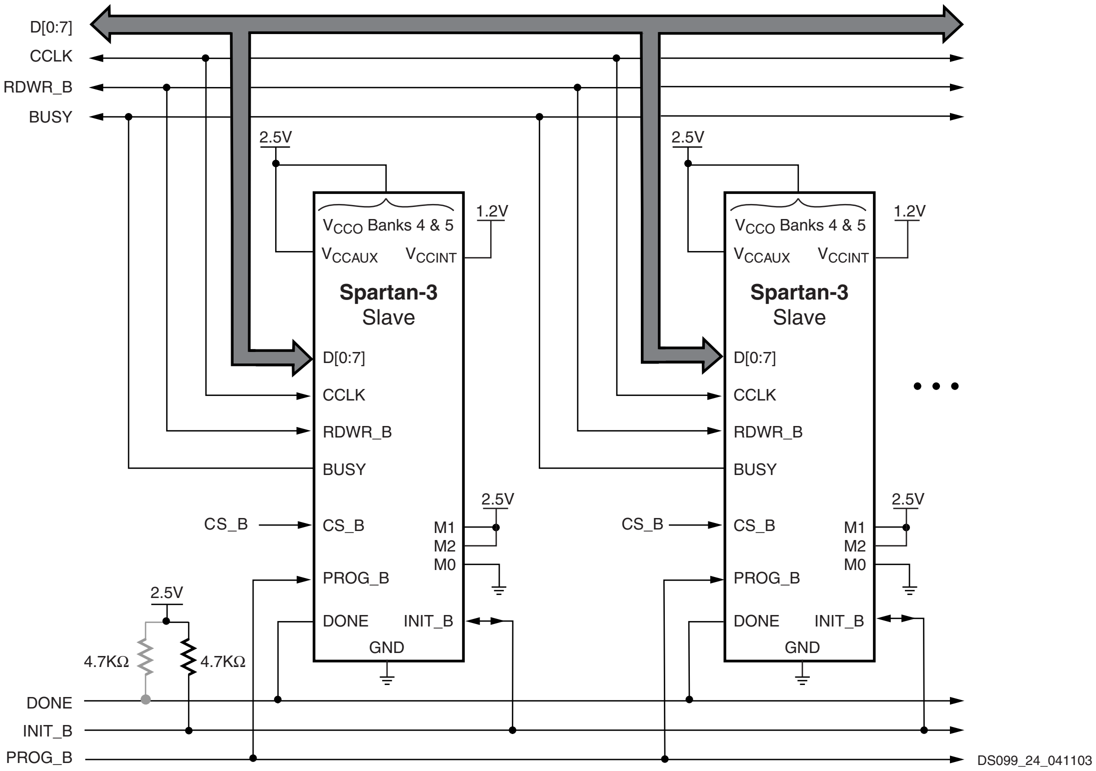
To define the SelectIO™ interface signaling standard in a design, set the IOSTANDARD attribute to the appropriate setting. Xilinx provides a variety of different methods for applying the IOSTANDARD for maximum flexibility. For a full description of different methods of applying attributes to control IOSTANDARD, refer to the “Using I/O Resources” chapter in UG331.

Together with placing the appropriate I/O symbol, two externally applied voltage levels, V_{CCO} and V_{REF}, select the desired signal standard. The V_{CCO} lines provide current to the output driver. The voltage on these lines determines the output voltage swing for all standards except GTL and GTLP.

All single-ended standards except the LVCMOS, LVTTL, and PCI varieties require a Reference Voltage (V_{REF}) to bias the input-switching threshold. Once a configuration data file is loaded into the FPGA that calls for the I/Os of a given bank to use such a signal standard, a few specifically reserved I/O pins on the same bank automatically convert to V_{REF} inputs. When using one of the LVCMOS standards, these pins remain I/Os because the V_{CCO} voltage biases the input-switching threshold, so there is no need for V_{REF}. Select the V_{CCO} and V_{REF} levels to suit the desired single-ended standard according to Table 8.

(e.g. all configuration pins taken together) when operating in the User mode. This is accomplished by setting the *Persist* option to *Yes*.

Multiple FPGAs can be configured using the Slave Parallel mode and can be made to start-up simultaneously. Figure 27 shows the device connections. To configure multiple devices in this way, wire the individual CCLK, Data, RDWR_B, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by deasserting the CS_B pin of each device in turn and writing the appropriate data.



Notes:

1. There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.
2. If the FPGAs use different configuration data files, configure them in sequence by first asserting the CS_B of one FPGA then asserting the CS_B of the other FPGA.
3. For information on how to program the FPGA using 3.3V signals and power, see 3.3V-Tolerant Configuration Interface.

Figure 27: **Connection Diagram for Slave Parallel Configuration**

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
HSLVDCI_25			0.27	0.31	ns
HSLVDCI_33			0.28	0.32	ns
HSTL_I			0.60	0.69	ns
HSTL_I_DCI			0.59	0.68	ns
HSTL_III			0.19	0.22	ns
HSTL_III_DCI			0.20	0.23	ns
HSTL_I_18			0.18	0.21	ns
HSTL_I_DCI_18			0.17	0.19	ns
HSTL_II_18			–0.02	–0.01	ns
HSTL_II_DCI_18			0.75	0.86	ns
HSTL_III_18			0.28	0.32	ns
HSTL_III_DCI_18			0.28	0.32	ns
LVCMOS12	Slow	2 mA	7.60	8.73	ns
		4 mA	7.42	8.53	ns
		6 mA	6.67	7.67	ns
	Fast	2 mA	3.16	3.63	ns
		4 mA	2.70	3.10	ns
		6 mA	2.41	2.77	ns
LVCMOS15	Slow	2 mA	4.55	5.23	ns
		4 mA	3.76	4.32	ns
		6 mA	3.57	4.11	ns
		8 mA	3.55	4.09	ns
		12 mA	3.00	3.45	ns
	Fast	2 mA	3.11	3.57	ns
		4 mA	1.71	1.96	ns
		6 mA	1.44	1.66	ns
		8 mA	1.26	1.44	ns
		12 mA	1.11	1.27	ns
LVDCI_15			1.51	1.74	ns
LVDCI_DV2_15			1.32	1.52	ns

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair** ***(Cont'd)***

Signal Standard (IOSTANDARD)			Package				
			VQ100	TQ144	PQ208	CP132	FT256, FG320, FG456, FG676, FG900, FG1156
LVDCI_15			6	6	6	6	14
LVDCI_DV2_15			6	6	6	6	14
HSLVDCI_15			6	6	6	6	14
LVCMOS18	Slow	2	19	13	13	29	64
		4	13	8	8	19	34
		6	8	8	8	9	22
		8	7	7	7	9	18
		12	5	5	5	5	13
		16	5	5	5	5	10
	Fast	2	13	13	13	19	36
		4	8	8	8	13	21
		6	8	8	8	8	13
		8	7	7	7	7	10
		12	5	5	5	5	9
		16	5	5	5	5	6
LVDCI_18			7	7	7	7	10
LVDCI_DV2_18			7	7	7	7	10
HSLVDCI_18			7	7	7	7	10
LVCMOS25	Slow	2	28	16	12	42	76
		4	13	10	10	19	46
		6	13	8	8	19	33
		8	7	7	7	9	24
		12	6	6	6	9	18
		16	6	6	6	6	11
		24	5	5	5	5	7
	Fast	2	17	12	12	26	42
		4	10	10	10	13	20
		6	8	8	8	13	15
		8	7	7	7	7	13
		12	6	6	6	6	11
		16	6	6	6	6	8
		24	5	5	5	5	5
LVDCI_25			7	7	7	7	11
LVDCI_DV2_25			7	7	7	7	11
HSLVDCI_25			7	7	7	7	11

Internal Logic Timing

Table 51: **CLB Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	–	0.63	–	0.72	ns
Setup Times						
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.46	–	0.53	–	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.27	–	1.57	–	ns
Hold Times						
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	–	0	–	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0.25	–	0.29	–	ns
Clock Timing						
T_{CH}	CLB CLK signal High pulse width	0.69	∞	0.79	∞	ns
T_{CL}	CLB CLK signal Low pulse width	0.69	∞	0.79	∞	ns
F_{TOG}	Maximum toggle frequency (for export control)	–	725	–	630	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	–	0.53	–	0.61	ns
Set/Reset Pulse Width						
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	0.76	–	0.87	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. The timing shown is for SLICEM.
3. For minimums, use the values reported by the Xilinx timing analyzer.

Table 61: **Switching Characteristics for the DFS**

Symbol	Description	Frequency Mode	Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_FX_LF	Frequency for the CLKFX and CLKFX180 outputs	Low	All	18	210	18	210	MHz
CLKOUT_FREQ_FX_HF		High	All	210	326[2]	210	307[2]	MHz
Output Clock Jitter								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs	All	All	Note 3	Note 3	Note 3	Note 3	ps
Duty Cycle[4]								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs	All	XC3S50	–	±100	–	±100	ps
			XC3S200	–	±100	–	±100	ps
			XC3S400	–	±250	–	±250	ps
			XC3S1000	–	±400	–	±400	ps
			XC3S1500	–	±400	–	±400	ps
			XC3S2000	–	±400	–	±400	ps
			XC3S4000	–	±400	–	±400	ps
			XC3S5000	–	±400	–	±400	ps
Phase Alignment								
CLKOUT_PHASE	Phase offset between the DFS output and the CLK0 output	All	All	–	±300	–	±300	ps
Lock Time								
LOCK_DLL_FX	When using the DFS in conjunction with the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.	All	All	–	10.0	–	10.0	ms
LOCK_FX	When using the DFS without the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. By asserting the LOCKED signal, the DFS indicates valid CLKFX and CLKFX180 signals.	All	All	–	10.0	–	10.0	ms

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32 and Table 60.
2. Mask revisions prior to the E mask revision have a CLKOUT_FREQ_FX_HF max of 280 MHz. See Mask and Fab Revisions, page 58.
3. Use the DCM Clocking Wizard in the ISE software for a Spartan-3 device specific number. Jitter number assumes 150 ps of input clock jitter.
4. The CLKFX and CLKFX180 outputs always approximate 50% duty cycles.
5. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) is in use.

Phase Shifter (PS)

Phase shifter operation is only supported if the DLL is in low-frequency mode, see Table 58. Fixed phase shift requires ISE software version 10.1.03 (or later).

Table 62: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Frequency Mode/ F_{CLKIN} Range		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Operating Frequency Ranges								
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	Low		1	167	1	167	MHz
Input Pulse Requirements								
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	Low	$F_{CLKIN} \leq 100$ MHz	40%	60%	40%	60%	-
			$F_{CLKIN} > 100$ MHz	45%	55%	45%	55%	-

Table 63: **Switching Characteristics for the PS in Variable or Fixed Phase Shift Mode**

Symbol	Description	Frequency Mode/ F_{CLKIN} Range	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Phase Shifting Range							
FINE_SHIFT_RANGE	Phase shift range	Low	–	10.0	–	10.0	ns
Lock Time							
LOCK_DLL_PS	When using the PS in conjunction with the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.	18 MHz $\leq F_{CLKIN} \leq$ 30 MHz	–	3.28	–	3.28	ms
		30 MHz $< F_{CLKIN} \leq$ 40 MHz	–	2.56	–	2.56	ms
		40 MHz $< F_{CLKIN} \leq$ 50 MHz	–	1.60	–	1.60	ms
		50 MHz $< F_{CLKIN} \leq$ 60 MHz	–	1.00	–	1.00	ms
		60 MHz $< F_{CLKIN} \leq$ 165 MHz	–	0.88	–	0.88	ms
LOCK_DLL_PS_FX	When using the PS in conjunction with the DLL and DFS: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.	Low	–	10.40	–	10.40	ms

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32 and Table 62.
2. The PS specifications in this table apply when the PS attribute CLKOUT_PHASE_SHIFT= VARIABLE or FIXED.

Table 72: **Dual-Purpose Configuration Pins for Parallel (SelectMAP) Configuration Modes *(Cont'd)***

<table>
<tr><th>Pin Name</th><th>Direction</th><th>Description</th></tr>
<tr><td>BUSY</td><td>Output</td><td>Configuration Data Rate Control for Parallel Mode:
In the Slave and Master Parallel modes, BUSY throttles the rate at which configuration data is loaded. BUSY is only necessary if CCLK operates at greater than 50 MHz. Ignore BUSY for frequencies of 50 MHz and below.
When BUSY is Low, the FPGA accepts the next configuration data byte on the next rising CCLK edge for which CS_B and RDWR_B are Low. When BUSY is High, the FPGA ignores the next configuration data byte. The next configuration data value must be held or reloaded until the next rising CCLK edge when BUSY is Low. When CS_B is High, BUSY is in a high impedance state.
<table>
<tr><th>BUSY</th><th>Function</th></tr>
<tr><td>0</td><td>The FPGA is ready to accept the next configuration data byte.</td></tr>
<tr><td>1</td><td>The FPGA is busy processing the current configuration data byte and is not ready to accept the next byte.</td></tr>
<tr><td>Hi-Z</td><td>If CS_B is High, then BUSY is high impedance.</td></tr>
</table>
This signal is located in Bank 4 and its output voltage is determined by VCCO_4. The BitGen option Persist permits this pin to retain its configuration function in the User mode.</td></tr>
<tr><td>INIT_B</td><td>Bidirectional (open-drain)</td><td>Initializing Configuration Memory/Configuration Error (active-Low):
See description under Serial Configuration Modes, page 112.</td></tr>
</table>

JTAG Configuration Mode

In the JTAG configuration mode all dual-purpose configuration pins are unused and behave exactly like user-I/O pins, as shown in Table 79. See Table 75 for Mode Select pin settings required for JTAG mode.

Dual-Purpose Pin I/O Standard During Configuration

During configuration, the dual-purpose pins default to CMOS input and output levels for the associated VCCO voltage supply pins. For example, in the Parallel configuration modes, both VCCO_4 and VCCO_5 are required. If connected to +2.5V, then the associated pins conform to the LVCMOS25 I/O standard. If connected to +3.3V, then the pins drive LVCMOS output levels and accept either LVTTL or LVCMOS input levels.

Dual-Purpose Pin Behavior After Configuration

After the configuration process completes, these pins, if they were borrowed during configuration, become user-I/O pins available to the application. If a dual-purpose configuration pin is not used during the configuration process—*i.e.*, the parallel configuration pins when using serial mode—then the pin behaves exactly like a general-purpose I/O. See I/O Type: Unrestricted, General-purpose I/O Pins section.

DCI: User I/O or Digitally Controlled Impedance Resistor Reference Input

These pins are individual user-I/O pins unless one of the I/O standards used in the bank requires the Digitally Controlled Impedance (DCI) feature. If DCI is used, then 1% precision resistors connected to the VRP_# and VRN_# pins match the impedance on the input or output buffers of the I/O standards that use DCI within the bank. The '#' character in the pin name indicates the associated I/O bank and is an integer, 0 through 7.

There are two DCI pins per I/O bank, except in the CP132 and TQ144 packages, which do not have any DCI inputs for Bank 5.

VRP and VRN Impedance Resistor Reference Inputs

The 1% precision impedance-matching resistor attached to the VRP_# pin controls the pull-up impedance of PMOS transistor in the input or output buffer. Consequently, the VRP_# pin must connect to ground. The 'P' character in "VRP" indicates that this pin controls the I/O buffer's PMOS transistor impedance. The VRP_# pin is used for both single and split termination.

The 1% precision impedance-matching resistor attached to the VRN_# pin controls the pull-down impedance of NMOS transistor in the input or output buffer. Consequently, the VRN_# pin must connect to VCCO. The ‘N’ character in “VRN” indicates that this pin controls the I/O buffer’s NMOS transistor impedance. The VRN_# pin is only used for split termination.

Each VRN or VRP reference input requires its own resistor. A single resistor cannot be shared between VRN or VRP pins associated with different banks.

During configuration, these pins behave exactly like user-I/O pins. The associated DCI behavior is not active or valid until after configuration completes.

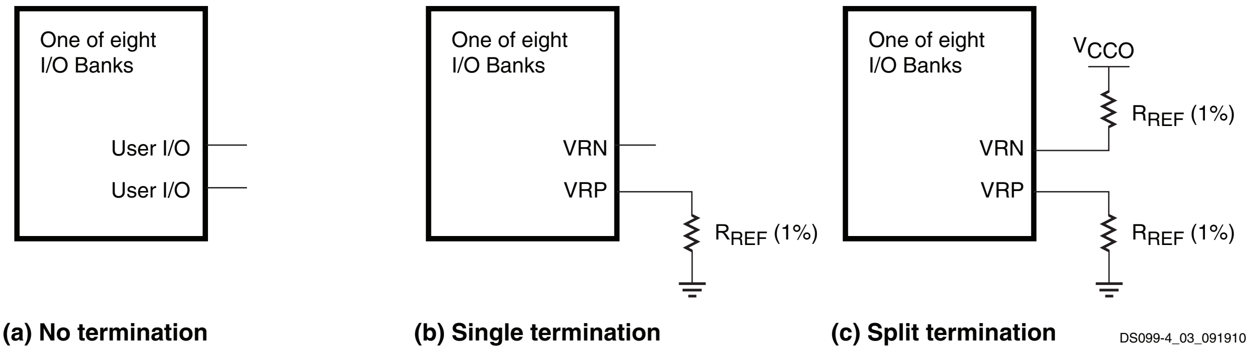
Also see Digitally Controlled Impedance (DCI), page 16.

DCI Termination Types

If the I/O in an I/O bank do not use the DCI feature, then no external resistors are required and both the VRP_# and VRN_# pins are available for user I/O, as shown in section [a] of Figure 42.

If the I/O standards within the associated I/O bank require single termination—such as GTL_DCI, GTLP_DCI, or HSTL_III_DCI—then only the VRP_# signal connects to a 1% precision impedance-matching resistor, as shown in section [b] of Figure 42. A resistor is not required for the VRN_# pin.

Finally, if the I/O standards with the associated I/O bank require split termination—such as HSTL_I_DCI, SSTL2_I_DCI, SSTL2_II_DCI, or LVDS_25_DCI and LVDSEXT_25_DCI receivers—then both the VRP_# and VRN_# pins connect to separate 1% precision impedance-matching resistors, as shown in section [c] of Figure 42. Neither pin is available for user I/O.



(a) No termination **(b) Single termination** **(c) Split termination**

Figure 42: **DCI Termination Types**

GCLK: Global Clock Buffer Inputs or General-Purpose I/O Pins

These pins are user-I/O pins unless they specifically connect to one of the eight low-skew global clock buffers on the device, specified using the IBUFG primitive.

There are eight GCLK pins per device and two each appear in the top-edge banks, Bank 0 and 1, and the bottom-edge banks, Banks 4 and 5. See Figure 40 for a picture of bank labeling.

During configuration, these pins behave exactly like user-I/O pins.

Also see Global Clock Network, page 42.

CONFIG: Dedicated Configuration Pins

The dedicated configuration pins control the configuration process and are not available as user-I/O pins. Every package has seven dedicated configuration pins. All CONFIG-type pins are powered by the +2.5V VCCAUX supply.

Also see Configuration, page 46.

HSWAP_EN: Disable Pull-up Resistors During Configuration

As shown in Table 76, a Low on this asynchronous pin enables pull-up resistors on all user I/Os not actively involved in the configuration process, although only until device configuration completes. A High disables the pull-up resistors during configuration, which is the desired state for some applications.

The dedicated configuration CONFIG pins (CCLK, DONE, PROG_B, HSWAP_EN, M2, M1, M0), the JTAG pins (TDI, TMS, TCK, TDO) and the INIT_B always have active pull-up resistors during configuration, regardless of the value on HSWAP_EN.

After configuration, HSWAP_EN becomes a "don’t care" input and any pull-up resistors previously enabled by HSWAP_EN are disabled. If a user I/O in the application requires a pull-up resistor after configuration, place a PULLUP primitive on the associated I/O pin or, for some pins, set the associated bitstream generator option.

Table 76: **HSWAP_EN Encoding**

HSWAP_EN	Function
During Configuration	
0	Enable pull-up resistors on all pins not actively involved in the configuration process. Pull-ups are only active until configuration completes. See Table 79.
1	No pull-up resistors during configuration.
After Configuration, User Mode	
X	This pin has no function except during device configuration.

Notes:

1. X = don’t care, either 0 or 1.

The Bitstream generator option HswapenPin determines whether a pull-up resistor to VCCAUX, a pull-down resistor, or no resistor is present on HSWAP_EN after configuration.

JTAG: Dedicated JTAG Port Pins

Table 77: **JTAG Pin Descriptions**

Pin Name	Direction	Description	Bitstream Generation Option
TCK	Input	**Test Clock:** The TCK clock signal synchronizes all boundary scan operations on its rising edge.	The BitGen option **TckPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.
TDI	Input	**Test Data Input:** TDI is the serial data input for all JTAG instruction and data registers. This input is sampled on the rising edge of TCK.	The BitGen option **TdiPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.
TMS	Input	**Test Mode Select:** The TMS input controls the sequence of states through which the JTAG TAP state machine passes. This input is sampled on the rising edge of TCK.	The BitGen option **TmsPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.
TDO	Output	**Test Data Output:** The TDO pin is the data output for all JTAG instruction and data registers. This output is sampled on the rising edge of TCK. The TDO output is an active totem-pole driver and is not like the open-collector TDO output on Virtex®-II Pro FPGAs.	The BitGen option **TdoPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.

These pins are dedicated connections to the four-wire IEEE 1532/IEEE 1149.1 JTAG port, shown in Figure 43 and described in Table 77. The JTAG port is used for boundary-scan testing, device configuration, application debugging, and possibly an additional serial port for the application. These pins are dedicated and are not available as user-I/O pins. Every package has four dedicated JTAG pins and these pins are powered by the +2.5V VCCAUX supply.

For additional information on JTAG configuration, see Boundary-Scan (JTAG) Mode, page 50.

User I/Os by Bank

Table 92 indicates how the available user-I/O pins are distributed between the eight I/O banks on the TQ144 package.

Table 92: **User I/Os Per Bank in TQ144 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	10	5	0	2	1	2
	1	9	4	0	2	1	2
Right	2	14	10	0	2	2	0
	3	15	11	0	2	2	0
Bottom	4	11	0	6	2	1	2
	5	9	0	6	0	1	2
Left	6	14	10	0	2	2	0
	7	15	11	0	2	2	0

TQ144 Footprint

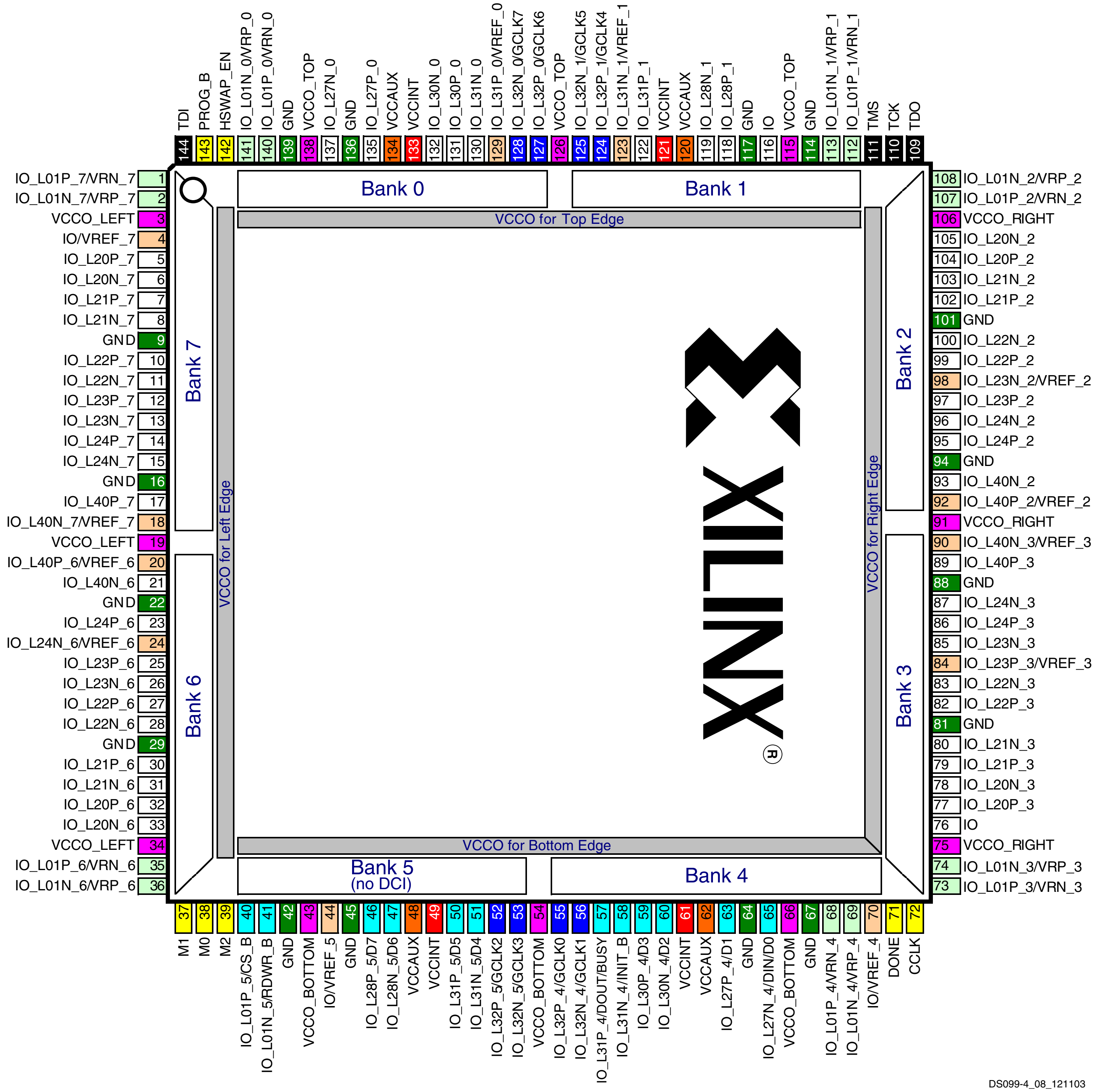


Figure 46: **TQ144 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

51	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	12	**VREF:** User I/O or input voltage reference for bank
14	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input	12	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	16	**GND:** Ground	4	**VCCAUX:** Auxiliary voltage supply (+2.5V)

PQ208: 208-lead Plastic Quad Flat Pack

The 208-lead plastic quad flat package, PQ208, supports three different Spartan-3 devices, including the XC3S50, the XC3S200, and the XC3S400. The footprints for the XC3S200 and XC3S400 are identical, as shown in Table 93 and Figure 47. The XC3S50, however, has fewer I/O pins resulting in 17 unconnected pins on the PQ208 package, labeled as "N.C." In Table 93 and Figure 47, these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in Table 93 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S50 pinout and the pinout for the XC3S200 and XC3S400, then that difference is highlighted in Table 93. If the table entry is shaded grey, then there is an unconnected pin on the XC3S50 that maps to a user-I/O pin on the XC3S200 and XC3S400. If the table entry is shaded tan, then the unconnected pin on the XC3S50 maps to a VREF-type pin on the XC3S200 and XC3S400. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S50 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S50 device to an XC3S200 or XC3S400 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip

Pinout Table

Table 93: **PQ208 Package Pinout**

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
0	IO	IO	P189	I/O
0	IO	IO	P197	I/O
0	N.C. (◆)	IO/VREF_0	P200	VREF
0	IO/VREF_0	IO/VREF_0	P205	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	P204	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	P203	DCI
0	IO_L25N_0	IO_L25N_0	P199	I/O
0	IO_L25P_0	IO_L25P_0	P198	I/O
0	IO_L27N_0	IO_L27N_0	P196	I/O
0	IO_L27P_0	IO_L27P_0	P194	I/O
0	IO_L30N_0	IO_L30N_0	P191	I/O
0	IO_L30P_0	IO_L30P_0	P190	I/O
0	IO_L31N_0	IO_L31N_0	P187	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	P185	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	P184	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	P183	GCLK
0	VCCO_0	VCCO_0	P188	VCCO
0	VCCO_0	VCCO_0	P201	VCCO
1	IO	IO	P167	I/O
1	IO	IO	P175	I/O
1	IO	IO	P182	I/O
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	P162	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	P161	DCI

User I/Os by Bank

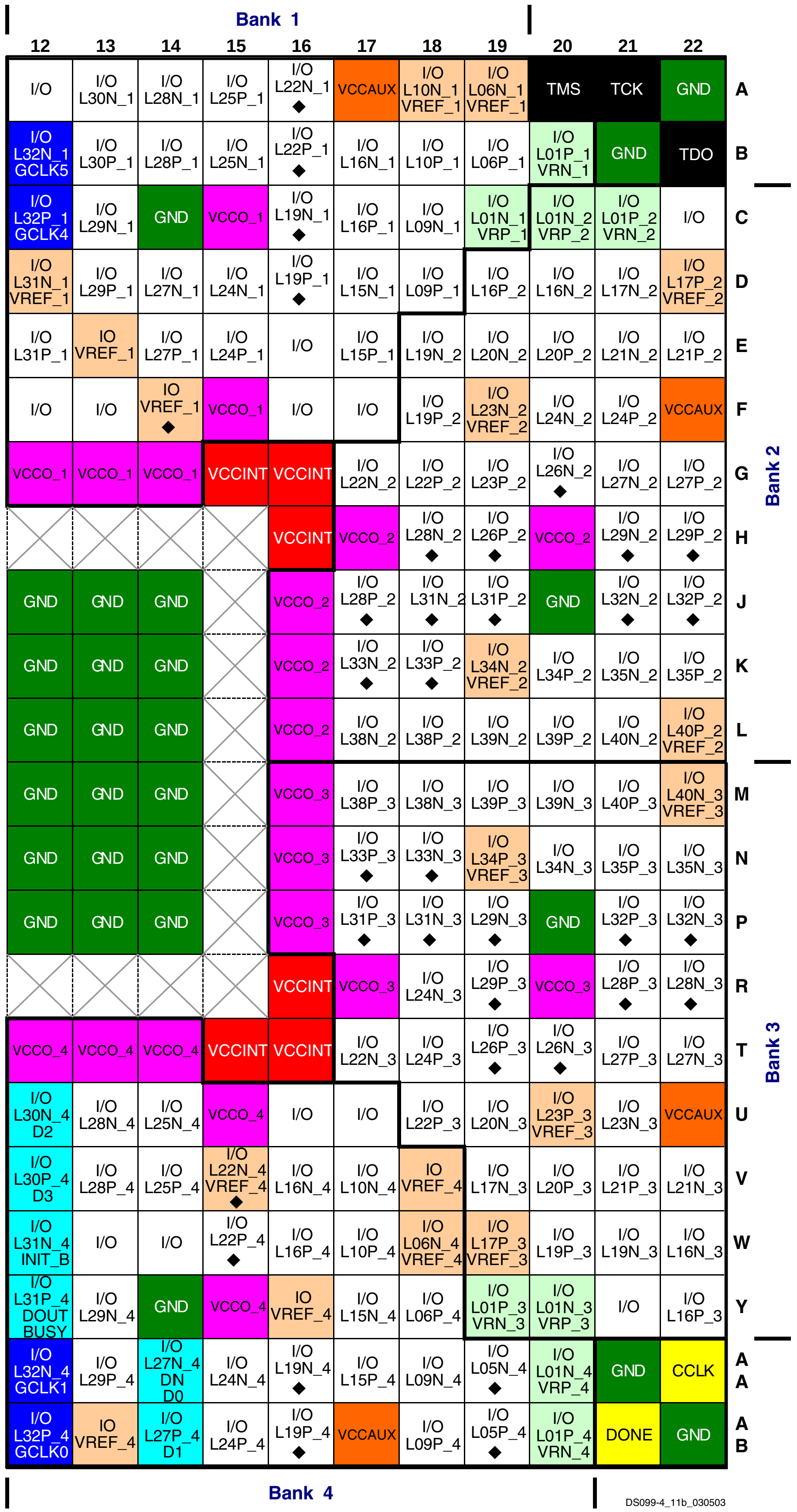
Table 97 indicates how the available user-I/O pins are distributed between the eight I/O banks on the FT256 package.

Table 97: **User I/Os Per Bank in FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	20	13	0	2	3	2
	1	20	13	0	2	3	2
Right	2	23	18	0	2	3	0
	3	23	18	0	2	3	0
Bottom	4	21	8	6	2	3	2
	5	20	7	6	2	3	2
Left	6	23	18	0	2	3	0
	7	23	18	0	2	3	0

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
3	IO_L16P_3	IO_L16P_3	Y22	I/O
3	IO_L17N_3	IO_L17N_3	V19	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	W19	VREF
3	IO_L19N_3	IO_L19N_3	W21	I/O
3	IO_L19P_3	IO_L19P_3	W20	I/O
3	IO_L20N_3	IO_L20N_3	U19	I/O
3	IO_L20P_3	IO_L20P_3	V20	I/O
3	IO_L21N_3	IO_L21N_3	V22	I/O
3	IO_L21P_3	IO_L21P_3	V21	I/O
3	IO_L22N_3	IO_L22N_3	T17	I/O
3	IO_L22P_3	IO_L22P_3	U18	I/O
3	IO_L23N_3	IO_L23N_3	U21	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	U20	VREF
3	IO_L24N_3	IO_L24N_3	R18	I/O
3	IO_L24P_3	IO_L24P_3	T18	I/O
3	N.C. (◆)	IO_L26N_3	T20	I/O
3	N.C. (◆)	IO_L26P_3	T19	I/O
3	IO_L27N_3	IO_L27N_3	T22	I/O
3	IO_L27P_3	IO_L27P_3	T21	I/O
3	N.C. (◆)	IO_L28N_3	R22	I/O
3	N.C. (◆)	IO_L28P_3	R21	I/O
3	N.C. (◆)	IO_L29N_3	P19	I/O
3	N.C. (◆)	IO_L29P_3	R19	I/O
3	N.C. (◆)	IO_L31N_3	P18	I/O
3	N.C. (◆)	IO_L31P_3	P17	I/O
3	N.C. (◆)	IO_L32N_3	P22	I/O
3	N.C. (◆)	IO_L32P_3	P21	I/O
3	N.C. (◆)	IO_L33N_3	N18	I/O
3	N.C. (◆)	IO_L33P_3	N17	I/O
3	IO_L34N_3	IO_L34N_3	N20	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	N19	VREF
3	IO_L35N_3	IO_L35N_3	N22	I/O
3	IO_L35P_3	IO_L35P_3	N21	I/O
3	IO_L38N_3	IO_L38N_3	M18	I/O
3	IO_L38P_3	IO_L38P_3	M17	I/O
3	IO_L39N_3	IO_L39N_3	M20	I/O
3	IO_L39P_3	IO_L39P_3	M19	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	M22	VREF
3	IO_L40P_3	IO_L40P_3	M21	I/O
3	VCCO_3	VCCO_3	M16	VCCO



12	13	14	15	16	17	18	19	20	21	22	
I/O	I/O L30N_1	I/O L28N_1	I/O L25P_1	I/O L22N_1 ◆	VCCAUX	I/O L10N_1 VREF_1	I/O L06N_1 VREF_1	TMS	TCK	GND	A
I/O L32N_1 GCLK5	I/O L30P_1	I/O L28P_1	I/O L25N_1	I/O L22P_1 ◆	I/O L16N_1	I/O L10P_1	I/O L06P_1	I/O L01P_1 VRN_1	GND	TDO	B
I/O L32P_1 GCLK4	I/O L29N_1	GND	VCCO_1	I/O L19N_1 ◆	I/O L16P_1	I/O L09N_1	I/O L01N_1 VRP_1	I/O L01N_2 VRP_2	I/O L01P_2 VRN_2	I/O	C
I/O L31N_1 VREF_1	I/O L29P_1	I/O L27N_1	I/O L24N_1	I/O L19P_1 ◆	I/O L15N_1	I/O L09P_1	I/O L16P_2	I/O L16N_2	I/O L17N_2	I/O L17P_2 VREF_2	D
I/O L31P_1	IO VREF_1	I/O L27P_1	I/O L24P_1	I/O	I/O L15P_1	I/O L19N_2	I/O L20N_2	I/O L20P_2	I/O L21N_2	I/O L21P_2	E
I/O	I/O	IO VREF_1 ◆	VCCO_1	I/O	I/O	I/O L19P_2	I/O L23N_2 VREF_2	I/O L24N_2	I/O L24P_2	VCCAUX	F
VCCO_1	VCCO_1	VCCO_1	VCCINT	VCCINT	I/O L22N_2	I/O L22P_2	I/O L23P_2	I/O L26N_2 ◆	I/O L27N_2	I/O L27P_2	G
				VCCINT	VCCO_2	I/O L28N_2 ◆	I/O L26P_2 ◆	VCCO_2	I/O L29N_2 ◆	I/O L29P_2 ◆	H
GND	GND	GND		VCCO_2	I/O L28P_2 ◆	I/O L31N_2 ◆	I/O L31P_2 ◆	GND	I/O L32N_2 ◆	I/O L32P_2 ◆	J
GND	GND	GND		VCCO_2	I/O L33N_2 ◆	I/O L33P_2 ◆	I/O L34N_2 VREF_2	I/O L34P_2	I/O L35N_2	I/O L35P_2	K
GND	GND	GND		VCCO_2	I/O L38N_2	I/O L38P_2	I/O L39N_2	I/O L39P_2	I/O L40N_2	I/O L40P_2 VREF_2	L
GND	GND	GND		VCCO_3	I/O L38P_3	I/O L38N_3	I/O L39P_3	I/O L39N_3	I/O L40P_3	I/O L40N_3 VREF_3	M
GND	GND	GND		VCCO_3	I/O L33P_3 ◆	I/O L33N_3 ◆	I/O L34P_3 VREF_3	I/O L34N_3	I/O L35P_3	I/O L35N_3	N
GND	GND	GND		VCCO_3	I/O L31P_3 ◆	I/O L31N_3 ◆	I/O L29N_3 ◆	GND	I/O L32P_3 ◆	I/O L32N_3 ◆	P
				VCCINT	VCCO_3	I/O L24N_3	I/O L29P_3 ◆	VCCO_3	I/O L28P_3 ◆	I/O L28N_3 ◆	R
VCCO_4	VCCO_4	VCCO_4	VCCINT	VCCINT	I/O L22N_3	I/O L24P_3	I/O L26P_3 ◆	I/O L26N_3 ◆	I/O L27P_3	I/O L27N_3	T
I/O L30N_4 D2	I/O L28N_4	I/O L25N_4	VCCO_4	I/O	I/O	I/O L22P_3	I/O L20N_3	I/O L23P_3 VREF_3	I/O L23N_3	VCCAUX	U
I/O L30P_4 D3	I/O L28P_4	I/O L25P_4	I/O L22N_4 VREF_4 ◆	I/O L16N_4	I/O L10N_4	IO VREF_4	I/O L17N_3	I/O L20P_3	I/O L21P_3	I/O L21N_3	V
I/O L31N_4 INIT_B	I/O	I/O	I/O L22P_4 ◆	I/O L16P_4	I/O L10P_4	I/O L06N_4 VREF_4	I/O L17P_3 VREF_3	I/O L19P_3	I/O L19N_3	I/O L16N_3	W
I/O L31P_4 DOUT BUSY	I/O L29N_4	GND	VCCO_4	IO VREF_4	I/O L15N_4	I/O L06P_4	I/O L01P_3 VRN_3	I/O L01N_3 VRP_3	I/O	I/O L16P_3	Y
I/O L32N_4 GCLK1	I/O L29P_4	I/O L27N_4 DN D0	I/O L24N_4	I/O L19N_4 ◆	I/O L15P_4	I/O L09N_4	I/O L05N_4 ◆	I/O L01N_4 VRP_4	GND	CCLK	AA
I/O L32P_4 GCLK0	IO VREF_4	I/O L27P_4 D1	I/O L24P_4	I/O L19P_4 ◆	VCCAUX	I/O L09P_4	I/O L05P_4 ◆	I/O L01P_4 VRN_4	DONE	GND	AB

Figure 52: FG456 Package Footprint (Top View) Continued

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	W12	VCCINT
N/A	VCCINT	VCCINT	M13	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	M14	VCCINT
N/A	VCCINT	VCCINT	W14	VCCINT
N/A	VCCINT	VCCINT	L15	VCCINT
N/A	VCCINT	VCCINT	Y15	VCCINT
N/A	VCCINT	VCCINT	L16	VCCINT
N/A	VCCINT	VCCINT	Y16	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	W17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	W18	VCCINT
N/A	VCCINT	VCCINT	M19	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	P19	VCCINT
N/A	VCCINT	VCCINT	U19	VCCINT
N/A	VCCINT	VCCINT	V19	VCCINT
N/A	VCCINT	VCCINT	W19	VCCINT
N/A	VCCINT	VCCINT	L20	VCCINT
N/A	VCCINT	VCCINT	R20	VCCINT
N/A	VCCINT	VCCINT	T20	VCCINT
N/A	VCCINT	VCCINT	Y20	VCCINT
VCCAUX	CCLK	CCLK	AH28	CONFIG
VCCAUX	DONE	DONE	AJ28	CONFIG
VCCAUX	HSWAP_EN	HSWAP_EN	A3	CONFIG
VCCAUX	M0	M0	AJ3	CONFIG
VCCAUX	M1	M1	AH3	CONFIG
VCCAUX	M2	M2	AK3	CONFIG
VCCAUX	PROG_B	PROG_B	B3	CONFIG
VCCAUX	TCK	TCK	B28	JTAG
VCCAUX	TDI	TDI	C3	JTAG
VCCAUX	TDO	TDO	C28	JTAG
VCCAUX	TMS	TMS	A28	JTAG

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L24P_3	IO_L24P_3	AC26	I/O
3	IO_L26N_3	IO_L26N_3	AA28	I/O
3	IO_L26P_3	IO_L26P_3	AA27	I/O
3	IO_L27N_3	IO_L27N_3	AA30	I/O
3	IO_L27P_3	IO_L27P_3	AA29	I/O
3	IO_L28N_3	IO_L28N_3	AA32	I/O
3	IO_L28P_3	IO_L28P_3	AA31	I/O
3	IO_L29N_3	IO_L29N_3	AA34	I/O
3	IO_L29P_3	IO_L29P_3	AA33	I/O
3	IO_L30N_3	IO_L30N_3	Y29	I/O
3	IO_L30P_3	IO_L30P_3	Y28	I/O
3	IO_L31N_3	IO_L31N_3	Y32	I/O
3	IO_L31P_3	IO_L31P_3	Y31	I/O
3	IO_L32N_3	IO_L32N_3	Y34	I/O
3	IO_L32P_3	IO_L32P_3	Y33	I/O
3	IO_L33N_3	IO_L33N_3	W25	I/O
3	IO_L33P_3	IO_L33P_3	Y26	I/O
3	IO_L34N_3	IO_L34N_3	W29	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	W28	VREF
3	IO_L35N_3	IO_L35N_3	W33	I/O
3	IO_L35P_3	IO_L35P_3	W32	I/O
3	IO_L37N_3	IO_L37N_3	V28	I/O
3	IO_L37P_3	IO_L37P_3	V27	I/O
3	IO_L38N_3	IO_L38N_3	V30	I/O
3	IO_L38P_3	IO_L38P_3	V29	I/O
3	IO_L39N_3	IO_L39N_3	V32	I/O
3	IO_L39P_3	IO_L39P_3	V31	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	V34	VREF
3	IO_L40P_3	IO_L40P_3	V33	I/O
3	N.C. (◆)	IO_L41N_3	AH32	I/O
3	N.C. (◆)	IO_L41P_3	AH31	I/O
3	N.C. (◆)	IO_L44N_3	AD29	I/O
3	N.C. (◆)	IO_L44P_3	AD28	I/O
3	IO_L45N_3	IO_L45N_3	AC34	I/O
3	IO_L45P_3	IO_L45P_3	AC33	I/O
3	IO_L46N_3	IO_L46N_3	AB28	I/O
3	IO_L46P_3	IO_L46P_3	AB27	I/O
3	IO_L47N_3	IO_L47N_3	AB32	I/O
3	IO_L47P_3	IO_L47P_3	AB31	I/O
3	IO_L48N_3	IO_L48N_3	AA24	I/O

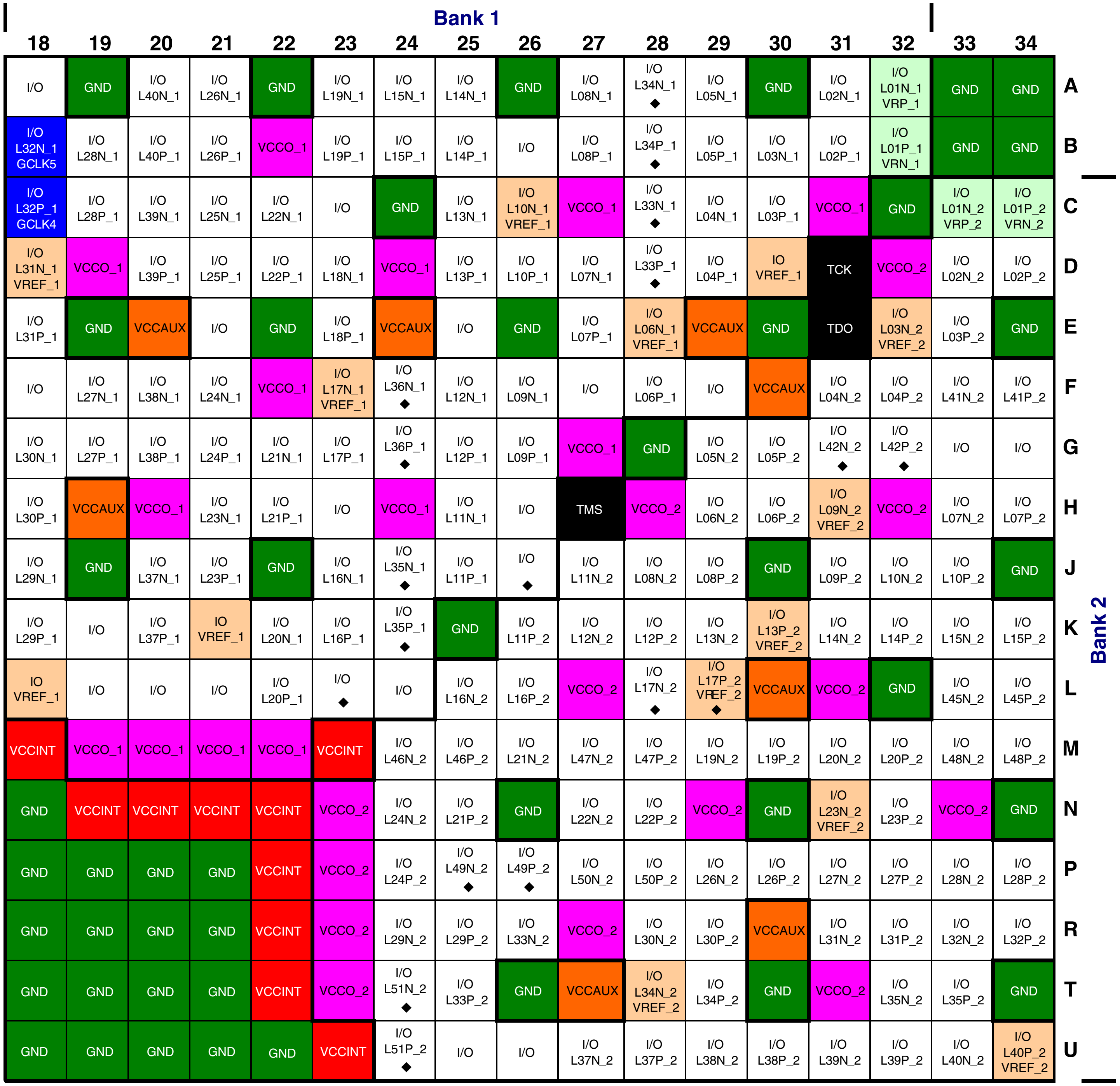
Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
6	IO_L16N_6	IO_L16N_6	AE2	I/O
6	IO_L16P_6	IO_L16P_6	AE1	I/O
6	IO_L17N_6	IO_L17N_6	AD10	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	AD9	VREF
6	IO_L19N_6	IO_L19N_6	AD2	I/O
6	IO_L19P_6	IO_L19P_6	AD1	I/O
6	IO_L20N_6	IO_L20N_6	AC11	I/O
6	IO_L20P_6	IO_L20P_6	AC10	I/O
6	IO_L21N_6	IO_L21N_6	AC8	I/O
6	IO_L21P_6	IO_L21P_6	AC7	I/O
6	IO_L22N_6	IO_L22N_6	AC6	I/O
6	IO_L22P_6	IO_L22P_6	AC5	I/O
6	IO_L23N_6	IO_L23N_6	AC2	I/O
6	IO_L23P_6	IO_L23P_6	AC1	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	AC9	VREF
6	IO_L24P_6	IO_L24P_6	AB10	I/O
6	IO_L25N_6	IO_L25N_6	AB8	I/O
6	IO_L25P_6	IO_L25P_6	AB7	I/O
6	IO_L26N_6	IO_L26N_6	AB4	I/O
6	IO_L26P_6	IO_L26P_6	AB3	I/O
6	IO_L27N_6	IO_L27N_6	AB11	I/O
6	IO_L27P_6	IO_L27P_6	AA11	I/O
6	IO_L28N_6	IO_L28N_6	AA8	I/O
6	IO_L28P_6	IO_L28P_6	AA7	I/O
6	IO_L29N_6	IO_L29N_6	AA6	I/O
6	IO_L29P_6	IO_L29P_6	AA5	I/O
6	IO_L30N_6	IO_L30N_6	AA4	I/O
6	IO_L30P_6	IO_L30P_6	AA3	I/O
6	IO_L31N_6	IO_L31N_6	AA2	I/O
6	IO_L31P_6	IO_L31P_6	AA1	I/O
6	IO_L32N_6	IO_L32N_6	Y11	I/O
6	IO_L32P_6	IO_L32P_6	Y10	I/O
6	IO_L33N_6	IO_L33N_6	Y4	I/O
6	IO_L33P_6	IO_L33P_6	Y3	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	Y2	VREF
6	IO_L34P_6	IO_L34P_6	Y1	I/O
6	IO_L35N_6	IO_L35N_6	Y9	I/O
6	IO_L35P_6	IO_L35P_6	W10	I/O
6	IO_L36N_6	IO_L36N_6	W7	I/O
6	IO_L36P_6	IO_L36P_6	W6	I/O

Top Right Corner of FG1156 Package (Top View)

All Devices

12	**DUAL:** Configuration pin, then possible user I/O
16	**DCI:** User I/O or reference resistor input for bank
8	**GCLK:** User I/O or global clock buffer input
7	**CONFIG:** Dedicated configuration pins
4	**JTAG:** Dedicated JTAG port pins
104	**VCCO:** Output voltage supply for bank
40	**VCCINT:** Internal core voltage supply (+1.2V)
32	**VCCAUX:** Auxiliary voltage supply (+2.5V)
184	**GND:** Ground



Bank 1

Bank 2

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
I/O	GND	I/O L40N_1	I/O L26N_1	GND	I/O L19N_1	I/O L15N_1	I/O L14N_1	GND	I/O L08N_1	I/O L34N_1 ◆	I/O L05N_1	GND	I/O L02N_1	I/O L01N_1 VRP_1	GND	GND	A
I/O L32N_1 GCLK5	I/O L28N_1	I/O L40P_1	I/O L26P_1	VCCO_1	I/O L19P_1	I/O L15P_1	I/O L14P_1	I/O	I/O L08P_1	I/O L34P_1 ◆	I/O L05P_1	I/O L03N_1	I/O L02P_1	I/O L01P_1 VRN_1	GND	GND	B
I/O L32P_1 GCLK4	I/O L28P_1	I/O L39N_1	I/O L25N_1	I/O L22N_1	I/O	GND	I/O L13N_1	I/O L10N_1 VREF_1	VCCO_1	I/O L33N_1 ◆	I/O L04N_1	I/O L03P_1	VCCO_1	GND	I/O L01N_2 VRP_2	I/O L01P_2 VRN_2	C
I/O L31N_1 VREF_1	VCCO_1	I/O L39P_1	I/O L25P_1	I/O L22P_1	I/O L18N_1	VCCO_1	I/O L13P_1	I/O L10P_1	I/O L07N_1	I/O L33P_1 ◆	I/O L04P_1	IO VREF_1	TCK	VCCO_2	I/O L02N_2	I/O L02P_2	D
I/O L31P_1	GND	VCCAUX	I/O	GND	I/O L18P_1	VCCAUX	I/O	GND	I/O L07P_1	I/O L06N_1 VREF_1	VCCAUX	GND	TDO	I/O L03N_2 VREF_2	I/O L03P_2	GND	E
I/O	I/O L27N_1	I/O L38N_1	I/O L24N_1	VCCO_1	I/O L17N_1 VREF_1	I/O L36N_1 ◆	I/O L12N_1	I/O L09N_1	I/O	I/O L06P_1	I/O	VCCAUX	I/O L04N_2	I/O L04P_2	I/O L41N_2	I/O L41P_2	F
I/O L30N_1	I/O L27P_1	I/O L38P_1	I/O L24P_1	I/O L21N_1	I/O L17P_1	I/O L36P_1 ◆	I/O L12P_1	I/O L09P_1	VCCO_1	GND	I/O L05N_2	I/O L05P_2	I/O L42N_2 ◆	I/O L42P_2 ◆	I/O	I/O	G
I/O L30P_1	VCCAUX	VCCO_1	I/O L23N_1	I/O L21P_1	I/O	VCCO_1	I/O L11N_1	I/O	TMS	VCCO_2	I/O L06N_2	I/O L06P_2	I/O L09N_2 VREF_2	VCCO_2	I/O L07N_2	I/O L07P_2	H
I/O L29N_1	GND	I/O L37N_1	I/O L23P_1	GND	I/O L16N_1	I/O L35N_1 ◆	I/O L11P_1	I/O ◆	I/O L11N_2	I/O L08N_2	I/O L08P_2	GND	I/O L09P_2	I/O L10N_2	I/O L10P_2	GND	J
I/O L29P_1	I/O	I/O L37P_1	IO VREF_1	I/O L20N_1	I/O L16P_1	I/O L35P_1 ◆	GND	I/O L11P_2	I/O L12N_2	I/O L12P_2	I/O L13N_2	I/O L13P_2 VREF_2	I/O L14N_2	I/O L14P_2	I/O L15N_2	I/O L15P_2	K
IO VREF_1	I/O	I/O	I/O	I/O L20P_1	I/O ◆	I/O	I/O L16N_2	I/O L16P_2	VCCO_2	I/O L17N_2 ◆	I/O L17P_2 VREF_2 ◆	VCCAUX	VCCO_2	GND	I/O L45N_2	I/O L45P_2	L
VCCINT	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCINT	I/O L46N_2	I/O L46P_2	I/O L21N_2	I/O L47N_2	I/O L47P_2	I/O L19N_2	I/O L19P_2	I/O L20N_2	I/O L20P_2	I/O L48N_2	I/O L48P_2	M
GND	VCCINT	VCCINT	VCCINT	VCCINT	VCCO_2	I/O L24N_2	I/O L21P_2	GND	I/O L22N_2	I/O L22P_2	VCCO_2	GND	I/O L23N_2 VREF_2	I/O L23P_2	VCCO_2	GND	N
GND	GND	GND	GND	VCCINT	VCCO_2	I/O L24P_2	I/O L49N_2 ◆	I/O L49P_2 ◆	I/O L50N_2	I/O L50P_2	I/O L26N_2	I/O L26P_2	I/O L27N_2	I/O L27P_2	I/O L28N_2	I/O L28P_2	P
GND	GND	GND	GND	VCCINT	VCCO_2	I/O L29N_2	I/O L29P_2	I/O L33N_2	VCCO_2	I/O L30N_2	I/O L30P_2	VCCAUX	I/O L31N_2	I/O L31P_2	I/O L32N_2	I/O L32P_2	R
GND	GND	GND	GND	VCCINT	VCCO_2	I/O L51N_2 ◆	I/O L33P_2	GND	VCCAUX	I/O L34N_2 VREF_2	I/O L34P_2	GND	VCCO_2	I/O L35N_2	I/O L35P_2	GND	T
GND	GND	GND	GND	GND	VCCINT	I/O L51P_2 ◆	I/O	I/O	I/O L37N_2	I/O L37P_2	I/O L38N_2	I/O L38P_2	I/O L39N_2	I/O L39P_2	I/O L40N_2	I/O L40P_2 VREF_2	U

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Figure 58: FG1156 Package Footprint (Top View) Continued