Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	480
Number of Logic Elements/Cells	4320
Total RAM Bits	221184
Number of I/O	97
Number of Gates	200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s200-4tqg144c

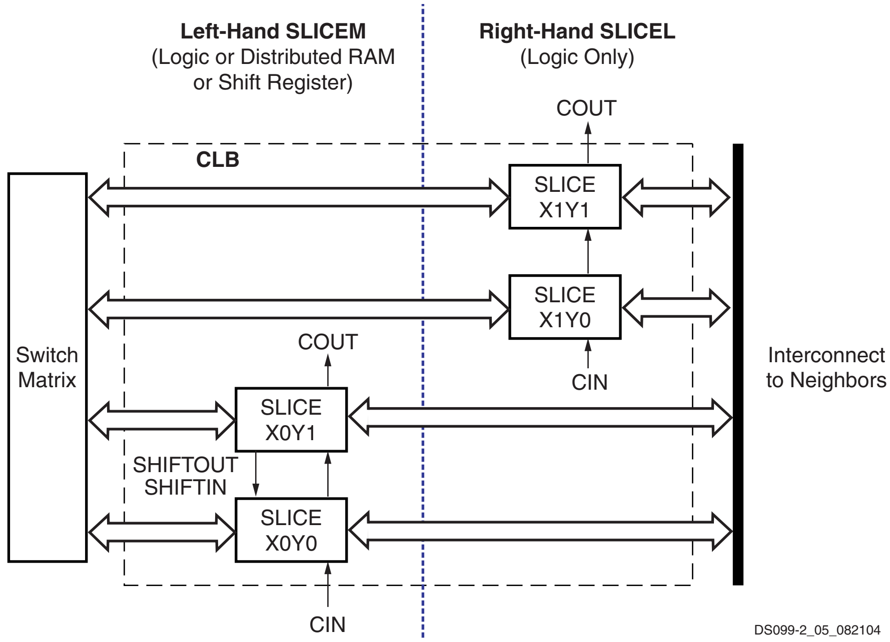

Figure 11: **Arrangement of Slices within the CLB**

Elements Within a Slice

All four slices have the following elements in common: two logic function generators, two storage elements, wide-function multiplexers, carry logic, and arithmetic gates, as shown in Figure 12, page 24. Both the left-hand and right-hand slice pairs use these elements to provide logic, arithmetic, and ROM functions. Besides these, the left-hand pair supports two additional functions: storing data using Distributed RAM and shifting data with 16-bit registers. Figure 12 is a diagram of the left-hand slice; therefore, it represents a superset of the elements and connections to be found in all slices. See Function Generator, page 25 for more information.

The RAM-based function generator—also known as a Look-Up Table or LUT—is the main resource for implementing logic functions. Furthermore, the LUTs in each left-hand slice pair can be configured as Distributed RAM or a 16-bit shift register. For information on the former, refer to the chapter entitled “Using Look-Up Tables as Distributed RAM” in UG331; for information on the latter, refer to the chapter entitled “Using Look-Up Tables as Shift Registers” in UG331. The function generators located in the upper and lower portions of the slice are referred to as the "G" and "F", respectively.

The storage element, which is programmable as either a D-type flip-flop or a level-sensitive latch, provides a means for synchronizing data to a clock signal, among other uses. The storage elements in the upper and lower portions of the slice are called FFY and FFX, respectively.

Wide-function multiplexers effectively combine LUTs in order to permit more complex logic operations. Each slice has two of these multiplexers with F5MUX in the lower portion of the slice and FiMUX in the upper portion. Depending on the slice, FiMUX takes on the name F6MUX, F7MUX, or F8MUX. For more details on the multiplexers, refer to the chapter entitled “Using Dedicated Multiplexers” in UG331.

The carry chain, together with various dedicated arithmetic logic gates, support fast and efficient implementations of math operations. The carry chain enters the slice as CIN and exits as COUT. Five multiplexers control the chain: CYINIT, CY0F, and CYMUXF in the lower portion as well as CY0G and CYMUXG in the upper portion. The dedicated arithmetic logic includes the exclusive-OR gates XORG and XORF (upper and lower portions of the slice, respectively) as well as the AND gates GAND and FAND (upper and lower portions, respectively). For more details on the carry logic, refer to the chapter entitled “Using Carry and Arithmetic Logic” in UG331.

Main Logic Paths

Central to the operation of each slice are two nearly identical data paths, distinguished using the terms *top* and *bottom*. The description that follows uses names associated with the bottom path. (The top path names appear in parentheses.) The basic path originates at an interconnect-switch matrix outside the CLB. Four lines, F1 through F4 (or G1 through G4 on the

The output frequency (f_{CLKFX}) can be expressed as a function of the incoming clock frequency (f_{CLKIN}) as follows:

$$f_{CLKFX} = f_{CLKIN}(CLKFX\_MULTIPLY/CLKFX\_DIVIDE) \quad \textit{Equation 3}$$

Regarding the two attributes, it is possible to assign any combination of integer values, provided that two conditions are met:

- The two values fall within their corresponding ranges, as specified in Table 18.
- The f_{CLKFX} frequency calculated from the above expression accords with the DCM's operating frequency specifications.

For example, if CLKFX_MULTIPLY = 5 and CLKFX_DIVIDE = 3, then the frequency of the output clock signal would be 5/3 that of the input clock signal.

DFS Frequency Modes

The DFS supports two operating modes, High Frequency and Low Frequency, with each specified over a different clock frequency range. The DFS_FREQUENCY_MODE attribute chooses between the two modes. When the attribute is set to LOW, the Low Frequency mode permits the two DFS outputs to operate over a low-to-moderate frequency range. When the attribute is set to HIGH, the High Frequency mode allows both these outputs to operate at the highest possible frequencies.

DFS With or Without the DLL

The DFS component can be used with or without the DLL component:

Without the DLL, the DFS component multiplies or divides the CLKIN signal frequency according to the respective CLKFX_MULTIPLY and CLKFX_DIVIDE values, generating a clock with the new target frequency on the CLKFX and CLKFX180 outputs. Though classified as belonging to the DLL component, the CLKIN input is shared with the DFS component. This case does not employ feedback loop; therefore, it cannot correct for clock distribution delay.

With the DLL, the DFS operates as described in the preceding case, only with the additional benefit of eliminating the clock distribution delay. In this case, a feedback loop from the CLK0 output to the CLKFB input must be present.

The DLL and DFS components work together to achieve this phase correction as follows: Given values for the CLKFX_MULTIPLY and CLKFX_DIVIDE attributes, the DLL selects the delay element for which the output clock edge coincides with the input clock edge whenever mathematically possible. For example, when CLKFX_MULTIPLY = 5 and CLKFX_DIVIDE = 3, the input and output clock edges will coincide every three input periods, which is equivalent in time to five output periods.

Smaller CLKFX_MULTIPLY and CLKFX_DIVIDE values achieve faster lock times. With no factors common to the two attributes, alignment will occur once with every number of cycles equal to the CLKFX_DIVIDE value. Therefore, it is recommended that the user reduce these values by factoring wherever possible. For example, given CLKFX_MULTIPLY = 9 and CLKFX_DIVIDE = 6, removing a factor of three yields CLKFX_MULTIPLY = 3 and CLKFX_DIVIDE = 2. While both value-pairs will result in the multiplication of clock frequency by 3/2, the latter value-pair will enable the DLL to lock more quickly.

Table 18: **DFS Attributes**

Attribute	Description	Values
DFS_FREQUENCY_MODE	Chooses between High Frequency and Low Frequency modes	Low, High
CLKFX_MULTIPLY	Frequency multiplier constant	Integer from 2 to 32
CLKFX_DIVIDE	Frequency divisor constant	Integer from 1 to 32

Table 19: **DFS Signals**

Signal	Direction	Description
CLKFX	Output	Multiplies the CLKIN frequency by the attribute-value ratio (CLKFX_MULTIPLY/CLKFX_DIVIDE) to generate a clock signal with a new target frequency.
CLKFX180	Output	Generates a clock signal with same frequency as CLKFX, only shifted 180° out-of-phase.

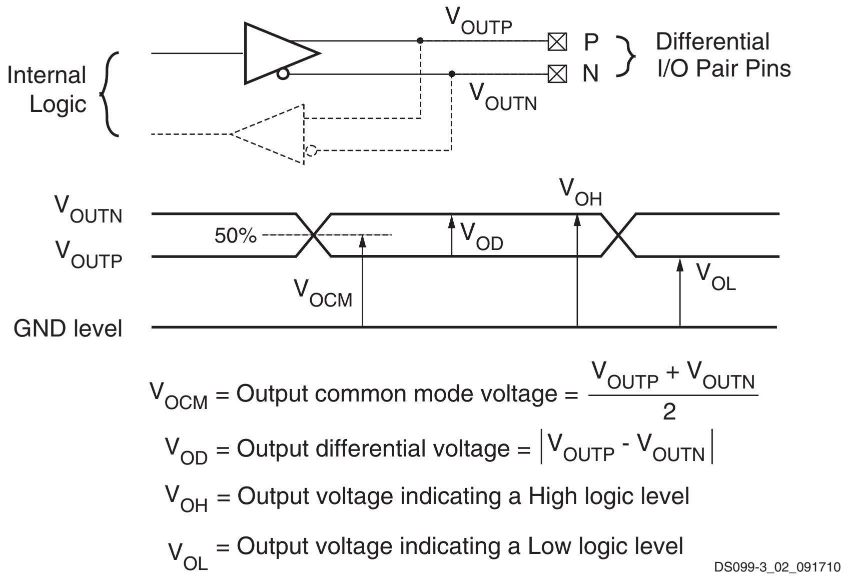

Figure 33: **Differential Output Voltages**

Table 38: **DC Characteristics of User I/Os Using Differential Signal Standards**

Signal Standard	Mask[3] Revision	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
		Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LDT_25 (ULVDS_25)	All	430[4]	600	670	0.495	0.600	0.715	0.71	0.50
LVDS_25	All	100	–	600	0.80	–	1.6	0.85	1.55
	'E'	200	–	500	1.0	–	1.5	1.10	1.40
BLVDS_25[5]	All	250	350	450	–	1.20	–	–	–
LVDSEXT_25	All	100	–	600	0.80	–	1.6	0.85	1.55
	'E'	300	–	700	1.0	–	1.5	1.15	1.35
LVPECL_25[5]	All	–	–	-	–	–	-	1.35	1.005
RSDS_25[6]	All	100	–	600	0.80	–	1.6	0.85	1.55
	'E'	200	–	500	1.0	–	1.5	1.10	1.40
DIFF_HSTL_II_18	All	–	–	–	–	–	–	$V_{CCO} – 0.40$	0.40
DIFF_SSTL2_II	All	–	–	–	–	–	–	$V_{TT} + 0.80$	$V_{TT} – 0.80$

Notes:
1. The numbers in this table are based on the conditions set forth in Table 32 and Table 37.
2. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
3. Mask revision E devices have tighter output ranges but can be used in any design that was in a previous revision. See Mask and Fab Revisions, page 58.
4. This value must be compatible with the receiver to which the FPGA's output pair is connected.
5. Each LVPECL_25 or BLVDS_25 output-pair requires three external resistors for proper output operation as shown in Figure 34. Each LVPECL_25 or BLVDS_25 input-pair uses a 100W termination resistor at the receiver.
6. Only one of the differential standards RSDS_25, LDT_25, LVDS_25, and LVDSEXT_25 may be used for outputs within a bank. Each differential standard input-pair requires an external 100Ω termination resistor.

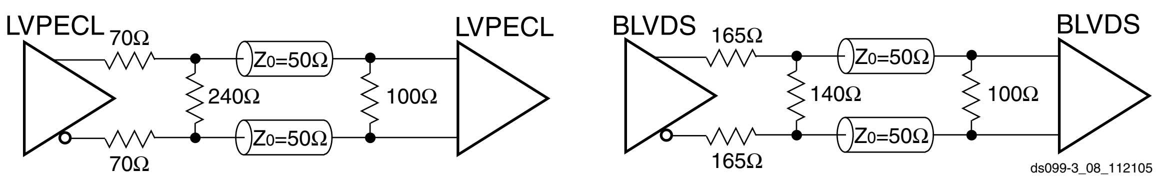

Figure 34: **External Termination Required for LVPECL and BLVDS Output and Input**

Table 42: **Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	Device	Speed Grade -5 Min	Speed Grade -4 Min	Units
Hold Times						
T_{IOICKP}	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25[(3)], IOBDELAY = NONE	XC3S50	-0.55	-0.55	ns
			XC3S200	-0.29	-0.29	ns
			XC3S400	-0.29	-0.29	ns
			XC3S1000	-0.55	-0.55	ns
			XC3S1500	-0.55	-0.55	ns
			XC3S2000	-0.55	-0.55	ns
			XC3S4000	-0.61	-0.61	ns
			XC3S5000	-0.68	-0.68	ns
$T_{IOICKPD}$	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25[(3)], IOBDELAY = IFD	XC3S50	-2.74	-2.74	ns
			XC3S200	-3.00	-3.00	ns
			XC3S400	-2.90	-2.90	ns
			XC3S1000	-3.24	-3.24	ns
			XC3S1500	-3.55	-3.55	ns
			XC3S2000	-4.57	-4.57	ns
			XC3S4000	-4.96	-4.96	ns
			XC3S5000	-5.09	-5.09	ns
Set/Reset Pulse Width						
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB		All	0.66	0.76	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 44.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 44. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 44: **Input Timing Adjustments for IOB *(Cont'd)***

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
LVCMOS15	0.42	0.49	ns
LVDCI_15	0.38	0.43	ns
LVDCI_DV2_15	0.38	0.44	ns
LVCMOS18	0.24	0.28	ns
LVDCI_18	0.29	0.33	ns
LVDCI_DV2_18	0.28	0.33	ns
LVCMOS25	0	0	ns
LVDCI_25	0.05	0.05	ns
LVDCI_DV2_25	0.04	0.04	ns
LVCMOS33, LVDCI_33, LVDCI_DV2_33	–0.05	–0.02	ns
LVTTL	0.18	0.21	ns
PCI33_3	0.20	0.22	ns
SSTL18_I, SSTL18_I_DCI	0.39	0.45	ns
SSTL18_II	0.39	0.45	ns
SSTL2_I, SSTL2_I_DCI	0.40	0.46	ns
SSTL2_II, SSTL2_II_DCI	0.36	0.41	ns
Differential Standards			
LDT_25 (ULVDS_25)	0.76	0.88	ns
LVDS_25, LVDS_25_DCI	0.65	0.75	ns
BLVDS_25	0.34	0.39	ns
LVDSEXT_25, LVDSEXT_25_DCI	0.80	0.92	ns
LVPECL_25	0.18	0.21	ns
RSDS_25	0.43	0.50	ns
DIFF_HSTL_II_18, DIFF_HSTL_II_18_DCI	0.34	0.39	ns
DIFF_SSTL2_II, DIFF_SSTL2_II_DCI	0.65	0.75	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32, Table 35, and Table 37.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package				
			VQ100	TQ144	PQ208	CP132	FT256, FG320, FG456, FG676, FG900, FG1156
LVDCI_15			6	6	6	6	14
LVDCI_DV2_15			6	6	6	6	14
HSLVDCI_15			6	6	6	6	14
LVCMOS18	Slow	2	19	13	13	29	64
		4	13	8	8	19	34
		6	8	8	8	9	22
		8	7	7	7	9	18
		12	5	5	5	5	13
		16	5	5	5	5	10
	Fast	2	13	13	13	19	36
		4	8	8	8	13	21
		6	8	8	8	8	13
		8	7	7	7	7	10
		12	5	5	5	5	9
		16	5	5	5	5	6
LVDCI_18			7	7	7	7	10
LVDCI_DV2_18			7	7	7	7	10
HSLVDCI_18			7	7	7	7	10
LVCMOS25	Slow	2	28	16	12	42	76
		4	13	10	10	19	46
		6	13	8	8	19	33
		8	7	7	7	9	24
		12	6	6	6	9	18
		16	6	6	6	6	11
		24	5	5	5	5	7
	Fast	2	17	12	12	26	42
		4	10	10	10	13	20
		6	8	8	8	13	15
		8	7	7	7	7	13
		12	6	6	6	6	11
		16	6	6	6	6	8
		24	5	5	5	5	5
LVDCI_25			7	7	7	7	11
LVDCI_DV2_25			7	7	7	7	11
HSLVDCI_25			7	7	7	7	11

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 58 and Table 59) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 60 through Table 63) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 58 and Table 59.

Period jitter and cycle-cycle jitter are two (of many) different ways of characterizing clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the average clock period of all clock cycles in the collection of clock periods sampled (usually from 100,000 to more than a million samples for specification purposes). In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Delay-Locked Loop (DLL)

Table 58: **Recommended Operating Conditions for the DLL**

Symbol	Description	Frequency Mode/ F_{CLKIN} Range	Speed Grade -5 Min	Speed Grade -5 Max	Speed Grade -4 Min	Speed Grade -4 Max	Units
Input Frequency Ranges							
F_{CLKIN} CLKIN_FREQ_DLL_LF	Frequency for the CLKIN input	Low	18[2]	167[3]	18[2]	167[3]	MHz
F_{CLKIN} CLKIN_FREQ_DLL_HF		High	48	280[3]	48	280[3][4]	MHz
Input Pulse Requirements							
CLKIN_PULSE	CLKIN pulse width as a percentage of the CLKIN period	$F_{CLKIN} \leq 100$ MHz	40%	60%	40%	60%	-
		$F_{CLKIN} > 100$ MHz	45%	55%	45%	55%	-
Input Clock Jitter Tolerance and Delay Path Variation[5]							
CLKIN_CYC_JITT_DLL_LF	Cycle-to-cycle jitter at the CLKIN input	Low	–	±300	–	±300	ps
CLKIN_CYC_JITT_DLL_HF		High	–	±150	–	±150	ps
CLKIN_PER_JITT_DLL_LF	Period jitter at the CLKIN input	All	–	±1	–	±1	ns
CLKIN_PER_JITT_DLL_HF			–		–		
CLKFB_DELAY_VAR_EXT	Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input	All	–	±1	–	±1	ns

Notes:
1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower F_{CLKIN} frequencies. See Table 60.
3. The CLKIN_DIVIDE_BY_2 attribute can be used to increase the effective input frequency range up to F_{BUFG}. When set to TRUE, CLKIN_DIVIDE_BY_2 divides the incoming clock frequency by two as it enters the DCM.
4. Industrial temperature range devices have additional requirements for continuous clocking, as specified in Table 64.
5. CLKIN input jitter beyond these limits may cause the DCM to lose lock. See UG331 for more details.

Table 70: **Spartan-3 FPGA Pin Definitions *(Cont'd)***

Pin Name	Direction	Description
TDI	Input	**JTAG Test Data Input:** TDI is the serial data input for all JTAG instruction and data registers. This pin has an internal pull-up resistor to VCCAUX during configuration.
TMS	Input	**JTAG Test Mode Select:** The serial TMS input controls the operation of the JTAG port. This pin has an internal pull-up resistor to VCCAUX during configuration.
TDO	Output	**JTAG Test Data Output:** TDO is the serial data output for all JTAG instruction and data registers. This pin has an internal pull-up resistor to VCCAUX during configuration.
VCCO: I/O bank output voltage supply pins		
VCCO_#	Supply	**Power Supply for Output Buffer Drivers (per bank):** These pins power the output drivers within a specific I/O bank.
VCCAUX: Auxiliary voltage supply pins		
VCCAUX	Supply	**Power Supply for Auxiliary Circuits:** +2.5V power pins for auxiliary circuits, including the Digital Clock Managers (DCMs), the dedicated configuration pins (CONFIG), and the dedicated JTAG pins. All VCCAUX pins must be connected.
VCCINT: Internal core voltage supply pins		
VCCINT	Supply	**Power Supply for Internal Core Logic:** +1.2V power pins for the internal logic. All pins must be connected.
GND: Ground supply pins		
GND	Supply	**Ground:** Ground pins, which are connected to the power supply's return path. All pins must be connected.
N.C.: Unconnected package pins		
N.C.		**Unconnected Package Pin:** These package pins are unconnected.

Notes:
1. All unused inputs and bidirectional pins must be tied either High or Low. For unused enable inputs, apply the level that disables the associated function. One common approach is to activate internal pull-up or pull-down resistors. An alternative approach is to externally connect the pin to either VCCO or GND.
2. All outputs are of the totem-pole type — i.e., they can drive High as well as Low logic levels — except for the cases where "Open Drain" is indicated. The latter can only drive a Low logic level and require a pull-up resistor to produce a High logic level.

Detailed, Functional Pin Descriptions

I/O Type: Unrestricted, General-purpose I/O Pins

After configuration, I/O-type pins are inputs, outputs, bidirectional I/O, three-state outputs, open-drain outputs, or open-source outputs, as defined in the application

Pins labeled "IO" support all SelectIO™ interface signal standards except differential standards. A given device at most only has a few of these pins.

A majority of the general-purpose I/O pins are labeled in the format "IO_Lxxy_#". These pins support all SelectIO signal standards, including the differential standards such as LVDS, ULVDS, BLVDS, RSDS, or LDT.

For additional information, see IOBs, page 10

Once the FPGA enters User mode after completing configuration, the DONE pin no longer drives the DONE pin Low. The bitstream generator option DonePin determines whether or not a pull-up resistor is present on the DONE pin to pull the pin to VCCAUX. If the pull-up resistor is eliminated, then the DONE pin must be pulled High using an external pull-up resistor or one of the FPGAs in the design must actively drive the DONE pin High via the DriveDone bitstream generator option.

The bitstream generator option DriveDone causes the FPGA to actively drive the DONE output High after configuration. This option should only be used in single-FPGA designs or on the last FPGA in a multi-FPGA daisy-chain.

By default, the bitstream generator software retains the pull-up resistor and does not actively drive the DONE pin as highlighted in Table 74, which shows the interaction of these bitstream options in single- and multi-FPGA designs.

Table 74: **DonePin and DriveDone Bitstream Option Interaction**

DonePin	DriveDone	Single- or Multi-FPGA Design	Comments
Pullnone	No	Single	External pull-up resistor, with value between 330Ω to 3.3kΩ, required on DONE.
Pullnone	No	Multi	External pull-up resistor, with value between 330Ω to 3.3kΩ, required on common node connecting to all DONE pins.
Pullnone	Yes	Single	OK, no external requirements.
Pullnone	Yes	Multi	DriveDone on last device in daisy-chain only. No external requirements.
Pullup	No	Single	OK, but pull-up on DONE pin has slow rise time. May require 330Ω pull-up resistor for high CCLK frequencies.
Pullup	No	Multi	External pull-up resistor, with value between 330Ω to 3.3kΩ, required on common node connecting to all DONE pins.
Pullup	Yes	Single	OK, no external requirements.
Pullup	Yes	Multi	DriveDone on last device in daisy-chain only. No external requirements.

M2, M1, M0: Configuration Mode Selection

The M2, M1, and M0 inputs select the FPGA configuration mode, as described in Table 75. The logic levels applied to the mode pins are sampled on the rising edge of INIT_B.

Table 75: **Spartan-3 FPGA Mode Select Settings**

Configuration Mode	M2	M1	M0
Master Serial	0	0	0
Slave Serial	1	1	1
Master Parallel	0	1	1
Slave Parallel	1	1	0
JTAG	1	0	1
Reserved	0	0	1
Reserved	0	1	0
Reserved	1	0	0
After Configuration	X	X	X

Notes:
1. X = don't care, either 0 or 1.

Before and during configuration, the mode pins have an internal pull-up resistor to VCCAUX, regardless of the HSWAP_EN pin. If the mode pins are unconnected, then the FPGA defaults to the Slave Serial configuration mode. After configuration successfully completes, any levels applied to these input are ignored. Furthermore, the bitstream generator options M0Pin, M1Pin, and M2Pin determines whether a pull-up resistor, pull-down resistor, or no resistor is present on its respective mode pin, M0, M1, or M2.

All VCCAUX inputs must be connected together and to the +2.5V voltage supply. Furthermore, there must be sufficient supply decoupling to guarantee problem-free operation, as described in XAPP623.

Because VCCAUX connects to the DCMs and the DCMs are sensitive to voltage changes, be sure that the VCCAUX supply and the ground return paths are designed for low noise and low voltage drop, especially that caused by a large number of simultaneous switching I/Os.

GND Type: Ground

All GND pins must be connected and have a low resistance path back to the various VCCO, VCCINT, and VCCAUX supplies.

Pin Behavior During Configuration

Table 79 shows how various pins behave during the FPGA configuration process. The actual behavior depends on the values applied to the M2, M1, and M0 mode select pins and the HSWAP_EN pin. The mode select pins determine which of the DUAL type pins are active during configuration. In JTAG configuration mode, none of the DUAL-type pins are used for configuration and all behave as user-I/O pins.

All DUAL-type pins not actively used during configuration and all I/O-type, DCI-type, VREF-type, GCLK-type pins are high impedance (floating, three-stated, Hi-Z) during the configuration process. These pins are indicated in Table 79 as shaded table entries or cells. These pins have a pull-up resistor to their associated VCCO if the HSWAP_EN pin is Low. When HSWAP_EN is High, these pull-up resistors are disabled during configuration.

Some pins always have an active pull-up resistor during configuration, regardless of the value applied to the HSWAP_EN pin. After configuration, these pull-up resistors are controlled by Bitstream Options.

- All the dedicated CONFIG-type configuration pins (CCLK, PROG_B, DONE, M2, M1, M0, and HSWAP_EN) have a pull-up resistor to VCCAUX.
- All JTAG-type pins (TCK, TDI, TMS, TDO) have a pull-up resistor to VCCAUX.
- The INIT_B DUAL-purpose pin has a pull-up resistor to VCCO_4 or VCCO_BOTTOM, depending on package style.

After configuration completes, some pins have optional behavior controlled by the configuration bitstream loaded into the part. For example, via the bitstream, all unused I/O pins can be collectively configured as input pins with either a pull-up resistor, a pull-down resistor, or be left in a high-impedance state.

Table 79: **Pin Behavior After Power-Up, During Configuration**

Pin Name	Configuration Mode Settings <M2:M1:M0>					Bitstream Configuration Option
	Serial Modes		SelectMap Parallel Modes		JTAG Mode <1:0:1>	
	Master <0:0:0>	Slave <1:1:1>	Master <0:1:1>	Slave <1:1:0>		
I/O: General-purpose I/O pins						
IO						UnusedPin
IO_Lxxy_#						UnusedPin
DUAL: Dual-purpose configuration pins						
IO_Lxxy_#/ DIN/D0	DIN (I)	DIN (I)	D0 (I/O)	D0 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D1			D1 (I/O)	D1 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D2			D2 (I/O)	D2 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D3			D3 (I/O)	D3 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D4			D4 (I/O)	D4 (I/O)		Persist UnusedPin

Table 85: **Maximum User I/Os by Package**

Device	Package	Maximum User I/Os	Maximum Differential Pairs	All Possible I/O Pins by Type					N.C.
				I/O	DUAL	DCI	VREF	GCLK	
XC3S50	VQ100	63	29	22	12	14	7	8	0
XC3S200	VQ100	63	29	22	12	14	7	8	0
XC3S50	CP132[(1)]	89	44	44	12	14	11	8	0
XC3S50	TQ144	97	46	51	12	14	12	8	0
XC3S200	TQ144	97	46	51	12	14	12	8	0
XC3S400	TQ144	97	46	51	12	14	12	8	0
XC3S50	PQ208	124	56	72	12	16	16	8	17
XC3S200	PQ208	141	62	83	12	16	22	8	0
XC3S400	PQ208	141	62	83	12	16	22	8	0
XC3S200	FT256	173	76	113	12	16	24	8	0
XC3S400	FT256	173	76	113	12	16	24	8	0
XC3S1000	FT256	173	76	113	12	16	24	8	0
XC3S400	FG320	221	100	156	12	16	29	8	0
XC3S1000	FG320	221	100	156	12	16	29	8	0
XC3S1500	FG320	221	100	156	12	16	29	8	0
XC3S400	FG456	264	116	196	12	16	32	8	69
XC3S1000	FG456	333	149	261	12	16	36	8	0
XC3S1500	FG456	333	149	261	12	16	36	8	0
XC3S2000	FG456	333	149	261	12	16	36	8	0
XC3S1000	FG676	391	175	315	12	16	40	8	98
XC3S1500	FG676	487	221	403	12	16	48	8	2
XC3S2000	FG676	489	221	405	12	16	48	8	0
XC3S4000	FG676	489	221	405	12	16	48	8	0
XC3S5000	FG676	489	221	405	12	16	48	8	0
XC3S2000	FG900	565	270	481	12	16	48	8	68
XC3S4000	FG900	633	300	549	12	16	48	8	0
XC3S5000	FG900	633	300	549	12	16	48	8	0
XC3S4000	FG1156[(1)]	712	312	621	12	16	55	8	73
XC3S5000	FG1156[(1)]	784	344	692	12	16	56	8	1

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Electronic versions of the package pinout tables and footprints are available for download from the Xilinx website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs. Download the files from the following location:

http://www.xilinx.com/support/documentation/data_sheets/s3_pin.zip

User I/Os by Bank

Table 94 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S50 in the PQ208 package. Similarly, Table 95 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S200 and XC3S400 in the PQ208 package.

Table 94: **User I/Os Per Bank for XC3S50 in PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	15	9	0	2	2	2
	1	15	9	0	2	2	2
Right	2	16	13	0	2	2	0
	3	16	12	0	2	2	0
Bottom	4	15	3	6	2	2	2
	5	15	3	6	2	2	2
Left	6	16	12	0	2	2	0
	7	16	12	0	2	2	0

Table 95: **User I/Os Per Bank for XC3S200 and XC3S400 in PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	16	9	0	2	3	2
	1	15	9	0	2	2	2
Right	2	19	14	0	2	3	0
	3	20	15	0	2	3	0
Bottom	4	17	4	6	2	3	2
	5	15	3	6	2	2	2
Left	6	19	14	0	2	3	0
	7	20	15	0	2	3	0

FT256 Footprint

Bank 0 (columns 3–8), Bank 1 (columns 9–14), Bank 2 (rows A–H, right), Bank 3 (rows J–R, right), Bank 4 (columns 9–14, bottom), Bank 5 (columns 3–8, bottom), Bank 6 (rows J–R, left), Bank 7 (rows A–H, left)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	TDI	IO VREF_0	I/O L01P_0 VRN_0	I/O	VCCAUX	I/O	I/O L32P_0 GCLK6	I/O	I/O L31N_1 VREF_1	VCCAUX	I/O	I/O L10N_1 VREF_1	I/O L01N_1 VRP_1	TDO	GND
B	I/O L01P_7 VRN_7	GND	PROG_B	I/O L01N_0 VRP_0	I/O L25P_0	I/O L28P_0	I/O L30P_0	I/O L32N_0 GCLK7	GND	I/O L31P_1	I/O L29N_1	I/O L27N_1	I/O L10P_1	I/O L01P_1 VRN_1	GND	I/O L01N_2 VRP_2
C	I/O L01N_7 VRP_7	I/O L16N_7	I/O L16P_7 VREF_7	HSWAP_EN	I/O L25N_0	I/O L28N_0	I/O L30N_0	I/O L31P_0 VREF_0	I/O L32N_1 GCLK5	I/O	I/O L29P_1	I/O L27P_1	TMS	TCK	I/O L16N_2	I/O L01P_2 VRN_2
D	I/O L17N_7	I/O L17P_7	I/O L19P_7	VCCINT	IO VREF_0	I/O L27P_0	I/O L29P_0	I/O L31N_0	I/O L32P_1 GCLK4	I/O L30N_1	I/O L28N_1	IO VREF_1	VCCINT	I/O L16P_2	I/O L17N_2	I/O L17P_2 VREF_2
E	I/O L20N_7	I/O L20P_7	I/O L19N_7 VREF_7	I/O L21P_7	VCCINT	I/O L27N_0	I/O L29N_0	VCCO_0	VCCO_1	I/O L30P_1	I/O L28P_1	VCCINT	I/O L19N_2	I/O L19P_2	I/O L20N_2	I/O L20P_2
F	VCCAUX	I/O L22N_7	I/O L22P_7	I/O L21N_7	I/O L23P_7	GND	VCCO_0	VCCO_0	VCCO_1	VCCO_1	GND	I/O L21N_2	I/O L21P_2	I/O L22N_2	I/O L22P_2	VCCAUX
G	I/O L40P_7	I/O	I/O L24N_7	I/O L24P_7	I/O L23N_7	VCCO_7	GND	GND	GND	GND	VCCO_2	I/O L23N_2 VREF_2	I/O L23P_2	I/O L24N_2	I/O L24P_2	I/O
H	I/O L40N_7 VREF_7	GND	I/O L39N_7	I/O L39P_7	VCCO_7	VCCO_7	GND	GND	GND	GND	VCCO_2	VCCO_2	I/O L39N_2	I/O L39P_2	I/O L40N_2	I/O L40P_2 VREF_2
J	I/O L40P_6 VREF_6	I/O L40N_6	I/O L39P_6	I/O L39N_6	VCCO_6	VCCO_6	GND	GND	GND	GND	VCCO_3	VCCO_3	I/O L39P_3	I/O L39N_3	GND	I/O L40N_3 VREF_3
K	I/O	I/O L24P_6	I/O L24N_6 VREF_6	I/O L23P_6	I/O L23N_6	VCCO_6	GND	GND	GND	GND	VCCO_3	I/O L23N_3	I/O L24P_3	I/O L24N_3	I/O	I/O L40P_3
L	VCCAUX	I/O L22P_6	I/O L22N_6	I/O L21P_6	I/O L21N_6	GND	VCCO_5	VCCO_5	VCCO_4	VCCO_4	GND	I/O L23P_3 VREF_3	I/O L21N_3	I/O L22P_3	I/O L22N_3	VCCAUX
M	I/O L20P_6	I/O L20N_6	I/O L19P_6	I/O L19N_6	VCCINT	I/O L28P_5 D7	I/O L30P_5	VCCO_5	VCCO_4	I/O L29N_4	I/O L27N_4 DIN D0	VCCINT	I/O L21P_3	I/O L19N_3	I/O L20P_3	I/O L20N_3
N	I/O L17P_6 VREF_6	I/O L17N_6	I/O L16P_6	VCCINT	I/O	I/O L28N_5 D6	I/O L30N_5	I/O L32P_5 GCLK2	I/O L31N_4 INIT_B	I/O L29P_4	I/O L27P_4 D1	IO VREF_4	VCCINT	I/O L19P_3	I/O L17P_3 VREF_3	I/O L17N_3
P	I/O L01P_6 VRN_6	I/O L16N_6	M0	M2	I/O L27P_5	I/O L29P_5 VREF_5	I/O	I/O L32N_5 GCLK3	I/O L31P_4 DOUT BUSY	I/O L30N_4 D2	I/O L28N_4	I/O L25N_4	IO VREF_4	I/O L16P_3	I/O L16N_3	I/O L01N_3 VRP_3
R	I/O L01N_6 VRP_6	GND	I/O L01P_5 CS_B	I/O L10P_5 VRN_5	I/O L27N_5 VREF_5	I/O L29N_5	I/O L31P_5 D5	GND	I/O L32N_4 GCLK1	I/O L30P_4 D3	I/O L28P_4	I/O L25P_4	I/O L01N_4 VRP_4	DONE	GND	I/O L01P_3 VRN_3
T	GND	M1	I/O L01N_5 RDWR_B	I/O L10N_5 VRP_5	I/O	VCCAUX	I/O L31N_5 D4	IO VREF_5	I/O L32P_4 GCLK0	IO VREF_4	VCCAUX	I/O	I/O L01P_4 VRN_4	I/O	CCLK	GND

DS099-4_10_030503

Figure 49: **FT256 Package Footprint (Top View)**

113	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	24	**VREF:** User I/O or input voltage reference for bank
16	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input	24	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	8	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	32	**GND:** Ground	8	**VCCAUX:** Auxiliary voltage supply (+2.5V)

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
0	N.C. (◆)	IO_L22N_0	E8	I/O
0	N.C. (◆)	IO_L22P_0	D8	I/O
0	IO_L24N_0	IO_L24N_0	B8	I/O
0	IO_L24P_0	IO_L24P_0	A8	I/O
0	IO_L25N_0	IO_L25N_0	F9	I/O
0	IO_L25P_0	IO_L25P_0	E9	I/O
0	IO_L27N_0	IO_L27N_0	B9	I/O
0	IO_L27P_0	IO_L27P_0	A9	I/O
0	IO_L28N_0	IO_L28N_0	F10	I/O
0	IO_L28P_0	IO_L28P_0	E10	I/O
0	IO_L29N_0	IO_L29N_0	C10	I/O
0	IO_L29P_0	IO_L29P_0	B10	I/O
0	IO_L30N_0	IO_L30N_0	F11	I/O
0	IO_L30P_0	IO_L30P_0	E11	I/O
0	IO_L31N_0	IO_L31N_0	D11	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C11	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B11	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A11	GCLK
0	VCCO_0	VCCO_0	C8	VCCO
0	VCCO_0	VCCO_0	F8	VCCO
0	VCCO_0	VCCO_0	G9	VCCO
0	VCCO_0	VCCO_0	G10	VCCO
0	VCCO_0	VCCO_0	G11	VCCO
1	IO	IO	A12	I/O
1	IO	IO	E16	I/O
1	IO	IO	F12	I/O
1	IO	IO	F13	I/O
1	IO	IO	F16	I/O
1	IO	IO	F17	I/O
1	IO/VREF_1	IO/VREF_1	E13	VREF
1	N.C. (◆)	IO/VREF_1	F14	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	C19	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B20	DCI
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	A19	VREF
1	IO_L06P_1	IO_L06P_1	B19	I/O
1	IO_L09N_1	IO_L09N_1	C18	I/O
1	IO_L09P_1	IO_L09P_1	D18	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	A18	VREF
1	IO_L10P_1	IO_L10P_1	B18	I/O
1	IO_L15N_1	IO_L15N_1	D17	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	H9	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	H10	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	J11	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	J12	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	J13	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	K13	VCCO
1	IO	IO	IO	IO	IO	A14	I/O
1	IO	IO	IO	IO	IO	A22	I/O
1	IO	IO	IO	IO	IO	A23	I/O
1	IO	IO	IO	IO	IO	D16	I/O
1	IO	IO	IO	IO	IO_L17P_1[(3)]	E18	I/O
1	IO	IO	IO	IO	IO	F14	I/O
1	IO	IO	IO	IO	IO	F20	I/O
1	IO	IO	IO	IO	IO	G19	I/O
1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	C15	VREF
1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	C17	VREF
1	N.C. (◆)	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO_L17N_1/VREF_1[(3)]	D18	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	D22	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	E22	DCI
1	IO_L04N_1	IO_L04N_1	IO_L04N_1	IO_L04N_1	IO_L04N_1	B23	I/O
1	IO_L04P_1	IO_L04P_1	IO_L04P_1	IO_L04P_1	IO_L04P_1	C23	I/O
1	IO_L05N_1	IO_L05N_1	IO_L05N_1	IO_L05N_1	IO_L05N_1	E21	I/O
1	IO_L05P_1	IO_L05P_1	IO_L05P_1	IO_L05P_1	IO_L05P_1	F21	I/O
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	B22	VREF
1	IO_L06P_1	IO_L06P_1	IO_L06P_1	IO_L06P_1	IO_L06P_1	C22	I/O
1	IO_L07N_1	IO_L07N_1	IO_L07N_1	IO_L07N_1	IO_L07N_1	C21	I/O
1	IO_L07P_1	IO_L07P_1	IO_L07P_1	IO_L07P_1	IO_L07P_1	D21	I/O
1	IO_L08N_1	IO_L08N_1	IO_L08N_1	IO_L08N_1	IO_L08N_1	A21	I/O
1	IO_L08P_1	IO_L08P_1	IO_L08P_1	IO_L08P_1	IO_L08P_1	B21	I/O
1	IO_L09N_1	IO_L09N_1	IO_L09N_1	IO_L09N_1	IO_L09N_1	D20	I/O
1	IO_L09P_1	IO_L09P_1	IO_L09P_1	IO_L09P_1	IO_L09P_1	E20	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	A20	VREF
1	IO_L10P_1	IO_L10P_1	IO_L10P_1	IO_L10P_1	IO_L10P_1	B20	I/O
1	N.C. (◆)	IO_L11N_1	IO_L11N_1	IO_L11N_1	IO_L11N_1	E19	I/O
1	N.C. (◆)	IO_L11P_1	IO_L11P_1	IO_L11P_1	IO_L11P_1	F19	I/O
1	N.C. (◆)	IO_L12N_1	IO_L12N_1	IO_L12N_1	IO_L12N_1	C19	I/O
1	N.C. (◆)	IO_L12P_1	IO_L12P_1	IO_L12P_1	IO_L12P_1	D19	I/O
1	IO_L15N_1	IO_L15N_1	IO_L15N_1	IO_L15N_1	IO_L15N_1	A19	I/O
1	IO_L15P_1	IO_L15P_1	IO_L15P_1	IO_L15P_1	IO_L15P_1	B19	I/O
1	IO_L16N_1	IO_L16N_1	IO_L16N_1	IO_L16N_1	IO_L16N_1	F18	I/O
1	IO_L16P_1	IO_L16P_1	IO_L16P_1	IO_L16P_1	IO_L16P_1	G18	I/O
1	N.C. (◆)	IO_L18N_1	IO_L18N_1	IO_L18N_1	IO[(3)]	B18	I/O

FG900: 900-lead Fine-pitch Ball Grid Array

The 900-lead fine-pitch ball grid array package, FG900, supports three different Spartan-3 devices, including the XC3S2000, the XC3S4000, and the XC3S5000. The footprints for the XC3S4000 and XC3S5000 are identical, as shown in Table 107 and Figure 55. The XC3S2000, however, has fewer I/O pins which consequently results in 68 unconnected pins on the FG900 package, labeled as “N.C.” In Table 107 and Figure 55, these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in Table 107 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S2000 pinout and the pinout for the XC3S4000 and XC3S5000, then that difference is highlighted in Table 107. If the table entry is shaded, then there is an unconnected pin on the XC3S2000 that maps to a user-I/O pin on the XC3S4000 and XC3S5000.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 107: **FG900 Package Pinout**

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO	IO	E15	I/O
0	IO	IO	K15	I/O
0	IO	IO	D13	I/O
0	IO	IO	K13	I/O
0	IO	IO	G8	I/O
0	IO/VREF_0	IO/VREF_0	F9	VREF
0	IO/VREF_0	IO/VREF_0	C4	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	B4	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	A4	DCI
0	IO_L02N_0	IO_L02N_0	B5	I/O
0	IO_L02P_0	IO_L02P_0	A5	I/O
0	IO_L03N_0	IO_L03N_0	D5	I/O
0	IO_L03P_0	IO_L03P_0	E6	I/O
0	IO_L04N_0	IO_L04N_0	C6	I/O
0	IO_L04P_0	IO_L04P_0	B6	I/O
0	IO_L05N_0	IO_L05N_0	F6	I/O
0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	F7	VREF
0	IO_L06N_0	IO_L06N_0	D7	I/O
0	IO_L06P_0	IO_L06P_0	C7	I/O
0	IO_L07N_0	IO_L07N_0	F8	I/O
0	IO_L07P_0	IO_L07P_0	E8	I/O
0	IO_L08N_0	IO_L08N_0	D8	I/O
0	IO_L08P_0	IO_L08P_0	C8	I/O
0	IO_L09N_0	IO_L09N_0	B8	I/O
0	IO_L09P_0	IO_L09P_0	A8	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO_L30N_0	IO_L30N_0	G15	I/O
0	IO_L30P_0	IO_L30P_0	F15	I/O
0	IO_L31N_0	IO_L31N_0	D15	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C15	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B15	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A15	GCLK
0	N.C. (◆)	IO_L35N_0	B7	I/O
0	N.C. (◆)	IO_L35P_0	A7	I/O
0	N.C. (◆)	IO_L36N_0	G7	I/O
0	N.C. (◆)	IO_L36P_0	H8	I/O
0	N.C. (◆)	IO_L37N_0	E9	I/O
0	N.C. (◆)	IO_L37P_0	D9	I/O
0	N.C. (◆)	IO_L38N_0	B9	I/O
0	N.C. (◆)	IO_L38P_0	A9	I/O
0	VCCO_0	VCCO_0	C5	VCCO
0	VCCO_0	VCCO_0	E7	VCCO
0	VCCO_0	VCCO_0	C9	VCCO
0	VCCO_0	VCCO_0	G9	VCCO
0	VCCO_0	VCCO_0	J11	VCCO
0	VCCO_0	VCCO_0	L12	VCCO
0	VCCO_0	VCCO_0	C13	VCCO
0	VCCO_0	VCCO_0	G13	VCCO
0	VCCO_0	VCCO_0	L13	VCCO
0	VCCO_0	VCCO_0	L14	VCCO
1	IO	IO	E25	I/O
1	IO	IO	J21	I/O
1	IO	IO	K20	I/O
1	IO	IO	F18	I/O
1	IO	IO	F16	I/O
1	IO	IO	A16	I/O
1	IO/VREF_1	IO/VREF_1	J17	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	A27	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B27	DCI
1	IO_L02N_1	IO_L02N_1	D26	I/O
1	IO_L02P_1	IO_L02P_1	C27	I/O
1	IO_L03N_1	IO_L03N_1	A26	I/O
1	IO_L03P_1	IO_L03P_1	B26	I/O
1	IO_L04N_1	IO_L04N_1	B25	I/O
1	IO_L04P_1	IO_L04P_1	C25	I/O
1	IO_L05N_1	IO_L05N_1	F24	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
1	IO_L25P_1	IO_L25P_1	D19	I/O
1	IO_L26N_1	IO_L26N_1	A19	I/O
1	IO_L26P_1	IO_L26P_1	B19	I/O
1	IO_L27N_1	IO_L27N_1	F17	I/O
1	IO_L27P_1	IO_L27P_1	G17	I/O
1	IO_L28N_1	IO_L28N_1	B17	I/O
1	IO_L28P_1	IO_L28P_1	C17	I/O
1	IO_L29N_1	IO_L29N_1	J16	I/O
1	IO_L29P_1	IO_L29P_1	K16	I/O
1	IO_L30N_1	IO_L30N_1	G16	I/O
1	IO_L30P_1	IO_L30P_1	H16	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D16	VREF
1	IO_L31P_1	IO_L31P_1	E16	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B16	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C16	GCLK
1	N.C. (◆)	IO_L37N_1	H18	I/O
1	N.C. (◆)	IO_L37P_1	J18	I/O
1	N.C. (◆)	IO_L38N_1	D18	I/O
1	N.C. (◆)	IO_L38P_1	E18	I/O
1	N.C. (◆)	IO_L39N_1	A18	I/O
1	N.C. (◆)	IO_L39P_1	B18	I/O
1	N.C. (◆)	IO_L40N_1	K17	I/O
1	N.C. (◆)	IO_L40P_1	K18	I/O
1	VCCO_1	VCCO_1	L17	VCCO
1	VCCO_1	VCCO_1	C18	VCCO
1	VCCO_1	VCCO_1	G18	VCCO
1	VCCO_1	VCCO_1	L18	VCCO
1	VCCO_1	VCCO_1	L19	VCCO
1	VCCO_1	VCCO_1	J20	VCCO
1	VCCO_1	VCCO_1	C22	VCCO
1	VCCO_1	VCCO_1	G22	VCCO
1	VCCO_1	VCCO_1	E24	VCCO
1	VCCO_1	VCCO_1	C26	VCCO
2	IO	IO	J25	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C29	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C30	DCI
2	IO_L02N_2	IO_L02N_2	D27	I/O
2	IO_L02P_2	IO_L02P_2	D28	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	D29	VREF
2	IO_L03P_2	IO_L03P_2	D30	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	C2	DCI
7	IO_L02N_7	IO_L02N_7	D1	I/O
7	IO_L02P_7	IO_L02P_7	D2	I/O
7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	E2	VREF
7	IO_L03P_7	IO_L03P_7	E3	I/O
7	IO_L04N_7	IO_L04N_7	F3	I/O
7	IO_L04P_7	IO_L04P_7	F4	I/O
7	IO_L05N_7	IO_L05N_7	F1	I/O
7	IO_L05P_7	IO_L05P_7	F2	I/O
7	IO_L06N_7	IO_L06N_7	G5	I/O
7	IO_L06P_7	IO_L06P_7	G6	I/O
7	IO_L07N_7	IO_L07N_7	H5	I/O
7	IO_L07P_7	IO_L07P_7	H6	I/O
7	IO_L08N_7	IO_L08N_7	H1	I/O
7	IO_L08P_7	IO_L08P_7	H2	I/O
7	IO_L09N_7	IO_L09N_7	J6	I/O
7	IO_L09P_7	IO_L09P_7	J7	I/O
7	IO_L10N_7	IO_L10N_7	J4	I/O
7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	H4	VREF
7	IO_L11N_7	IO_L11N_7	J2	I/O
7	IO_L11P_7	IO_L11P_7	J3	I/O
7	IO_L12N_7	IO_L12N_7	K9	I/O
7	IO_L12P_7	IO_L12P_7	J8	I/O
7	IO_L13N_7	IO_L13N_7	K7	I/O
7	IO_L13P_7	IO_L13P_7	K8	I/O
7	IO_L14N_7	IO_L14N_7	K5	I/O
7	IO_L14P_7	IO_L14P_7	K6	I/O
7	IO_L15N_7	IO_L15N_7	K3	I/O
7	IO_L15P_7	IO_L15P_7	K4	I/O
7	IO_L16N_7	IO_L16N_7	K1	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	K2	VREF
7	IO_L17N_7	IO_L17N_7	L9	I/O
7	IO_L17P_7	IO_L17P_7	L10	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	L1	VREF
7	IO_L19P_7	IO_L19P_7	L2	I/O
7	IO_L20N_7	IO_L20N_7	M10	I/O
7	IO_L20P_7	IO_L20P_7	M11	I/O
7	IO_L21N_7	IO_L21N_7	M7	I/O
7	IO_L21P_7	IO_L21P_7	M8	I/O
7	IO_L22N_7	IO_L22N_7	M5	I/O

User I/Os by Bank

Note: The FG(G)1156 package is discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Table 111 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S4000 in the FG1156 package. Similarly, Table 112 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S5000 in the FG1156 package.

Table 111: **User I/Os Per Bank for XC3S4000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	90	79	0	2	7	2
	1	90	79	0	2	7	2
Right	2	88	80	0	2	6	0
	3	88	79	0	2	7	0
Bottom	4	90	73	6	2	7	2
	5	90	73	6	2	7	2
Left	6	88	79	0	2	7	0
	7	88	79	0	2	7	0

Notes:
1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

Table 112: **User I/Os Per Bank for XC3S5000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	100	89	0	2	7	2
	1	100	89	0	2	7	2
Right	2	96	87	0	2	7	0
	3	96	87	0	2	7	0
Bottom	4	100	83	6	2	7	2
	5	100	83	6	2	7	2
Left	6	96	87	0	2	7	0
	7	96	87	0	2	7	0

Notes:
1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.