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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

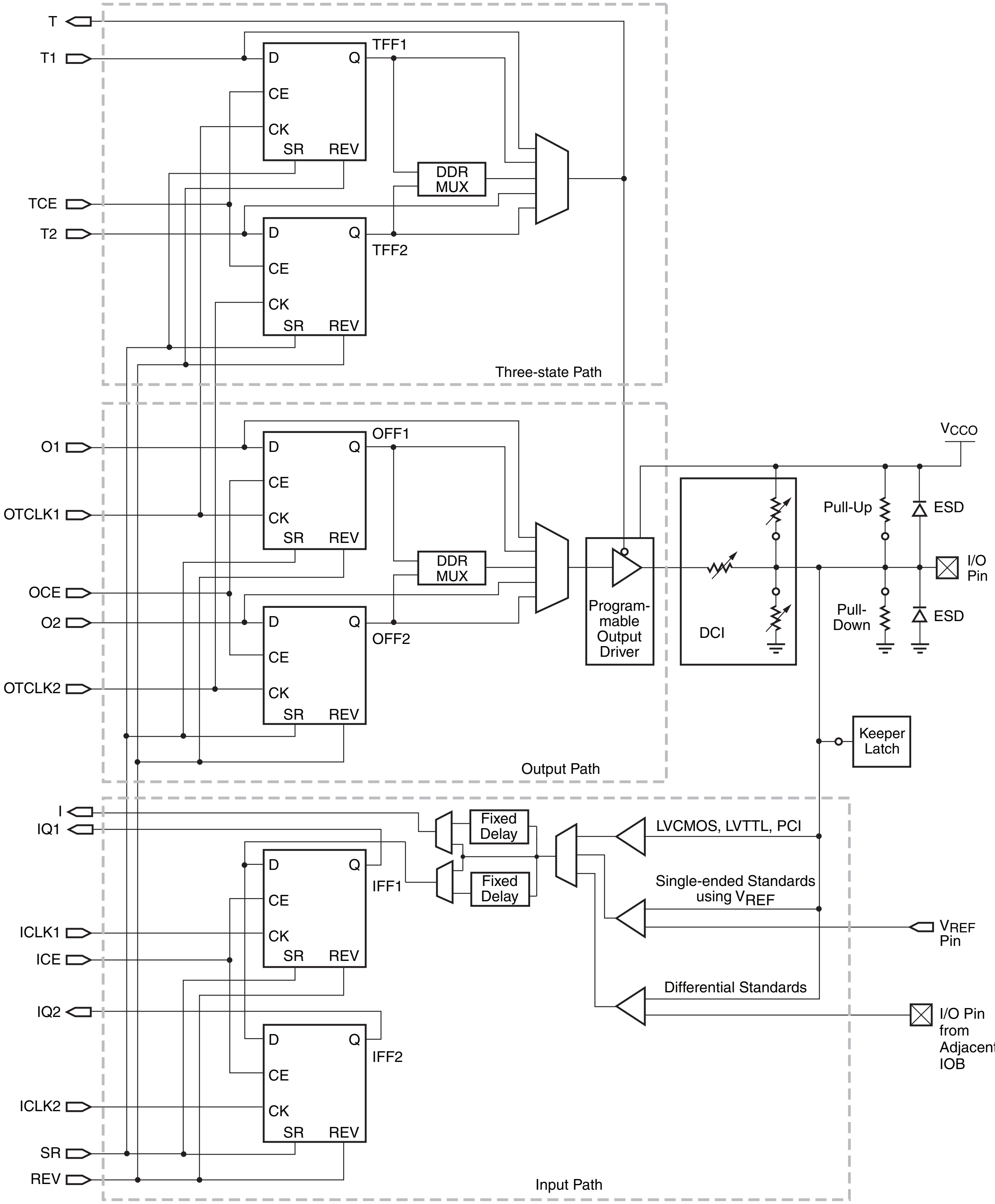
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	480
Number of Logic Elements/Cells	4320
Total RAM Bits	221184
Number of I/O	63
Number of Gates	200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s200-4vqg100c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Note: All IOB signals originating from the FPGA's internal logic have an optional polarity inverter.

DS099-2_01_091410

Figure 7: **Simplified IOB Diagram**

Arrangement of RAM Blocks on Die

The XC3S50 has one column of block RAM. The Spartan-3 devices ranging from the XC3S200 to XC3S2000 have two columns of block RAM. The XC3S4000 and XC3S5000 have four columns. The position of the columns on the die is shown in Figure 1, page 3. For a given device, the total available RAM blocks are distributed equally among the columns. Table 12 shows the number of RAM blocks, the data storage capacity, and the number of columns for each device.

Table 12: **Number of RAM Blocks by Device**

Device	Total Number of RAM Blocks	Total Addressable Locations (Bits)	Number of Columns
XC3S50	4	73,728	1
XC3S200	12	221,184	2
XC3S400	16	294,912	2
XC3S1000	24	442,368	2
XC3S1500	32	589,824	2
XC3S2000	40	737,280	2
XC3S4000	96	1,769,472	4
XC3S5000	104	1,916,928	4

Block RAM and multipliers have interconnects between them that permit simultaneous operation; however, since the multiplier shares inputs with the upper data bits of block RAM, the maximum data path width of the block RAM is 18 bits in this case.

The Internal Structure of the Block RAM

The block RAM has a dual port structure. The two identical data ports called A and B permit independent access to the common RAM block, which has a maximum capacity of 18,432 bits—or 16,384 bits when no parity lines are used. Each port has its own dedicated set of data, control and clock lines for synchronous read and write operations. There are four basic data paths, as shown in Figure 13: (1) write to and read from Port A, (2) write to and read from Port B, (3) data transfer from Port A to Port B, and (4) data transfer from Port B to Port A.

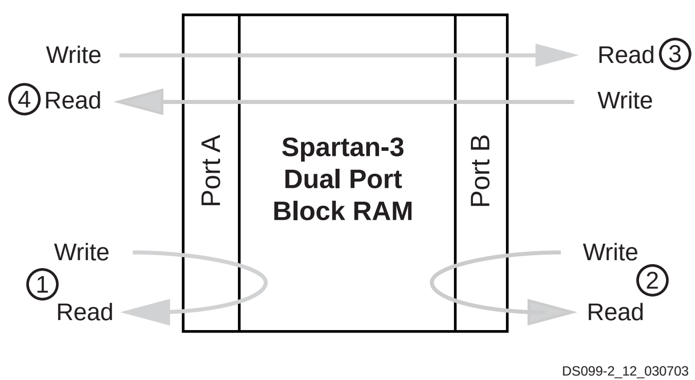
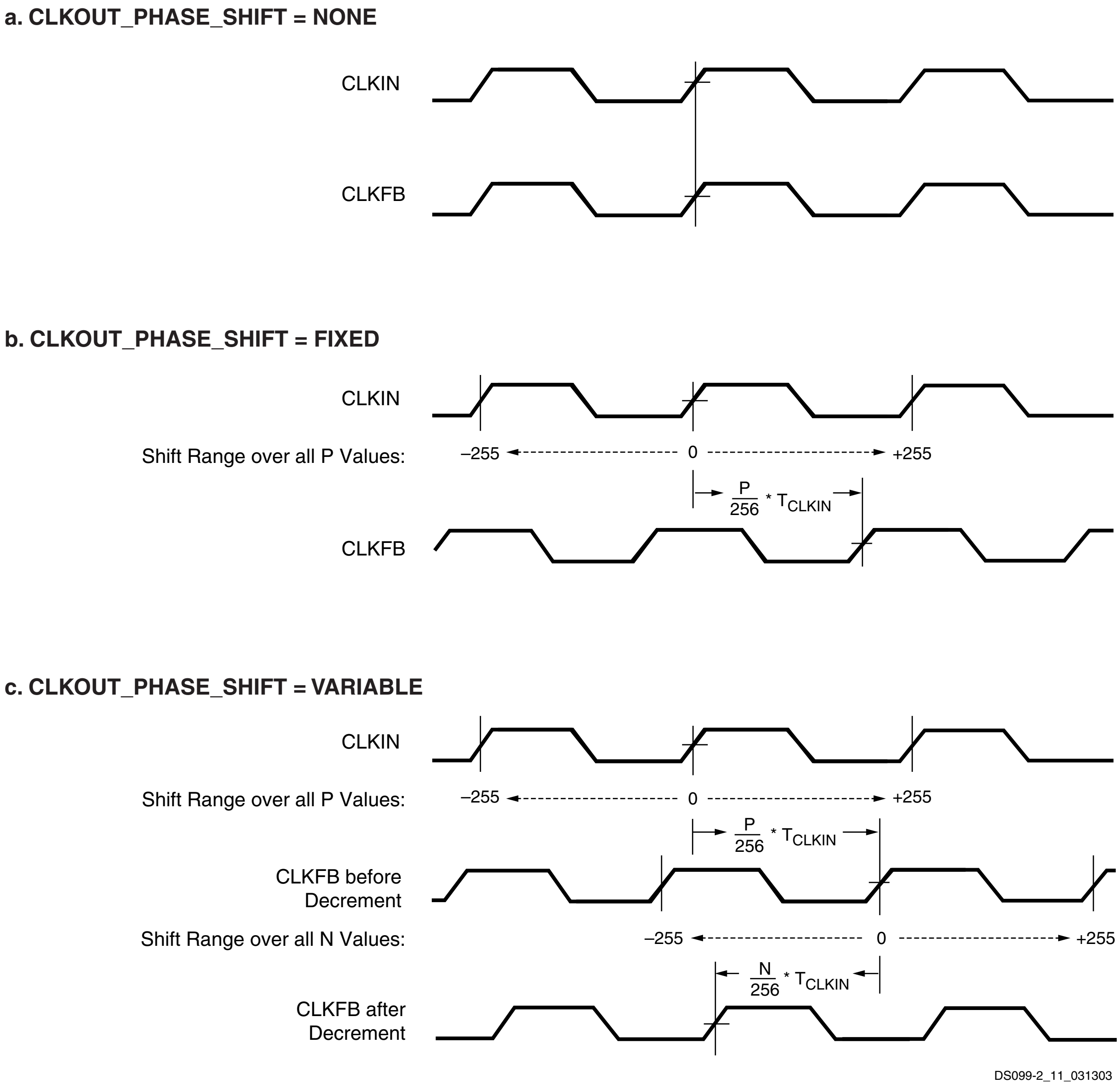


Figure 13: **Block RAM Data Paths**

Block RAM Port Signal Definitions

Representations of the dual-port primitive RAMB16_S[w_A]_S[w_B] and the single-port primitive RAMB16_S[w] with their associated signals are shown in Figure 14. These signals are defined in Table 13.



Notes:
1. P represents the integer value ranging from –255 to +255 to which the PHASE_SHIFT attribute is assigned.
2. N is an integer value ranging from –255 to +255 that represents the net phase shift effect from a series of increment and/or decrement operations.
   N = {Total number of increments} – {Total number of decrements}
   A positive value for N indicates a net increment; a negative value indicates a net decrement.

Figure 23: **Phase Shifter Waveforms**

The Status Logic Component

The Status Logic component not only reports on the state of the DCM but also provides a means of resetting the DCM to an initial known state. The signals associated with the Status Logic component are described in Table 22.

As a rule, the Reset (RST) input is asserted only upon configuring the device or changing the CLKIN frequency. A DCM reset does not affect attribute values (e.g., CLKFX_MULTIPLY and CLKFX_DIVIDE). If not used, RST must be tied to GND.

The eight bits of the STATUS bus are defined in Table 23.

Configuration

Spartan-3 devices are configured by loading application specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are "Dedicated" to one function only, while others, indicated by the term "Dual-Purpose", can be re-used as general-purpose User I/Os once configuration is complete.

Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M0, M1, and M2 are Dedicated pins. The mode pin settings are shown in Table 26.

Table 26: **Spartan-3 FPGAs Configuration Mode Pin Settings**

Configuration Mode[1]	M0	M1	M2	Synchronizing Clock	Data Width	Serial DOUT[2]
Master Serial	0	0	0	CCLK Output	1	Yes
Slave Serial	1	1	1	CCLK Input	1	Yes
Master Parallel	1	1	0	CCLK Output	8	No
Slave Parallel	0	1	1	CCLK Input	8	No
JTAG	1	0	1	TCK Input	1	No

Notes:
1. The voltage levels on the M0, M1, and M2 pins select the configuration mode.
2. The daisy chain is possible only in the Serial modes when DOUT is used.

The HSWAP_EN input pin defines whether the I/O pins that are not actively used during configuration have pull-up resistors during configuration. By default, HSWAP_EN is tied High (via an internal pull-up resistor if left floating) which shuts off the pull-up resistors on the user I/O pins during configuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration. The Dedicated configuration pins (CCLK, DONE, PROG_B, M2, M1, M0, HSWAP_EN) and the JTAG pins (TDI, TMS, TCK, and TDO) always have a pull-up resistor to VCCAUX during configuration, regardless of the value on the HSWAP_EN pin. Similarly, the dual-purpose INIT_B pin has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM, depending on the package style.

Depending on the chosen configuration mode, the FPGA either generates a CCLK output, or CCLK is an input accepting an externally generated clock.

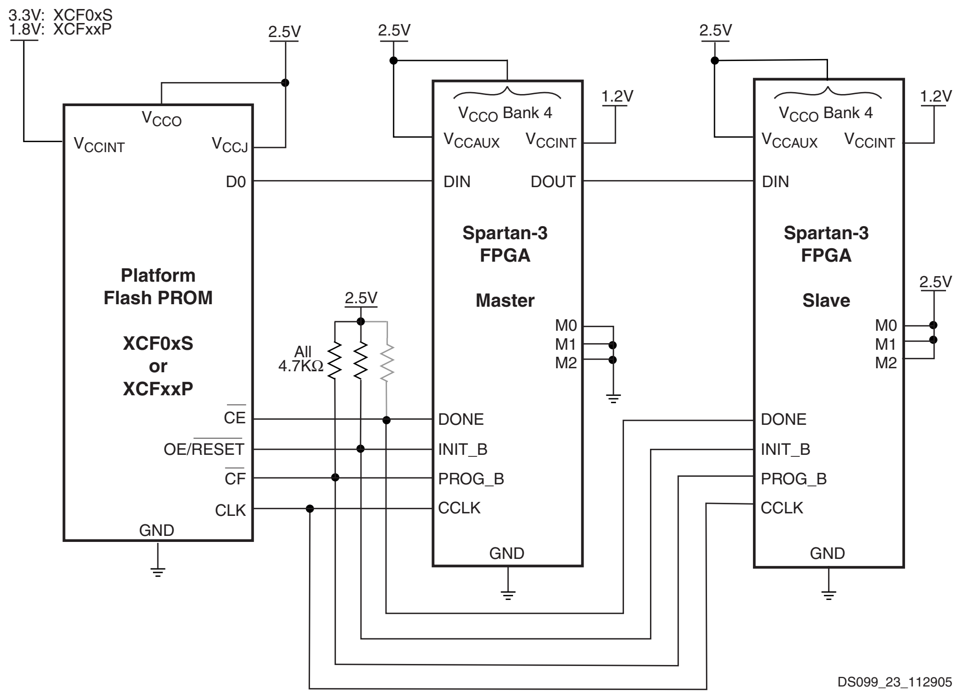
A persist option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected then the configuration pins with the exception of CCLK, PROG_B, and DONE can be used as user I/O in normal operation. The persist option does not apply to the boundary-scan related pins. The persist feature is valuable in applications that readback configuration data after entering the User mode.

Table 27 lists the total number of bits required to configure each FPGA as well as the PROMs suitable for storing those bits. See DS123: *Platform Flash In-System Programmable Configuration PROMs* data sheet for more information.

Table 27: **Spartan-3 FPGA Configuration Data**

Device	File Sizes	Xilinx Platform Flash PROM	
		Serial Configuration	Parallel Configuration
XC3S50	439,264	XCF01S	XCF08P
XC3S200	1,047,616	XCF01S	XCF08P
XC3S400	1,699,136	XCF02S	XCF08P
XC3S1000	3,223,488	XCF04S	XCF08P
XC3S1500	5,214,784	XCF08P	XCF08P
XC3S2000	7,673,024	XCF08P	XCF08P
XC3S4000	11,316,864	XCF16P	XCF16P
XC3S5000	13,271,936	XCF16P	XCF16P

The maximum bitstream length that Spartan-3 FPGAs support in serial daisy-chains is 4,294,967,264 bits (4 Gbits), roughly equivalent to a daisy-chain with 323 XC3S5000 FPGAs. This is a limit only for serial daisy-chains where configuration data is passed via the FPGA's DOUT pin. There is no such limit for JTAG chains.



Notes:

1. There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.
2. For information on how to program the FPGA using 3.3V signals and power, see 3.3V-Tolerant Configuration Interface.

Figure 26: **Connection Diagram for Master and Slave Serial Configuration**

Slave Serial mode is selected by applying <111> to the mode pins (M0, M1, and M2). A pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

Master Serial Mode

In Master Serial mode, the FPGA drives CCLK pin, which behaves as a bidirectional I/O pin. The FPGA in the center of Figure 26 is set for Master Serial mode and connects to the serial configuration PROM and to the CCLK inputs of any slave FPGAs in a configuration daisy-chain. The master FPGA drives the configuration clock on the CCLK pin to the Xilinx Serial PROM, which, in response, provides bit-serial data to the FPGA's DIN input. The FPGA accepts this data on each rising CCLK edge. After the master FPGA finishes configuring, it passes data on its DOUT pin to the next FPGA device in a daisy-chain. The DOUT data appears after the falling CCLK clock edge.

The Master Serial mode interface is identical to Slave Serial except that an internal oscillator generates the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK, which always starts at a default frequency of 6 MHz. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

Slave Parallel Mode (SelectMAP)

The Parallel or SelectMAP modes support the fastest configuration. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data. An external source provides 8-bit-wide data, CCLK, an active-Low Chip Select (CS_B) signal and an active-Low Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the Slave Parallel mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, it is possible to use any of the Multipurpose pins (DIN/D0-D7, DOUT/BUSY, INIT_B, CS_B, and RDWR_B) as User I/Os. To do this, simply set the BitGen option *Persist* to *No* and assign the desired signals to multipurpose configuration pins using the Xilinx development software. Alternatively, it is possible to continue using the configuration port

Revision History

Date	Version No.	Description
04/11/03	1.0	Initial Xilinx release
05/19/03	1.1	Added Block RAM column, DCMs, and multipliers to XC3S50 descriptions.
07/11/03	1.2	Explained the configuration port *Persist* option in Slave Parallel Mode (SelectMAP) section. Updated Figure 8 and Double-Data-Rate Transmission section to indicate that DDR clocking for the XC3S50 is the same as that for all other Spartan-3 devices. Updated description of I/O voltage tolerance in ESD Protection section. In Table 10, changed input termination type for DCI version of the LVCMOS standard to *None*. Added additional flexibility for making DLL connections in Figure 21 and accompanying text. In the Configuration section, inserted an explanation of how to choose power supplies for the configuration interface, including guidelines for achieving 3.3V-tolerance.
08/24/04	1.3	Showed inversion of 3-state signal (Figure 7). Clarified description of pull-up and pull-down resistors (Table 6 and page 13). Added information on operating block RAM with multipliers to page 26. Corrected output buffer name in Figure 21. Corrected description of how DOUT is synchronized to CCLK (page 47).
08/19/05	1.4	Corrected description of WRITE_FIRST and READ_FIRST in Table 13. Added note regarding address setup and hold time requirements whenever a block RAM port is enabled (Table 13). Added information in the maximum length of a Configuration daisy-chain. Added reference to XAPP453 in 3.3V-Tolerant Configuration Interface section. Added information on the STATUS[2] DCM output (Table 23). Added information on CCLK behavior and termination recommendations to Configuration. Added Additional Configuration Details section. Added Powering Spartan-3 FPGAs section. Removed GSR from Figure 31 because its timing is not programmable.
04/03/06	2.0	Updated Figure 7. Updated Figure 14. Updated Table 10. Updated Figure 22. Corrected Platform Flash supply voltage name and value in Figure 26 and Figure 28. Added No Internal Charge Pumps or Free-Running Oscillators. Corrected a few minor typographical errors.
04/26/06	2.1	Added more information on the pull-up resistors that are active during configuration to Configuration. Added information to Boundary-Scan (JTAG) Mode about potential interactions when configuring via JTAG if the mode select pins are set for other than JTAG.
05/25/07	2.2	Added Spartan-3 FPGA Design Documentation. Noted SSTL2_I_DCI 25-Ohm driver in Table 10 and Table 11. Added note that pull-down is active during boundary scan tests.
11/30/07	2.3	Updated links to documentation on xilinx.com.
06/25/08	2.4	Added HSLVDCI to Table 10. Updated formatting and links.
12/04/09	2.5	Updated HSLVDCI description in Digitally Controlled Impedance (DCI). Updated the low-voltage differential signaling V_{CCO} values in Table 10. Noted that the CP132 package is being discontinued in The Organization of IOBs into Banks. Updated rule 4 in Rules Concerning Banks. Added software version requirement in The Fixed Phase Mode.
10/29/12	3.0	Added Notice of Disclaimer. Per XCN07022, updated the discontinued FG1156 and FGG1156 package discussion throughout document. Per XCN08011, updated the discontinued CP132 and CPG132 package discussion throughout document. This product is not recommended for new designs.

Table 34: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical(1)	Commercial Maximum(1)	Industrial Maximum(1)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50	5	24	31	mA
		XC3S200	10	54	80	mA
		XC3S400	15	110	157	mA
		XC3S1000	35	160	262	mA
		XC3S1500	45	260	332	mA
		XC3S2000	60	360	470	mA
		XC3S4000	100	450	810	mA
		XC3S5000	120	600	870	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50	1.5	2.0	2.5	mA
		XC3S200	1.5	3.0	3.5	mA
		XC3S400	1.5	3.0	3.5	mA
		XC3S1000	2.0	4.0	5.0	mA
		XC3S1500	2.5	4.0	5.0	mA
		XC3S2000	3.0	5.0	6.0	mA
		XC3S4000	3.5	5.0	6.0	mA
		XC3S5000	3.5	5.0	6.0	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50	7	20	22	mA
		XC3S200	10	30	33	mA
		XC3S400	15	40	44	mA
		XC3S1000	20	50	55	mA
		XC3S1500	35	75	85	mA
		XC3S2000	45	90	100	mA
		XC3S4000	55	110	125	mA
		XC3S5000	70	130	145	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using devices with typical processing at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). Maximum values are the production test limits measured for each device at the maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.465V, and V_{CCAUX} = 2.625V. The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements, the use of DCI standards, etc.), measured quiescent current levels may be different than the values in the table. Use the XPower Estimator or XPower Analyzer for more accurate estimates. See Note 2.
2. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3 XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer, part of the Xilinx ISE development software, uses the FPGA netlist as input to provide more accurate maximum and typical estimates.
3. The maximum numbers in this table also indicate the minimum current each power rail requires in order for the FPGA to power-on successfully, once all three rails are supplied. If V_{CCINT} is applied before V_{CCAUX}, there may be temporary additional I_{CCINT} current until V_{CCAUX} is applied. See Surplus I_{CCINT} if V_{CCINT} Applied before V_{CCAUX}, page 54

Table 36: **DC Characteristics of User I/Os Using Single-Ended Standards *(Cont'd)***

Signal Standard (IOSTANDARD) and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVCMOS33[4]	2	2	–2	0.4	$V_{CCO} - 0.4$
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_33, LVDCI_DV2_33		Note 3	Note 3		
LVTTL[4]	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
PCI33_3		Note 6	Note 6	$0.10V_{CCO}$	$0.90V_{CCO}$
SSTL18_I		6.7	–6.7	$V_{TT} - 0.475$	$V_{TT} + 0.475$
SSTL18_I_DCI		Note 3	Note 3		
SSTL18_II		13.4	–13.4	$V_{TT} - 0.475$	$V_{TT} + 0.475$
SSTL2_I		8.1	–8.1	$V_{TT} - 0.61$	$V_{TT} + 0.61$
SSTL2_I_DCI		Note 3	Note 3		
SSTL2_II[7]		16.2	–16.2	$V_{TT} - 0.81$	$V_{TT} + 0.81$
SSTL2_II_DCI[7]		Note 3	Note 3		

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32 and Table 35.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL} – the output current condition under which VOL is tested
   I_{OH} – the output current condition under which VOH is tested
   V_{OL} – the output voltage that indicates a Low logic level
   V_{OH} – the output voltage that indicates a High logic level
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
   V_{CCO} – the supply voltage for output drivers as well as LVCMOS, LVTTL, and PCI inputs
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{TT} – the voltage applied to a resistor termination
3. Tested according to the standard's relevant specifications. When using the DCI version of a standard on a given I/O bank, that bank will consume more power than if the non-DCI version had been used instead. The additional power is drawn for the purpose of impedance-matching at the I/O pins. A portion of this power is dissipated in the two RREF resistors.
4. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for both the Fast and Slow slew attributes.
5. All dedicated output pins (CCLK, DONE, and TDO) and dual-purpose totem-pole output pins (D0-D7 and BUSY/DOUT) exhibit the characteristics of LVCMOS25 with 12 mA drive and slow slew rate. For information concerning the use of 3.3V signals, see 3.3V-Tolerant Configuration Interface, page 47.
6. Tested according to the relevant PCI specifications. For more information, see XAPP457.
7. The minimum usable V_{TT} voltage is 1.25V.

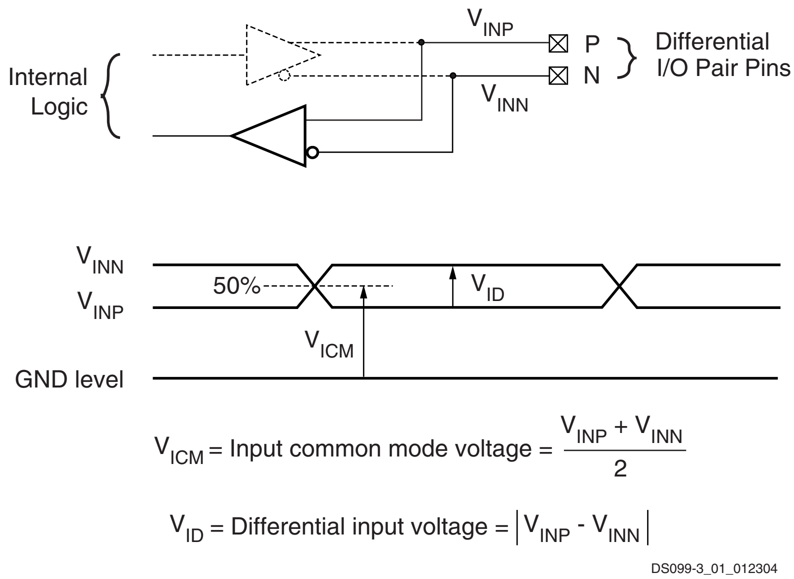


Figure 32: **Differential Input Voltages**

Table 37: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

Signal Standard (IOSTANDARD)	V_{CCO}[1]			V_{ID}[3]			V_{ICM}		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LDT_25 (ULVDS_25)	2.375	2.50	2.625	200	600	1000	0.44	0.60	0.78
LVDS_25, LVDS_25_DCI	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20
BLVDS_25	2.375	2.50	2.625	-	350	-	-	1.25	-
LVDSEXT_25, LVDSEXT_25_DCI	2.375	2.50	2.625	100	540	1000	0.30	1.20	2.20
LVPECL_25	2.375	2.50	2.625	100	-	-	0.30	1.20	2.00
RSDS_25	2.375	2.50	2.625	100	200	-	-	1.20	-
DIFF_HSTL_II_18, DIFF_HSTL_II_18_DCI	1.70	1.80	1.90	200	-	-	0.80	-	1.00
DIFF_SSTL2_II, DIFF_SSTL2_II_DCI	2.375	2.50	2.625	300	-	-	1.05	-	1.45

Notes:

1. V_{CCO} only supplies differential output drivers, not input circuits.
2. V_{REF} inputs are not used for any of the differential I/O standards.
3. V_{ID} is a differential measurement.

Table 56: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{BCKO}	When reading from the Block RAM, the time from the active transition at the CLK input to data appearing at the DOUT output	–	2.09	–	2.40	ns
Setup Times						
T_{BDCK}	Time from the setup of data at the DIN inputs to the active transition at the CLK input of the Block RAM	0.43	–	0.49	–	ns
Hold Times						
T_{BCKD}	Time from the active transition at the Block RAM's CLK input to the point where data is last held at the DIN inputs	0	–	0	–	ns
Clock Timing						
T_{BPWH}	Block RAM CLK signal High pulse width	1.19	∞	1.37	∞	ns
T_{BPWL}	Block RAM CLK signal Low pulse width	1.19	∞	1.37	∞	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. For minimums, use the values reported by the Xilinx timing analyzer.

Clock Distribution Switching Characteristics

Table 57: **Clock Distribution Switching Characteristics**

Description	Symbol	Maximum		Units
		Speed Grade		
		-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I-input to O-output delay	T_{GIO}	0.36	0.41	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0- and I1-inputs. Same as BUFGCE enable CE-input	T_{GSI}	0.53	0.60	ns

Notes:
1. For minimums, use the values reported by the Xilinx timing analyzer.

CCLK: Configuration Clock

The configuration clock signal on this pin synchronizes the reading or writing of configuration data. The CCLK pin is an input-only pin for the Slave Serial and Slave Parallel configuration modes. In the Master Serial and Master Parallel configuration modes, the FPGA drives the CCLK pin and CCLK should be treated as a full bidirectional I/O pin for signal integrity analysis.

Although the CCLK frequency is relatively low, Spartan-3 FPGA output edge rates are fast. Any potential signal integrity problems on the CCLK board trace can cause FPGA configuration to fail. Therefore, pay careful attention to the CCLK signal integrity on the printed circuit board. Signal integrity simulation with IBIS is recommended. For all configuration modes except JTAG, consider the signal integrity at every CCLK trace destination, including the FPGA's CCLK pin. For more details on CCLK design considerations, see Chapter 2 of UG332, *Spartan-3 Generation Configuration User Guide*.

During configuration, the CCLK pin has a pull-up resistor to VCCAUX, regardless of the HSWAP_EN pin. After configuration, the CCLK pin is pulled High to VCCAUX by default as defined by the ***CclkPin*** bitstream selection, although this behavior is programmable. Any clocks applied to CCLK after configuration are ignored unless the bitstream option ***Persist*** is set to ***Yes***, which retains the configuration interface. ***Persist*** is set to ***No*** by default. However, if ***Persist*** is set to ***Yes***, then all clock edges are potentially active events, depending on the other configuration control signals.

The bitstream generator option ***ConfigRate*** determines the frequency of the internally-generated CCLK oscillator required for the Master configuration modes. The actual frequency is approximate due to the characteristics of the silicon oscillator and varies by up to 50% over the temperature and voltage range. By default, CCLK operates at approximately 6 MHz. Via the ***ConfigRate*** option, the oscillator frequency is set at approximately 3, 6, 12, 25, or 50 MHz. At power-on, CCLK always starts operation at its lowest frequency. The device does not start operating at the higher frequency until the ConfigRate control bits are loaded during the configuration process.

PROG_B: Program/Configure Device

This asynchronous pin initiates the configuration or re-configuration processes. A Low-going pulse resets the configuration logic, initializing the configuration memory. This initialization process cannot finish until PROG_B returns High. Asserting PROG_B Low for an extended period delays the configuration process. At power-up, there is always a pull-up resistor to VCCAUX on this pin, regardless of the HSWAP_EN input. After configuration, the bitstream generator option ***ProgPin*** determines whether or not the pull-up resistor is present. By default, the ***ProgPin*** option retains the pull-up resistor.

After configuration, hold the PROG_B input High. Any Low-going pulse on PROG_B lasting 300 ns or longer restarts the configuration process.

Table 73: **PROG_B Operation**

PROG_B Input	Response
Power-up	Automatically initiates configuration process.
Low-going pulse	Initiate (re-)configuration process and continue to completion.
Extended Low	Initiate (re-)configuration process and stall process at step where configuration memory is cleared. Process is stalled until PROG_B returns High.
1	If the configuration process is started, continue to completion. If configuration process is complete, stay in User mode.

DONE: Configuration Done, Delay Start-Up Sequence

The FPGA produces a Low-to-High transition on this pin indicating that the configuration process is complete. The bitstream generator option ***DriveDone*** determines whether this pin functions as a totem-pole output that can drive High or as an open-drain output. If configured as an open-drain output—which is the default behavior—then a pull-up resistor is required to produce a High logic level. There is a bitstream option that provides an internal pull-up resistor, otherwise an external pull-up resistor is required.

The open-drain option permits the DONE lines of multiple FPGAs to be tied together, so that the common node transitions High only after all of the FPGAs have completed configuration. Externally holding the open-drain DONE pin Low delays the start-up sequence, which marks the transition to user mode.

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3 FPGA is reported using either the XPower Estimator (XPE) or the XPower Analyzer integrated in the Xilinx ISE development software. Table 86 provides the thermal characteristics for the various Spartan-3 device/package offerings.

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference per watt between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 86: **Spartan-3 FPGA Package Thermal Characteristics**

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
VQ(G)100	XC3S50	12.0	–	46.2	38.4	35.8	34.9	°C/Watt
	XC3S200	10.0	–	40.5	33.7	31.3	30.5	°C/Watt
CP(G)132[1]	XC3S50	14.5	32.8	53.0	46.4	44.0	42.5	°C/Watt
TQ(G)144	XC3S50	7.6	–	41.0	31.9	27.2	25.6	°C/Watt
	XC3S200	6.6	–	34.5	26.9	23.0	21.6	°C/Watt
	XC3S400	6.1	–	32.8	25.5	21.8	20.4	°C/Watt
PQ(G)208	XC3S50	10.6	–	37.4	27.6	24.4	22.6	°C/Watt
	XC3S200	8.6	–	36.2	26.7	23.6	21.9	°C/Watt
	XC3S400	7.5	–	35.4	26.1	23.1	21.4	°C/Watt
FT(G)256	XC3S200	9.9	22.9	31.7	25.6	24.5	24.2	°C/Watt
	XC3S400	7.9	19.0	28.4	22.8	21.5	21.0	°C/Watt
	XC3S1000	5.6	14.7	24.8	19.2	18.0	17.5	°C/Watt
FG(G)320	XC3S400	8.9	13.9	24.4	19.0	17.8	17.0	°C/Watt
	XC3S1000	7.8	11.8	22.3	17.0	15.8	15.0	°C/Watt
	XC3S1500	6.7	9.8	20.3	15.18	13.8	13.1	°C/Watt
FG(G)456	XC3S400	8.4	13.6	20.8	15.1	13.9	13.4	°C/Watt
	XC3S1000	6.4	10.6	19.3	13.4	12.3	11.7	°C/Watt
	XC3S1500	4.9	8.3	18.3	12.4	11.2	10.7	°C/Watt
	XC3S2000	3.7	6.5	17.7	11.7	10.5	10.0	°C/Watt
FG(G)676	XC3S1000	6.0	10.4	17.9	13.7	12.6	12.0	°C/Watt
	XC3S1500	4.9	8.8	16.8	12.4	11.3	10.7	°C/Watt
	XC3S2000	4.1	7.9	15.6	11.1	9.9	9.3	°C/Watt
	XC3S4000	3.6	7.0	15.0	10.5	9.3	8.7	°C/Watt
	XC3S5000	3.4	6.3	14.7	10.3	9.1	8.5	°C/Watt
FG(G)900	XC3S2000	3.7	7.0	14.3	10.3	9.3	8.8	°C/Watt
	XC3S4000	3.3	6.4	13.6	9.7	8.7	8.2	°C/Watt
	XC3S5000	2.9	5.9	13.1	9.2	8.1	7.6	°C/Watt

Table 87: **VQ100 Package Pinout *(Cont'd)***

Bank	XC3S50 XC3S200 Pin Name	VQ100 Pin Number	Type
6	IO_L40P_6/VREF_6	P13	VREF
6	VCCO_6	P19	VCCO
7	IO_L01N_7/VRP_7	P2	DCI
7	IO_L01P_7/VRN_7	P1	DCI
7	IO_L21N_7	P5	I/O
7	IO_L21P_7	P4	I/O
7	IO_L23N_7	P9	I/O
7	IO_L23P_7	P8	I/O
7	IO_L40N_7/VREF_7	P12	VREF
7	IO_L40P_7	P11	I/O
7	VCCO_7	P6	VCCO
N/A	GND	P3	GND
N/A	GND	P10	GND
N/A	GND	P20	GND
N/A	GND	P29	GND
N/A	GND	P41	GND
N/A	GND	P56	GND
N/A	GND	P66	GND
N/A	GND	P73	GND
N/A	GND	P82	GND
N/A	GND	P95	GND
N/A	VCCAUX	P7	VCCAUX
N/A	VCCAUX	P33	VCCAUX
N/A	VCCAUX	P58	VCCAUX
N/A	VCCAUX	P84	VCCAUX
N/A	VCCINT	P18	VCCINT
N/A	VCCINT	P45	VCCINT
N/A	VCCINT	P69	VCCINT
N/A	VCCINT	P93	VCCINT
VCCAUX	CCLK	P52	CONFIG
VCCAUX	DONE	P51	CONFIG
VCCAUX	HSWAP_EN	P98	CONFIG
VCCAUX	M0	P25	CONFIG
VCCAUX	M1	P24	CONFIG
VCCAUX	M2	P26	CONFIG
VCCAUX	PROG_B	P99	CONFIG
VCCAUX	TCK	P77	JTAG
VCCAUX	TDI	P100	JTAG

CP132: 132-Ball Chip-Scale Package

Note: The CP132 and CPG132 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

The pinout and footprint for the XC3S50 in the 132-ball chip-scale package, CP132, appear in Table 89 and Figure 45.

All the package pins appear in Table 89 and are sorted by bank number, then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The CP132 footprint has eight I/O banks. However, the voltage supplies for the two I/O banks along an edge are connected together internally. Consequently, there are four output voltage supplies, labeled VCCO_TOP, VCCO_RIGHT, VCCO_BOTTOM, and VCCO_LEFT.

Pinout Table

Table 89: **CP132 Package Pinout**

Bank	XC3S50 Pin Name	CP132 Ball	Type
0	IO_L01N_0/VRP_0	A3	DCI
0	IO_L01P_0/VRN_0	C4	DCI
0	IO_L27N_0	C5	I/O
0	IO_L27P_0	B5	I/O
0	IO_L30N_0	B6	I/O
0	IO_L30P_0	A6	I/O
0	IO_L31N_0	C7	I/O
0	IO_L31P_0/VREF_0	B7	VREF
0	IO_L32N_0/GCLK7	A7	GCLK
0	IO_L32P_0/GCLK6	C8	GCLK
1	IO_L01N_1/VRP_1	A13	DCI
1	IO_L01P_1/VRN_1	B13	DCI
1	IO_L27N_1	C11	I/O
1	IO_L27P_1	A12	I/O
1	IO_L28N_1	A11	I/O
1	IO_L28P_1	B11	I/O
1	IO_L31N_1/VREF_1	C9	VREF
1	IO_L31P_1	A10	I/O
1	IO_L32N_1/GCLK5	A8	GCLK
1	IO_L32P_1/GCLK4	A9	GCLK
2	IO_L01N_2/VRP_2	D12	DCI
2	IO_L01P_2/VRN_2	C14	DCI
2	IO_L20N_2	E12	I/O
2	IO_L20P_2	E13	I/O
2	IO_L21N_2	E14	I/O
2	IO_L21P_2	F12	I/O
2	IO_L23N_2/VREF_2	F13	VREF
2	IO_L23P_2	F14	I/O
2	IO_L24N_2	G12	I/O

Table 91: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
2	IO_L23N_2/VREF_2	P98	VREF
2	IO_L23P_2	P97	I/O
2	IO_L24N_2	P96	I/O
2	IO_L24P_2	P95	I/O
2	IO_L40N_2	P93	I/O
2	IO_L40P_2/VREF_2	P92	VREF
3	IO	P76	I/O
3	IO_L01N_3/VRP_3	P74	DCI
3	IO_L01P_3/VRN_3	P73	DCI
3	IO_L20N_3	P78	I/O
3	IO_L20P_3	P77	I/O
3	IO_L21N_3	P80	I/O
3	IO_L21P_3	P79	I/O
3	IO_L22N_3	P83	I/O
3	IO_L22P_3	P82	I/O
3	IO_L23N_3	P85	I/O
3	IO_L23P_3/VREF_3	P84	VREF
3	IO_L24N_3	P87	I/O
3	IO_L24P_3	P86	I/O
3	IO_L40N_3/VREF_3	P90	VREF
3	IO_L40P_3	P89	I/O
4	IO/VREF_4	P70	VREF
4	IO_L01N_4/VRP_4	P69	DCI
4	IO_L01P_4/VRN_4	P68	DCI
4	IO_L27N_4/DIN/D0	P65	DUAL
4	IO_L27P_4/D1	P63	DUAL
4	IO_L30N_4/D2	P60	DUAL
4	IO_L30P_4/D3	P59	DUAL
4	IO_L31N_4/INIT_B	P58	DUAL
4	IO_L31P_4/DOUT/BUSY	P57	DUAL
4	IO_L32N_4/GCLK1	P56	GCLK
4	IO_L32P_4/GCLK0	P55	GCLK
5	IO/VREF_5	P44	VREF
5	IO_L01N_5/RDWR_B	P41	DUAL
5	IO_L01P_5/CS_B	P40	DUAL
5	IO_L28N_5/D6	P47	DUAL
5	IO_L28P_5/D7	P46	DUAL
5	IO_L31N_5/D4	P51	DUAL
5	IO_L31P_5/D5	P50	DUAL
5	IO_L32N_5/GCLK3	P53	GCLK

TQ144 Footprint

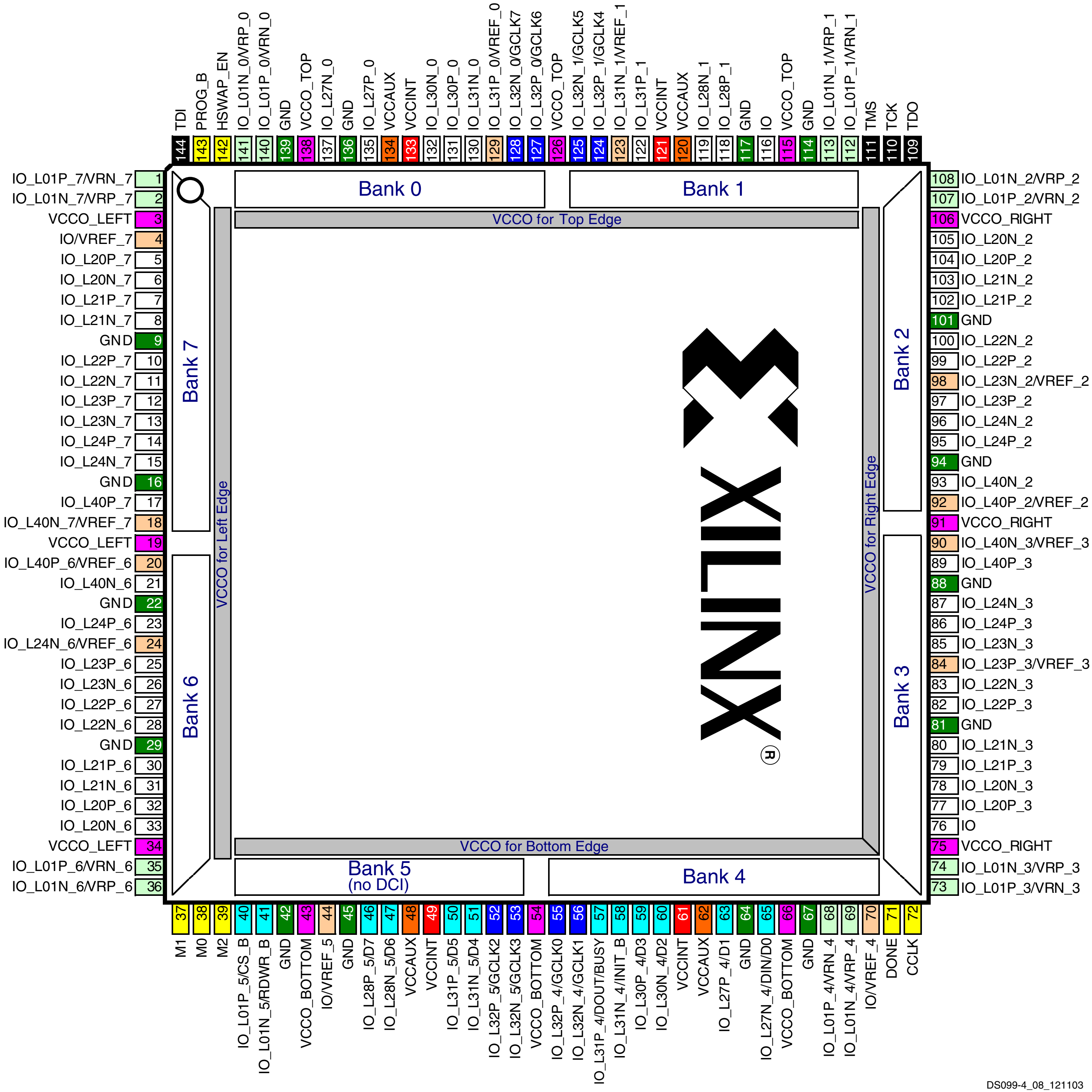


Figure 46: **TQ144 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

51	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	12	**VREF:** User I/O or input voltage reference for bank
14	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input	12	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	16	**GND:** Ground	4	**VCCAUX:** Auxiliary voltage supply (+2.5V)

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
N/A	VCCINT	N6	VCCINT
N/A	VCCINT	N7	VCCINT
VCCAUX	CCLK	T15	CONFIG
VCCAUX	DONE	R15	CONFIG
VCCAUX	HSWAP_EN	E6	CONFIG
VCCAUX	M0	P5	CONFIG
VCCAUX	M1	U3	CONFIG
VCCAUX	M2	R4	CONFIG
VCCAUX	PROG_B	E5	CONFIG
VCCAUX	TCK	E14	JTAG
VCCAUX	TDI	D4	JTAG
VCCAUX	TDO	D15	JTAG
VCCAUX	TMS	B16	JTAG

User I/Os by Bank

Table 99 indicates how the available user-I/O pins are distributed between the eight I/O banks on the FG320 package.

Table 99: **User I/Os Per Bank in FG320 Package**

Package Edge	I/O Bank	Maximum I/O	Maximum LVDS Pairs	All Possible I/O Pins by Type				
				I/O	DUAL	DCI	VREF	GCLK
Top	0	26	11	19	0	2	3	2
	1	26	11	19	0	2	3	2
Right	2	29	14	23	0	2	4	0
	3	29	14	23	0	2	4	0
Bottom	4	27	11	13	6	2	4	2
	5	26	11	13	6	2	3	2
Left	6	29	14	23	0	2	4	0
	7	29	14	23	0	2	4	0

FG320 Footprint

Bank 0 | Bank 1

Bank 7 (rows A–J, left) | Bank 2 (rows A–J, right) | Bank 6 (rows K–V, left) | Bank 3 (rows K–V, right)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	GND	I/O L01N_0 VRP_0	I/O L01P_0 VRN_0	I/O L15N_0	I/O L15P_0	GND	I/O L30N_0	I/O L30P_0	I/O L31P_0 VREF_0	I/O L31N_1 VREF_1	I/O	I/O VREF_1	GND	I/O L16N_1	I/O L10N_1 VREF_1	I/O L01N_1 VRP_1	I/O L01P_1 VRN_1	GND
B	I/O L16P_7 VREF_7	GND	I/O VREF_0	I/O L09N_0	I/O L25N_0	I/O L25P_0	VCCAUX	VCCO_0	I/O L31N_0	I/O L31P_1	VCCO_1	VCCAUX	I/O	I/O L16P_1	I/O L10P_1	TMS	GND	I/O L16N_2
C	I/O L16N_7	I/O L01P_7 VRN_7	I/O L01N_7 VRP_7	I/O L09P_0	I/O L10N_0	VCCO_0	I/O L27N_0	I/O L28N_0	GND	GND	I/O L30N_1	I/O L28N_1	VCCO_1	I/O L15N_1	I/O L15P_1	I/O L01N_2 VRP_2	I/O L01P_2 VRN_2	I/O L16P_2
D	I/O L17N_7	I/O L17P_7	I/O L19P_7	TDI	I/O L10P_0	I/O VREF_0	I/O L27P_0	I/O L28P_0	I/O	I/O	I/O L30P_1	I/O L28P_1	I/O L24P_1	I/O L24N_1	TDO	I/O L19N_2	I/O L17N_2	I/O L17P_2 VREF_2
E	I/O L20P_7	I/O L20N_7	I/O L19N_7 VREF_7	I/O L21N_7	PROG_B	HSWAP_ EN	I/O	I/O L29N_0	I/O L32N_0 GCLK7	I/O L32N_1 GCLK5	I/O L29P_1	I/O L27P_1	I/O L27N_1	TCK	I/O L21P_2	I/O L19P_2	I/O L20N_2	I/O L20P_2
F	GND	I/O L23P_7	VCCO_7	I/O L21P_7	I/O L22P_7	VCCINT	VCCINT	I/O L29P_0	I/O L32P_0 GCLK6	I/O L32P_1 GCLK4	I/O L29N_1	VCCINT	VCCINT	I/O L22N_2	I/O L21N_2	VCCO_2	I/O L23P_2	GND
G	I/O L23N_7	VCCAUX	I/O L24P_7	I/O L24N_7	I/O L22N_7	VCCINT	GND	VCCO_0	VCCO_0	VCCO_1	VCCO_1	GND	VCCINT	I/O L22P_2	I/O L24N_2	I/O L24P_2	VCCAUX	I/O L23N_2 VREF_2
H	I/O L35N_7	I/O L35P_7	I/O L34P_7	I/O L34N_7	I/O L27N_7	I/O L27P_7 VREF_7	VCCO_7	GND	GND	GND	GND	VCCO_2	I/O L27N_2	I/O L27P_2	I/O L34P_2	I/O L34N_2 VREF_2	I/O L35N_2	I/O L35P_2
J	I/O L39N_7	I/O L39P_7	GND	I/O L40P_7	I/O L40N_7 VREF_7	I/O	VCCO_7	GND			GND	VCCO_2	I/O	I/O L40P_2 VREF_2	I/O L40N_2	GND	I/O L39P_2	I/O L39N_2
K	I/O L40N_6	I/O L40P_6 VREF_6	GND	I/O L39P_6	I/O L39N_6	I/O	VCCO_6	GND			GND	VCCO_3	I/O L39N_3	I/O L39P_3	I/O	GND	I/O L40N_3 VREF_3	I/O L40P_3
L	I/O L35P_6	I/O L35N_6	I/O L34N_6 VREF_6	I/O L34P_6	I/O L27P_6	I/O L27N_6	VCCO_6	GND	GND	GND	GND	VCCO_3	I/O L27P_3	I/O L27N_3	I/O L34N_3	I/O L34P_3 VREF_3	I/O L35P_3	I/O L35N_3
M	I/O L24P_6	VCCAUX	I/O L23N_6	I/O L23P_6	I/O L22P_6	VCCINT	GND	VCCO_5	VCCO_5	VCCO_4	VCCO_4	GND	VCCINT	I/O L22N_3	I/O L23N_3	I/O L23P_3 VREF_3	VCCAUX	I/O L24N_3
N	GND	I/O L24N_6 VREF_6	VCCO_6	I/O L21N_6	I/O L22N_6	VCCINT	VCCINT	I/O	I/O L32N_5 GCLK3	I/O L32N_4 GCLK1	I/O L30N_4 D2	VCCINT	VCCINT	I/O L22P_3	I/O L21P_3	VCCO_3	I/O L24P_3	GND
P	I/O L20P_6	I/O L20N_6	I/O L19P_6	I/O L21P_6	M0	I/O L27N_5 VREF_5	I/O L27P_5	I/O	I/O L32P_5 GCLK2	I/O L32P_4 GCLK0	I/O L30P_4 D3	I/O	I/O L25P_4	I/O L06N_4 VREF_4	I/O L21N_3	I/O L17N_3	I/O L20P_3	I/O L20N_3
R	I/O L17P_6 VREF_6	I/O L17N_6	I/O L19N_6	M2	I/O L15P_5	I/O L15N_5	I/O L28N_5 D6	I/O L30N_5	I/O VREF_5	I/O VREF_4	I/O L29N_4	I/O L27P_4 D1	I/O L25N_4	I/O L06P_4	DONE	I/O L17P_3 VREF_3	I/O L19N_3	I/O L19P_3
T	I/O L16P_6	I/O L01P_6 VRN_6	I/O L01N_6 VRP_6	I/O L06P_5	I/O L06N_5	VCCO_5	I/O L28P_5 D7	I/O L30P_5	GND	GND	I/O L29P_4	I/O L27N_4 DIN D0	VCCO_4	I/O L10N_4	CCLK	I/O L01P_3 VRN_3	I/O L01N_3 VRP_3	I/O L16N_3
U	I/O L16N_6	GND	M1	I/O L10P_5 VRN_5	I/O L16P_5	I/O	VCCAUX	VCCO_5	I/O L31N_5 D4	I/O L31N_4 INIT_B	VCCO_4	VCCAUX	I/O VREF_4	I/O L10P_4	I/O L09N_4	I/O L01N_4 VRP_4	GND	I/O L16P_3
V	GND	I/O L01P_5 CS_B	I/O L01N_5 RDWR_B	I/O L10N_5 VRP_5	I/O L16N_5	GND	I/O L29P_5 VREF_5	I/O L29N_5	I/O L31P_5 D5	I/O L31P_4 DOUT BUSY	I/O L28P_4	I/O L28N_4	GND	I/O	I/O L09P_4	I/O L01P_4 VRN_4	I/O VREF_4	GND

Bank 5 | Bank 4

ds099-3_16_121103

Figure 50: **FG320 Package Footprint (Top View)**

156	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	29	**VREF:** User I/O or input voltage reference for bank
16	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input	28	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	12	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	40	**GND:** Ground	8	**VCCAUX:** Auxiliary voltage supply (+2.5V)

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
N/A	GND	GND	GND	GND	GND	D15	GND
N/A	GND	GND	GND	GND	GND	D23	GND
N/A	GND	GND	GND	GND	GND	K11	GND
N/A	GND	GND	GND	GND	GND	K12	GND
N/A	GND	GND	GND	GND	GND	K15	GND
N/A	GND	GND	GND	GND	GND	K16	GND
N/A	GND	GND	GND	GND	GND	L10	GND
N/A	GND	GND	GND	GND	GND	L11	GND
N/A	GND	GND	GND	GND	GND	L12	GND
N/A	GND	GND	GND	GND	GND	L13	GND
N/A	GND	GND	GND	GND	GND	L14	GND
N/A	GND	GND	GND	GND	GND	L15	GND
N/A	GND	GND	GND	GND	GND	L16	GND
N/A	GND	GND	GND	GND	GND	L17	GND
N/A	GND	GND	GND	GND	GND	M4	GND
N/A	GND	GND	GND	GND	GND	M10	GND
N/A	GND	GND	GND	GND	GND	M11	GND
N/A	GND	GND	GND	GND	GND	M12	GND
N/A	GND	GND	GND	GND	GND	M13	GND
N/A	GND	GND	GND	GND	GND	M14	GND
N/A	GND	GND	GND	GND	GND	M15	GND
N/A	GND	GND	GND	GND	GND	M16	GND
N/A	GND	GND	GND	GND	GND	M17	GND
N/A	GND	GND	GND	GND	GND	M23	GND
N/A	GND	GND	GND	GND	GND	N11	GND
N/A	GND	GND	GND	GND	GND	N12	GND
N/A	GND	GND	GND	GND	GND	N13	GND
N/A	GND	GND	GND	GND	GND	N14	GND
N/A	GND	GND	GND	GND	GND	N15	GND
N/A	GND	GND	GND	GND	GND	N16	GND
N/A	GND	GND	GND	GND	GND	P11	GND
N/A	GND	GND	GND	GND	GND	P12	GND
N/A	GND	GND	GND	GND	GND	P13	GND
N/A	GND	GND	GND	GND	GND	P14	GND
N/A	GND	GND	GND	GND	GND	P15	GND
N/A	GND	GND	GND	GND	GND	P16	GND
N/A	GND	GND	GND	GND	GND	R4	GND
N/A	GND	GND	GND	GND	GND	R10	GND
N/A	GND	GND	GND	GND	GND	R11	GND
N/A	GND	GND	GND	GND	GND	R12	GND
N/A	GND	GND	GND	GND	GND	R13	GND
N/A	GND	GND	GND	GND	GND	R14	GND
N/A	GND	GND	GND	GND	GND	R15	GND

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
0	IO_L23P_0	IO_L23P_0	J15	I/O
0	IO_L24N_0	IO_L24N_0	G15	I/O
0	IO_L24P_0	IO_L24P_0	F15	I/O
0	IO_L25N_0	IO_L25N_0	D15	I/O
0	IO_L25P_0	IO_L25P_0	C15	I/O
0	IO_L26N_0	IO_L26N_0	B15	I/O
0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	A15	VREF
0	IO_L27N_0	IO_L27N_0	G16	I/O
0	IO_L27P_0	IO_L27P_0	F16	I/O
0	IO_L28N_0	IO_L28N_0	C16	I/O
0	IO_L28P_0	IO_L28P_0	B16	I/O
0	IO_L29N_0	IO_L29N_0	J17	I/O
0	IO_L29P_0	IO_L29P_0	H17	I/O
0	IO_L30N_0	IO_L30N_0	G17	I/O
0	IO_L30P_0	IO_L30P_0	F17	I/O
0	IO_L31N_0	IO_L31N_0	D17	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C17	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B17	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A17	GCLK
0	N.C. (◆)	IO_L33N_0	D7	I/O
0	N.C. (◆)	IO_L33P_0	C7	I/O
0	N.C. (◆)	IO_L34N_0	B7	I/O
0	N.C. (◆)	IO_L34P_0	A7	I/O
0	IO_L35N_0	IO_L35N_0	E8	I/O
0	IO_L35P_0	IO_L35P_0	D8	I/O
0	IO_L36N_0	IO_L36N_0	B8	I/O
0	IO_L36P_0	IO_L36P_0	A8	I/O
0	IO_L37N_0	IO_L37N_0	D10	I/O
0	IO_L37P_0	IO_L37P_0	C10	I/O
0	IO_L38N_0	IO_L38N_0	B10	I/O
0	IO_L38P_0	IO_L38P_0	A10	I/O
0	N.C. (◆)	IO_L39N_0	G11	I/O
0	N.C. (◆)	IO_L39P_0	F11	I/O
0	N.C. (◆)	IO_L40N_0	B11	I/O
0	N.C. (◆)	IO_L40P_0	A11	I/O
0	VCCO_0	VCCO_0	B13	VCCO
0	VCCO_0	VCCO_0	C4	VCCO
0	VCCO_0	VCCO_0	C8	VCCO
0	VCCO_0	VCCO_0	D11	VCCO
0	VCCO_0	VCCO_0	D16	VCCO