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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	480
Number of Logic Elements/Cells	4320
Total RAM Bits	221184
Number of I/O	173
Number of Gates	200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s200-5ft256c

Spartan-3 FPGA Design Documentation

The functionality of the Spartan®-3 FPGA family is described in the following documents. The topics covered in each guide are listed.

- UG331: *Spartan-3 Generation FPGA User Guide*
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Software Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
- UG332: *Spartan-3 Generation Configuration User Guide*
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx Platform Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples

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For specific hardware examples, see the Spartan-3 FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- Spartan-3 FPGA Starter Kit Board page
  http://www.xilinx.com/s3starter
- UG130: *Spartan-3 FPGA Starter Kit User Guide*

Table 10: **DCI I/O Standards**

Category of Signal Standard	Signal Standard (IOSTANDARD)	V_{CCO} (V)		V_{REF} for Inputs (V)	Termination Type	
		For Outputs	For Inputs		At Output	At Input
Single-Ended						
Gunning Transceiver Logic	GTL_DCI	1.2	1.2	0.8	Single	Single
	GTLP_DCI	1.5	1.5	1.0		
High-Speed Transceiver Logic	HSTL_I_DCI	1.5	1.5	0.75	None	Split
	HSTL_III_DCI	1.5	1.5	0.9	None	Single
	HSTL_I_DCI_18	1.8	1.8	0.9	None	Split
	HSTL_II_DCI_18 DIFF_HSTL_II_18_DCI	1.8	1.8	0.9	Split	
	HSTL_III_DCI_18	1.8	1.8	1.1	None	Single
Low-Voltage CMOS	LVDCI_15	1.5	1.5	–	Controlled impedance driver	None
	LVDCI_18	1.8	1.8	–		
	LVDCI_25	2.5	2.5	–		
	LVDCI_33(2)	3.3	3.3	–		
	LVDCI_DV2_15	1.5	1.5	–	Controlled driver with half-impedance	
	LVDCI_DV2_18	1.8	1.8	–		
	LVDCI_DV2_25	2.5	2.5	–		
	LVDCI_DV2_33	3.3	3.3	–		
Hybrid HSTL Input and LVCMOS Output	HSLVDCI_15	1.5	1.5	0.75	Controlled impedance driver	None
	HSLVDCI_18	1.8	1.8	0.9		
	HSLVDCI_25	2.5	2.5	1.25		
	HSLVDCI_33	3.3	3.3	1.65		
Stub Series Terminated Logic(3)	SSTL18_I_DCI	1.8	1.8	0.9	25Ω driver	Split
	SSTL2_I_DCI	2.5	2.5	1.25	25Ω driver	
	SSTL2_II_DCI DIFF_SSTL2_II_DCI	2.5	2.5	1.25	Split with 25Ω driver	
Differential						
Low-Voltage Differential Signaling	LVDS_25_DCI	N/A	2.5	–	None	Split on each line of pair
	LVDSEXT_25_DCI	N/A	2.5	–		

Notes:

1. DCI signal standards are not supported in Bank 5 of any Spartan-3 FPGA packaged in a VQ100, CP132, or TQ144 package.
2. Equivalent to LVTTL DCI.
3. The SSTL18_II signal standard does not have a DCI equivalent.

Table 36: **DC Characteristics of User I/Os Using Single-Ended Standards**

Signal Standard (IOSTANDARD) and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
GTL		32	–	0.4	–
GTL_DCI		Note 3	Note 3		
GTLP		36	–	0.6	–
GTLP_DCI		Note 3	Note 3		
HSLVDCI_15		Note 3	Note 3	0.4	V_{CCO} – 0.4
HSLVDCI_18					
HSLVDCI_25					
HSLVDCI_33					
HSTL_I		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI		Note 3	Note 3		
HSTL_III		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI		Note 3	Note 3		
HSTL_I_18		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI_18		Note 3	Note 3		
HSTL_II_18		16	–16	0.4	V_{CCO} – 0.4
HSTL_II_DCI_18		Note 3	Note 3		
HSTL_III_18		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI_18		Note 3	Note 3		
LVCMOS12(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
LVCMOS15(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
LVDCI_15, LVDCI_DV2_15		Note 3	Note 3		
LVCMOS18(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
LVDCI_18, LVDCI_DV2_18		Note 3	Note 3		
LVCMOS25(4,5)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_25, LVDCI_DV2_25		Note 3	Note 3		

Simultaneously Switching Output Guidelines

This section provides guidelines for the maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins, of a given output signal standard, that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 49 and Table 50 provide the essential SSO guidelines. For each device/package combination, Table 49 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and will possibly not match the physical number of pairs. For each output signal standard and drive strength, Table 50 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The Table 50 guidelines are categorized by package style. Multiply the appropriate numbers from Table 49 and Table 50 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines may result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 49 x Table 50

The recommended maximum SSO values assume that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The number of SSOs allowed for quad-flat packages (VQ, TQ, PQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 49: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	VQ100	CP132 (1)(2)	TQ144 (1)	PQ208	FT256	FG320	FG456	FG676	FG900	FG1156 (2)
XC3S50	1	1.5	1.5	2	–	–	–	–	–	–
XC3S200	1	–	1.5	2	3	–	–	–	–	–
XC3S400	–	–	1.5	2	3	3	5	–	–	–
XC3S1000	–	–	–	–	3	3	5	5	–	–
XC3S1500	–	–	–	–	–	3	5	6	–	–
XC3S2000	–	–	–	–	–	–	5	6	9	–
XC3S4000	–	–	–	–	–	–	–	6	10	12
XC3S5000	–	–	–	–	–	–	–	6	10	12

Notes:

1. The V_{CCO} lines for the pair of banks on each side of the CP132 and TQ144 packages are internally tied together. Each pair of interconnected banks shares three V_{CCO}/GND pairs. Consequently, the per bank number is 1.5.
2. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.
3. The information in this table also applies to Pb-free packages.

Table 59: **Switching Characteristics for the DLL**

Symbol	Description	Frequency Mode / FCLKIN Range	Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_1X_LF	Frequency for the CLK0, CLK90, CLK180, and CLK270 outputs	Low	All	18	167	18	167	MHz
CLKOUT_FREQ_1X_HF	Frequency for the CLK0 and CLK180 outputs	High		48	280	48	280	MHz
CLKOUT_FREQ_2X_LF(3)	Frequency for the CLK2X and CLK2X180 outputs	Low		36	334	36	334	MHz
CLKOUT_FREQ_DV_LF	Frequency for the CLKDV output	Low		1.125	110	1.125	110	MHz
CLKOUT_FREQ_DV_HF		High		3	185	3	185	MHz
Output Clock Jitter(4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output	All	All	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			–	±200	–	±200	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			–	±300	–	±300	ps
Duty Cycle								
CLKOUT_DUTY_CYCLE_DLL(5)	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs	All	XC3S50	–	±150	–	±150	ps
			XC3S200	–	±150	–	±150	ps
			XC3S400	–	±250	–	±250	ps
			XC3S1000	–	±400	–	±400	ps
			XC3S1500	–	±400	–	±400	ps
			XC3S2000	–	±400	–	±400	ps
			XC3S4000	–	±400	–	±400	ps
			XC3S5000	–	±400	–	±400	ps
Phase Alignment								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs	All	All	–	±150	–	±150	ps
CLKOUT_PHASE	Phase offset between any two DLL outputs (except CLK2X and CLK0)			–	±140	–	±140	ps
	Phase offset between the CLK2X and CLK0 outputs			–	±250	–	±250	ps

Table 59: **Switching Characteristics for the DLL *(Cont'd)***

Symbol	Description	Frequency Mode / FCLKIN Range	Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Lock Time								
LOCK_DLL	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	18 MHz ≤ F_{CLKIN} ≤ 30 MHz	All	–	2.88	–	2.88	ms
		30 MHz < F_{CLKIN} ≤ 40 MHz		–	2.16	–	2.16	ms
		40 MHz < F_{CLKIN} ≤ 50 MHz		–	1.20	–	1.20	ms
		50 MHz < F_{CLKIN} ≤ 60 MHz		–	0.60	–	0.60	ms
		F_{CLKIN} > 60 MHz		–	0.48	–	0.48	ms
Delay Lines								
DCM_TAP	Delay tap resolution	All	All	30.0	60.0	30.0	60.0	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32 and Table 58.
2. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
3. Only mask revision 'E' and later devices (see Mask and Fab Revisions, page 58) and all revisions of the XC3S50 and the XC3S1000 support DLL feedback using the CLK2X output. For all other Spartan-3 devices, use feedback from the CLK0 output (instead of the CLK2X output) and set the CLK_FEEDBACK attribute to 1X.
4. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
5. This specification only applies if the attribute DUTY_CYCLE_CORRECTION = TRUE.

Digital Frequency Synthesizer (DFS)

Table 60: **Recommended Operating Conditions for the DFS**

Symbol		Description	Frequency Mode	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input	All	1	280	1	280	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input	Low	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF			High	–	±150	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input	All	–	±1	–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 58.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.

Table 70: **Spartan-3 FPGA Pin Definitions *(Cont'd)***

Pin Name	Direction	Description
TDI	Input	**JTAG Test Data Input:** TDI is the serial data input for all JTAG instruction and data registers. This pin has an internal pull-up resistor to VCCAUX during configuration.
TMS	Input	**JTAG Test Mode Select:** The serial TMS input controls the operation of the JTAG port. This pin has an internal pull-up resistor to VCCAUX during configuration.
TDO	Output	**JTAG Test Data Output:** TDO is the serial data output for all JTAG instruction and data registers. This pin has an internal pull-up resistor to VCCAUX during configuration.
VCCO: I/O bank output voltage supply pins		
VCCO_#	Supply	**Power Supply for Output Buffer Drivers (per bank):** These pins power the output drivers within a specific I/O bank.
VCCAUX: Auxiliary voltage supply pins		
VCCAUX	Supply	**Power Supply for Auxiliary Circuits:** +2.5V power pins for auxiliary circuits, including the Digital Clock Managers (DCMs), the dedicated configuration pins (CONFIG), and the dedicated JTAG pins. All VCCAUX pins must be connected.
VCCINT: Internal core voltage supply pins		
VCCINT	Supply	**Power Supply for Internal Core Logic:** +1.2V power pins for the internal logic. All pins must be connected.
GND: Ground supply pins		
GND	Supply	**Ground:** Ground pins, which are connected to the power supply's return path. All pins must be connected.
N.C.: Unconnected package pins		
N.C.		**Unconnected Package Pin:** These package pins are unconnected.

Notes:

1. All unused inputs and bidirectional pins must be tied either High or Low. For unused enable inputs, apply the level that disables the associated function. One common approach is to activate internal pull-up or pull-down resistors. An alternative approach is to externally connect the pin to either VCCO or GND.
2. All outputs are of the totem-pole type — i.e., they can drive High as well as Low logic levels — except for the cases where "Open Drain" is indicated. The latter can only drive a Low logic level and require a pull-up resistor to produce a High logic level.

Detailed, Functional Pin Descriptions

I/O Type: Unrestricted, General-purpose I/O Pins

After configuration, I/O-type pins are inputs, outputs, bidirectional I/O, three-state outputs, open-drain outputs, or open-source outputs, as defined in the application

Pins labeled "IO" support all SelectIO™ interface signal standards except differential standards. A given device at most only has a few of these pins.

A majority of the general-purpose I/O pins are labeled in the format "IO_Lxxy_#". These pins support all SelectIO signal standards, including the differential standards such as LVDS, ULVDS, BLVDS, RSDS, or LDT.

For additional information, see IOBs, page 10

Table 80: **Bitstream Options Affecting Spartan-3 Device Pins *(Cont'd)***

Affected Pin Name(s)	Bitstream Generation Function	Option Variable Name	Values (Default)
CCLK	After configuration, this bitstream option either pulls CCLK to VCCAUX via a pull-up resistor, or allows CCLK to float.	CclkPin	• **Pullup** • Pullnone
CCLK	For Master configuration modes, this option sets the approximate frequency, in MHz, for the internal silicon oscillator.	ConfigRate	• 3, **6**, 12, 25, 50
PROG_B	A pull-up resistor to VCCAUX exists on PROG_B during configuration. After configuration, this bitstream option either pulls PROG_B to VCCAUX via a pull-up resistor, or allows PROG_B to float.	ProgPin	• **Pullup** • Pullnone
DONE	After configuration, this bitstream option either pulls DONE to VCCAUX via a pull-up resistor, or allows DONE to float. See also DriveDone option.	DonePin	• **Pullup** • Pullnone
DONE	If set to Yes, this option allows the FPGA's DONE pin to drive High when configuration completes. By default, the DONE is an open-drain output and can only drive Low. Only single FPGAs and the last FPGA in a multi-FPGA daisy-chain should use this option.	DriveDone	• **No** • Yes
M2	After configuration, this bitstream option either pulls M2 to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows M2 to float.	M2Pin	• **Pullup** • Pulldown • Pullnone
M1	After configuration, this bitstream option either pulls M1 to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows M1 to float.	M1Pin	• **Pullup** • Pulldown • Pullnone
M0	After configuration, this bitstream option either pulls M0 to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows M0 to float.	M0Pin	• **Pullup** • Pulldown • Pullnone
HSWAP_EN	After configuration, this bitstream option either pulls HSWAP_EN to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows HSWAP_EN to float.	HswapenPin	• **Pullup** • Pulldown • Pullnone
TDI	After configuration, this bitstream option either pulls TDI to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows TDI to float.	TdiPin	• **Pullup** • Pulldown • Pullnone
TMS	After configuration, this bitstream option either pulls TMS to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows TMS to float.	TmsPin	• **Pullup** • Pulldown • Pullnone
TCK	After configuration, this bitstream option either pulls TCK to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows TCK to float.	TckPin	• **Pullup** • Pulldown • Pullnone
TDO	After configuration, this bitstream option either pulls TDO to VCCAUX via a pull-up resistor, to ground via a pull-down resistor, or allows TDO to float.	TdoPin	• **Pullup** • Pulldown • Pullnone

Setting Bitstream Generator Options

Refer to the "BitGen" chapter in the Xilinx ISE® software documentation.

Table 87: **VQ100 Package Pinout *(Cont'd)***

Bank	XC3S50 XC3S200 Pin Name	VQ100 Pin Number	Type
6	IO_L40P_6/VREF_6	P13	VREF
6	VCCO_6	P19	VCCO
7	IO_L01N_7/VRP_7	P2	DCI
7	IO_L01P_7/VRN_7	P1	DCI
7	IO_L21N_7	P5	I/O
7	IO_L21P_7	P4	I/O
7	IO_L23N_7	P9	I/O
7	IO_L23P_7	P8	I/O
7	IO_L40N_7/VREF_7	P12	VREF
7	IO_L40P_7	P11	I/O
7	VCCO_7	P6	VCCO
N/A	GND	P3	GND
N/A	GND	P10	GND
N/A	GND	P20	GND
N/A	GND	P29	GND
N/A	GND	P41	GND
N/A	GND	P56	GND
N/A	GND	P66	GND
N/A	GND	P73	GND
N/A	GND	P82	GND
N/A	GND	P95	GND
N/A	VCCAUX	P7	VCCAUX
N/A	VCCAUX	P33	VCCAUX
N/A	VCCAUX	P58	VCCAUX
N/A	VCCAUX	P84	VCCAUX
N/A	VCCINT	P18	VCCINT
N/A	VCCINT	P45	VCCINT
N/A	VCCINT	P69	VCCINT
N/A	VCCINT	P93	VCCINT
VCCAUX	CCLK	P52	CONFIG
VCCAUX	DONE	P51	CONFIG
VCCAUX	HSWAP_EN	P98	CONFIG
VCCAUX	M0	P25	CONFIG
VCCAUX	M1	P24	CONFIG
VCCAUX	M2	P26	CONFIG
VCCAUX	PROG_B	P99	CONFIG
VCCAUX	TCK	P77	JTAG
VCCAUX	TDI	P100	JTAG

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
2	IO_L20N_2	E17	I/O
2	IO_L20P_2	E18	I/O
2	IO_L21N_2	F15	I/O
2	IO_L21P_2	E15	I/O
2	IO_L22N_2	F14	I/O
2	IO_L22P_2	G14	I/O
2	IO_L23N_2/VREF_2	G18	VREF
2	IO_L23P_2	F17	I/O
2	IO_L24N_2	G15	I/O
2	IO_L24P_2	G16	I/O
2	IO_L27N_2	H13	I/O
2	IO_L27P_2	H14	I/O
2	IO_L34N_2/VREF_2	H16	VREF
2	IO_L34P_2	H15	I/O
2	IO_L35N_2	H17	I/O
2	IO_L35P_2	H18	I/O
2	IO_L39N_2	J18	I/O
2	IO_L39P_2	J17	I/O
2	IO_L40N_2	J15	I/O
2	IO_L40P_2/VREF_2	J14	VREF
2	VCCO_2	F16	VCCO
2	VCCO_2	H12	VCCO
2	VCCO_2	J12	VCCO
3	IO	K15	I/O
3	IO_L01N_3/VRP_3	T17	DCI
3	IO_L01P_3/VRN_3	T16	DCI
3	IO_L16N_3	T18	I/O
3	IO_L16P_3	U18	I/O
3	IO_L17N_3	P16	I/O
3	IO_L17P_3/VREF_3	R16	VREF
3	IO_L19N_3	R17	I/O
3	IO_L19P_3	R18	I/O
3	IO_L20N_3	P18	I/O
3	IO_L20P_3	P17	I/O
3	IO_L21N_3	P15	I/O
3	IO_L21P_3	N15	I/O
3	IO_L22N_3	M14	I/O
3	IO_L22P_3	N14	I/O
3	IO_L23N_3	M15	I/O
3	IO_L23P_3/VREF_3	M16	VREF

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
3	VCCO_3	VCCO_3	N16	VCCO
3	VCCO_3	VCCO_3	P16	VCCO
3	VCCO_3	VCCO_3	R17	VCCO
3	VCCO_3	VCCO_3	R20	VCCO
4	IO	IO	U16	I/O
4	IO	IO	U17	I/O
4	IO	IO	W13	I/O
4	IO	IO	W14	I/O
4	IO/VREF_4	IO/VREF_4	AB13	VREF
4	IO/VREF_4	IO/VREF_4	V18	VREF
4	IO/VREF_4	IO/VREF_4	Y16	VREF
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	AA20	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	AB20	DCI
4	N.C. (◆)	IO_L05N_4	AA19	I/O
4	N.C. (◆)	IO_L05P_4	AB19	I/O
4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	W18	VREF
4	IO_L06P_4	IO_L06P_4	Y18	I/O
4	IO_L09N_4	IO_L09N_4	AA18	I/O
4	IO_L09P_4	IO_L09P_4	AB18	I/O
4	IO_L10N_4	IO_L10N_4	V17	I/O
4	IO_L10P_4	IO_L10P_4	W17	I/O
4	IO_L15N_4	IO_L15N_4	Y17	I/O
4	IO_L15P_4	IO_L15P_4	AA17	I/O
4	IO_L16N_4	IO_L16N_4	V16	I/O
4	IO_L16P_4	IO_L16P_4	W16	I/O
4	N.C. (◆)	IO_L19N_4	AA16	I/O
4	N.C. (◆)	IO_L19P_4	AB16	I/O
4	N.C. (◆)	IO_L22N_4/ VREF_4	V15	VREF
4	N.C. (◆)	IO_L22P_4	W15	I/O
4	IO_L24N_4	IO_L24N_4	AA15	I/O
4	IO_L24P_4	IO_L24P_4	AB15	I/O
4	IO_L25N_4	IO_L25N_4	U14	I/O
4	IO_L25P_4	IO_L25P_4	V14	I/O
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	AA14	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	AB14	DUAL
4	IO_L28N_4	IO_L28N_4	U13	I/O
4	IO_L28P_4	IO_L28P_4	V13	I/O
4	IO_L29N_4	IO_L29N_4	Y13	I/O
4	IO_L29P_4	IO_L29P_4	AA13	I/O

User I/Os by Bank

Table 101 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S400 in the FG456 package. Similarly, Table 102 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1000, XC3S1500, and XC3S2000 in the FG456 package.

Table 101: **User I/Os Per Bank for XC3S400 in FG456 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	35	27	0	2	4	2
	1	35	27	0	2	4	2
Right	2	31	25	0	2	4	0
	3	31	25	0	2	4	0
Bottom	4	35	21	6	2	4	2
	5	35	21	6	2	4	2
Left	6	31	25	0	2	4	0
	7	31	25	0	2	4	0

Table 102: **User I/Os Per Bank for XC3S1000, XC3S1500, and XC3S2000 in FG456 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	40	31	0	2	5	2
	1	40	31	0	2	5	2
Right	2	43	37	0	2	4	0
	3	43	37	0	2	4	0
Bottom	4	41	26	6	2	5	2
	5	40	25	6	2	5	2
Left	6	43	37	0	2	4	0
	7	43	37	0	2	4	0

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
1	N.C. (◆)	IO_L18P_1	IO_L18P_1	IO_L18P_1	IO[3]	C18	I/O
1	IO_L19N_1	IO_L19N_1	IO_L19N_1	IO_L19N_1	IO_L19N_1	F17	I/O
1	IO_L19P_1	IO_L19P_1	IO_L19P_1	IO_L19P_1	IO_L19P_1	G17	I/O
1	IO_L22N_1	IO_L22N_1	IO_L22N_1	IO_L22N_1	IO_L22N_1	D17	I/O
1	IO_L22P_1	IO_L22P_1	IO_L22P_1	IO_L22P_1	IO_L22P_1	E17	I/O
1	N.C. (◆)	IO_L23N_1	IO_L23N_1	IO_L23N_1	IO_L23N_1	A17	I/O
1	N.C. (◆)	IO_L23P_1	IO_L23P_1	IO_L23P_1	IO_L23P_1	B17	I/O
1	IO_L24N_1	IO_L24N_1	IO_L24N_1	IO_L24N_1	IO_L24N_1	G16	I/O
1	IO_L24P_1	IO_L24P_1	IO_L24P_1	IO_L24P_1	IO_L24P_1	H16	I/O
1	IO_L25N_1	IO_L25N_1	IO_L25N_1	IO_L25N_1	IO_L25N_1	E16	I/O
1	IO_L25P_1	IO_L25P_1	IO_L25P_1	IO_L25P_1	IO_L25P_1	F16	I/O
1	N.C. (◆)	IO_L26N_1	IO_L26N_1	IO_L26N_1	IO_L26N_1	A16	I/O
1	N.C. (◆)	IO_L26P_1	IO_L26P_1	IO_L26P_1	IO_L26P_1	B16	I/O
1	IO_L27N_1	IO_L27N_1	IO_L27N_1	IO_L27N_1	IO_L27N_1	G15	I/O
1	IO_L27P_1	IO_L27P_1	IO_L27P_1	IO_L27P_1	IO_L27P_1	H15	I/O
1	IO_L28N_1	IO_L28N_1	IO_L28N_1	IO_L28N_1	IO_L28N_1	E15	I/O
1	IO_L28P_1	IO_L28P_1	IO_L28P_1	IO_L28P_1	IO_L28P_1	F15	I/O
1	IO_L29N_1	IO_L29N_1	IO_L29N_1	IO_L29N_1	IO_L29N_1	A15	I/O
1	IO_L29P_1	IO_L29P_1	IO_L29P_1	IO_L29P_1	IO_L29P_1	B15	I/O
1	IO_L30N_1	IO_L30N_1	IO_L30N_1	IO_L30N_1	IO_L30N_1	G14	I/O
1	IO_L30P_1	IO_L30P_1	IO_L30P_1	IO_L30P_1	IO_L30P_1	H14	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D14	VREF
1	IO_L31P_1	IO_L31P_1	IO_L31P_1	IO_L31P_1	IO_L31P_1	E14	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B14	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C14	GCLK
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	C16	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	C20	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	H17	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	H18	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J14	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J15	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J16	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	K14	VCCO
2	N.C. (◆)	N.C. (■)	IO	IO	IO	F22	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C25	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C26	DCI
2	IO_L02N_2	IO_L02N_2	IO_L02N_2	IO_L02N_2	IO_L02N_2	E23	I/O
2	IO_L02P_2	IO_L02P_2	IO_L02P_2	IO_L02P_2	IO_L02P_2	E24	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2[1]	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	D25	VREF[1]
2	IO_L03P_2	IO_L03P_2	IO_L03P_2	IO_L03P_2	IO_L03P_2	D26	I/O
2	N.C. (◆)	IO_L05N_2	IO_L05N_2	IO_L05N_2	IO_L05N_2	E25	I/O
2	N.C. (◆)	IO_L05P_2	IO_L05P_2	IO_L05P_2	IO_L05P_2	E26	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO_L10N_0	IO_L10N_0	J9	I/O
0	IO_L10P_0	IO_L10P_0	H9	I/O
0	IO_L11N_0	IO_L11N_0	G10	I/O
0	IO_L11P_0	IO_L11P_0	F10	I/O
0	IO_L12N_0	IO_L12N_0	C10	I/O
0	IO_L12P_0	IO_L12P_0	B10	I/O
0	IO_L13N_0	IO_L13N_0	J10	I/O
0	IO_L13P_0	IO_L13P_0	K11	I/O
0	IO_L14N_0	IO_L14N_0	H11	I/O
0	IO_L14P_0	IO_L14P_0	G11	I/O
0	IO_L15N_0	IO_L15N_0	F11	I/O
0	IO_L15P_0	IO_L15P_0	E11	I/O
0	IO_L16N_0	IO_L16N_0	D11	I/O
0	IO_L16P_0	IO_L16P_0	C11	I/O
0	IO_L17N_0	IO_L17N_0	B11	I/O
0	IO_L17P_0	IO_L17P_0	A11	I/O
0	IO_L18N_0	IO_L18N_0	K12	I/O
0	IO_L18P_0	IO_L18P_0	J12	I/O
0	IO_L19N_0	IO_L19N_0	H12	I/O
0	IO_L19P_0	IO_L19P_0	G12	I/O
0	IO_L20N_0	IO_L20N_0	F12	I/O
0	IO_L20P_0	IO_L20P_0	E12	I/O
0	IO_L21N_0	IO_L21N_0	D12	I/O
0	IO_L21P_0	IO_L21P_0	C12	I/O
0	IO_L22N_0	IO_L22N_0	B12	I/O
0	IO_L22P_0	IO_L22P_0	A12	I/O
0	IO_L23N_0	IO_L23N_0	J13	I/O
0	IO_L23P_0	IO_L23P_0	H13	I/O
0	IO_L24N_0	IO_L24N_0	F13	I/O
0	IO_L24P_0	IO_L24P_0	E13	I/O
0	IO_L25N_0	IO_L25N_0	B13	I/O
0	IO_L25P_0	IO_L25P_0	A13	I/O
0	IO_L26N_0	IO_L26N_0	K14	I/O
0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	J14	VREF
0	IO_L27N_0	IO_L27N_0	G14	I/O
0	IO_L27P_0	IO_L27P_0	F14	I/O
0	IO_L28N_0	IO_L28N_0	C14	I/O
0	IO_L28P_0	IO_L28P_0	B14	I/O
0	IO_L29N_0	IO_L29N_0	J15	I/O
0	IO_L29P_0	IO_L29P_0	H15	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
4	IO_L11P_4	IO_L11P_4	AE21	I/O
4	IO_L12N_4	IO_L12N_4	AH21	I/O
4	IO_L12P_4	IO_L12P_4	AJ21	I/O
4	IO_L13N_4	IO_L13N_4	AB21	I/O
4	IO_L13P_4	IO_L13P_4	AA20	I/O
4	IO_L14N_4	IO_L14N_4	AC20	I/O
4	IO_L14P_4	IO_L14P_4	AD20	I/O
4	IO_L15N_4	IO_L15N_4	AE20	I/O
4	IO_L15P_4	IO_L15P_4	AF20	I/O
4	IO_L16N_4	IO_L16N_4	AG20	I/O
4	IO_L16P_4	IO_L16P_4	AH20	I/O
4	IO_L17N_4	IO_L17N_4	AJ20	I/O
4	IO_L17P_4	IO_L17P_4	AK20	I/O
4	IO_L18N_4	IO_L18N_4	AA19	I/O
4	IO_L18P_4	IO_L18P_4	AB19	I/O
4	IO_L19N_4	IO_L19N_4	AC19	I/O
4	IO_L19P_4	IO_L19P_4	AD19	I/O
4	IO_L20N_4	IO_L20N_4	AE19	I/O
4	IO_L20P_4	IO_L20P_4	AF19	I/O
4	IO_L21N_4	IO_L21N_4	AG19	I/O
4	IO_L21P_4	IO_L21P_4	AH19	I/O
4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	AJ19	VREF
4	IO_L22P_4	IO_L22P_4	AK19	I/O
4	IO_L23N_4	IO_L23N_4	AB18	I/O
4	IO_L23P_4	IO_L23P_4	AC18	I/O
4	IO_L24N_4	IO_L24N_4	AE18	I/O
4	IO_L24P_4	IO_L24P_4	AF18	I/O
4	IO_L25N_4	IO_L25N_4	AJ18	I/O
4	IO_L25P_4	IO_L25P_4	AK18	I/O
4	IO_L26N_4	IO_L26N_4	AA17	I/O
4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	AB17	VREF
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	AD17	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	AE17	DUAL
4	IO_L28N_4	IO_L28N_4	AH17	I/O
4	IO_L28P_4	IO_L28P_4	AJ17	I/O
4	IO_L29N_4	IO_L29N_4	AB16	I/O
4	IO_L29P_4	IO_L29P_4	AC16	I/O
4	IO_L30N_4/D2	IO_L30N_4/D2	AD16	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	AE16	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	AG16	DUAL

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
6	IO_L28P_6	IO_L28P_6	W1	I/O
6	IO_L29N_6	IO_L29N_6	W10	I/O
6	IO_L29P_6	IO_L29P_6	V10	I/O
6	N.C. (◆)	IO_L30N_6	V9	I/O
6	N.C. (◆)	IO_L30P_6	V8	I/O
6	IO_L31N_6	IO_L31N_6	W5	I/O
6	IO_L31P_6	IO_L31P_6	V6	I/O
6	IO_L32N_6	IO_L32N_6	V5	I/O
6	IO_L32P_6	IO_L32P_6	V4	I/O
6	IO_L33N_6	IO_L33N_6	V2	I/O
6	IO_L33P_6	IO_L33P_6	V1	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	U10	VREF
6	IO_L34P_6	IO_L34P_6	U9	I/O
6	IO_L35N_6	IO_L35N_6	U7	I/O
6	IO_L35P_6	IO_L35P_6	U6	I/O
6	N.C. (◆)	IO_L36N_6	U3	I/O
6	N.C. (◆)	IO_L36P_6	U2	I/O
6	IO_L37N_6	IO_L37N_6	T10	I/O
6	IO_L37P_6	IO_L37P_6	T9	I/O
6	IO_L38N_6	IO_L38N_6	T6	I/O
6	IO_L38P_6	IO_L38P_6	T5	I/O
6	IO_L39N_6	IO_L39N_6	T4	I/O
6	IO_L39P_6	IO_L39P_6	T3	I/O
6	IO_L40N_6	IO_L40N_6	T2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	T1	VREF
6	N.C. (◆)	IO_L45N_6	Y4	I/O
6	N.C. (◆)	IO_L45P_6	Y3	I/O
6	N.C. (◆)	IO_L52N_6	T8	I/O
6	N.C. (◆)	IO_L52P_6	T7	I/O
6	VCCO_6	VCCO_6	V3	VCCO
6	VCCO_6	VCCO_6	AB3	VCCO
6	VCCO_6	VCCO_6	AF3	VCCO
6	VCCO_6	VCCO_6	AD5	VCCO
6	VCCO_6	VCCO_6	V7	VCCO
6	VCCO_6	VCCO_6	AB7	VCCO
6	VCCO_6	VCCO_6	Y9	VCCO
6	VCCO_6	VCCO_6	U11	VCCO
6	VCCO_6	VCCO_6	V11	VCCO
6	VCCO_6	VCCO_6	W11	VCCO
7	IO	IO	J6	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	C1	DCI
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	C2	DCI
7	IO_L02N_7	IO_L02N_7	D3	I/O
7	IO_L02P_7	IO_L02P_7	D4	I/O
7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	D1	VREF
7	IO_L03P_7	IO_L03P_7	D2	I/O
7	IO_L04N_7	IO_L04N_7	E1	I/O
7	IO_L04P_7	IO_L04P_7	E2	I/O
7	IO_L05N_7	IO_L05N_7	F5	I/O
7	IO_L05P_7	IO_L05P_7	E4	I/O
7	IO_L06N_7	IO_L06N_7	F2	I/O
7	IO_L06P_7	IO_L06P_7	F3	I/O
7	IO_L07N_7	IO_L07N_7	G3	I/O
7	IO_L07P_7	IO_L07P_7	G4	I/O
7	IO_L08N_7	IO_L08N_7	G1	I/O
7	IO_L08P_7	IO_L08P_7	G2	I/O
7	IO_L09N_7	IO_L09N_7	H7	I/O
7	IO_L09P_7	IO_L09P_7	G6	I/O
7	IO_L10N_7	IO_L10N_7	H5	I/O
7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	H6	VREF
7	IO_L11N_7	IO_L11N_7	H3	I/O
7	IO_L11P_7	IO_L11P_7	H4	I/O
7	IO_L13N_7	IO_L13N_7	H1	I/O
7	IO_L13P_7	IO_L13P_7	H2	I/O
7	IO_L14N_7	IO_L14N_7	J4	I/O
7	IO_L14P_7	IO_L14P_7	J5	I/O
7	IO_L15N_7	IO_L15N_7	J1	I/O
7	IO_L15P_7	IO_L15P_7	J2	I/O
7	IO_L16N_7	IO_L16N_7	K9	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	J8	VREF
7	IO_L17N_7	IO_L17N_7	K6	I/O
7	IO_L17P_7	IO_L17P_7	K7	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	K2	VREF
7	IO_L19P_7	IO_L19P_7	K3	I/O
7	IO_L20N_7	IO_L20N_7	L10	I/O
7	IO_L20P_7	IO_L20P_7	K10	I/O
7	IO_L21N_7	IO_L21N_7	L7	I/O
7	IO_L21P_7	IO_L21P_7	L8	I/O
7	IO_L22N_7	IO_L22N_7	L5	I/O
7	IO_L22P_7	IO_L22P_7	L6	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	GND	GND	K30	GND
N/A	GND	GND	P30	GND
N/A	GND	GND	U30	GND
N/A	GND	GND	AA30	GND
N/A	GND	GND	AE30	GND
N/A	GND	GND	AJ30	GND
N/A	GND	GND	AK30	GND
N/A	GND	GND	AK2	GND
N/A	VCCAUX	VCCAUX	F4	VCCAUX
N/A	VCCAUX	VCCAUX	K4	VCCAUX
N/A	VCCAUX	VCCAUX	P4	VCCAUX
N/A	VCCAUX	VCCAUX	U4	VCCAUX
N/A	VCCAUX	VCCAUX	AA4	VCCAUX
N/A	VCCAUX	VCCAUX	AE4	VCCAUX
N/A	VCCAUX	VCCAUX	D6	VCCAUX
N/A	VCCAUX	VCCAUX	AG6	VCCAUX
N/A	VCCAUX	VCCAUX	D10	VCCAUX
N/A	VCCAUX	VCCAUX	AG10	VCCAUX
N/A	VCCAUX	VCCAUX	D14	VCCAUX
N/A	VCCAUX	VCCAUX	AG14	VCCAUX
N/A	VCCAUX	VCCAUX	D17	VCCAUX
N/A	VCCAUX	VCCAUX	AG17	VCCAUX
N/A	VCCAUX	VCCAUX	D21	VCCAUX
N/A	VCCAUX	VCCAUX	AG21	VCCAUX
N/A	VCCAUX	VCCAUX	D25	VCCAUX
N/A	VCCAUX	VCCAUX	AG25	VCCAUX
N/A	VCCAUX	VCCAUX	F27	VCCAUX
N/A	VCCAUX	VCCAUX	K27	VCCAUX
N/A	VCCAUX	VCCAUX	P27	VCCAUX
N/A	VCCAUX	VCCAUX	U27	VCCAUX
N/A	VCCAUX	VCCAUX	AA27	VCCAUX
N/A	VCCAUX	VCCAUX	AE27	VCCAUX
N/A	VCCINT	VCCINT	L11	VCCINT
N/A	VCCINT	VCCINT	R11	VCCINT
N/A	VCCINT	VCCINT	T11	VCCINT
N/A	VCCINT	VCCINT	Y11	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	N12	VCCINT
N/A	VCCINT	VCCINT	P12	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	W12	VCCINT
N/A	VCCINT	VCCINT	M13	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	M14	VCCINT
N/A	VCCINT	VCCINT	W14	VCCINT
N/A	VCCINT	VCCINT	L15	VCCINT
N/A	VCCINT	VCCINT	Y15	VCCINT
N/A	VCCINT	VCCINT	L16	VCCINT
N/A	VCCINT	VCCINT	Y16	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	W17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	W18	VCCINT
N/A	VCCINT	VCCINT	M19	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	P19	VCCINT
N/A	VCCINT	VCCINT	U19	VCCINT
N/A	VCCINT	VCCINT	V19	VCCINT
N/A	VCCINT	VCCINT	W19	VCCINT
N/A	VCCINT	VCCINT	L20	VCCINT
N/A	VCCINT	VCCINT	R20	VCCINT
N/A	VCCINT	VCCINT	T20	VCCINT
N/A	VCCINT	VCCINT	Y20	VCCINT
VCCAUX	CCLK	CCLK	AH28	CONFIG
VCCAUX	DONE	DONE	AJ28	CONFIG
VCCAUX	HSWAP_EN	HSWAP_EN	A3	CONFIG
VCCAUX	M0	M0	AJ3	CONFIG
VCCAUX	M1	M1	AH3	CONFIG
VCCAUX	M2	M2	AK3	CONFIG
VCCAUX	PROG_B	PROG_B	B3	CONFIG
VCCAUX	TCK	TCK	B28	JTAG
VCCAUX	TDI	TDI	C3	JTAG
VCCAUX	TDO	TDO	C28	JTAG
VCCAUX	TMS	TMS	A28	JTAG

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	AN32	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	AP32	DCI
4	IO_L02N_4	IO_L02N_4	AN31	I/O
4	IO_L02P_4	IO_L02P_4	AP31	I/O
4	IO_L03N_4	IO_L03N_4	AM30	I/O
4	IO_L03P_4	IO_L03P_4	AN30	I/O
4	IO_L04N_4	IO_L04N_4	AN27	I/O
4	IO_L04P_4	IO_L04P_4	AP27	I/O
4	IO_L05N_4	IO_L05N_4	AH26	I/O
4	IO_L05P_4	IO_L05P_4	AJ26	I/O
4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	AL26	VREF
4	IO_L06P_4	IO_L06P_4	AM26	I/O
4	IO_L07N_4	IO_L07N_4	AF25	I/O
4	IO_L07P_4	IO_L07P_4	AG25	I/O
4	IO_L08N_4	IO_L08N_4	AH25	I/O
4	IO_L08P_4	IO_L08P_4	AJ25	I/O
4	IO_L09N_4	IO_L09N_4	AL25	I/O
4	IO_L09P_4	IO_L09P_4	AM25	I/O
4	IO_L10N_4	IO_L10N_4	AN25	I/O
4	IO_L10P_4	IO_L10P_4	AP25	I/O
4	IO_L11N_4	IO_L11N_4	AD23	I/O
4	IO_L11P_4	IO_L11P_4	AE23	I/O
4	IO_L12N_4	IO_L12N_4	AF23	I/O
4	IO_L12P_4	IO_L12P_4	AG23	I/O
4	IO_L13N_4	IO_L13N_4	AJ23	I/O
4	IO_L13P_4	IO_L13P_4	AK23	I/O
4	IO_L14N_4	IO_L14N_4	AL23	I/O
4	IO_L14P_4	IO_L14P_4	AM23	I/O
4	IO_L15N_4	IO_L15N_4	AN23	I/O
4	IO_L15P_4	IO_L15P_4	AP23	I/O
4	IO_L16N_4	IO_L16N_4	AG22	I/O
4	IO_L16P_4	IO_L16P_4	AH22	I/O
4	IO_L17N_4	IO_L17N_4	AL22	I/O
4	IO_L17P_4	IO_L17P_4	AM22	I/O
4	IO_L18N_4	IO_L18N_4	AD21	I/O
4	IO_L18P_4	IO_L18P_4	AE21	I/O
4	IO_L19N_4	IO_L19N_4	AG21	I/O
4	IO_L19P_4	IO_L19P_4	AH21	I/O
4	IO_L20N_4	IO_L20N_4	AJ21	I/O
4	IO_L20P_4	IO_L20P_4	AK21	I/O