AMD Xilinx - XC3S200-5FTG256C Datasheet

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Details	
Product Status	Active
Number of LABs/CLBs	480
Number of Logic Elements/Cells	4320
Total RAM Bits	221184
Number of I/O	173
Number of Gates	200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s200-5ftg256c

Spartan-3 FPGA Design Documentation

The functionality of the Spartan®-3 FPGA family is described in the following documents. The topics covered in each guide are listed.

- UG331: *Spartan-3 Generation FPGA User Guide*
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Software Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
- UG332: *Spartan-3 Generation Configuration User Guide*
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx Platform Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples

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For specific hardware examples, see the Spartan-3 FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- Spartan-3 FPGA Starter Kit Board page
  http://www.xilinx.com/s3starter
- UG130: *Spartan-3 FPGA Starter Kit User Guide*

Function Generator

Each of the two LUTs (F and G) in a slice have four logic inputs (A1-A4) and a single output (D). This permits any four-variable Boolean logic operation to be programmed into them. Furthermore, wide function multiplexers can be used to effectively combine LUTs within the same CLB or across different CLBs, making logic functions with still more input variables possible.

The LUTs in both the right-hand and left-hand slice-pairs not only support the logic functions described above, but also can function as ROM that is initialized with data at the time of configuration.

The LUTs in the left-hand slice-pair (even-numbered columns such as X0 in Figure 11) of each CLB support two additional functions that the right-hand slice-pair (odd-numbered columns such as X1) do not.

First, it is possible to program the “left-hand LUTs” as distributed RAM. This type of memory affords moderate amounts of data buffering anywhere along a data path. One left-hand LUT stores 16 bits. Multiple left-hand LUTs can be combined in various ways to store larger amounts of data. A dual port option combines two LUTs so that memory access is possible from two independent data lines. A Distributed ROM option permits pre-loading the memory with data during FPGA configuration.

Second, it is possible to program each left-hand LUT as a 16-bit shift register. Used in this way, each LUT can delay serial data anywhere from one to 16 clock cycles. The four left-hand LUTs of a single CLB can be combined to produce delays up to 64 clock cycles. The SHIFTIN and SHIFTOUT lines cascade LUTs to form larger shift registers. It is also possible to combine shift registers across more than one CLB. The resulting programmable delays can be used to balance the timing of data pipelines.

Block RAM Overview

All Spartan-3 devices support block RAM, which is organized as configurable, synchronous 18Kbit blocks. Block RAM stores relatively large amounts of data more efficiently than the distributed RAM feature described earlier. (The latter is better suited for buffering small amounts of data anywhere along signal paths.) This section describes basic Block RAM functions. For more information, refer to the chapter entitled “Using Block RAM” in UG331.

The aspect ratio—i.e., width vs. depth—of each block RAM is configurable. Furthermore, multiple blocks can be cascaded to create still wider and/or deeper memories.

A choice among primitives determines whether the block RAM functions as dual- or single-port memory. A name of the form RAMB16_S[w_A]_S[w_B] calls out the dual-port primitive, where the integers w_A and w_B specify the total data path width at ports w_A and w_B, respectively. Thus, a RAMB16_S9_S18 is a dual-port RAM with a 9-bit-wide Port A and an 18-bit-wide Port B. A name of the form RAMB16_S[w] identifies the single-port primitive, where the integer w specifies the total data path width of the lone port. A RAMB16_S18 is a single-port RAM with an 18-bit-wide port. Other memory functions—e.g., FIFOs, data path width conversion, ROM, etc.—are readily available using the CORE Generator™ software, part of the Xilinx development software.

The product of w and n yields the total block RAM capacity. Equation 1 and Equation 2 show that as the data bus width increases, the number of address lines along with the number of addressable memory locations decreases. Using the permissible DI/DO bus widths as inputs to these equations provides the bus width and memory capacity measures shown in Table 14.

Table 14: **Port Aspect Ratios for Port A or B**

DI/DO Bus Width (w – p Bits)	DIP/DOP Bus Width (p Bits)	Total Data Path Width (w Bits)	ADDR Bus Width (r Bits)	No. of Addressable Locations (n)	Block RAM Capacity (Bits)
1	0	1	14	16,384	16,384
2	0	2	13	8,192	16,384
4	0	4	12	4,096	16,384
8	1	9	11	2,048	18,432
16	2	18	10	1,024	18,432
32	4	36	9	512	18,432

Block RAM Data Operations

Writing data to and accessing data from the block RAM are synchronous operations that take place independently on each of the two ports.

The waveforms for the write operation are shown in the top half of the Figure 15, Figure 16, and Figure 17. When the WE and EN signals enable the active edge of CLK, data at the DI input bus is written to the block RAM location addressed by the ADDR lines.

There are a number of different conditions under which data can be accessed at the DO outputs. Basic data access always occurs when the WE input is inactive. Under this condition, data stored in the memory location addressed by the ADDR lines passes through a transparent output latch to the DO outputs. The timing for basic data access is shown in the portions of Figure 15, Figure 16, and Figure 17 during which WE is Low.

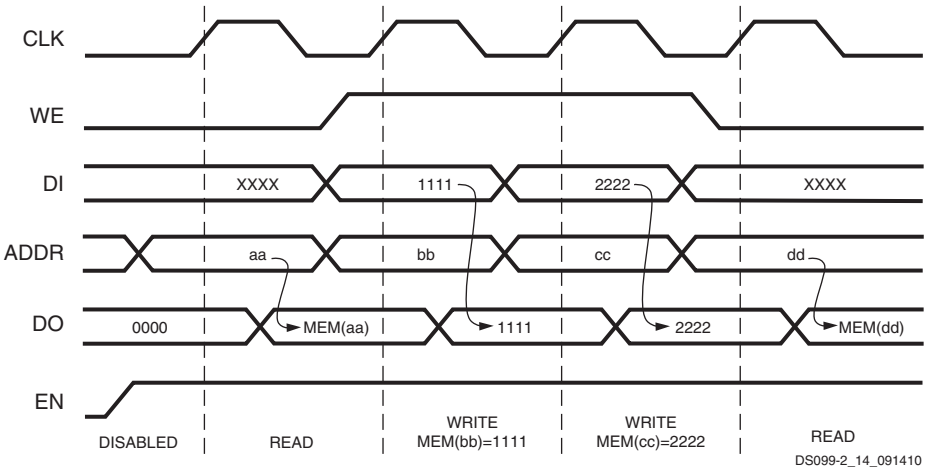

Figure 15: **Waveforms of Block RAM Data Operations with WRITE_FIRST Selected**

Data can also be accessed on the DO outputs when asserting the WE input. This is accomplished using two different attributes:

Choosing the WRITE_FIRST attribute, data is written to the addressed memory location on an enabled active CLK edge and is also passed to the DO outputs. WRITE_FIRST timing is shown in the portion of Figure 15 during which WE is High.

Choosing the READ_FIRST attribute, data already stored in the addressed location pass to the DO outputs before that location is overwritten with new data from the DI inputs on an enabled active CLK edge. READ_FIRST timing is shown in the portion of Figure 16 during which WE is High.

The output frequency (f_{CLKFX}) can be expressed as a function of the incoming clock frequency (f_{CLKIN}) as follows:

$$f_{CLKFX} = f_{CLKIN}(CLKFX\_MULTIPLY/CLKFX\_DIVIDE) \quad \textit{Equation 3}$$

Regarding the two attributes, it is possible to assign any combination of integer values, provided that two conditions are met:

- The two values fall within their corresponding ranges, as specified in Table 18.
- The f_{CLKFX} frequency calculated from the above expression accords with the DCM's operating frequency specifications.

For example, if CLKFX_MULTIPLY = 5 and CLKFX_DIVIDE = 3, then the frequency of the output clock signal would be 5/3 that of the input clock signal.

DFS Frequency Modes

The DFS supports two operating modes, High Frequency and Low Frequency, with each specified over a different clock frequency range. The DFS_FREQUENCY_MODE attribute chooses between the two modes. When the attribute is set to LOW, the Low Frequency mode permits the two DFS outputs to operate over a low-to-moderate frequency range. When the attribute is set to HIGH, the High Frequency mode allows both these outputs to operate at the highest possible frequencies.

DFS With or Without the DLL

The DFS component can be used with or without the DLL component:

Without the DLL, the DFS component multiplies or divides the CLKIN signal frequency according to the respective CLKFX_MULTIPLY and CLKFX_DIVIDE values, generating a clock with the new target frequency on the CLKFX and CLKFX180 outputs. Though classified as belonging to the DLL component, the CLKIN input is shared with the DFS component. This case does not employ feedback loop; therefore, it cannot correct for clock distribution delay.

With the DLL, the DFS operates as described in the preceding case, only with the additional benefit of eliminating the clock distribution delay. In this case, a feedback loop from the CLK0 output to the CLKFB input must be present.

The DLL and DFS components work together to achieve this phase correction as follows: Given values for the CLKFX_MULTIPLY and CLKFX_DIVIDE attributes, the DLL selects the delay element for which the output clock edge coincides with the input clock edge whenever mathematically possible. For example, when CLKFX_MULTIPLY = 5 and CLKFX_DIVIDE = 3, the input and output clock edges will coincide every three input periods, which is equivalent in time to five output periods.

Smaller CLKFX_MULTIPLY and CLKFX_DIVIDE values achieve faster lock times. With no factors common to the two attributes, alignment will occur once with every number of cycles equal to the CLKFX_DIVIDE value. Therefore, it is recommended that the user reduce these values by factoring wherever possible. For example, given CLKFX_MULTIPLY = 9 and CLKFX_DIVIDE = 6, removing a factor of three yields CLKFX_MULTIPLY = 3 and CLKFX_DIVIDE = 2. While both value-pairs will result in the multiplication of clock frequency by 3/2, the latter value-pair will enable the DLL to lock more quickly.

Table 18: **DFS Attributes**

Attribute	Description	Values
DFS_FREQUENCY_MODE	Chooses between High Frequency and Low Frequency modes	Low, High
CLKFX_MULTIPLY	Frequency multiplier constant	Integer from 2 to 32
CLKFX_DIVIDE	Frequency divisor constant	Integer from 1 to 32

Table 19: **DFS Signals**

Signal	Direction	Description
CLKFX	Output	Multiplies the CLKIN frequency by the attribute-value ratio (CLKFX_MULTIPLY/CLKFX_DIVIDE) to generate a clock signal with a new target frequency.
CLKFX180	Output	Generates a clock signal with same frequency as CLKFX, only shifted 180° out-of-phase.

Table 28: **Absolute Maximum Ratings *(Cont'd)***

Symbol	Description	Conditions	Min	Max	Units
I_{IK}	Input clamp current per I/O pin	–0.5 V < V_{IN} < (V_{CCO} + 0.5 V)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage pins relative to GND	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{SOL}	Soldering temperature(4)		–	220	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. All User I/O and Dual-Purpose pins (DIN/D0, D1–D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B) draw power from the V_{CCO} power rail of the associated bank. Keeping VIN within 500 mV of the associated V_{CCO} rails or ground rail ensures that the internal diode junctions that exist between each of these pins and the V_{CCO} and GND rails do not turn on. Table 32 specifies the V_{CCO} range used to determine the max limit. Input voltages outside the –0.5V to V_{CCO}+0.5V voltage range are permissible provided that the I_{IK} input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Prolonged exposure to such current may compromise device reliability. A sustained current of 10 mA will not compromise device reliability. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Generation FPGAs* for more details. The VIN limits apply to both the DC and AC components of signals. Simple application solutions are available that show how to handle overshoot/undershoot as well as achieve PCI compliance. Refer to the following application notes: XAPP457, *Powering and Configuring Spartan-3 Generation FPGAs in Compliant PCI Applications* and XAPP659, *Virtex®-II Pro / Virtex-II Pro X 3.3V I/O Design Guidelines*.
3. All Dedicated pins (M0–M2, CCLK, PROG_B, DONE, HSWAP_EN, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} rail do not turn on. Table 32 specifies the V_{CCAUX} range used to determine the max limit. When V_{CCAUX} is at its maximum recommended operating level (2.625V), V_{IN} max < 3.125V. As long as the V_{IN} max specification is met, oxide stress is not possible. For information concerning the use of 3.3V signals, see the 3.3V-Tolerant Configuration Interface, page 47. See also XAPP459.
4. For soldering guidelines, see UG112, *Device Packaging and Thermal Characteristics* and XAPP427, *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Table 29: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO4T}	Threshold for the V_{CCO} Bank 4 supply	0.4	1.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order. When applying V_{CCINT} power before V_{CCAUX} power, the FPGA may draw a *surplus* current in addition to the quiescent current levels specified in Table 34. Applying V_{CCAUX} eliminates the surplus current. The FPGA does not use any of the surplus current for the power-on process. For this power sequence, make sure that regulators with foldback features will not shut down inadvertently.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 4, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.
3. If a brown-out condition occurs where V_{CCAUX} or V_{CCINT} drops below the retention voltage indicated in Table 31, then V_{CCAUX} or V_{CCINT} must drop below the minimum power-on reset voltage in order to clear out the device configuration content.

Table 35: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

Signal Standard (IOSTANDARD)	V_{CCO}			V_{REF}			V_{IL}	V_{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
GTL[3]	–	–	–	0.74	0.8	0.86	V_{REF} – 0.05	V_{REF} + 0.05
GTL_DCI	–	1.2	–	0.74	0.8	0.86	V_{REF} – 0.05	V_{REF} + 0.05
GTLP[3]	–	–	–	0.88	1	1.12	V_{REF} – 0.1	V_{REF} + 0.1
GTLP_DCI	–	1.5	–	0.88	1	1.12	V_{REF} – 0.1	V_{REF} + 0.1
HSLVDCI_15	1.4	1.5	1.6	–	0.75	–	V_{REF} – 0.1	V_{REF} + 0.1
HSLVDCI_18	1.7	1.8	1.9	–	0.9	–	V_{REF} – 0.1	V_{REF} + 0.1
HSLVDCI_25	2.3	2.5	2.7	–	1.25	–	V_{REF} – 0.1	V_{REF} + 0.1
HSLVDCI_33	3.0	3.3	3.465	–	1.65	–	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_I, HSTL_I_DCI	1.4	1.5	1.6	0.68	0.75	0.9	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_III, HSTL_III_DCI	1.4	1.5	1.6	–	0.9	–	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_I_18, HSTL_I_DCI_18	1.7	1.8	1.9	0.8	0.9	1.1	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_II_18, HSTL_II_DCI_18	1.7	1.8	1.9	–	0.9	–	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_III_18, HSTL_III_DCI_18	1.7	1.8	1.9	–	1.1	–	V_{REF} – 0.1	V_{REF} + 0.1
LVCMOS12	1.14	1.2	1.3	–	–	–	$0.37V_{CCO}$	$0.58V_{CCO}$
LVCMOS15, LVDCI_15, LVDCI_DV2_15	1.4	1.5	1.6	–	–	–	$0.30V_{CCO}$	$0.70V_{CCO}$
LVCMOS18, LVDCI_18, LVDCI_DV2_18	1.7	1.8	1.9	–	–	–	$0.30V_{CCO}$	$0.70V_{CCO}$
LVCMOS25[4,5], LVDCI_25, LVDCI_DV2_25[4]	2.3	2.5	2.7	–	–	–	0.7	1.7
LVCMOS33, LVDCI_33, LVDCI_DV2_33[4]	3.0	3.3	3.465	–	–	–	0.8	2.0
LVTTL	3.0	3.3	3.465	–	–	–	0.8	2.0
PCI33_3[7]	3.0	3.3	3.465	–	–	–	$0.30V_{CCO}$	$0.50V_{CCO}$
SSTL18_I, SSTL18_I_DCI	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} – 0.125	V_{REF} + 0.125
SSTL18_II	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} – 0.125	V_{REF} + 0.125
SSTL2_I, SSTL2_I_DCI	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} – 0.15	V_{REF} + 0.15
SSTL2_II, SSTL2_II_DCI	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} – 0.15	V_{REF} + 0.15

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} – the supply voltage for output drivers as well as LVCMOS, LVTTL, and PCI inputs
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
2. For device operation, the maximum signal voltage (V_{IH} max) may be as high as V_{IN} max. See Table 28.
3. Because the GTL and GTLP standards employ open-drain output buffers, V_{CCO} lines do not supply current to the I/O circuit, rather this current is provided using an external pull-up resistor connected from the I/O pin to a termination voltage (V_{TT}). Nevertheless, the voltage applied to the associated V_{CCO} lines must always be at or above V_{TT} and I/O pad voltages.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS25 or LVCMOS33 standards.
5. All dedicated pins (M0-M2, CCLK, PROG_B, DONE, HSWAP_EN, TCK, TDI, TDO, and TMS) use the LVCMOS standard and draw power from the V_{CCAUX} rail (2.5V). The dual-purpose configuration pins (DIN/D0, D1-D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B) use the LVCMOS standard before the user mode. For these pins, apply 2.5V to the V_{CCO} Bank 4 and V_{CCO} Bank 5 rails at power-on and throughout configuration. For information concerning the use of 3.3V signals, see 3.3V-Tolerant Configuration Interface, page 47.
6. The Global Clock Inputs (GCLK0-GCLK7) are dual-purpose pins to which any signal standard can be assigned.
7. For more information, see XAPP457.

Table 45: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max[3]	Max[3]	
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OTCLK input to data appearing at the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	XC3S200 XC3S400	1.28	1.46	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.94	2.23	ns
T_{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin		XC3S200 XC3S400	1.28	1.47	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.95	2.24	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25[2], 12 mA output drive, Fast slew rate	XC3S200 XC3S400	2.10	2.41	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	2.77	3.18	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) net to setting/resetting data at the Output pin		All	8.07	9.28	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 47.
3. For minimums, use the values reported by the Xilinx timing analyzer.

The 1% precision impedance-matching resistor attached to the VRN_# pin controls the pull-down impedance of NMOS transistor in the input or output buffer. Consequently, the VRN_# pin must connect to VCCO. The 'N' character in "VRN" indicates that this pin controls the I/O buffer's NMOS transistor impedance. The VRN_# pin is only used for split termination.

Each VRN or VRP reference input requires its own resistor. A single resistor cannot be shared between VRN or VRP pins associated with different banks.

During configuration, these pins behave exactly like user-I/O pins. The associated DCI behavior is not active or valid until after configuration completes.

Also see Digitally Controlled Impedance (DCI), page 16.

DCI Termination Types

If the I/O in an I/O bank do not use the DCI feature, then no external resistors are required and both the VRP_# and VRN_# pins are available for user I/O, as shown in section [a] of Figure 42.

If the I/O standards within the associated I/O bank require single termination—such as GTL_DCI, GTLP_DCI, or HSTL_III_DCI—then only the VRP_# signal connects to a 1% precision impedance-matching resistor, as shown in section [b] of Figure 42. A resistor is not required for the VRN_# pin.

Finally, if the I/O standards with the associated I/O bank require split termination—such as HSTL_I_DCI, SSTL2_I_DCI, SSTL2_II_DCI, or LVDS_25_DCI and LVDSEXT_25_DCI receivers—then both the VRP_# and VRN_# pins connect to separate 1% precision impedance-matching resistors, as shown in section [c] of Figure 42. Neither pin is available for user I/O.

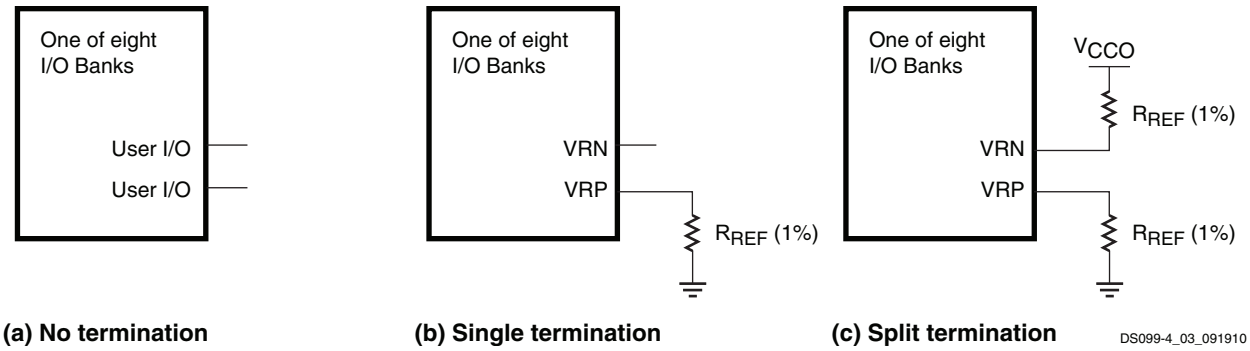

Figure 42: **DCI Termination Types**

GCLK: Global Clock Buffer Inputs or General-Purpose I/O Pins

These pins are user-I/O pins unless they specifically connect to one of the eight low-skew global clock buffers on the device, specified using the IBUFG primitive.

There are eight GCLK pins per device and two each appear in the top-edge banks, Bank 0 and 1, and the bottom-edge banks, Banks 4 and 5. See Figure 40 for a picture of bank labeling.

During configuration, these pins behave exactly like user-I/O pins.

Also see Global Clock Network, page 42.

CONFIG: Dedicated Configuration Pins

The dedicated configuration pins control the configuration process and are not available as user-I/O pins. Every package has seven dedicated configuration pins. All CONFIG-type pins are powered by the +2.5V VCCAUX supply.

Also see Configuration, page 46.

Table 86: **Spartan-3 FPGA Package Thermal Characteristics *(Cont'd)***

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
FG(G)1156[1]	XC3S4000	1.9	–	14.7	11.4	10.1	9.0	°C/Watt
	XC3S5000	1.9	8.9	14.5	11.3	10.0	8.9	°C/Watt

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

VQ100: 100-lead Very-Thin Quad Flat Package

The XC3S50 and the XC3S200 devices are available in the 100-lead very-thin quad flat package, VQ100. Both devices share a common footprint for this package as shown in Table 87 and Figure 44.

All the package pins appear in Table 87 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 87: **VQ100 Package Pinout**

Bank	XC3S50 XC3S200 Pin Name	VQ100 Pin Number	Type
0	IO_L01N_0/VRP_0	P97	DCI
0	IO_L01P_0/VRN_0	P96	DCI
0	IO_L31N_0	P92	I/O
0	IO_L31P_0/VREF_0	P91	VREF
0	IO_L32N_0/GCLK7	P90	GCLK
0	IO_L32P_0/GCLK6	P89	GCLK
0	VCCO_0	P94	VCCO
1	IO	P81	I/O
1	IO_L01N_1/VRP_1	P80	DCI
1	IO_L01P_1/VRN_1	P79	DCI
1	IO_L31N_1/VREF_1	P86	VREF
1	IO_L31P_1	P85	I/O
1	IO_L32N_1/GCLK5	P88	GCLK
1	IO_L32P_1/GCLK4	P87	GCLK
1	VCCO_1	P83	VCCO
2	IO_L01N_2/VRP_2	P75	DCI
2	IO_L01P_2/VRN_2	P74	DCI
2	IO_L21N_2	P72	I/O
2	IO_L21P_2	P71	I/O
2	IO_L24N_2	P68	I/O
2	IO_L24P_2	P67	I/O

Table 89: **CP132 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	CP132 Ball	Type
6	IO_L22N_6	K1	I/O
6	IO_L22P_6	J3	I/O
6	IO_L23N_6	J2	I/O
6	IO_L23P_6	J1	I/O
6	IO_L24N_6/VREF_6	H3	VREF
6	IO_L24P_6	H2	I/O
6	IO_L40N_6	H1	I/O
6	IO_L40P_6/VREF_6	G3	VREF
7	IO_L01N_7/VRP_7	B2	DCI
7	IO_L01P_7/VRN_7	B1	DCI
7	IO_L21N_7	C1	I/O
7	IO_L21P_7	D3	I/O
7	IO_L22N_7	D1	I/O
7	IO_L22P_7	D2	I/O
7	IO_L23N_7	E2	I/O
7	IO_L23P_7	E3	I/O
7	IO_L24N_7	F3	I/O
7	IO_L24P_7	E1	I/O
7	IO_L40N_7/VREF_7	G1	VREF
7	IO_L40P_7	F2	I/O
0,1	VCCO_TOP	B12	VCCO
0,1	VCCO_TOP	A4	VCCO
0,1	VCCO_TOP	B8	VCCO
2,3	VCCO_RIGHT	D13	VCCO
2,3	VCCO_RIGHT	H13	VCCO
2,3	VCCO_RIGHT	M12	VCCO
4,5	VCCO_BOTTOM	N7	VCCO
4,5	VCCO_BOTTOM	P11	VCCO
4,5	VCCO_BOTTOM	N3	VCCO
6,7	VCCO_LEFT	G2	VCCO
6,7	VCCO_LEFT	L2	VCCO
6,7	VCCO_LEFT	C3	VCCO
N/A	GND	B4	GND
N/A	GND	B9	GND
N/A	GND	C2	GND
N/A	GND	C12	GND
N/A	GND	D14	GND
N/A	GND	F1	GND
N/A	GND	J14	GND
N/A	GND	L1	GND

TQ144: 144-lead Thin Quad Flat Package

The XC3S50, the XC3S200, and the XC3S400 are available in the 144-lead thin quad flat package, TQ144. All devices share a common footprint for this package as shown in Table 91 and Figure 46.

The TQ144 package only has four separate VCCO inputs, unlike the BGA packages, which have eight separate VCCO inputs. The TQ144 package has a separate VCCO input for the top, bottom, left, and right. However, there are still eight separate I/O banks, as shown in Table 91 and Figure 46. Banks 0 and 1 share the VCCO_TOP input, Banks 2 and 3 share the VCCO_RIGHT input, Banks 4 and 5 share the VCCO_BOTTOM input, and Banks 6 and 7 share the VCCO_LEFT input.

All the package pins appear in Table 91 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 91: **TQ144 Package Pinout**

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
0	IO_L01N_0/VRP_0	P141	DCI
0	IO_L01P_0/VRN_0	P140	DCI
0	IO_L27N_0	P137	I/O
0	IO_L27P_0	P135	I/O
0	IO_L30N_0	P132	I/O
0	IO_L30P_0	P131	I/O
0	IO_L31N_0	P130	I/O
0	IO_L31P_0/VREF_0	P129	VREF
0	IO_L32N_0/GCLK7	P128	GCLK
0	IO_L32P_0/GCLK6	P127	GCLK
1	IO	P116	I/O
1	IO_L01N_1/VRP_1	P113	DCI
1	IO_L01P_1/VRN_1	P112	DCI
1	IO_L28N_1	P119	I/O
1	IO_L28P_1	P118	I/O
1	IO_L31N_1/VREF_1	P123	VREF
1	IO_L31P_1	P122	I/O
1	IO_L32N_1/GCLK5	P125	GCLK
1	IO_L32P_1/GCLK4	P124	GCLK
2	IO_L01N_2/VRP_2	P108	DCI
2	IO_L01P_2/VRN_2	P107	DCI
2	IO_L20N_2	P105	I/O
2	IO_L20P_2	P104	I/O
2	IO_L21N_2	P103	I/O
2	IO_L21P_2	P102	I/O
2	IO_L22N_2	P100	I/O
2	IO_L22P_2	P99	I/O

User I/Os by Bank

Table 94 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S50 in the PQ208 package. Similarly, Table 95 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S200 and XC3S400 in the PQ208 package.

Table 94: **User I/Os Per Bank for XC3S50 in PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	15	9	0	2	2	2
	1	15	9	0	2	2	2
Right	2	16	13	0	2	2	0
	3	16	12	0	2	2	0
Bottom	4	15	3	6	2	2	2
	5	15	3	6	2	2	2
Left	6	16	12	0	2	2	0
	7	16	12	0	2	2	0

Table 95: **User I/Os Per Bank for XC3S200 and XC3S400 in PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	16	9	0	2	3	2
	1	15	9	0	2	2	2
Right	2	19	14	0	2	3	0
	3	20	15	0	2	3	0
Bottom	4	17	4	6	2	3	2
	5	15	3	6	2	2	2
Left	6	19	14	0	2	3	0
	7	20	15	0	2	3	0

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
N/A	GND	T16	GND
N/A	VCCAUX	A6	VCCAUX
N/A	VCCAUX	A11	VCCAUX
N/A	VCCAUX	F1	VCCAUX
N/A	VCCAUX	F16	VCCAUX
N/A	VCCAUX	L1	VCCAUX
N/A	VCCAUX	L16	VCCAUX
N/A	VCCAUX	T6	VCCAUX
N/A	VCCAUX	T11	VCCAUX
N/A	VCCINT	D4	VCCINT
N/A	VCCINT	D13	VCCINT
N/A	VCCINT	E5	VCCINT
N/A	VCCINT	E12	VCCINT
N/A	VCCINT	M5	VCCINT
N/A	VCCINT	M12	VCCINT
N/A	VCCINT	N4	VCCINT
N/A	VCCINT	N13	VCCINT
VCCAUX	CCLK	T15	CONFIG
VCCAUX	DONE	R14	CONFIG
VCCAUX	HSWAP_EN	C4	CONFIG
VCCAUX	M0	P3	CONFIG
VCCAUX	M1	T2	CONFIG
VCCAUX	M2	P4	CONFIG
VCCAUX	PROG_B	B3	CONFIG
VCCAUX	TCK	C14	JTAG
VCCAUX	TDI	A2	JTAG
VCCAUX	TDO	A15	JTAG
VCCAUX	TMS	C13	JTAG

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
3	IO_L24N_3	M18	I/O
3	IO_L24P_3	N17	I/O
3	IO_L27N_3	L14	I/O
3	IO_L27P_3	L13	I/O
3	IO_L34N_3	L15	I/O
3	IO_L34P_3/VREF_3	L16	VREF
3	IO_L35N_3	L18	I/O
3	IO_L35P_3	L17	I/O
3	IO_L39N_3	K13	I/O
3	IO_L39P_3	K14	I/O
3	IO_L40N_3/VREF_3	K17	VREF
3	IO_L40P_3	K18	I/O
3	VCCO_3	K12	VCCO
3	VCCO_3	L12	VCCO
3	VCCO_3	N16	VCCO
4	IO	P12	I/O
4	IO	V14	I/O
4	IO/VREF_4	R10	VREF
4	IO/VREF_4	U13	VREF
4	IO/VREF_4	V17	VREF
4	IO_L01N_4/VRP_4	U16	DCI
4	IO_L01P_4/VRN_4	V16	DCI
4	IO_L06N_4/VREF_4	P14	VREF
4	IO_L06P_4	R14	I/O
4	IO_L09N_4	U15	I/O
4	IO_L09P_4	V15	I/O
4	IO_L10N_4	T14	I/O
4	IO_L10P_4	U14	I/O
4	IO_L25N_4	R13	I/O
4	IO_L25P_4	P13	I/O
4	IO_L27N_4/DIN/D0	T12	DUAL
4	IO_L27P_4/D1	R12	DUAL
4	IO_L28N_4	V12	I/O
4	IO_L28P_4	V11	I/O
4	IO_L29N_4	R11	I/O
4	IO_L29P_4	T11	I/O
4	IO_L30N_4/D2	N11	DUAL
4	IO_L30P_4/D3	P11	DUAL
4	IO_L31N_4/INIT_B	U10	DUAL

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
7	IO_L20P_7	E1	I/O
7	IO_L21N_7	E4	I/O
7	IO_L21P_7	F4	I/O
7	IO_L22N_7	G5	I/O
7	IO_L22P_7	F5	I/O
7	IO_L23N_7	G1	I/O
7	IO_L23P_7	F2	I/O
7	IO_L24N_7	G4	I/O
7	IO_L24P_7	G3	I/O
7	IO_L27N_7	H5	I/O
7	IO_L27P_7/VREF_7	H6	VREF
7	IO_L34N_7	H4	I/O
7	IO_L34P_7	H3	I/O
7	IO_L35N_7	H1	I/O
7	IO_L35P_7	H2	I/O
7	IO_L39N_7	J1	I/O
7	IO_L39P_7	J2	I/O
7	IO_L40N_7/VREF_7	J5	VREF
7	IO_L40P_7	J4	I/O
7	VCCO_7	F3	VCCO
7	VCCO_7	H7	VCCO
7	VCCO_7	J7	VCCO
N/A	GND	A1	GND
N/A	GND	A13	GND
N/A	GND	A18	GND
N/A	GND	A6	GND
N/A	GND	B17	GND
N/A	GND	B2	GND
N/A	GND	C10	GND
N/A	GND	C9	GND
N/A	GND	F1	GND
N/A	GND	F18	GND
N/A	GND	G12	GND
N/A	GND	G7	GND
N/A	GND	H10	GND
N/A	GND	H11	GND
N/A	GND	H8	GND
N/A	GND	H9	GND
N/A	GND	J11	GND
N/A	GND	J16	GND

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
3	IO_L16P_3	IO_L16P_3	Y22	I/O
3	IO_L17N_3	IO_L17N_3	V19	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	W19	VREF
3	IO_L19N_3	IO_L19N_3	W21	I/O
3	IO_L19P_3	IO_L19P_3	W20	I/O
3	IO_L20N_3	IO_L20N_3	U19	I/O
3	IO_L20P_3	IO_L20P_3	V20	I/O
3	IO_L21N_3	IO_L21N_3	V22	I/O
3	IO_L21P_3	IO_L21P_3	V21	I/O
3	IO_L22N_3	IO_L22N_3	T17	I/O
3	IO_L22P_3	IO_L22P_3	U18	I/O
3	IO_L23N_3	IO_L23N_3	U21	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	U20	VREF
3	IO_L24N_3	IO_L24N_3	R18	I/O
3	IO_L24P_3	IO_L24P_3	T18	I/O
3	N.C. (◆)	IO_L26N_3	T20	I/O
3	N.C. (◆)	IO_L26P_3	T19	I/O
3	IO_L27N_3	IO_L27N_3	T22	I/O
3	IO_L27P_3	IO_L27P_3	T21	I/O
3	N.C. (◆)	IO_L28N_3	R22	I/O
3	N.C. (◆)	IO_L28P_3	R21	I/O
3	N.C. (◆)	IO_L29N_3	P19	I/O
3	N.C. (◆)	IO_L29P_3	R19	I/O
3	N.C. (◆)	IO_L31N_3	P18	I/O
3	N.C. (◆)	IO_L31P_3	P17	I/O
3	N.C. (◆)	IO_L32N_3	P22	I/O
3	N.C. (◆)	IO_L32P_3	P21	I/O
3	N.C. (◆)	IO_L33N_3	N18	I/O
3	N.C. (◆)	IO_L33P_3	N17	I/O
3	IO_L34N_3	IO_L34N_3	N20	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	N19	VREF
3	IO_L35N_3	IO_L35N_3	N22	I/O
3	IO_L35P_3	IO_L35P_3	N21	I/O
3	IO_L38N_3	IO_L38N_3	M18	I/O
3	IO_L38P_3	IO_L38P_3	M17	I/O
3	IO_L39N_3	IO_L39N_3	M20	I/O
3	IO_L39P_3	IO_L39P_3	M19	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	M22	VREF
3	IO_L40P_3	IO_L40P_3	M21	I/O
3	VCCO_3	VCCO_3	M16	VCCO

FG456 Footprint

Left Half of FG456 Package (Top View)

XC3S400 (264 max. user I/O)

196 **I/O:** Unrestricted, general-purpose user I/O

32 **VREF:** User I/O or input voltage reference for bank

69 **N.C.:** Unconnected pins for XC3S400 (◆)

XC3S1000, XC3S1500, XC3S2000 (333 max user I/O)

261 **I/O:** Unrestricted, general-purpose user I/O

36 **VREF:** User I/O or input voltage reference for bank

0 **N.C.:** No unconnected pins in this package

All devices

12 **DUAL:** Configuration pin, then possible user I/O

8 **GCLK:** User I/O or global clock buffer input

16 **DCI:** User I/O or reference resistor input for bank

7 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

12 **VCCINT:** Internal core voltage supply (+1.2V)

40 **VCCO:** Output voltage supply for bank

8 **VCCAUX:** Auxiliary voltage supply (+2.5V)

52 **GND:** Ground

	Bank 0										
	1	2	3	4	5	6	7	8	9	10	11
A	GND	PROG_B	IO VREF_0	I/O L01P_0 VRN_0	I/O L09P_0	VCCAUX	I/O L19P_0 ◆	I/O L24P_0	I/O L27P_0	I/O	I/O L32P_0 GCLK6
B	TDI	GND	HSWAP_EN	I/O L01N_0 VRP_0	I/O L09N_0	I/O L15P_0	I/O L19N_0 ◆	I/O L24N_0	I/O L27N_0	I/O L29P_0	I/O L32N_0 GCLK7
C	I/O L16P_7 VREF_7	I/O	I/O L01N_7 VRP_7	I/O L01P_7 VRN_7	I/O L06P_0	I/O L15N_0	IO VREF_0	VCCO_0	GND	I/O L29N_0	I/O L31P_0 VREF_0
D	I/O L16N_7	I/O L19P_7	I/O L19N_7 VREF_7	I/O L17P_7	I/O L06N_0	I/O L10P_0	I/O L16P_0	I/O L22P_0 ◆	I/O	I/O	I/O L31N_0
E	I/O L21N_7	I/O L21P_7	I/O L20P_7	I/O L17N_7	IO VREF_0 ◆	I/O L10N_0	I/O L16N_0	I/O L22N_0 ◆	I/O L25P_0	I/O L28P_0	I/O L30P_0
F	VCCAUX	I/O L23N_7	I/O L23P_7	I/O L20N_7	I/O L22P_7	I/O	IO VREF_0	VCCO_0	I/O L25N_0	I/O L28N_0	I/O L30N_0
G	I/O L27N_7	I/O L27P_7 VREF_7	I/O L26N_7 ◆	I/O L26P_7 ◆	I/O L24P_7	I/O L22N_7	VCCINT	VCCINT	VCCO_0	VCCO_0	VCCO_0
H	I/O L28N_7 ◆	I/O L28P_7 ◆	VCCO_7	I/O L29P_7 ◆	I/O L24N_7	VCCO_7	VCCINT				
J	I/O L32N_7 ◆	I/O L32P_7 ◆	GND	I/O L29N_7 ◆	I/O L31N_7 ◆	I/O L31P_7 ◆	VCCO_7		GND	GND	GND
K	I/O L35N_7	I/O L35P_7	I/O L34N_7	I/O L34P_7	I/O L33N_7 ◆	I/O L33P_7 ◆	VCCO_7		GND	GND	GND
L	I/O L40N_7 VREF_7	I/O L40P_7	I/O L39N_7	I/O L39P_7	I/O L38N_7	I/O L38P_7	VCCO_7		GND	GND	GND
M	I/O L40P_6 VREF_6	I/O L40N_6	I/O L39P_6	I/O L39N_6	I/O L38P_6	I/O L38N_6	VCCO_6		GND	GND	GND
N	I/O L35P_6	I/O L35N_6	I/O L34P_6	I/O L34N_6 VREF_6	I/O L33P_6 ◆	I/O L33N_6 ◆	VCCO_6		GND	GND	GND
P	I/O L32P_6 ◆	I/O L32N_6 ◆	GND	I/O L31P_6 ◆	I/O L31N_6 ◆	I/O L28P_6 ◆	VCCO_6		GND	GND	GND
R	I/O L29P_6 ◆	I/O L29N_6 ◆	VCCO_6	I/O L26P_6 ◆	I/O L28N_6 ◆	VCCO_6	VCCINT				
T	I/O L27P_6	I/O L27N_6	I/O L26N_6 ◆	I/O L23P_6	I/O L22P_6	I/O L22N_6	VCCINT	VCCINT	VCCO_5	VCCO_5	VCCO_5
U	VCCAUX	I/O L24P_6	I/O L24N_6 VREF_6	I/O L23N_6	I/O L19P_6	IO VREF_5	I/O	VCCO_5	I/O ◆	I/O	I/O
V	I/O L21P_6	I/O L21N_6	I/O L20P_6	I/O L20N_6	I/O L19N_6	I/O L15P_5	I/O	I/O L24P_5	I/O L27P_5	I/O	I/O L31P_5 D5
W	I/O L17P_6 VREF_6	I/O L17N_6	I/O L16P_6	I/O L16N_6	I/O L09P_5	I/O L15N_5	I/O L19P_5 VREF_5 ◆	I/O L24N_5	I/O L27N_5 VREF_5	I/O L29P_5 VREF_5	I/O L31N_5 D4
Y	I/O	I/O L01P_6 VRN_6	I/O L01N_6 VRP_6	I/O L01N_5 RDWR_B	I/O L09N_5	I/O L16P_5	I/O L19N_5 ◆	VCCO_5	GND	I/O L29N_5	I/O L32P_5 GCLK2
AA	M1	GND	I/O L01P_5 CS_B	I/O L06P_5	I/O L10P_5 VRN_5	I/O L16N_5	I/O L22P_5 ◆	I/O L25P_5	I/O L28P_5 D7	I/O L30P_5	I/O L32N_5 GCLK3
AB	GND	M0	M2	I/O L06N_5	I/O L10N_5 VRP_5	VCCAUX	I/O L22N_5 ◆	I/O L25N_5	I/O L28N_5 D6	I/O L30N_5	IO VREF_5

Bank 7 (rows G–L) · Bank 6 (rows M–T) · Bank 5 (columns 7–11)

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Figure 51: **FG456 Package Footprint (Top View)**

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
N/A	GND	GND	GND	GND	GND	D15	GND
N/A	GND	GND	GND	GND	GND	D23	GND
N/A	GND	GND	GND	GND	GND	K11	GND
N/A	GND	GND	GND	GND	GND	K12	GND
N/A	GND	GND	GND	GND	GND	K15	GND
N/A	GND	GND	GND	GND	GND	K16	GND
N/A	GND	GND	GND	GND	GND	L10	GND
N/A	GND	GND	GND	GND	GND	L11	GND
N/A	GND	GND	GND	GND	GND	L12	GND
N/A	GND	GND	GND	GND	GND	L13	GND
N/A	GND	GND	GND	GND	GND	L14	GND
N/A	GND	GND	GND	GND	GND	L15	GND
N/A	GND	GND	GND	GND	GND	L16	GND
N/A	GND	GND	GND	GND	GND	L17	GND
N/A	GND	GND	GND	GND	GND	M4	GND
N/A	GND	GND	GND	GND	GND	M10	GND
N/A	GND	GND	GND	GND	GND	M11	GND
N/A	GND	GND	GND	GND	GND	M12	GND
N/A	GND	GND	GND	GND	GND	M13	GND
N/A	GND	GND	GND	GND	GND	M14	GND
N/A	GND	GND	GND	GND	GND	M15	GND
N/A	GND	GND	GND	GND	GND	M16	GND
N/A	GND	GND	GND	GND	GND	M17	GND
N/A	GND	GND	GND	GND	GND	M23	GND
N/A	GND	GND	GND	GND	GND	N11	GND
N/A	GND	GND	GND	GND	GND	N12	GND
N/A	GND	GND	GND	GND	GND	N13	GND
N/A	GND	GND	GND	GND	GND	N14	GND
N/A	GND	GND	GND	GND	GND	N15	GND
N/A	GND	GND	GND	GND	GND	N16	GND
N/A	GND	GND	GND	GND	GND	P11	GND
N/A	GND	GND	GND	GND	GND	P12	GND
N/A	GND	GND	GND	GND	GND	P13	GND
N/A	GND	GND	GND	GND	GND	P14	GND
N/A	GND	GND	GND	GND	GND	P15	GND
N/A	GND	GND	GND	GND	GND	P16	GND
N/A	GND	GND	GND	GND	GND	R4	GND
N/A	GND	GND	GND	GND	GND	R10	GND
N/A	GND	GND	GND	GND	GND	R11	GND
N/A	GND	GND	GND	GND	GND	R12	GND
N/A	GND	GND	GND	GND	GND	R13	GND
N/A	GND	GND	GND	GND	GND	R14	GND
N/A	GND	GND	GND	GND	GND	R15	GND

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	C1	DCI
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	C2	DCI
7	IO_L02N_7	IO_L02N_7	D3	I/O
7	IO_L02P_7	IO_L02P_7	D4	I/O
7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	D1	VREF
7	IO_L03P_7	IO_L03P_7	D2	I/O
7	IO_L04N_7	IO_L04N_7	E1	I/O
7	IO_L04P_7	IO_L04P_7	E2	I/O
7	IO_L05N_7	IO_L05N_7	F5	I/O
7	IO_L05P_7	IO_L05P_7	E4	I/O
7	IO_L06N_7	IO_L06N_7	F2	I/O
7	IO_L06P_7	IO_L06P_7	F3	I/O
7	IO_L07N_7	IO_L07N_7	G3	I/O
7	IO_L07P_7	IO_L07P_7	G4	I/O
7	IO_L08N_7	IO_L08N_7	G1	I/O
7	IO_L08P_7	IO_L08P_7	G2	I/O
7	IO_L09N_7	IO_L09N_7	H7	I/O
7	IO_L09P_7	IO_L09P_7	G6	I/O
7	IO_L10N_7	IO_L10N_7	H5	I/O
7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	H6	VREF
7	IO_L11N_7	IO_L11N_7	H3	I/O
7	IO_L11P_7	IO_L11P_7	H4	I/O
7	IO_L13N_7	IO_L13N_7	H1	I/O
7	IO_L13P_7	IO_L13P_7	H2	I/O
7	IO_L14N_7	IO_L14N_7	J4	I/O
7	IO_L14P_7	IO_L14P_7	J5	I/O
7	IO_L15N_7	IO_L15N_7	J1	I/O
7	IO_L15P_7	IO_L15P_7	J2	I/O
7	IO_L16N_7	IO_L16N_7	K9	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	J8	VREF
7	IO_L17N_7	IO_L17N_7	K6	I/O
7	IO_L17P_7	IO_L17P_7	K7	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	K2	VREF
7	IO_L19P_7	IO_L19P_7	K3	I/O
7	IO_L20N_7	IO_L20N_7	L10	I/O
7	IO_L20P_7	IO_L20P_7	K10	I/O
7	IO_L21N_7	IO_L21N_7	L7	I/O
7	IO_L21P_7	IO_L21P_7	L8	I/O
7	IO_L22N_7	IO_L22N_7	L5	I/O
7	IO_L22P_7	IO_L22P_7	L6	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L24P_3	IO_L24P_3	AC26	I/O
3	IO_L26N_3	IO_L26N_3	AA28	I/O
3	IO_L26P_3	IO_L26P_3	AA27	I/O
3	IO_L27N_3	IO_L27N_3	AA30	I/O
3	IO_L27P_3	IO_L27P_3	AA29	I/O
3	IO_L28N_3	IO_L28N_3	AA32	I/O
3	IO_L28P_3	IO_L28P_3	AA31	I/O
3	IO_L29N_3	IO_L29N_3	AA34	I/O
3	IO_L29P_3	IO_L29P_3	AA33	I/O
3	IO_L30N_3	IO_L30N_3	Y29	I/O
3	IO_L30P_3	IO_L30P_3	Y28	I/O
3	IO_L31N_3	IO_L31N_3	Y32	I/O
3	IO_L31P_3	IO_L31P_3	Y31	I/O
3	IO_L32N_3	IO_L32N_3	Y34	I/O
3	IO_L32P_3	IO_L32P_3	Y33	I/O
3	IO_L33N_3	IO_L33N_3	W25	I/O
3	IO_L33P_3	IO_L33P_3	Y26	I/O
3	IO_L34N_3	IO_L34N_3	W29	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	W28	VREF
3	IO_L35N_3	IO_L35N_3	W33	I/O
3	IO_L35P_3	IO_L35P_3	W32	I/O
3	IO_L37N_3	IO_L37N_3	V28	I/O
3	IO_L37P_3	IO_L37P_3	V27	I/O
3	IO_L38N_3	IO_L38N_3	V30	I/O
3	IO_L38P_3	IO_L38P_3	V29	I/O
3	IO_L39N_3	IO_L39N_3	V32	I/O
3	IO_L39P_3	IO_L39P_3	V31	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	V34	VREF
3	IO_L40P_3	IO_L40P_3	V33	I/O
3	N.C. (◆)	IO_L41N_3	AH32	I/O
3	N.C. (◆)	IO_L41P_3	AH31	I/O
3	N.C. (◆)	IO_L44N_3	AD29	I/O
3	N.C. (◆)	IO_L44P_3	AD28	I/O
3	IO_L45N_3	IO_L45N_3	AC34	I/O
3	IO_L45P_3	IO_L45P_3	AC33	I/O
3	IO_L46N_3	IO_L46N_3	AB28	I/O
3	IO_L46P_3	IO_L46P_3	AB27	I/O
3	IO_L47N_3	IO_L47N_3	AB32	I/O
3	IO_L47P_3	IO_L47P_3	AB31	I/O
3	IO_L48N_3	IO_L48N_3	AA24	I/O