AMD Xilinx - XC3S200-5VQ100C Datasheet

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	480
Number of Logic Elements/Cells	4320
Total RAM Bits	221184
Number of I/O	63
Number of Gates	200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s200-5vq100c

IOBs

For additional information, refer to the chapter entitled “Using I/O Resources” in UG331: *Spartan-3 Generation FPGA User Guide*.

IOB Overview

The Input/Output Block (IOB) provides a programmable, bidirectional interface between an I/O pin and the FPGA’s internal logic.

A simplified diagram of the IOB’s internal structure appears in Figure 7. There are three main signal paths within the IOB: the output path, input path, and 3-state path. Each path has its own pair of storage elements that can act as either registers or latches. For more information, see the Storage Element Functions section. The three main signal paths are as follows:

- The input path carries data from the pad, which is bonded to a package pin, through an optional programmable delay element directly to the I line. There are alternate routes through a pair of storage elements to the IQ1 and IQ2 lines. The IOB outputs I, IQ1, and IQ2 all lead to the FPGA’s internal logic. The delay element can be set to ensure a hold time of zero.
- The output path, starting with the O1 and O2 lines, carries data from the FPGA’s internal logic through a multiplexer and then a three-state driver to the IOB pad. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.
- The 3-state path determines when the output driver is high impedance. The T1 and T2 lines carry data from the FPGA’s internal logic through a multiplexer to the output driver. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements. When the T1 or T2 lines are asserted High, the output driver is high-impedance (floating, hi-Z). The output driver is active-Low enabled.
- All signal paths entering the IOB, including those associated with the storage elements, have an inverter option. Any inverter placed on these paths is automatically absorbed into the IOB.

Storage Element Functions

There are three pairs of storage elements in each IOB, one pair for each of the three paths. It is possible to configure each of these storage elements as an edge-triggered D-type flip-flop (FD) or a level-sensitive latch (LD).

The storage-element-pair on either the Output path or the Three-State path can be used together with a special multiplexer to produce Double-Data-Rate (DDR) transmission. This is accomplished by taking data synchronized to the clock signal’s rising edge and converting them to bits synchronized on both the rising and the falling edge. The combination of two registers and a multiplexer is referred to as a Double-Data-Rate D-type flip-flop (FDDR). See Double-Data-Rate Transmission, page 12 for more information.

The signal paths associated with the storage element are described in Table 5.

Table 5: **Storage Element Signal Description**

Storage Element Signal	Description	Function
D	Data input	Data at this input is stored on the active edge of CK enabled by CE. For latch operation when the input is enabled, data passes directly to the output Q.
Q	Data output	The data on this output reflects the state of the storage element. For operation as a latch in transparent mode, Q will mirror the data at D.
CK	Clock input	A signal’s active edge on this input with CE asserted, loads data into the storage element.
CE	Clock Enable input	When asserted, this input enables CK. If not connected, CE defaults to the asserted state.
SR	Set/Reset	Forces storage element into the state specified by the SRHIGH/SRLOW attributes. The SYNC/ASYNC attribute setting determines if the SR input is synchronized to the clock or not.
REV	Reverse	Used together with SR. Forces storage element into the state opposite from what SR does.

Table 9: **Differential I/O Standards**

Signal Standard (IOSTANDARD)	V_{CCO} (Volts)		V_{REF} for Inputs (Volts)
	For Outputs	For Inputs	
LDT_25 (ULVDS_25)	2.5	–	–
LVDS_25	2.5	–	–
BLVDS_25	2.5	–	–
LVDSEXT_25	2.5	–	–
LVPECL_25	2.5	–	–
RSDS_25	2.5	–	–
DIFF_HSTL_II_18	1.8	–	–
DIFF_SSTL2_II	2.5	–	–

Notes:

1. See Table 10 for a listing of the differential DCI standards.

The need to supply V_{REF} and V_{CCO} imposes constraints on which standards can be used in the same bank. See The Organization of IOBs into Banks section for additional guidelines concerning the use of the V_{CCO} and V_{REF} lines.

Digitally Controlled Impedance (DCI)

When the round-trip delay of an output signal—i.e., from output to input and back again—exceeds rise and fall times, it is common practice to add termination resistors to the line carrying the signal. These resistors effectively match the impedance of a device's I/O to the characteristic impedance of the transmission line, thereby preventing reflections that adversely affect signal integrity. However, with the high I/O counts supported by modern devices, adding resistors requires significantly more components and board area. Furthermore, for some packages—e.g., ball grid arrays—it may not always be possible to place resistors close to pins.

DCI answers these concerns by providing two kinds of on-chip terminations: Parallel terminations make use of an integrated resistor network. Series terminations result from controlling the impedance of output drivers. DCI actively adjusts both parallel and series terminations to accurately match the characteristic impedance of the transmission line. This adjustment process compensates for differences in I/O impedance that can result from normal variation in the ambient temperature, the supply voltage and the manufacturing process. When the output driver turns off, the series termination, by definition, approaches a very high impedance; in contrast, parallel termination resistors remain at the targeted values.

DCI is available only for certain I/O standards, as listed in Table 10. DCI is selected by applying the appropriate I/O standard extensions to symbols or components. There are five basic ways to configure terminations, as shown in Table 11. The DCI I/O standard determines which of these terminations is put into effect.

HSTL_I_DCI-, HSTL_III_DCI-, and SSTL2_I_DCI-type outputs do not require the VRN and VRP reference resistors. Likewise, LVDCI-type inputs do not require the VRN and VRP reference resistors. In a bank without any DCI I/O or a bank containing non-DCI I/O and purely HSTL_I_DCI- or HSTL_III_DCI-type outputs, or SSTL2_I_DCI-type outputs or LVDCI-type inputs, the associated VRN and VRP pins can be used as general-purpose I/O pins.

The HSLVDCI (High-Speed LVDCI) standard is intended for bidirectional use. The driver is identical to LVDCI, while the input is identical to HSTL. By using a V_{REF}-referenced input, HSLVDCI allows greater input sensitivity at the receiver than when using a single-ended LVCMOS-type receiver.

Table 10: **DCI I/O Standards**

Category of Signal Standard	Signal Standard (IOSTANDARD)	V_{CCO} (V)		V_{REF} for Inputs (V)	Termination Type	
		For Outputs	For Inputs		At Output	At Input
Single-Ended						
Gunning Transceiver Logic	GTL_DCI	1.2	1.2	0.8	Single	Single
	GTLP_DCI	1.5	1.5	1.0		
High-Speed Transceiver Logic	HSTL_I_DCI	1.5	1.5	0.75	None	Split
	HSTL_III_DCI	1.5	1.5	0.9	None	Single
	HSTL_I_DCI_18	1.8	1.8	0.9	None	Split
	HSTL_II_DCI_18 DIFF_HSTL_II_18_DCI	1.8	1.8	0.9	Split	
	HSTL_III_DCI_18	1.8	1.8	1.1	None	Single
Low-Voltage CMOS	LVDCI_15	1.5	1.5	–	Controlled impedance driver	None
	LVDCI_18	1.8	1.8	–		
	LVDCI_25	2.5	2.5	–		
	LVDCI_33[2]	3.3	3.3	–		
	LVDCI_DV2_15	1.5	1.5	–	Controlled driver with half-impedance	
	LVDCI_DV2_18	1.8	1.8	–		
	LVDCI_DV2_25	2.5	2.5	–		
	LVDCI_DV2_33	3.3	3.3	–		
Hybrid HSTL Input and LVCMOS Output	HSLVDCI_15	1.5	1.5	0.75	Controlled impedance driver	None
	HSLVDCI_18	1.8	1.8	0.9		
	HSLVDCI_25	2.5	2.5	1.25		
	HSLVDCI_33	3.3	3.3	1.65		
Stub Series Terminated Logic[3]	SSTL18_I_DCI	1.8	1.8	0.9	25Ω driver	Split
	SSTL2_I_DCI	2.5	2.5	1.25	25Ω driver	
	SSTL2_II_DCI DIFF_SSTL2_II_DCI	2.5	2.5	1.25	Split with 25Ω driver	
Differential						
Low-Voltage Differential Signaling	LVDS_25_DCI	N/A	2.5	–	None	Split on each line of pair
	LVDSEXT_25_DCI	N/A	2.5	–		

Notes:

1. DCI signal standards are not supported in Bank 5 of any Spartan-3 FPGA packaged in a VQ100, CP132, or TQ144 package.
2. Equivalent to LVTTL DCI.
3. The SSTL18_II signal standard does not have a DCI equivalent.

- **Phase Shifting:** The DCM provides the ability to shift the phase of all its output clock signals with respect to its input clock signal.

The DCM has four functional components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), the Phase Shifter (PS), and the Status Logic. Each component has its associated signals, as shown in Figure 19.

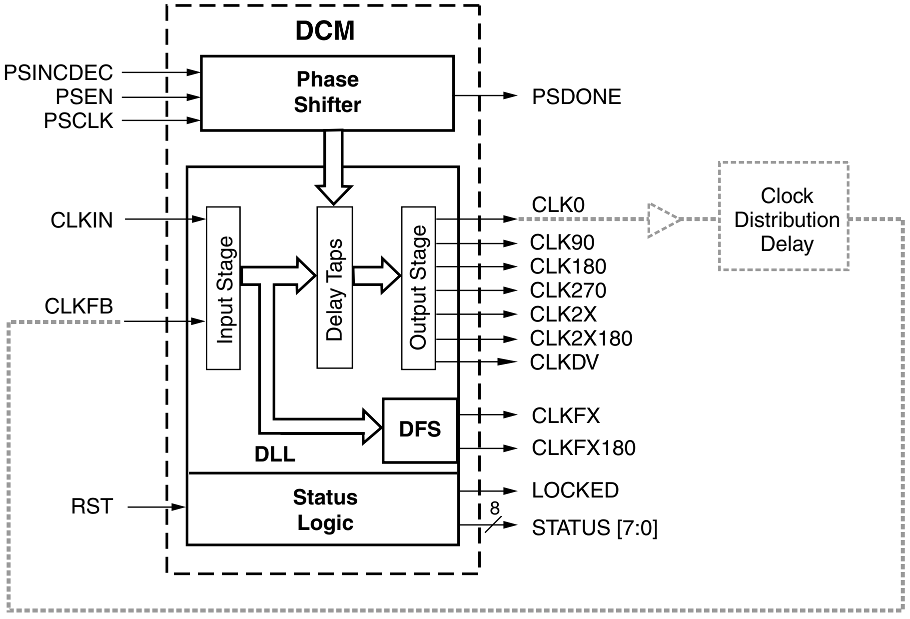

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Figure 19: **DCM Functional Blocks and Associated Signals**

Delay-Locked Loop (DLL)

The most basic function of the DLL component is to eliminate clock skew. The main signal path of the DLL consists of an input stage, followed by a series of discrete delay elements or *taps,* which in turn leads to an output stage. This path together with logic for phase detection and control forms a system complete with feedback as shown in Figure 20.

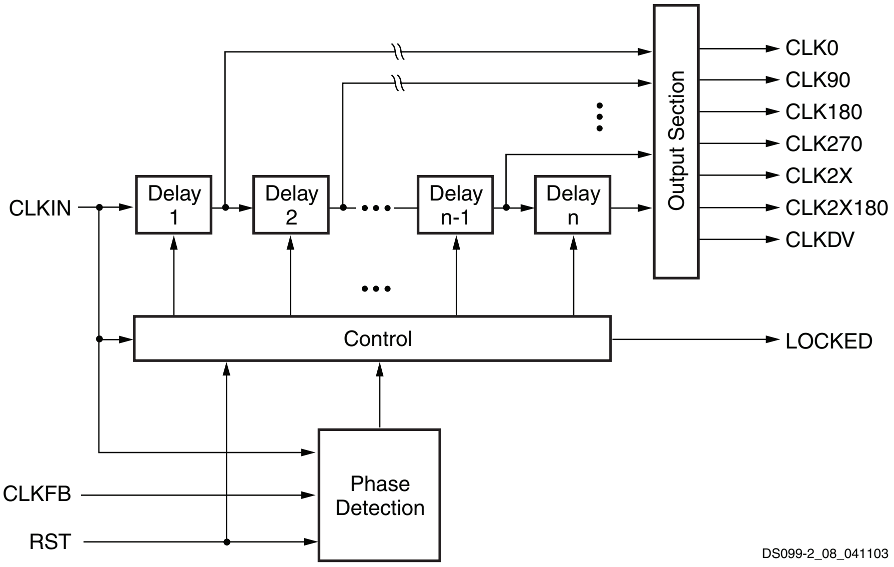

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Figure 20: **Simplified Functional Diagram of DLL**

Table 41: **System-Synchronous Pin-to-Pin Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IOBDELAY = IFD, without DCM	XC3S50	–0.98	–0.93	ns
			XC3S200	–0.40	–0.35	ns
			XC3S400	–0.27	–0.22	ns
			XC3S1000	–1.19	–1.14	ns
			XC3S1500	–1.43	–1.38	ns
			XC3S2000	–2.33	–2.28	ns
			XC3S4000	–2.47	–2.42	ns
			XC3S5000	–2.66	–2.61	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *subtract* the appropriate adjustment from Table 44. If this is true of the data Input, *add* the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *add* the appropriate Input adjustment from Table 44. If this is true of the data Input, *subtract* the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Table 42: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Setup Times						
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2), IOBDELAY = NONE	XC3S50	1.65	1.89	ns
			XC3S200	1.37	1.57	ns
			XC3S400	1.37	1.57	ns
			XC3S1000	1.65	1.89	ns
			XC3S1500	1.65	1.89	ns
			XC3S2000	1.65	1.89	ns
			XC3S4000	1.73	1.99	ns
			XC3S5000	1.82	2.09	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the IFF's ICLK input. The Input Delay is programmed.	LVCMOS25(2), IOBDELAY = IFD	XC3S50	4.39	5.04	ns
			XC3S200	4.76	5.47	ns
			XC3S400	4.63	5.32	ns
			XC3S1000	5.02	5.76	ns
			XC3S1500	5.40	6.20	ns
			XC3S2000	6.68	7.68	ns
			XC3S4000	7.16	8.24	ns
			XC3S5000	7.33	8.42	ns

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair**

Signal Standard (IOSTANDARD)			Package				
			VQ100	**TQ144**	**PQ208**	**CP132**	**FT256, FG320, FG456, FG676, FG900, FG1156**
Single-Ended Standards							
GTL			0	0	0	1	14
GTL_DCI			0	0	0	1	14
GTLP			0	0	0	1	19
GTLP_DCI			0	0	0	1	19
HSLVDCI_15			6	6	6	6	14
HSLVDCI_18			7	7	7	7	10
HSLVDCI_25			7	7	7	7	11
HSLVDCI_33			10	10	10	10	10
HSTL_I			11	11	11	11	17
HSTL_I_DCI			11	11	11	11	17
HSTL_III			7	7	7	7	7
HSTL_III_DCI			7	7	7	7	7
HSTL_I_18			13	13	13	13	17
HSTL_I_DCI_18			13	13	13	13	17
HSTL_II_18			9	9	9	9	9
HSTL_II_DCI_18			9	9	9	9	9
HSTL_III_18			8	8	8	8	8
HSTL_III_DCI_18			8	8	8	8	8
LVCMOS12	Slow	2	17	17	17	17	55
		4	13	13	13	13	32
		6	10	10	10	10	18
	Fast	2	12	12	12	12	31
		4	11	11	11	11	13
		6	9	9	9	9	9
LVCMOS15	Slow	2	16	12	12	19	55
		4	8	7	7	9	31
		6	7	7	7	9	18
		8	6	6	6	6	15
		12	5	5	5	5	10
	Fast	2	10	10	10	13	25
		4	6	7	7	7	16
		6	7	7	7	7	13
		8	6	6	6	6	11
		12	6	6	6	6	7

Table 70: **Spartan-3 FPGA Pin Definitions *(Cont'd)***

Pin Name	Direction	Description
GCLK: Global clock buffer inputs		
IO_Lxxy_#/GCLK0, IO_Lxxy_#/GCLK1, IO_Lxxy_#/GCLK2, IO_Lxxy_#/GCLK3, IO_Lxxy_#/GCLK4, IO_Lxxy_#/GCLK5, IO_Lxxy_#/GCLK6, IO_Lxxy_#/GCLK7	Input if connected to global clock buffers Otherwise, same as I/O	**Global Buffer Input:** Direct input to a low-skew global clock buffer. If not connected to a global clock buffer, this pin is a user I/O.
VREF: I/O bank input reference voltage pins		
IO_Lxxy_#/VREF_# or IO/VREF_#	Voltage supply input when VREF pins are used within a bank. Otherwise, same as I/O	**Input Buffer Reference Voltage for Special I/O Standards (per bank):** If required to support special I/O standards, all the VREF pins within a bank connect to a input threshold voltage source. If not used as input reference voltage pins, these pins are available as individual user-I/O pins.
CONFIG: Dedicated configuration pins (pull-up resistor to VCCAUX always active during configuration, regardless of HSWAP_EN pin)		
CCLK	Input in Slave configuration modes Output in Master configuration modes	**Configuration Clock:** The configuration clock signal synchronizes configuration data. This pin has an internal pull-up resistor to VCCAUX during configuration.
PROG_B	Input	**Program/Configure Device:** Active Low asynchronous reset to configuration logic. Asserting PROG_B Low for an extended period delays the configuration process. This pin has an internal pull-up resistor to VCCAUX during configuration.
DONE	Bidirectional with open-drain or totem-pole Output	**Configuration Done, Delay Start-up Sequence:** A Low-to-High output transition on this bidirectional pin signals the end of the configuration process. The FPGA produces a Low-to-High transition on this pin to indicate that the configuration process is complete. The DriveDone bitstream generation option defines whether this pin functions as a totem-pole output that actively drives High or as an open-drain output. An open-drain output requires a pull-up resistor to produce a High logic level. The open-drain option permits the DONE lines of multiple FPGAs to be tied together, so that the common node transitions High only after all of the FPGAs have completed configuration. Externally holding the open-drain output Low delays the start-up sequence, which marks the transition to user mode.
M0, M1, M2	Input	**Configuration Mode Selection:** These inputs select the configuration mode. The logic levels applied to the mode pins are sampled on the rising edge of INIT_B. See Table 75. These pins have an internal pull-up resistor to VCCAUX during configuration, making Slave Serial the default configuration mode.
HSWAP_EN	Input	**Disable Pull-up Resistors During Configuration:** A Low on this pin enables pull-up resistors on all pins that are not actively involved in the configuration process. A High value disables all pull-ups, allowing the non-configuration pins to float.
JTAG: JTAG interface pins (pull-up resistor to VCCAUX always active during configuration, regardless of HSWAP_EN pin)		
TCK	Input	**JTAG Test Clock:** The TCK clock signal synchronizes all JTAG port operations. This pin has an internal pull-up resistor to VCCAUX during configuration.

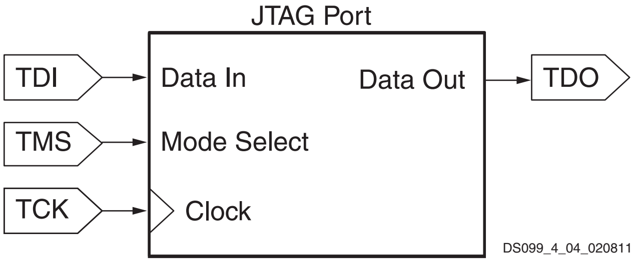


Figure 43: **JTAG Port**

IDCODE Register

Spartan-3 FPGAs contain a 32-bit identification register called the IDCODE register, as defined in the IEEE 1149.1 JTAG standard. The fixed value electrically identifies the manufacture (Xilinx) and the type of device being addressed over a JTAG chain. This register allows the JTAG host to identify the device being tested or programmed via JTAG. See Table 78.

Using JTAG Port After Configuration

The JTAG port is always active and available before, during, and after FPGA configuration. Add the BSCAN_SPARTAN3 primitive to the design to create user-defined JTAG instructions and JTAG chains to communicate with internal logic.

Furthermore, the contents of the User ID register within the JTAG port can be specified as a Bitstream Generation option. By default, the 32-bit User ID register contains `0xFFFFFFFF`.

Table 78: **Spartan-3 JTAG IDCODE Register Values (hexadecimal)**

Part Number	IDCODE Register
XC3S50	`0x0140C093`
XC3S200	`0x01414093`
XC3S400	`0x0141C093`
XC3S1000	`0x01428093`
XC3S1500	`0x01434093`
XC3S2000	`0x01440093`
XC3S4000	`0x01448093`
XC3S5000	`0x01450093`

Precautions When Using the JTAG Port in 3.3V Environments

The JTAG port is powered by the +2.5V VCCAUX power supply. When connecting to a 3.3V interface, the JTAG input pins must be current-limited using a series resistor. Similarly, the TDO pin is a CMOS output powered from +2.5V. The TDO output can directly drive a 3.3V input but with reduced noise immunity. See 3.3V-Tolerant Configuration Interface, page 47. See also XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional details.

The following interface precautions are recommended when connecting the JTAG port to a 3.3V interface.

- Avoid actively driving the JTAG input signals High with 3.3V signal levels. If required in the application, use series current-limiting resistors to keep the current below 10 mA per pin.
- If possible, drive the FPGA JTAG inputs with drivers that can be placed in high-impedance (Hi-Z) after using the JTAG port. Alternatively, drive the FPGA JTAG inputs with open-drain outputs, which only drive Low. In both cases, pull-up resistors are required. The FPGA JTAG pins have pull-up resistors to VCCAUX before configuration and optional pull-up resistors after configuration, controlled by Bitstream Options, page 125.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx website at the specified location in Table 83.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx website for each package.

Table 83: **Xilinx Package Mechanical Drawings**

Package	Web Link (URL)
VQ100 and VQG100	http://www.xilinx.com/support/documentation/package_specs/vq100.pdf
CP132 and CPG132(1)	http://www.xilinx.com/support/documentation/package_specs/cp132.pdf
TQ144 and TQG144	http://www.xilinx.com/support/documentation/package_specs/tq144.pdf
PQ208 and PQG208	http://www.xilinx.com/support/documentation/package_specs/pq208.pdf
FT256 and FTG256	http://www.xilinx.com/support/documentation/package_specs/ft256.pdf
FG320 and FGG320	http://www.xilinx.com/support/documentation/package_specs/fg320.pdf
FG456 and FGG456	http://www.xilinx.com/support/documentation/package_specs/fg456.pdf
FG676 and FGG676	http://www.xilinx.com/support/documentation/package_specs/fg676.pdf
FG900 and FGG900	http://www.xilinx.com/support/documentation/package_specs/fg900.pdf
FG1156 and FGG1156(1)	http://www.xilinx.com/support/documentation/package_specs/fg1156.pdf

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Power, Ground, and I/O by Package

Each package has three separate voltage supply inputs—VCCINT, VCCAUX, and VCCO—and a common ground return, GND. The numbers of pins dedicated to these functions varies by package, as shown in Table 84.

Table 84: **Power and Ground Supply Pins by Package**

Package	VCCINT	VCCAUX	VCCO	GND
VQ100	4	4	8	10
CP132(1)	4	4	12	12
TQ144	4	4	12	16
PQ208	4	8	12	28
FT256	8	8	24	32
FG320	12	8	28	40
FG456	12	8	40	52
FG676	20	16	64	76
FG900	32	24	80	120
FG1156(1)	40	32	104	184

Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

A majority of package pins are user-defined I/O pins. However, the numbers and characteristics of these I/O depends on the device type and the package in which it is available, as shown in Table 85. The table shows the maximum number of single-ended I/O pins available, assuming that all I/O-, DUAL-, DCI-, VREF-, and GCLK-type pins are used as general-purpose I/O. Likewise, the table shows the maximum number of differential pin-pairs available on the package. Finally, the table shows how the total maximum user I/Os are distributed by pin type, including the number of unconnected—i.e., N.C.—pins on the device.

Table 85: **Maximum User I/Os by Package**

Device	Package	Maximum User I/Os	Maximum Differential Pairs	All Possible I/O Pins by Type					N.C.
				I/O	DUAL	DCI	VREF	GCLK	
XC3S50	VQ100	63	29	22	12	14	7	8	0
XC3S200	VQ100	63	29	22	12	14	7	8	0
XC3S50	CP132[1]	89	44	44	12	14	11	8	0
XC3S50	TQ144	97	46	51	12	14	12	8	0
XC3S200	TQ144	97	46	51	12	14	12	8	0
XC3S400	TQ144	97	46	51	12	14	12	8	0
XC3S50	PQ208	124	56	72	12	16	16	8	17
XC3S200	PQ208	141	62	83	12	16	22	8	0
XC3S400	PQ208	141	62	83	12	16	22	8	0
XC3S200	FT256	173	76	113	12	16	24	8	0
XC3S400	FT256	173	76	113	12	16	24	8	0
XC3S1000	FT256	173	76	113	12	16	24	8	0
XC3S400	FG320	221	100	156	12	16	29	8	0
XC3S1000	FG320	221	100	156	12	16	29	8	0
XC3S1500	FG320	221	100	156	12	16	29	8	0
XC3S400	FG456	264	116	196	12	16	32	8	69
XC3S1000	FG456	333	149	261	12	16	36	8	0
XC3S1500	FG456	333	149	261	12	16	36	8	0
XC3S2000	FG456	333	149	261	12	16	36	8	0
XC3S1000	FG676	391	175	315	12	16	40	8	98
XC3S1500	FG676	487	221	403	12	16	48	8	2
XC3S2000	FG676	489	221	405	12	16	48	8	0
XC3S4000	FG676	489	221	405	12	16	48	8	0
XC3S5000	FG676	489	221	405	12	16	48	8	0
XC3S2000	FG900	565	270	481	12	16	48	8	68
XC3S4000	FG900	633	300	549	12	16	48	8	0
XC3S5000	FG900	633	300	549	12	16	48	8	0
XC3S4000	FG1156[1]	712	312	621	12	16	55	8	73
XC3S5000	FG1156[1]	784	344	692	12	16	56	8	1

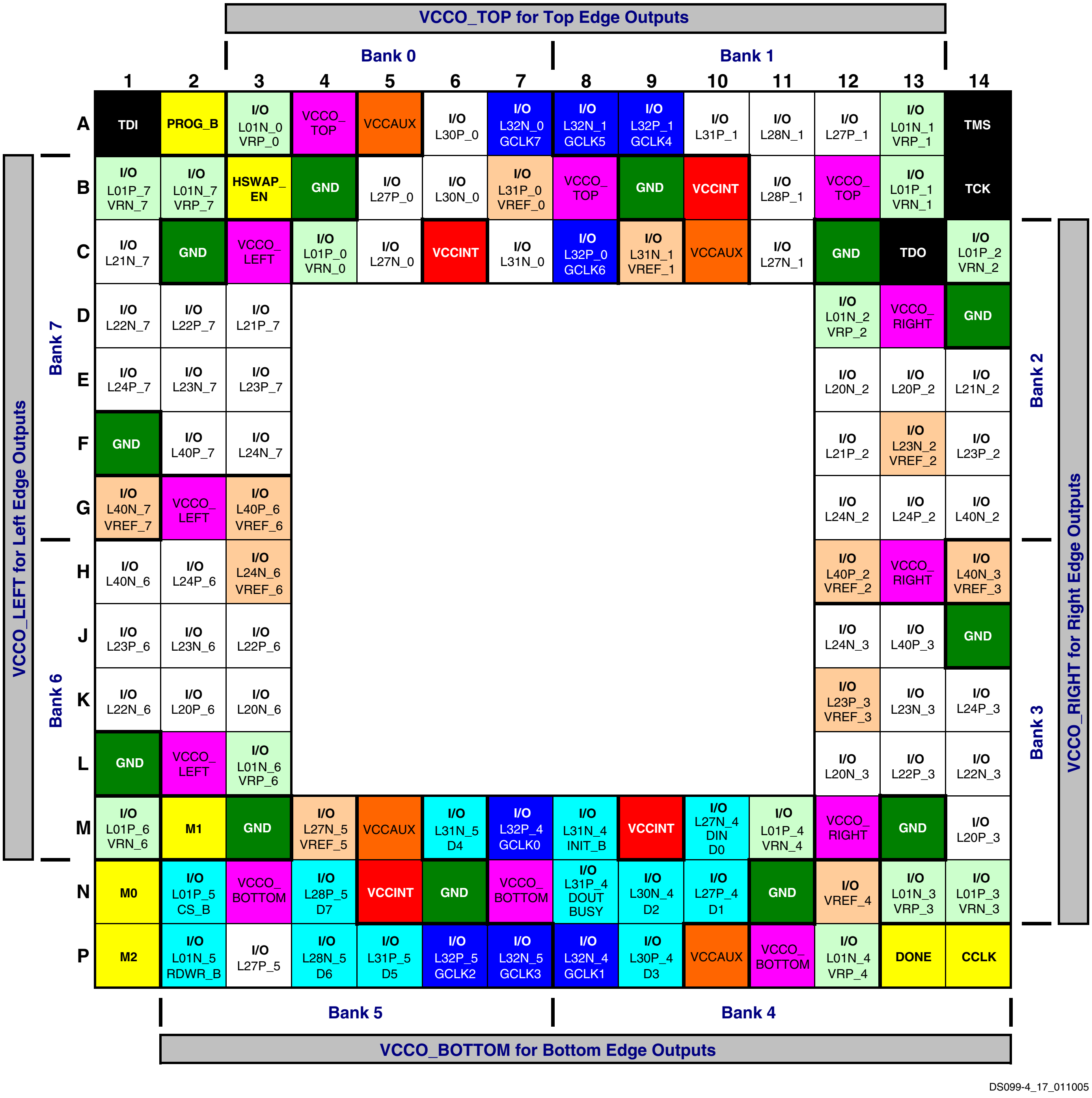
Notes:

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Electronic versions of the package pinout tables and footprints are available for download from the Xilinx website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs. Download the files from the following location:

http://www.xilinx.com/support/documentation/data_sheets/s3_pin.zip

CP132 Footprint



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	TDI	PROG_B	I/O L01N_0 VRP_0	VCCO_TOP	VCCAUX	I/O L30P_0	I/O L32N_0 GCLK7	I/O L32N_1 GCLK5	I/O L32P_1 GCLK4	I/O L31P_1	I/O L28N_1	I/O L27P_1	I/O L01N_1 VRP_1	TMS
B	I/O L01P_7 VRN_7	I/O L01N_7 VRP_7	HSWAP_EN	GND	I/O L27P_0	I/O L30N_0	I/O L31P_0 VREF_0	VCCO_TOP	GND	VCCINT	I/O L28P_1	VCCO_TOP	I/O L01P_1 VRN_1	TCK
C	I/O L21N_7	GND	VCCO_LEFT	I/O L01P_0 VRN_0	I/O L27N_0	VCCINT	I/O L31N_0	I/O L32P_0 GCLK6	I/O L31N_1 VREF_1	VCCAUX	I/O L27N_1	GND	TDO	I/O L01P_2 VRN_2
D	I/O L22N_7	I/O L22P_7	I/O L21P_7									I/O L01N_2 VRP_2	VCCO_RIGHT	GND
E	I/O L24P_7	I/O L23N_7	I/O L23P_7									I/O L20N_2	I/O L20P_2	I/O L21N_2
F	GND	I/O L40P_7	I/O L24N_7									I/O L21P_2	I/O L23N_2 VREF_2	I/O L23P_2
G	I/O L40N_7 VREF_7	VCCO_LEFT	I/O L40P_6 VREF_6									I/O L24N_2	I/O L24P_2	I/O L40N_2
H	I/O L40N_6	I/O L24P_6	I/O L24N_6 VREF_6									I/O L40P_2 VREF_2	VCCO_RIGHT	I/O L40N_3 VREF_3
J	I/O L23P_6	I/O L23N_6	I/O L22P_6									I/O L24N_3	I/O L40P_3	GND
K	I/O L22N_6	I/O L20P_6	I/O L20N_6									I/O L23P_3 VREF_3	I/O L23N_3	I/O L24P_3
L	GND	VCCO_LEFT	I/O L01N_6 VRP_6									I/O L20N_3	I/O L22P_3	I/O L22N_3
M	I/O L01P_6 VRN_6	M1	GND	I/O L27N_5 VREF_5	VCCAUX	I/O L31N_5 D4	I/O L32P_4 GCLK0	I/O L31N_4 INIT_B	VCCINT	I/O L27N_4 DIN D0	I/O L01P_4 VRN_4	VCCO_RIGHT	GND	I/O L20P_3
N	M0	I/O L01P_5 CS_B	VCCO_BOTTOM	I/O L28P_5 D7	VCCINT	GND	VCCO_BOTTOM	I/O L31P_4 DOUT BUSY	I/O L30N_4 D2	I/O L27P_4 D1	GND	I/O VREF_4	I/O L01N_3 VRP_3	I/O L01P_3 VRN_3
P	M2	I/O L01N_5 RDWR_B	I/O L27P_5	I/O L28N_5 D6	I/O L31P_5 D5	I/O L32P_5 GCLK2	I/O L32N_5 GCLK3	I/O L32N_4 GCLK1	I/O L30P_4 D3	VCCAUX	VCCO_BOTTOM	I/O L01N_4 VRP_4	DONE	CCLK

Figure 45: **CP132 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

44	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	11	**VREF:** User I/O or input voltage reference for bank
14	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O, input, or global buffer input	12	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	12	**GND:** Ground	4	**VCCAUX:** Auxiliary voltage supply (+2.5V)

TQ144 Footprint

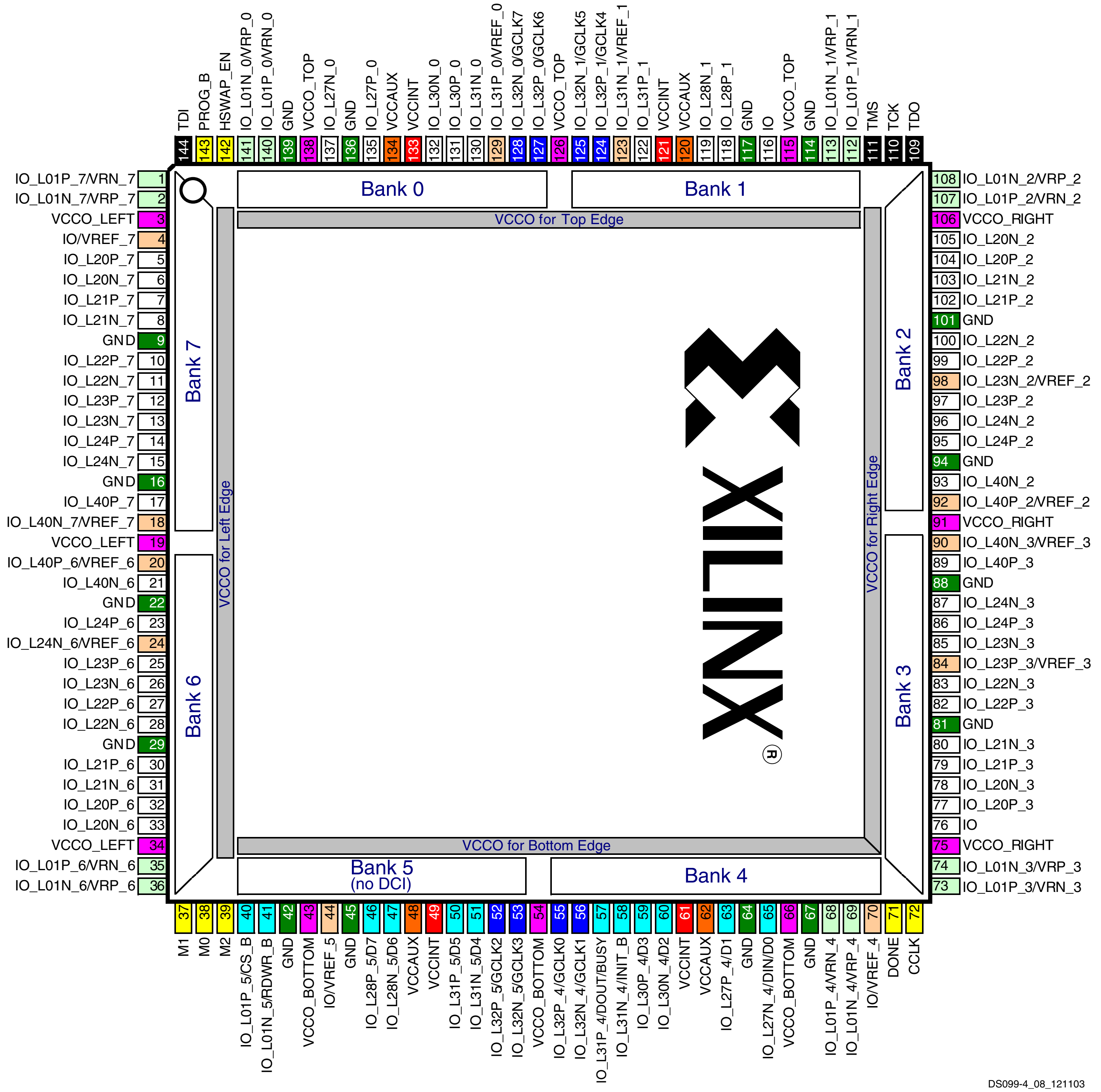


Figure 46: **TQ144 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

51	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	12	**VREF:** User I/O or input voltage reference for bank
14	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input	12	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	16	**GND:** Ground	4	**VCCAUX:** Auxiliary voltage supply (+2.5V)

Table 93: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	P166	VREF
1	IO_L10P_1	IO_L10P_1	P165	I/O
1	IO_L27N_1	IO_L27N_1	P169	I/O
1	IO_L27P_1	IO_L27P_1	P168	I/O
1	IO_L28N_1	IO_L28N_1	P172	I/O
1	IO_L28P_1	IO_L28P_1	P171	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	P178	VREF
1	IO_L31P_1	IO_L31P_1	P176	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	P181	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	P180	GCLK
1	VCCO_1	VCCO_1	P164	VCCO
1	VCCO_1	VCCO_1	P177	VCCO
2	N.C. (◆)	IO/VREF_2	P154	VREF
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	P156	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	P155	DCI
2	IO_L19N_2	IO_L19N_2	P152	I/O
2	IO_L19P_2	IO_L19P_2	P150	I/O
2	IO_L20N_2	IO_L20N_2	P149	I/O
2	IO_L20P_2	IO_L20P_2	P148	I/O
2	IO_L21N_2	IO_L21N_2	P147	I/O
2	IO_L21P_2	IO_L21P_2	P146	I/O
2	IO_L22N_2	IO_L22N_2	P144	I/O
2	IO_L22P_2	IO_L22P_2	P143	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	P141	VREF
2	IO_L23P_2	IO_L23P_2	P140	I/O
2	IO_L24N_2	IO_L24N_2	P139	I/O
2	IO_L24P_2	IO_L24P_2	P138	I/O
2	N.C. (◆)	IO_L39N_2	P137	I/O
2	N.C. (◆)	IO_L39P_2	P135	I/O
2	IO_L40N_2	IO_L40N_2	P133	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	P132	VREF
2	VCCO_2	VCCO_2	P136	VCCO
2	VCCO_2	VCCO_2	P153	VCCO
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	P107	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	P106	DCI
3	N.C. (◆)	IO_L17N_3	P109	I/O
3	N.C. (◆)	IO_L17P_3/VREF_3	P108	VREF
3	IO_L19N_3	IO_L19N_3	P113	I/O
3	IO_L19P_3	IO_L19P_3	P111	I/O
3	IO_L20N_3	IO_L20N_3	P115	I/O

User I/Os by Bank

Table 94 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S50 in the PQ208 package. Similarly, Table 95 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S200 and XC3S400 in the PQ208 package.

Table 94: **User I/Os Per Bank for XC3S50 in PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	15	9	0	2	2	2
	1	15	9	0	2	2	2
Right	2	16	13	0	2	2	0
	3	16	12	0	2	2	0
Bottom	4	15	3	6	2	2	2
	5	15	3	6	2	2	2
Left	6	16	12	0	2	2	0
	7	16	12	0	2	2	0

Table 95: **User I/Os Per Bank for XC3S200 and XC3S400 in PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	16	9	0	2	3	2
	1	15	9	0	2	2	2
Right	2	19	14	0	2	3	0
	3	20	15	0	2	3	0
Bottom	4	17	4	6	2	3	2
	5	15	3	6	2	2	2
Left	6	19	14	0	2	3	0
	7	20	15	0	2	3	0

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
2	IO_L20N_2	E17	I/O
2	IO_L20P_2	E18	I/O
2	IO_L21N_2	F15	I/O
2	IO_L21P_2	E15	I/O
2	IO_L22N_2	F14	I/O
2	IO_L22P_2	G14	I/O
2	IO_L23N_2/VREF_2	G18	VREF
2	IO_L23P_2	F17	I/O
2	IO_L24N_2	G15	I/O
2	IO_L24P_2	G16	I/O
2	IO_L27N_2	H13	I/O
2	IO_L27P_2	H14	I/O
2	IO_L34N_2/VREF_2	H16	VREF
2	IO_L34P_2	H15	I/O
2	IO_L35N_2	H17	I/O
2	IO_L35P_2	H18	I/O
2	IO_L39N_2	J18	I/O
2	IO_L39P_2	J17	I/O
2	IO_L40N_2	J15	I/O
2	IO_L40P_2/VREF_2	J14	VREF
2	VCCO_2	F16	VCCO
2	VCCO_2	H12	VCCO
2	VCCO_2	J12	VCCO
3	IO	K15	I/O
3	IO_L01N_3/VRP_3	T17	DCI
3	IO_L01P_3/VRN_3	T16	DCI
3	IO_L16N_3	T18	I/O
3	IO_L16P_3	U18	I/O
3	IO_L17N_3	P16	I/O
3	IO_L17P_3/VREF_3	R16	VREF
3	IO_L19N_3	R17	I/O
3	IO_L19P_3	R18	I/O
3	IO_L20N_3	P18	I/O
3	IO_L20P_3	P17	I/O
3	IO_L21N_3	P15	I/O
3	IO_L21P_3	N15	I/O
3	IO_L22N_3	M14	I/O
3	IO_L22P_3	N14	I/O
3	IO_L23N_3	M15	I/O
3	IO_L23P_3/VREF_3	M16	VREF

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
N/A	GND	GND	B21	GND
N/A	GND	GND	C9	GND
N/A	GND	GND	C14	GND
N/A	GND	GND	J3	GND
N/A	GND	GND	J9	GND
N/A	GND	GND	J10	GND
N/A	GND	GND	J11	GND
N/A	GND	GND	J12	GND
N/A	GND	GND	J13	GND
N/A	GND	GND	J14	GND
N/A	GND	GND	J20	GND
N/A	GND	GND	K9	GND
N/A	GND	GND	K10	GND
N/A	GND	GND	K11	GND
N/A	GND	GND	K12	GND
N/A	GND	GND	K13	GND
N/A	GND	GND	K14	GND
N/A	GND	GND	L9	GND
N/A	GND	GND	L10	GND
N/A	GND	GND	L11	GND
N/A	GND	GND	L12	GND
N/A	GND	GND	L13	GND
N/A	GND	GND	L14	GND
N/A	GND	GND	M9	GND
N/A	GND	GND	M10	GND
N/A	GND	GND	M11	GND
N/A	GND	GND	M12	GND
N/A	GND	GND	M13	GND
N/A	GND	GND	M14	GND
N/A	GND	GND	N9	GND
N/A	GND	GND	N10	GND
N/A	GND	GND	N11	GND
N/A	GND	GND	N12	GND
N/A	GND	GND	N13	GND
N/A	GND	GND	N14	GND
N/A	GND	GND	P3	GND
N/A	GND	GND	P9	GND
N/A	GND	GND	P10	GND
N/A	GND	GND	P11	GND
N/A	GND	GND	P12	GND

Table 103: **FG676 Package Pinout *(Cont'd)***

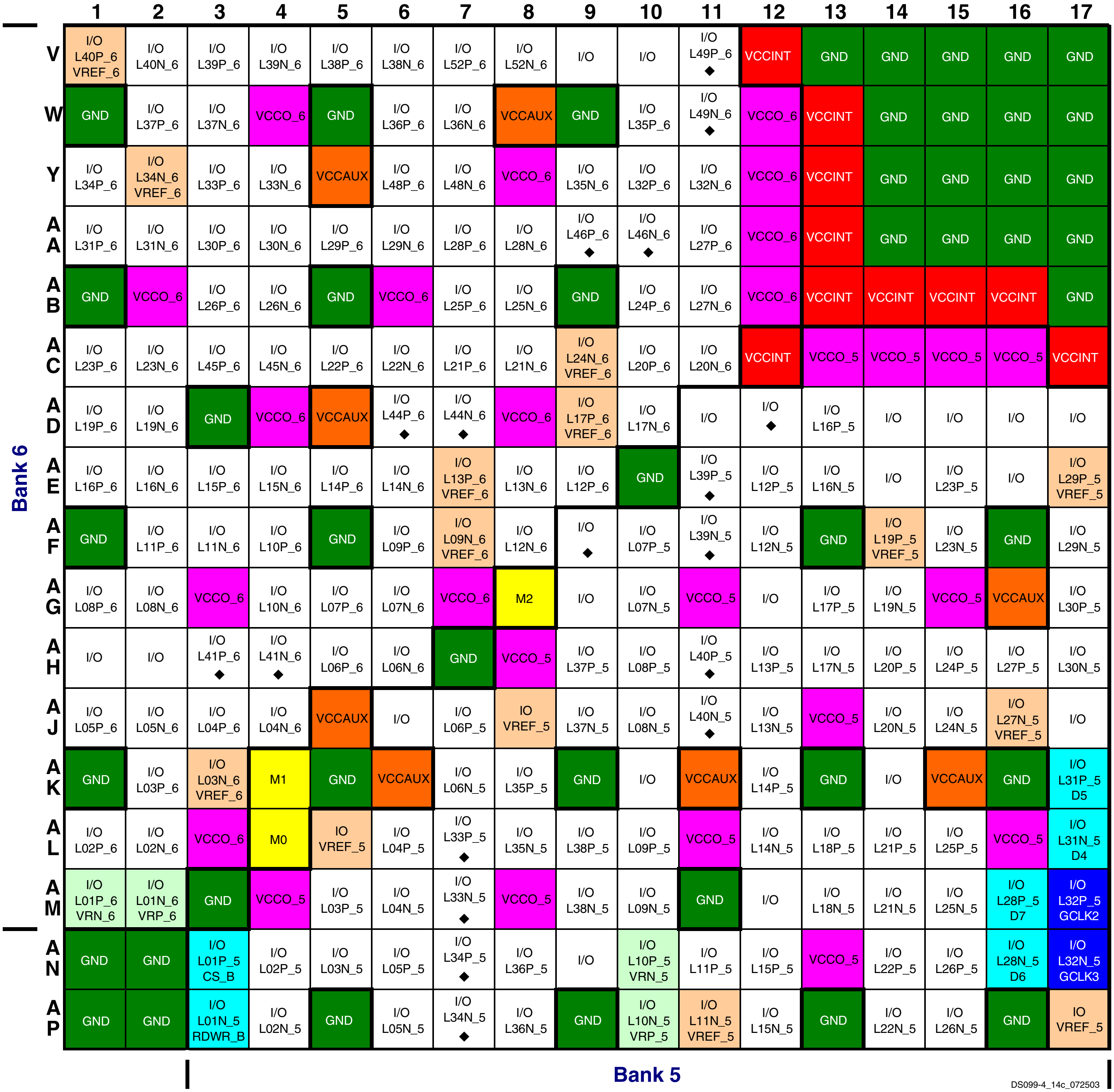
Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
2	N.C. (◆)	IO_L06N_2	IO_L06N_2	IO_L06N_2	IO_L06N_2	G20	I/O
2	N.C. (◆)	IO_L06P_2	IO_L06P_2	IO_L06P_2	IO_L06P_2	G21	I/O
2	N.C. (◆)	IO_L07N_2	IO_L07N_2	IO_L07N_2	IO_L07N_2	F23	I/O
2	N.C. (◆)	IO_L07P_2	IO_L07P_2	IO_L07P_2	IO_L07P_2	F24	I/O
2	N.C. (◆)	IO_L08N_2	IO_L08N_2	IO_L08N_2	IO_L08N_2	G22	I/O
2	N.C. (◆)	IO_L08P_2	IO_L08P_2	IO_L08P_2	IO_L08P_2	G23	I/O
2	N.C. (◆)	IO_L09N_2/VREF_2(1)	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	F25	VREF(1)
2	N.C. (◆)	IO_L09P_2	IO_L09P_2	IO_L09P_2	IO_L09P_2	F26	I/O
2	N.C. (◆)	IO_L10N_2	IO_L10N_2	IO_L10N_2	IO_L10N_2	G25	I/O
2	N.C. (◆)	IO_L10P_2	IO_L10P_2	IO_L10P_2	IO_L10P_2	G26	I/O
2	IO_L14N_2	IO_L14N_2	IO_L14N_2(2)	IO_L11N_2(2)	IO_L11N_2	H20	I/O
2	IO_L14P_2	IO_L14P_2	IO_L14P_2(2)	IO_L11P_2(2)	IO_L11P_2	H21	I/O
2	IO_L16N_2	IO_L16N_2	IO_L16N_2(2)	IO_L12N_2(2)	IO_L12N_2	H22	I/O
2	IO_L16P_2	IO_L16P_2	IO_L16P_2(2)	IO_L12P_2(2)	IO_L12P_2	J21	I/O
2	IO_L17N_2	IO_L17N_2	IO_L17N_2(2)	IO_L13N_2(2)	IO(3)	H23	I/O
2	IO_L17P_2/VREF_2	IO_L17P_2/VREF_2	IO_L17P_2(2)/VREF_2	IO_L13P_2(2)/VREF_2	IO/VREF_2(3)	H24	VREF
2	IO_L19N_2	IO_L19N_2	IO_L19N_2	IO_L19N_2	IO_L19N_2	H25	I/O
2	IO_L19P_2	IO_L19P_2	IO_L19P_2	IO_L19P_2	IO_L19P_2	H26	I/O
2	IO_L20N_2	IO_L20N_2	IO_L20N_2	IO_L20N_2	IO_L20N_2	J20	I/O
2	IO_L20P_2	IO_L20P_2	IO_L20P_2	IO_L20P_2	IO_L20P_2	K20	I/O
2	IO_L21N_2	IO_L21N_2	IO_L21N_2	IO_L21N_2	IO_L21N_2	J22	I/O
2	IO_L21P_2	IO_L21P_2	IO_L21P_2	IO_L21P_2	IO_L21P_2	J23	I/O
2	IO_L22N_2	IO_L22N_2	IO_L22N_2	IO_L22N_2	IO_L22N_2	J24	I/O
2	IO_L22P_2	IO_L22P_2	IO_L22P_2	IO_L22P_2	IO_L22P_2	J25	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	K21	VREF
2	IO_L23P_2	IO_L23P_2	IO_L23P_2	IO_L23P_2	IO_L23P_2	K22	I/O
2	IO_L24N_2	IO_L24N_2	IO_L24N_2	IO_L24N_2	IO_L24N_2	K23	I/O
2	IO_L24P_2	IO_L24P_2	IO_L24P_2	IO_L24P_2	IO_L24P_2	K24	I/O
2	IO_L26N_2	IO_L26N_2	IO_L26N_2	IO_L26N_2	IO_L26N_2	K25	I/O
2	IO_L26P_2	IO_L26P_2	IO_L26P_2	IO_L26P_2	IO_L26P_2	K26	I/O
2	IO_L27N_2	IO_L27N_2	IO_L27N_2	IO_L27N_2	IO_L27N_2	L19	I/O
2	IO_L27P_2	IO_L27P_2	IO_L27P_2	IO_L27P_2	IO_L27P_2	L20	I/O
2	IO_L28N_2	IO_L28N_2	IO_L28N_2	IO_L28N_2	IO_L28N_2	L21	I/O
2	IO_L28P_2	IO_L28P_2	IO_L28P_2	IO_L28P_2	IO_L28P_2	L22	I/O
2	IO_L29N_2	IO_L29N_2	IO_L29N_2	IO_L29N_2	IO_L29N_2	L25	I/O
2	IO_L29P_2	IO_L29P_2	IO_L29P_2	IO_L29P_2	IO_L29P_2	L26	I/O
2	IO_L31N_2	IO_L31N_2	IO_L31N_2	IO_L31N_2	IO_L31N_2	M19	I/O
2	IO_L31P_2	IO_L31P_2	IO_L31P_2	IO_L31P_2	IO_L31P_2	M20	I/O
2	IO_L32N_2	IO_L32N_2	IO_L32N_2	IO_L32N_2	IO_L32N_2	M21	I/O
2	IO_L32P_2	IO_L32P_2	IO_L32P_2	IO_L32P_2	IO_L32P_2	M22	I/O
2	IO_L33N_2	IO_L33N_2	IO_L33N_2	IO_L33N_2	IO_L33N_2	L23	I/O
2	IO_L33P_2	IO_L33P_2	IO_L33P_2	IO_L33P_2	IO_L33P_2	M24	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L24P_3	IO_L24P_3	AC26	I/O
3	IO_L26N_3	IO_L26N_3	AA28	I/O
3	IO_L26P_3	IO_L26P_3	AA27	I/O
3	IO_L27N_3	IO_L27N_3	AA30	I/O
3	IO_L27P_3	IO_L27P_3	AA29	I/O
3	IO_L28N_3	IO_L28N_3	AA32	I/O
3	IO_L28P_3	IO_L28P_3	AA31	I/O
3	IO_L29N_3	IO_L29N_3	AA34	I/O
3	IO_L29P_3	IO_L29P_3	AA33	I/O
3	IO_L30N_3	IO_L30N_3	Y29	I/O
3	IO_L30P_3	IO_L30P_3	Y28	I/O
3	IO_L31N_3	IO_L31N_3	Y32	I/O
3	IO_L31P_3	IO_L31P_3	Y31	I/O
3	IO_L32N_3	IO_L32N_3	Y34	I/O
3	IO_L32P_3	IO_L32P_3	Y33	I/O
3	IO_L33N_3	IO_L33N_3	W25	I/O
3	IO_L33P_3	IO_L33P_3	Y26	I/O
3	IO_L34N_3	IO_L34N_3	W29	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	W28	VREF
3	IO_L35N_3	IO_L35N_3	W33	I/O
3	IO_L35P_3	IO_L35P_3	W32	I/O
3	IO_L37N_3	IO_L37N_3	V28	I/O
3	IO_L37P_3	IO_L37P_3	V27	I/O
3	IO_L38N_3	IO_L38N_3	V30	I/O
3	IO_L38P_3	IO_L38P_3	V29	I/O
3	IO_L39N_3	IO_L39N_3	V32	I/O
3	IO_L39P_3	IO_L39P_3	V31	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	V34	VREF
3	IO_L40P_3	IO_L40P_3	V33	I/O
3	N.C. (◆)	IO_L41N_3	AH32	I/O
3	N.C. (◆)	IO_L41P_3	AH31	I/O
3	N.C. (◆)	IO_L44N_3	AD29	I/O
3	N.C. (◆)	IO_L44P_3	AD28	I/O
3	IO_L45N_3	IO_L45N_3	AC34	I/O
3	IO_L45P_3	IO_L45P_3	AC33	I/O
3	IO_L46N_3	IO_L46N_3	AB28	I/O
3	IO_L46P_3	IO_L46P_3	AB27	I/O
3	IO_L47N_3	IO_L47N_3	AB32	I/O
3	IO_L47P_3	IO_L47P_3	AB31	I/O
3	IO_L48N_3	IO_L48N_3	AA24	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
5	IO_L24P_5	IO_L24P_5	AH15	I/O
5	IO_L25N_5	IO_L25N_5	AM15	I/O
5	IO_L25P_5	IO_L25P_5	AL15	I/O
5	IO_L26N_5	IO_L26N_5	AP15	I/O
5	IO_L26P_5	IO_L26P_5	AN15	I/O
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	AJ16	VREF
5	IO_L27P_5	IO_L27P_5	AH16	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	AN16	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	AM16	DUAL
5	IO_L29N_5	IO_L29N_5	AF17	I/O
5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	AE17	VREF
5	IO_L30N_5	IO_L30N_5	AH17	I/O
5	IO_L30P_5	IO_L30P_5	AG17	I/O
5	IO_L31N_5/D4	IO_L31N_5/D4	AL17	DUAL
5	IO_L31P_5/D5	IO_L31P_5/D5	AK17	DUAL
5	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	AN17	GCLK
5	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	AM17	GCLK
5	N.C. (◆)	IO_L33N_5	AM7	I/O
5	N.C. (◆)	IO_L33P_5	AL7	I/O
5	N.C. (◆)	IO_L34N_5	AP7	I/O
5	N.C. (◆)	IO_L34P_5	AN7	I/O
5	IO_L35N_5	IO_L35N_5	AL8	I/O
5	IO_L35P_5	IO_L35P_5	AK8	I/O
5	IO_L36N_5	IO_L36N_5	AP8	I/O
5	IO_L36P_5	IO_L36P_5	AN8	I/O
5	IO_L37N_5	IO_L37N_5	AJ9	I/O
5	IO_L37P_5	IO_L37P_5	AH9	I/O
5	IO_L38N_5	IO_L38N_5	AM9	I/O
5	IO_L38P_5	IO_L38P_5	AL9	I/O
5	N.C. (◆)	IO_L39N_5	AF11	I/O
5	N.C. (◆)	IO_L39P_5	AE11	I/O
5	N.C. (◆)	IO_L40N_5	AJ11	I/O
5	N.C. (◆)	IO_L40P_5	AH11	I/O
5	VCCO_5	VCCO_5	AC13	VCCO
5	VCCO_5	VCCO_5	AC14	VCCO
5	VCCO_5	VCCO_5	AC15	VCCO
5	VCCO_5	VCCO_5	AC16	VCCO
5	VCCO_5	VCCO_5	AG11	VCCO
5	VCCO_5	VCCO_5	AG15	VCCO
5	VCCO_5	VCCO_5	AH8	VCCO



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
V	I/O L40P_6 VREF_6	I/O L40N_6	I/O L39P_6	I/O L39N_6	I/O L38P_6	I/O L38N_6	I/O L52P_6	I/O L52N_6	I/O	I/O	I/O L49P_6 ◆	VCCINT	GND	GND	GND	GND	GND
W	GND	I/O L37P_6	I/O L37N_6	VCCO_6	GND	I/O L36P_6	I/O L36N_6	VCCAUX	GND	I/O L35P_6	I/O L49N_6 ◆	VCCO_6	VCCINT	GND	GND	GND	GND
Y	I/O L34P_6	I/O L34N_6 VREF_6	I/O L33P_6	I/O L33N_6	VCCAUX	I/O L48P_6	I/O L48N_6	VCCO_6	I/O L35N_6	I/O L32P_6	I/O L32N_6	VCCO_6	VCCINT	GND	GND	GND	GND
AA	I/O L31P_6	I/O L31N_6	I/O L30P_6	I/O L30N_6	I/O L29P_6	I/O L29N_6	I/O L28P_6	I/O L28N_6	I/O L46P_6 ◆	I/O L46N_6 ◆	I/O L27P_6	VCCO_6	VCCINT	GND	GND	GND	GND
AB	GND	VCCO_6	I/O L26P_6	I/O L26N_6	GND	VCCO_6	I/O L25P_6	I/O L25N_6	GND	I/O L24P_6	I/O L27N_6	VCCO_6	VCCINT	VCCINT	VCCINT	VCCINT	GND
AC	I/O L23P_6	I/O L23N_6	I/O L45P_6	I/O L45N_6	I/O L22P_6	I/O L22N_6	I/O L21P_6	I/O L21N_6	I/O L24N_6 VREF_6	I/O L20P_6	I/O L20N_6	VCCINT	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCINT
AD	I/O L19P_6	I/O L19N_6	GND	VCCO_6	VCCAUX	I/O L44P_6 ◆	I/O L44N_6 ◆	VCCO_6	I/O L17P_6 VREF_6	I/O L17N_6	I/O	I/O ◆	I/O L16P_5	I/O	I/O	I/O	I/O
AE	I/O L16P_6	I/O L16N_6	I/O L15P_6	I/O L15N_6	I/O L14P_6	I/O L14N_6	I/O L13P_6 VREF_6	I/O L13N_6	I/O L12P_6	GND	I/O L39P_5 ◆	I/O L12P_5	I/O L16N_5	I/O	I/O L23P_5	I/O	I/O L29P_5 VREF_5
AF	GND	I/O L11P_6	I/O L11N_6	I/O L10P_6	GND	I/O L09P_6	I/O L09N_6 VREF_6	I/O L12N_6	I/O ◆	I/O L07P_5	I/O L39N_5 ◆	I/O L12N_5	GND	I/O L19P_5 VREF_5	I/O L23N_5	GND	I/O L29N_5
AG	I/O L08P_6	I/O L08N_6	VCCO_6	I/O L10N_6	I/O L07P_6	I/O L07N_6	VCCO_6	M2	I/O	I/O L07N_5	VCCO_5	I/O	I/O L17P_5	I/O L19N_5	VCCO_5	VCCAUX	I/O L30P_5
AH	I/O	I/O	I/O L41P_6 ◆	I/O L41N_6 ◆	I/O L06P_6	I/O L06N_6	GND	VCCO_5	I/O L37P_5	I/O L08P_5	I/O L40P_5 ◆	I/O L13P_5	I/O L17N_5	I/O L20P_5	I/O L24P_5	I/O L27P_5	I/O L30N_5
AJ	I/O L05P_6	I/O L05N_6	I/O L04P_6	I/O L04N_6	VCCAUX	I/O	I/O L06P_5	IO VREF_5	I/O L37N_5	I/O L08N_5	I/O L40N_5 ◆	I/O L13N_5	VCCO_5	I/O L20N_5	I/O L24N_5	I/O L27N_5 VREF_5	I/O
AK	GND	I/O L03P_6	I/O L03N_6 VREF_6	M1	GND	VCCAUX	I/O L06N_5	I/O L35P_5	GND	I/O	VCCAUX	I/O L14P_5	GND	I/O	VCCAUX	GND	I/O L31P_5 D5
AL	I/O L02P_6	I/O L02N_6	VCCO_6	M0	IO VREF_5	I/O L04P_5	I/O L33P_5 ◆	I/O L35N_5	I/O L38P_5	I/O L09P_5	VCCO_5	I/O L14N_5	I/O L18P_5	I/O L21P_5	I/O L25P_5	VCCO_5	I/O L31N_5 D4
AM	I/O L01P_6 VRN_6	I/O L01N_6 VRP_6	GND	VCCO_5	I/O L03P_5	I/O L04N_5	I/O L33N_5 ◆	VCCO_5	I/O L38N_5	I/O L09N_5	GND	I/O	I/O L18N_5	I/O L21N_5	I/O L25N_5	I/O L28P_5 D7	I/O L32P_5 GCLK2
AN	GND	GND	I/O L01P_5 CS_B	I/O L02P_5	I/O L03N_5	I/O L05P_5	I/O L34P_5 ◆	I/O L36P_5	I/O	I/O L10P_5 VRN_5	I/O L11P_5	I/O L15P_5	VCCO_5	I/O L22P_5	I/O L26P_5	I/O L28N_5 D6	I/O L32N_5 GCLK3
AP	GND	GND	I/O L01N_5 RDWR_B	I/O L02N_5	GND	I/O L05N_5	I/O L34N_5 ◆	I/O L36N_5	GND	I/O L10N_5 VRP_5	I/O L11N_5 VREF_5	I/O L15N_5	GND	I/O L22N_5	I/O L26N_5	GND	IO VREF_5

Bottom Left Corner of FG1156 Package (Top View)

Figure 59: FG1156 Package Footprint (Top View) Continued