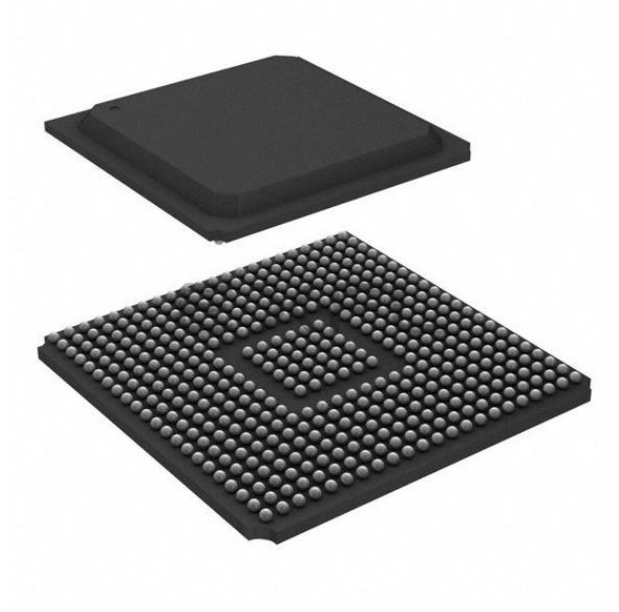
AMD Xilinx - XC3S2000-4FG456C Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	5120
Number of Logic Elements/Cells	46080
Total RAM Bits	737280
Number of I/O	333
Number of Gates	2000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s2000-4fg456c

According to Figure 7, the clock line OTCLK1 connects the CK inputs of the upper registers on the output and three-state paths. Similarly, OTCLK2 connects the CK inputs for the lower registers on the output and three-state paths. The upper and lower registers on the input path have independent clock lines: ICLK1 and ICLK2. The enable line OCE connects the CE inputs of the upper and lower registers on the output path. Similarly, TCE connects the CE inputs for the register pair on the three-state path and ICE does the same for the register pair on the input path. The Set/Reset (SR) line entering the IOB is common to all six registers, as is the Reverse (REV) line.

Each storage element supports numerous options in addition to the control over signal polarity described in the IOB Overview section. These are described in Table 6.

Table 6: **Storage Element Options**

Option Switch	Function	Specificity
FF/Latch	Chooses between an edge-sensitive flip-flop or a level-sensitive latch	Independent for each storage element.
SYNC/ASYNC	Determines whether SR is synchronous or asynchronous	Independent for each storage element.
SRHIGH/SRLOW	Determines whether SR acts as a Set, which forces the storage element to a logic “1" (SRHIGH) or a Reset, which forces a logic “0” (SRLOW).	Independent for each storage element, except when using FDDR. In the latter case, the selection for the upper element (OFF1 or TFF2) applies to both elements.
INIT1/INIT0	In the event of a Global Set/Reset, after configuration or upon activation of the GSR net, this switch decides whether to set or reset a storage element. By default, choosing SRLOW also selects INIT0; choosing SRHIGH also selects INIT1.	Independent for each storage element, except when using FDDR. In the latter case, selecting INIT0 for one element applies to both elements (even though INIT1 is selected for the other).

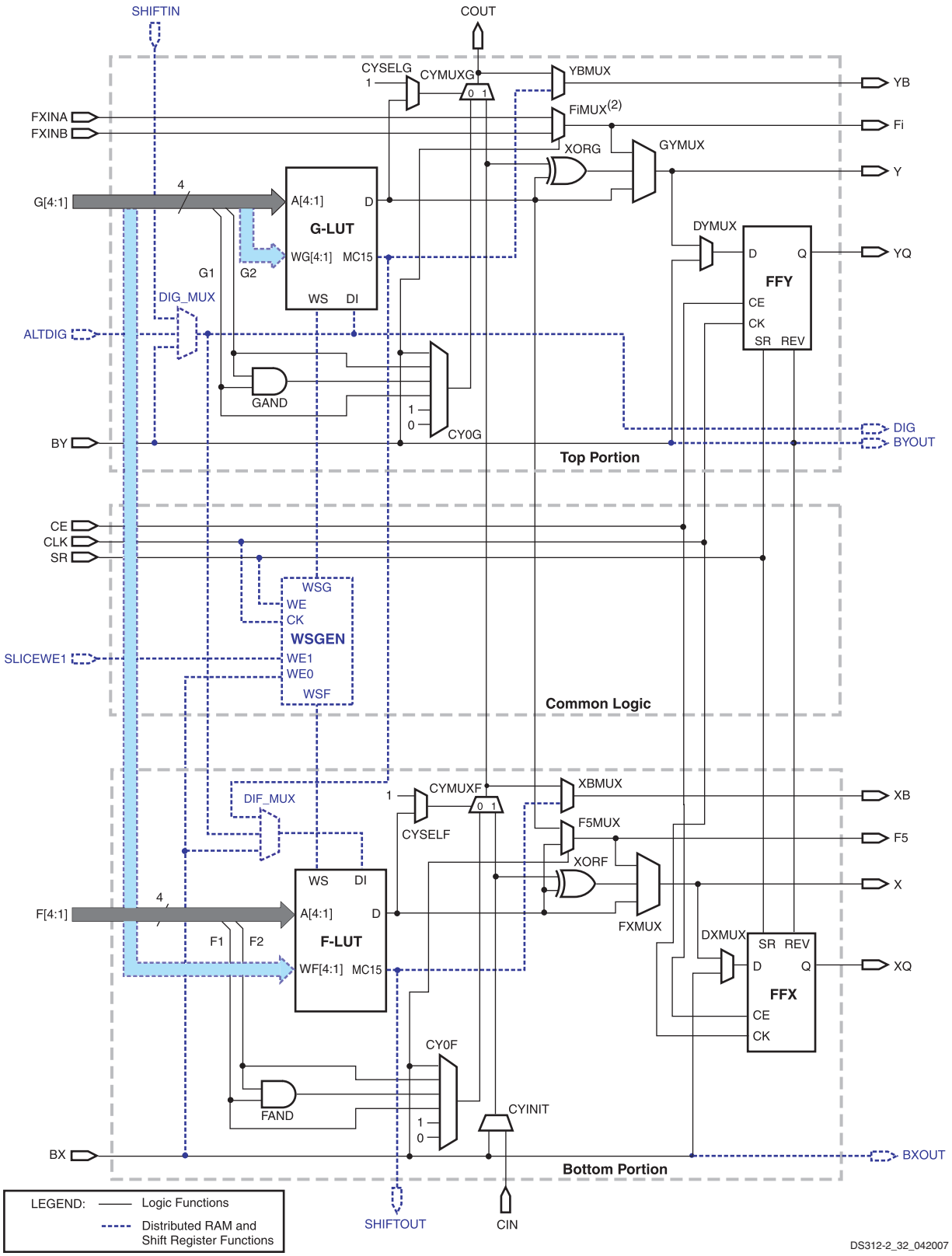
Double-Data-Rate Transmission

Double-Data-Rate (DDR) transmission describes the technique of synchronizing signals to both the rising and falling edges of the clock signal. Spartan-3 devices use register-pairs in all three IOB paths to perform DDR operations.

The pair of storage elements on the IOB’s Output path (OFF1 and OFF2), used as registers, combine with a special multiplexer to form a DDR D-type flip-flop (FDDR). This primitive permits DDR transmission where output data bits are synchronized to both the rising and falling edges of a clock. It is possible to access this function by placing either an FDDRRSE or an FDDRCPE component or symbol into the design. DDR operation requires two clock signals (50% duty cycle), one the inverted form of the other. These signals trigger the two registers in alternating fashion, as shown in Figure 8. Commonly, the Digital Clock Manager (DCM) generates the two clock signals by mirroring an incoming signal, then shifting it 180 degrees. This approach ensures minimal skew between the two signals.

The storage-element-pair on the Three-State path (TFF1 and TFF2) can also be combined with a local multiplexer to form an FDDR primitive. This permits synchronizing the output enable to both the rising and falling edges of a clock. This DDR operation is realized in the same way as for the output path.

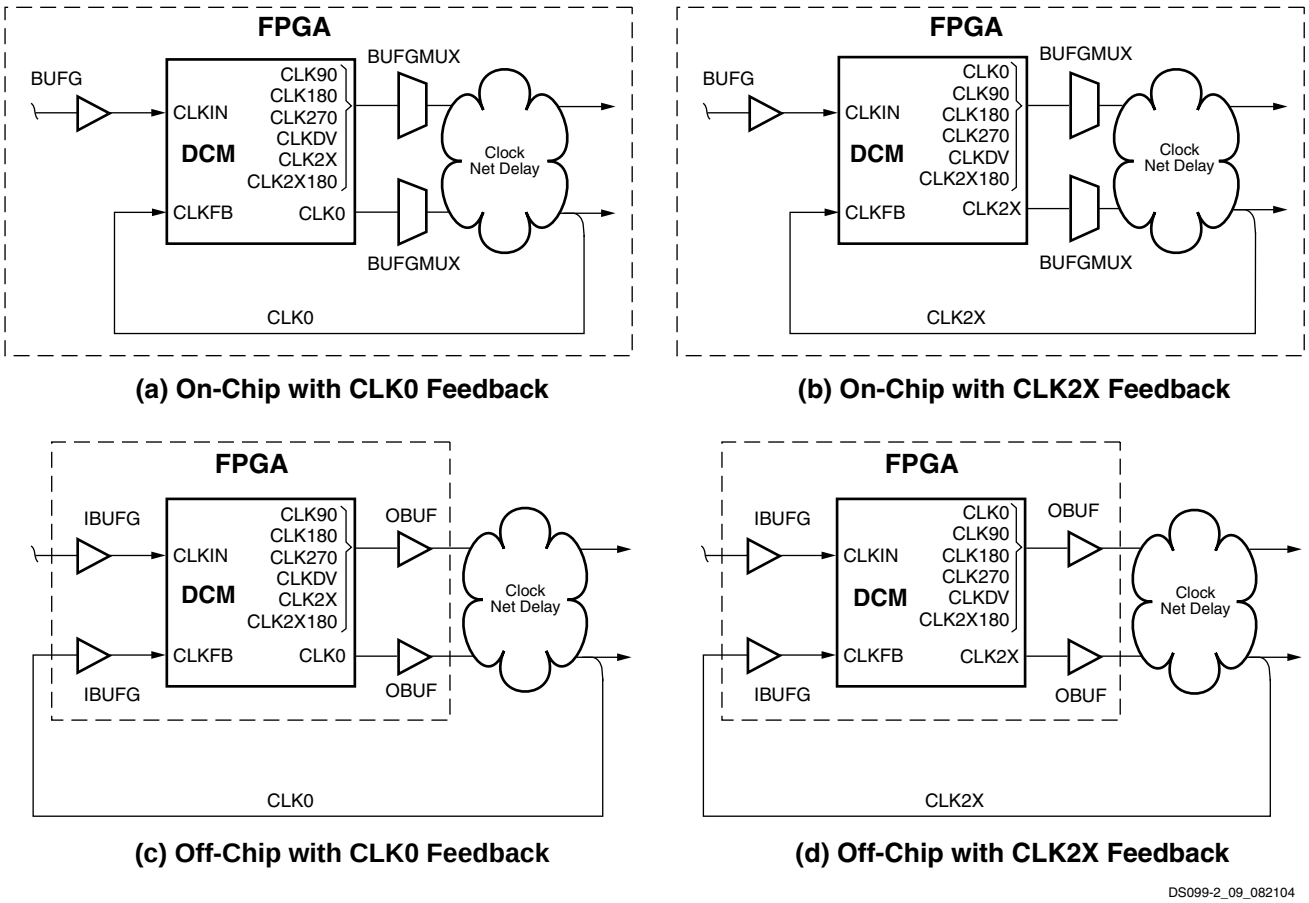
The storage-element-pair on the input path (IFF1 and IFF2) allows an I/O to receive a DDR signal. An incoming DDR clock signal triggers one register and the inverted clock signal triggers the other register. In this way, the registers take turns capturing bits of the incoming DDR data signal.



Notes:

1. Options to invert signal polarity as well as other options that enable lines for various functions are not shown.
2. The index i can be 6, 7, or 8, depending on the slice. In this position, the upper right-hand slice has an F8MUX, and the upper left-hand slice has an F7MUX. The lower right-hand and left-hand slices both have an F6MUX.

Figure 12: **Simplified Diagram of the Left-Hand SLICEM**



(a) On-Chip with CLK0 Feedback

(b) On-Chip with CLK2X Feedback

(c) Off-Chip with CLK0 Feedback

(d) Off-Chip with CLK2X Feedback

DS099-2_09_082104

Notes:

1. In the Low Frequency mode, all seven DLL outputs are available. In the High Frequency mode, only the CLK0, CLK180, and CLKDV outputs are available.

Figure 21: **Input Clock, Output Clock, and Feedback Connections for the DLL**

In the on-chip synchronization case (the [a] and [b] sections of Figure 21), it is possible to connect any of the DLL's seven output clock signals through general routing resources to the FPGA's internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. As shown in the [a] section of Figure 21, the feedback loop is created by routing CLK0 (or CLK2X, in the [b] section) to a global clock net, which in turn drives the CLKFB input.

In the off-chip synchronization case (the [c] and [d] sections of Figure 21), CLK0 (or CLK2X) plus any of the DLL's other output clock signals exit the FPGA using output buffers (OBUF) to drive an external clock network plus registers on the board. As shown in the [c] section of Figure 21, the feedback loop is formed by feeding CLK0 (or CLK2X, in the [d] section) back into the FPGA using an IBUFG, which directly accesses the global clock network, or an IBUF. Then, the global clock net is connected directly to the CLKFB input.

DLL Frequency Modes

The DLL supports two distinct operating modes, High Frequency and Low Frequency, with each specified over a different clock frequency range. The DLL_FREQUENCY_MODE attribute chooses between the two modes. When the attribute is set to LOW, the Low Frequency mode permits all seven DLL clock outputs to operate over a low-to-moderate frequency range. When the attribute is set to HIGH, the High Frequency mode allows the CLK0, CLK180 and CLKDV outputs to operate at the highest possible frequencies. The remaining DLL clock outputs are not available for use in High Frequency mode.

Accommodating High Input Frequencies

If the frequency of the CLKIN signal is high such that it exceeds the maximum permitted, divide it down to an acceptable value using the CLKIN_DIVIDE_BY_2 attribute. When this attribute is set to TRUE, the CLKIN frequency is divided by a factor of two just as it enters the DCM.

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
HSLVDCI_25			0.27	0.31	ns
HSLVDCI_33			0.28	0.32	ns
HSTL_I			0.60	0.69	ns
HSTL_I_DCI			0.59	0.68	ns
HSTL_III			0.19	0.22	ns
HSTL_III_DCI			0.20	0.23	ns
HSTL_I_18			0.18	0.21	ns
HSTL_I_DCI_18			0.17	0.19	ns
HSTL_II_18			–0.02	–0.01	ns
HSTL_II_DCI_18			0.75	0.86	ns
HSTL_III_18			0.28	0.32	ns
HSTL_III_DCI_18			0.28	0.32	ns
LVCMOS12	Slow	2 mA	7.60	8.73	ns
		4 mA	7.42	8.53	ns
		6 mA	6.67	7.67	ns
	Fast	2 mA	3.16	3.63	ns
		4 mA	2.70	3.10	ns
		6 mA	2.41	2.77	ns
LVCMOS15	Slow	2 mA	4.55	5.23	ns
		4 mA	3.76	4.32	ns
		6 mA	3.57	4.11	ns
		8 mA	3.55	4.09	ns
		12 mA	3.00	3.45	ns
	Fast	2 mA	3.11	3.57	ns
		4 mA	1.71	1.96	ns
		6 mA	1.44	1.66	ns
		8 mA	1.26	1.44	ns
		12 mA	1.11	1.27	ns
LVDCI_15			1.51	1.74	ns
LVDCI_DV2_15			1.32	1.52	ns

Simultaneously Switching Output Guidelines

This section provides guidelines for the maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins, of a given output signal standard, that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 49 and Table 50 provide the essential SSO guidelines. For each device/package combination, Table 49 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and will possibly not match the physical number of pairs. For each output signal standard and drive strength, Table 50 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The Table 50 guidelines are categorized by package style. Multiply the appropriate numbers from Table 49 and Table 50 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines may result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 49 x Table 50

The recommended maximum SSO values assume that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The number of SSOs allowed for quad-flat packages (VQ, TQ, PQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 49: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	VQ100	CP132 (1)(2)	TQ144 (1)	PQ208	FT256	FG320	FG456	FG676	FG900	FG1156 (2)
XC3S50	1	1.5	1.5	2	–	–	–	–	–	–
XC3S200	1	–	1.5	2	3	–	–	–	–	–
XC3S400	–	–	1.5	2	3	3	5	–	–	–
XC3S1000	–	–	–	–	3	3	5	5	–	–
XC3S1500	–	–	–	–	–	3	5	6	–	–
XC3S2000	–	–	–	–	–	–	5	6	9	–
XC3S4000	–	–	–	–	–	–	–	6	10	12
XC3S5000	–	–	–	–	–	–	–	6	10	12

Notes:

1. The V_{CCO} lines for the pair of banks on each side of the CP132 and TQ144 packages are internally tied together. Each pair of interconnected banks shares three V_{CCO}/GND pairs. Consequently, the per bank number is 1.5.
2. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.
3. The information in this table also applies to Pb-free packages.

Table 59: **Switching Characteristics for the DLL *(Cont'd)***

Symbol	Description	Frequency Mode / FCLKIN Range	Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Lock Time								
LOCK_DLL	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	18 MHz ≤ F_{CLKIN} ≤ 30 MHz	All	–	2.88	–	2.88	ms
		30 MHz < F_{CLKIN} ≤ 40 MHz		–	2.16	–	2.16	ms
		40 MHz < F_{CLKIN} ≤ 50 MHz		–	1.20	–	1.20	ms
		50 MHz < F_{CLKIN} ≤ 60 MHz		–	0.60	–	0.60	ms
		F_{CLKIN} > 60 MHz		–	0.48	–	0.48	ms
Delay Lines								
DCM_TAP	Delay tap resolution	All	All	30.0	60.0	30.0	60.0	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32 and Table 58.
2. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
3. Only mask revision 'E' and later devices (see Mask and Fab Revisions, page 58) and all revisions of the XC3S50 and the XC3S1000 support DLL feedback using the CLK2X output. For all other Spartan-3 devices, use feedback from the CLK0 output (instead of the CLK2X output) and set the CLK_FEEDBACK attribute to 1X.
4. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
5. This specification only applies if the attribute DUTY_CYCLE_CORRECTION = TRUE.

Digital Frequency Synthesizer (DFS)

Table 60: **Recommended Operating Conditions for the DFS**

Symbol		Description	Frequency Mode	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input	All	1	280	1	280	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input	Low	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF			High	–	±150	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input	All	–	±1	–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 58.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.

Table 79: **Pin Behavior After Power-Up, During Configuration *(Cont'd)***

Pin Name	Configuration Mode Settings <M2:M1:M0>					Bitstream Configuration Option
	Serial Modes		SelectMap Parallel Modes		JTAG Mode <1:0:1>	
	Master <0:0:0>	Slave <1:1:1>	Master <0:1:1>	Slave <1:1:0>		
VCCO: I/O bank output voltage supply pins						
VCCO_4 (for DUAL pins)	Same voltage as external interface	Same voltage as external interface	Same voltage as external interface	Same voltage as external interface	VCCO_4	N/A
VCCO_5 (for DUAL pins)	VCCO_5	VCCO_5	Same voltage as external interface	Same voltage as external interface	VCCO_5	N/A
VCCO_#	VCCO_#	VCCO_#	VCCO_#	VCCO_#	VCCO_#	N/A
VCCAUX: Auxiliary voltage supply pins						
VCCAUX	+2.5V	+2.5V	+2.5V	+2.5V	+2.5V	N/A
VCCINT: Internal core voltage supply pins						
VCCINT	+1.2V	+1.2V	+1.2V	+1.2V	+1.2V	N/A
GND: Ground supply pins						
GND	GND	GND	GND	GND	GND	N/A

Notes:

1. #= I/O bank number, an integer from 0 to 7.
2. (I) = input, (O) = output, (OD) = open-drain output, (I/O) = bidirectional, (I/OD) = bidirectional with open-drain output. Open-drain output requires pull-up to create logic High level.
3. Shaded cell indicates that the pin is high-impedance during configuration. To enable a soft pull-up resistor during configuration, drive or tie HSWAP_EN Low.

Bitstream Options

Table 80 lists the various bitstream options that affect pins on a Spartan-3 FPGA. The table shows the names of the affected pins, describes the function of the bitstream option, the name of the bitstream generator option variable, and the legal values for each variable. The default option setting for each variable is indicated with bold, underlined text.

Table 80: **Bitstream Options Affecting Spartan-3 Device Pins**

Affected Pin Name(s)	Bitstream Generation Function	Option Variable Name	Values (**Default**)
All unused I/O pins of type I/O, DUAL, GCLK, DCI, VREF	For all I/O pins that are unused in the application after configuration, this option defines whether the I/Os are individually tied to VCCO via a pull-up resistor, tied ground via a pull-down resistor, or left floating. If left floating, the unused pins should be connected to a defined logic level, either from a source internal to the FPGA or external.	UnusedPin	• **Pulldown** • Pullup • Pullnone
IO_Lxxy_#/DIN, IO_Lxxy_#/DOUT, IO_Lxxy_#/INIT_B	Serial configuration mode: If set to Yes, then these pins retain their functionality after configuration completes, allowing for device (re-)configuration. Readback is not supported in with serial mode.	Persist	• **No** • Yes
IO_Lxxy_#/D0, IO_Lxxy_#/D1, IO_Lxxy_#/D2, IO_Lxxy_#/D3, IO_Lxxy_#/D4, IO_Lxxy_#/D5, IO_Lxxy_#/D6, IO_Lxxy_#/D7, IO_Lxxy_#/CS_B, IO_Lxxy_#/RDWR_B, IO_Lxxy_#/BUSY, IO_Lxxy_#/INIT_B	Parallel configuration mode (also called SelectMAP): If set to Yes, then these pins retain their SelectMAP functionality after configuration completes, allowing for device readback and for partial or complete (re-)configuration.	Persist	• **No** • Yes

CP132: 132-Ball Chip-Scale Package

Note: The CP132 and CPG132 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

The pinout and footprint for the XC3S50 in the 132-ball chip-scale package, CP132, appear in Table 89 and Figure 45.

All the package pins appear in Table 89 and are sorted by bank number, then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The CP132 footprint has eight I/O banks. However, the voltage supplies for the two I/O banks along an edge are connected together internally. Consequently, there are four output voltage supplies, labeled VCCO_TOP, VCCO_RIGHT, VCCO_BOTTOM, and VCCO_LEFT.

Pinout Table

Table 89: **CP132 Package Pinout**

Bank	XC3S50 Pin Name	CP132 Ball	Type
0	IO_L01N_0/VRP_0	A3	DCI
0	IO_L01P_0/VRN_0	C4	DCI
0	IO_L27N_0	C5	I/O
0	IO_L27P_0	B5	I/O
0	IO_L30N_0	B6	I/O
0	IO_L30P_0	A6	I/O
0	IO_L31N_0	C7	I/O
0	IO_L31P_0/VREF_0	B7	VREF
0	IO_L32N_0/GCLK7	A7	GCLK
0	IO_L32P_0/GCLK6	C8	GCLK
1	IO_L01N_1/VRP_1	A13	DCI
1	IO_L01P_1/VRN_1	B13	DCI
1	IO_L27N_1	C11	I/O
1	IO_L27P_1	A12	I/O
1	IO_L28N_1	A11	I/O
1	IO_L28P_1	B11	I/O
1	IO_L31N_1/VREF_1	C9	VREF
1	IO_L31P_1	A10	I/O
1	IO_L32N_1/GCLK5	A8	GCLK
1	IO_L32P_1/GCLK4	A9	GCLK
2	IO_L01N_2/VRP_2	D12	DCI
2	IO_L01P_2/VRN_2	C14	DCI
2	IO_L20N_2	E12	I/O
2	IO_L20P_2	E13	I/O
2	IO_L21N_2	E14	I/O
2	IO_L21P_2	F12	I/O
2	IO_L23N_2/VREF_2	F13	VREF
2	IO_L23P_2	F14	I/O
2	IO_L24N_2	G12	I/O

Table 91: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
5	IO_L32P_5/GCLK2	P52	GCLK
6	IO_L01N_6/VRP_6	P36	DCI
6	IO_L01P_6/VRN_6	P35	DCI
6	IO_L20N_6	P33	I/O
6	IO_L20P_6	P32	I/O
6	IO_L21N_6	P31	I/O
6	IO_L21P_6	P30	I/O
6	IO_L22N_6	P28	I/O
6	IO_L22P_6	P27	I/O
6	IO_L23N_6	P26	I/O
6	IO_L23P_6	P25	I/O
6	IO_L24N_6/VREF_6	P24	VREF
6	IO_L24P_6	P23	I/O
6	IO_L40N_6	P21	I/O
6	IO_L40P_6/VREF_6	P20	VREF
7	IO/VREF_7	P4	VREF
7	IO_L01N_7/VRP_7	P2	DCI
7	IO_L01P_7/VRN_7	P1	DCI
7	IO_L20N_7	P6	I/O
7	IO_L20P_7	P5	I/O
7	IO_L21N_7	P8	I/O
7	IO_L21P_7	P7	I/O
7	IO_L22N_7	P11	I/O
7	IO_L22P_7	P10	I/O
7	IO_L23N_7	P13	I/O
7	IO_L23P_7	P12	I/O
7	IO_L24N_7	P15	I/O
7	IO_L24P_7	P14	I/O
7	IO_L40N_7/VREF_7	P18	VREF
7	IO_L40P_7	P17	I/O
0,1	VCCO_TOP	P126	VCCO
0,1	VCCO_TOP	P138	VCCO
0,1	VCCO_TOP	P115	VCCO
2,3	VCCO_RIGHT	P106	VCCO
2,3	VCCO_RIGHT	P75	VCCO
2,3	VCCO_RIGHT	P91	VCCO
4,5	VCCO_BOTTOM	P54	VCCO
4,5	VCCO_BOTTOM	P43	VCCO
4,5	VCCO_BOTTOM	P66	VCCO
6,7	VCCO_LEFT	P19	VCCO

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
2	VCCO_2	G11	VCCO
2	VCCO_2	H11	VCCO
2	VCCO_2	H12	VCCO
3	IO	K15	I/O
3	IO_L01N_3/VRP_3	P16	DCI
3	IO_L01P_3/VRN_3	R16	DCI
3	IO_L16N_3	P15	I/O
3	IO_L16P_3	P14	I/O
3	IO_L17N_3	N16	I/O
3	IO_L17P_3/VREF_3	N15	VREF
3	IO_L19N_3	M14	I/O
3	IO_L19P_3	N14	I/O
3	IO_L20N_3	M16	I/O
3	IO_L20P_3	M15	I/O
3	IO_L21N_3	L13	I/O
3	IO_L21P_3	M13	I/O
3	IO_L22N_3	L15	I/O
3	IO_L22P_3	L14	I/O
3	IO_L23N_3	K12	I/O
3	IO_L23P_3/VREF_3	L12	VREF
3	IO_L24N_3	K14	I/O
3	IO_L24P_3	K13	I/O
3	IO_L39N_3	J14	I/O
3	IO_L39P_3	J13	I/O
3	IO_L40N_3/VREF_3	J16	VREF
3	IO_L40P_3	K16	I/O
3	VCCO_3	J11	VCCO
3	VCCO_3	J12	VCCO
3	VCCO_3	K11	VCCO
4	IO	T12	I/O
4	IO	T14	I/O
4	IO/VREF_4	N12	VREF
4	IO/VREF_4	P13	VREF
4	IO/VREF_4	T10	VREF
4	IO_L01N_4/VRP_4	R13	DCI
4	IO_L01P_4/VRN_4	T13	DCI
4	IO_L25N_4	P12	I/O
4	IO_L25P_4	R12	I/O
4	IO_L27N_4/DIN/D0	M11	DUAL
4	IO_L27P_4/D1	N11	DUAL

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
2	IO_L20N_2	E17	I/O
2	IO_L20P_2	E18	I/O
2	IO_L21N_2	F15	I/O
2	IO_L21P_2	E15	I/O
2	IO_L22N_2	F14	I/O
2	IO_L22P_2	G14	I/O
2	IO_L23N_2/VREF_2	G18	VREF
2	IO_L23P_2	F17	I/O
2	IO_L24N_2	G15	I/O
2	IO_L24P_2	G16	I/O
2	IO_L27N_2	H13	I/O
2	IO_L27P_2	H14	I/O
2	IO_L34N_2/VREF_2	H16	VREF
2	IO_L34P_2	H15	I/O
2	IO_L35N_2	H17	I/O
2	IO_L35P_2	H18	I/O
2	IO_L39N_2	J18	I/O
2	IO_L39P_2	J17	I/O
2	IO_L40N_2	J15	I/O
2	IO_L40P_2/VREF_2	J14	VREF
2	VCCO_2	F16	VCCO
2	VCCO_2	H12	VCCO
2	VCCO_2	J12	VCCO
3	IO	K15	I/O
3	IO_L01N_3/VRP_3	T17	DCI
3	IO_L01P_3/VRN_3	T16	DCI
3	IO_L16N_3	T18	I/O
3	IO_L16P_3	U18	I/O
3	IO_L17N_3	P16	I/O
3	IO_L17P_3/VREF_3	R16	VREF
3	IO_L19N_3	R17	I/O
3	IO_L19P_3	R18	I/O
3	IO_L20N_3	P18	I/O
3	IO_L20P_3	P17	I/O
3	IO_L21N_3	P15	I/O
3	IO_L21P_3	N15	I/O
3	IO_L22N_3	M14	I/O
3	IO_L22P_3	N14	I/O
3	IO_L23N_3	M15	I/O
3	IO_L23P_3/VREF_3	M16	VREF

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
0	N.C. (◆)	IO_L22N_0	E8	I/O
0	N.C. (◆)	IO_L22P_0	D8	I/O
0	IO_L24N_0	IO_L24N_0	B8	I/O
0	IO_L24P_0	IO_L24P_0	A8	I/O
0	IO_L25N_0	IO_L25N_0	F9	I/O
0	IO_L25P_0	IO_L25P_0	E9	I/O
0	IO_L27N_0	IO_L27N_0	B9	I/O
0	IO_L27P_0	IO_L27P_0	A9	I/O
0	IO_L28N_0	IO_L28N_0	F10	I/O
0	IO_L28P_0	IO_L28P_0	E10	I/O
0	IO_L29N_0	IO_L29N_0	C10	I/O
0	IO_L29P_0	IO_L29P_0	B10	I/O
0	IO_L30N_0	IO_L30N_0	F11	I/O
0	IO_L30P_0	IO_L30P_0	E11	I/O
0	IO_L31N_0	IO_L31N_0	D11	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C11	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B11	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A11	GCLK
0	VCCO_0	VCCO_0	C8	VCCO
0	VCCO_0	VCCO_0	F8	VCCO
0	VCCO_0	VCCO_0	G9	VCCO
0	VCCO_0	VCCO_0	G10	VCCO
0	VCCO_0	VCCO_0	G11	VCCO
1	IO	IO	A12	I/O
1	IO	IO	E16	I/O
1	IO	IO	F12	I/O
1	IO	IO	F13	I/O
1	IO	IO	F16	I/O
1	IO	IO	F17	I/O
1	IO/VREF_1	IO/VREF_1	E13	VREF
1	N.C. (◆)	IO/VREF_1	F14	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	C19	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B20	DCI
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	A19	VREF
1	IO_L06P_1	IO_L06P_1	B19	I/O
1	IO_L09N_1	IO_L09N_1	C18	I/O
1	IO_L09P_1	IO_L09P_1	D18	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	A18	VREF
1	IO_L10P_1	IO_L10P_1	B18	I/O
1	IO_L15N_1	IO_L15N_1	D17	I/O

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	W9	VREF
5	IO_L27P_5	IO_L27P_5	V9	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	AB9	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	AA9	DUAL
5	IO_L29N_5	IO_L29N_5	Y10	I/O
5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	W10	VREF
5	IO_L30N_5	IO_L30N_5	AB10	I/O
5	IO_L30P_5	IO_L30P_5	AA10	I/O
5	IO_L31N_5/D4	IO_L31N_5/D4	W11	DUAL
5	IO_L31P_5/D5	IO_L31P_5/D5	V11	DUAL
5	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	AA11	GCLK
5	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	Y11	GCLK
5	VCCO_5	VCCO_5	T9	VCCO
5	VCCO_5	VCCO_5	T10	VCCO
5	VCCO_5	VCCO_5	T11	VCCO
5	VCCO_5	VCCO_5	U8	VCCO
5	VCCO_5	VCCO_5	Y8	VCCO
6	IO	IO	Y1	I/O
6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	Y3	DCI
6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	Y2	DCI
6	IO_L16N_6	IO_L16N_6	W4	I/O
6	IO_L16P_6	IO_L16P_6	W3	I/O
6	IO_L17N_6	IO_L17N_6	W2	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	W1	VREF
6	IO_L19N_6	IO_L19N_6	V5	I/O
6	IO_L19P_6	IO_L19P_6	U5	I/O
6	IO_L20N_6	IO_L20N_6	V4	I/O
6	IO_L20P_6	IO_L20P_6	V3	I/O
6	IO_L21N_6	IO_L21N_6	V2	I/O
6	IO_L21P_6	IO_L21P_6	V1	I/O
6	IO_L22N_6	IO_L22N_6	T6	I/O
6	IO_L22P_6	IO_L22P_6	T5	I/O
6	IO_L23N_6	IO_L23N_6	U4	I/O
6	IO_L23P_6	IO_L23P_6	T4	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	U3	VREF
6	IO_L24P_6	IO_L24P_6	U2	I/O
6	N.C. (◆)	IO_L26N_6	T3	I/O
6	N.C. (◆)	IO_L26P_6	R4	I/O
6	IO_L27N_6	IO_L27N_6	T2	I/O
6	IO_L27P_6	IO_L27P_6	T1	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	Y24	VCCO
4	IO	IO	IO	IO	IO	AA20	I/O
4	IO	IO	IO	IO	IO	AD15	I/O
4	N.C. (◆)	IO	IO	IO	IO	AD19	I/O
4	IO	IO	IO	IO	IO	AD23	I/O
4	IO	IO	IO	IO	IO	AF21	I/O
4	IO	IO	IO	IO	IO	AF22	I/O
4	IO	IO	IO	IO	IO	W15	I/O
4	IO	IO	IO	IO	IO	W16	I/O
4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	AB14	VREF
4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	AD25	VREF
4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	Y17	VREF
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	AB22	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	AC22	DCI
4	IO_L04N_4	IO_L04N_4	IO_L04N_4	IO_L04N_4	IO_L04N_4	AE24	I/O
4	IO_L04P_4	IO_L04P_4	IO_L04P_4	IO_L04P_4	IO_L04P_4	AF24	I/O
4	IO_L05N_4	IO_L05N_4	IO_L05N_4	IO_L05N_4	IO_L05N_4	AE23	I/O
4	IO_L05P_4	IO_L05P_4	IO_L05P_4	IO_L05P_4	IO_L05P_4	AF23	I/O
4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	AD22	VREF
4	IO_L06P_4	IO_L06P_4	IO_L06P_4	IO_L06P_4	IO_L06P_4	AE22	I/O
4	IO_L07N_4	IO_L07N_4	IO_L07N_4	IO_L07N_4	IO_L07N_4	AB21	I/O
4	IO_L07P_4	IO_L07P_4	IO_L07P_4	IO_L07P_4	IO_L07P_4	AC21	I/O
4	IO_L08N_4	IO_L08N_4	IO_L08N_4	IO_L08N_4	IO_L08N_4	AD21	I/O
4	IO_L08P_4	IO_L08P_4	IO_L08P_4	IO_L08P_4	IO_L08P_4	AE21	I/O
4	IO_L09N_4	IO_L09N_4	IO_L09N_4	IO_L09N_4	IO_L09N_4	AB20	I/O
4	IO_L09P_4	IO_L09P_4	IO_L09P_4	IO_L09P_4	IO_L09P_4	AC20	I/O
4	IO_L10N_4	IO_L10N_4	IO_L10N_4	IO_L10N_4	IO_L10N_4	AE20	I/O
4	IO_L10P_4	IO_L10P_4	IO_L10P_4	IO_L10P_4	IO_L10P_4	AF20	I/O
4	N.C. (◆)	IO_L11N_4	IO_L11N_4	IO_L11N_4	IO_L11N_4	Y19	I/O
4	N.C. (◆)	IO_L11P_4	IO_L11P_4	IO_L11P_4	IO_L11P_4	AA19	I/O
4	N.C. (◆)	IO_L12N_4	IO_L12N_4	IO_L12N_4	IO_L12N_4	AB19	I/O
4	N.C. (◆)	IO_L12P_4	IO_L12P_4	IO_L12P_4	IO_L12P_4	AC19	I/O
4	IO_L15N_4	IO_L15N_4	IO_L15N_4	IO_L15N_4	IO_L15N_4	AE19	I/O
4	IO_L15P_4	IO_L15P_4	IO_L15P_4	IO_L15P_4	IO_L15P_4	AF19	I/O
4	IO_L16N_4	IO_L16N_4	IO_L16N_4	IO_L16N_4	IO_L16N_4	Y18	I/O
4	IO_L16P_4	IO_L16P_4	IO_L16P_4	IO_L16P_4	IO_L16P_4	AA18	I/O
4	N.C. (◆)	IO_L17N_4	IO_L17N_4	IO_L17N_4	IO_L17N_4	AB18	I/O
4	N.C. (◆)	IO_L17P_4	IO_L17P_4	IO_L17P_4	IO_L17P_4	AC18	I/O
4	N.C. (◆)	IO_L18N_4	IO_L18N_4	IO_L18N_4	IO_L18N_4	AD18	I/O
4	N.C. (◆)	IO_L18P_4	IO_L18P_4	IO_L18P_4	IO_L18P_4	AE18	I/O
4	IO_L19N_4	IO_L19N_4	IO_L19N_4	IO_L19N_4	IO_L19N_4	AC17	I/O
4	IO_L19P_4	IO_L19P_4	IO_L19P_4	IO_L19P_4	IO_L19P_4	AA17	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	IO_L04N_2	IO_L04N_2	E29	I/O
2	IO_L04P_2	IO_L04P_2	E30	I/O
2	IO_L05N_2	IO_L05N_2	F28	I/O
2	IO_L05P_2	IO_L05P_2	F29	I/O
2	IO_L06N_2	IO_L06N_2	G27	I/O
2	IO_L06P_2	IO_L06P_2	G28	I/O
2	IO_L07N_2	IO_L07N_2	G29	I/O
2	IO_L07P_2	IO_L07P_2	G30	I/O
2	IO_L08N_2	IO_L08N_2	G25	I/O
2	IO_L08P_2	IO_L08P_2	H24	I/O
2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	H25	VREF
2	IO_L09P_2	IO_L09P_2	H26	I/O
2	IO_L10N_2	IO_L10N_2	H27	I/O
2	IO_L10P_2	IO_L10P_2	H28	I/O
2	IO_L12N_2	IO_L12N_2	H29	I/O
2	IO_L12P_2	IO_L12P_2	H30	I/O
2	IO_L13N_2	IO_L13N_2	J26	I/O
2	IO_L13P_2/VREF_2	IO_L13P_2/VREF_2	J27	VREF
2	IO_L14N_2	IO_L14N_2	J29	I/O
2	IO_L14P_2	IO_L14P_2	J30	I/O
2	IO_L15N_2	IO_L15N_2	J23	I/O
2	IO_L15P_2	IO_L15P_2	K22	I/O
2	IO_L16N_2	IO_L16N_2	K24	I/O
2	IO_L16P_2	IO_L16P_2	K25	I/O
2	IO_L19N_2	IO_L19N_2	L25	I/O
2	IO_L19P_2	IO_L19P_2	L26	I/O
2	IO_L20N_2	IO_L20N_2	L27	I/O
2	IO_L20P_2	IO_L20P_2	L28	I/O
2	IO_L21N_2	IO_L21N_2	L29	I/O
2	IO_L21P_2	IO_L21P_2	L30	I/O
2	IO_L22N_2	IO_L22N_2	M22	I/O
2	IO_L22P_2	IO_L22P_2	M23	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	M24	VREF
2	IO_L23P_2	IO_L23P_2	M25	I/O
2	IO_L24N_2	IO_L24N_2	M27	I/O
2	IO_L24P_2	IO_L24P_2	M28	I/O
2	IO_L26N_2	IO_L26N_2	M21	I/O
2	IO_L26P_2	IO_L26P_2	N21	I/O
2	IO_L27N_2	IO_L27N_2	N22	I/O
2	IO_L27P_2	IO_L27P_2	N23	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
1	VCCO_1	VCCO_1	M22	VCCO
2	IO	IO	G33	I/O
2	IO	IO	G34	I/O
2	IO	IO	U25	I/O
2	IO	IO	U26	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C33	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C34	DCI
2	IO_L02N_2	IO_L02N_2	D33	I/O
2	IO_L02P_2	IO_L02P_2	D34	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	E32	VREF
2	IO_L03P_2	IO_L03P_2	E33	I/O
2	IO_L04N_2	IO_L04N_2	F31	I/O
2	IO_L04P_2	IO_L04P_2	F32	I/O
2	IO_L05N_2	IO_L05N_2	G29	I/O
2	IO_L05P_2	IO_L05P_2	G30	I/O
2	IO_L06N_2	IO_L06N_2	H29	I/O
2	IO_L06P_2	IO_L06P_2	H30	I/O
2	IO_L07N_2	IO_L07N_2	H33	I/O
2	IO_L07P_2	IO_L07P_2	H34	I/O
2	IO_L08N_2	IO_L08N_2	J28	I/O
2	IO_L08P_2	IO_L08P_2	J29	I/O
2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	H31	VREF
2	IO_L09P_2	IO_L09P_2	J31	I/O
2	IO_L10N_2	IO_L10N_2	J32	I/O
2	IO_L10P_2	IO_L10P_2	J33	I/O
2	IO_L11N_2	IO_L11N_2	J27	I/O
2	IO_L11P_2	IO_L11P_2	K26	I/O
2	IO_L12N_2	IO_L12N_2	K27	I/O
2	IO_L12P_2	IO_L12P_2	K28	I/O
2	IO_L13N_2	IO_L13N_2	K29	I/O
2	IO_L13P_2/VREF_2	IO_L13P_2/VREF_2	K30	VREF
2	IO_L14N_2	IO_L14N_2	K31	I/O
2	IO_L14P_2	IO_L14P_2	K32	I/O
2	IO_L15N_2	IO_L15N_2	K33	I/O
2	IO_L15P_2	IO_L15P_2	K34	I/O
2	IO_L16N_2	IO_L16N_2	L25	I/O
2	IO_L16P_2	IO_L16P_2	L26	I/O
2	N.C. (◆)	IO_L17N_2	L28	I/O
2	N.C. (◆)	IO_L17P_2/ VREF_2	L29	VREF

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L48P_3	IO_L48P_3	AB24	I/O
3	N.C. (◆)	IO_L49N_3	AA26	I/O
3	N.C. (◆)	IO_L49P_3	AA25	I/O
3	IO_L50N_3	IO_L50N_3	Y25	I/O
3	IO_L50P_3	IO_L50P_3	Y24	I/O
3	N.C. (◆)	IO_L51N_3	V24	I/O
3	N.C. (◆)	IO_L51P_3	W24	I/O
3	VCCO_3	VCCO_3	AA23	VCCO
3	VCCO_3	VCCO_3	AB23	VCCO
3	VCCO_3	VCCO_3	AB29	VCCO
3	VCCO_3	VCCO_3	AB33	VCCO
3	VCCO_3	VCCO_3	AD27	VCCO
3	VCCO_3	VCCO_3	AD31	VCCO
3	VCCO_3	VCCO_3	AG28	VCCO
3	VCCO_3	VCCO_3	AG32	VCCO
3	VCCO_3	VCCO_3	AL32	VCCO
3	VCCO_3	VCCO_3	W23	VCCO
3	VCCO_3	VCCO_3	W31	VCCO
3	VCCO_3	VCCO_3	Y23	VCCO
3	VCCO_3	VCCO_3	Y27	VCCO
4	IO	IO	AD18	I/O
4	IO	IO	AD19	I/O
4	IO	IO	AD20	I/O
4	IO	IO	AD22	I/O
4	IO	IO	AE18	I/O
4	IO	IO	AE19	I/O
4	IO	IO	AE22	I/O
4	N.C. (◆)	IO	AE24	I/O
4	IO	IO	AF24	I/O
4	N.C. (◆)	IO	AF26	I/O
4	IO	IO	AG26	I/O
4	IO	IO	AG27	I/O
4	IO	IO	AJ27	I/O
4	IO	IO	AJ29	I/O
4	IO	IO	AK25	I/O
4	IO	IO	AN26	I/O
4	IO/VREF_4	IO/VREF_4	AF21	VREF
4	IO/VREF_4	IO/VREF_4	AH23	VREF
4	IO/VREF_4	IO/VREF_4	AK18	VREF
4	IO/VREF_4	IO/VREF_4	AL30	VREF

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	GND	GND	AN1	GND
N/A	GND	GND	AN2	GND
N/A	GND	GND	AN33	GND
N/A	GND	GND	AN34	GND
N/A	GND	GND	AP1	GND
N/A	GND	GND	AP13	GND
N/A	GND	GND	AP16	GND
N/A	GND	GND	AP19	GND
N/A	GND	GND	AP2	GND
N/A	GND	GND	AP22	GND
N/A	GND	GND	AP26	GND
N/A	GND	GND	AP30	GND
N/A	GND	GND	AP33	GND
N/A	GND	GND	AP34	GND
N/A	GND	GND	AP5	GND
N/A	GND	GND	AP9	GND
N/A	GND	GND	B1	GND
N/A	GND	GND	B2	GND
N/A	GND	GND	B33	GND
N/A	GND	GND	B34	GND
N/A	GND	GND	C11	GND
N/A	GND	GND	C24	GND
N/A	GND	GND	C3	GND
N/A	GND	GND	C32	GND
N/A	GND	GND	E1	GND
N/A	GND	GND	E13	GND
N/A	GND	GND	E16	GND
N/A	GND	GND	E19	GND
N/A	GND	GND	E22	GND
N/A	GND	GND	E26	GND
N/A	GND	GND	E30	GND
N/A	GND	GND	E34	GND
N/A	GND	GND	E5	GND
N/A	GND	GND	E9	GND
N/A	GND	GND	G28	GND
N/A	GND	GND	G7	GND
N/A	GND	GND	J1	GND
N/A	GND	GND	J13	GND
N/A	GND	GND	J16	GND
N/A	GND	GND	J19	GND

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
GND	GND	GND	GND	GND	VCCINT	I/O L51N_3 ◆	I/O	I/O	I/O L37P_3	I/O L37N_3	I/O L38P_3	I/O L38N_3	I/O L39P_3	I/O L39N_3	I/O L40P_3	I/O L40N_3 VREF_3	V
GND	GND	GND	GND	VCCINT	VCCO_3	I/O L51P_3 ◆	I/O L33N_3	GND	VCCAUX	I/O L34P_3 VREF_3	I/O L34N_3	GND	VCCO_3	I/O L35P_3	I/O L35N_3	GND	W
GND	GND	GND	GND	VCCINT	VCCO_3	I/O L50P_3	I/O L50N_3	I/O L33P_3	VCCO_3	I/O L30P_3	I/O L30N_3	VCCAUX	I/O L31P_3	I/O L31N_3	I/O L32P_3	I/O L32N_3	Y
GND	GND	GND	GND	VCCINT	VCCO_3	I/O L48N_3	I/O L49P_3 ◆	I/O L49N_3 ◆	I/O L26P_3	I/O L26N_3	I/O L27P_3	I/O L27N_3	I/O L28P_3	I/O L28N_3	I/O L29P_3	I/O L29N_3	AA
GND	VCCINT	VCCINT	VCCINT	VCCINT	VCCO_3	I/O L48P_3	I/O L24N_3	GND	I/O L46P_3	I/O L46N_3	VCCO_3	GND	I/O L47P_3	I/O L47N_3	VCCO_3	GND	AB
VCCINT	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCINT	I/O L20P_3	I/O L20N_3	I/O L24P_3	I/O L21P_3	I/O L21N_3	I/O L22P_3	I/O L22N_3	I/O L23P_3 VREF_3	I/O L23N_3	I/O L45P_3	I/O L45N_3	AC
I/O	I/O	I/O	I/O L18N_4	I/O	I/O L11N_4	DONE	I/O L17P_3 VREF_3	I/O L17N_3	VCCO_3	I/O L44P_3 ◆	I/O L44N_3 ◆	VCCAUX	VCCO_3	GND	I/O L19P_3	I/O L19N_3	AD
I/O	I/O	I/O L23N_4	I/O L18P_4	I/O	I/O L11P_4	I/O ◆	GND	I/O L12N_3	I/O L13P_3	I/O L13N_3 VREF_3	I/O L14P_3	I/O L14N_3	I/O L15P_3	I/O L15N_3	I/O L16P_3	I/O L16N_3	AE
I/O L29N_4	GND	I/O L23P_4	IO VREF_4	GND	I/O L12N_4	I/O	I/O L07N_4	I/O ◆	I/O L12P_3	I/O L09P_3 VREF_3	I/O L09N_3	GND	I/O L10N_3	I/O L11P_3	I/O L11N_3	GND	AF
I/O L29P_4	VCCAUX	VCCO_4	I/O L19N_4	I/O L16N_4	I/O L12P_4	VCCO_4	I/O L07P_4	I/O	I/O	VCCO_3	I/O L07P_3	I/O L07N_3	I/O L10P_3	VCCO_3	I/O L08P_3	I/O L08N_3	AG
I/O L30N_4 D2	I/O L27N_4 DIN D0	I/O L24N_4	I/O L19P_4	I/O L16P_4	IO VREF_4	I/O L39N_4 ◆	I/O L08N_4	I/O L05N_4	VCCO_4	GND	I/O L06P_3	I/O L06N_3	I/O L41P_3 ◆	I/O L41N_3 ◆	I/O	I/O	AH
I/O L30P_4 D3	I/O L27P_4 D1	I/O L24P_4	I/O L20N_4	VCCO_4	I/O L13N_4	I/O L39P_4 ◆	I/O L08P_4	I/O L05P_4	I/O	I/O L35N_4	I/O	VCCAUX	I/O L04P_3	I/O L04N_3	I/O L05P_3	I/O L05N_3	AJ
IO VREF_4	GND	VCCAUX	I/O L20P_4	GND	I/O L13P_4	VCCAUX	I/O	GND	I/O L38N_4	I/O L35P_4	VCCAUX	GND	N.C. ◆ ■	I/O L03P_3	I/O L03N_3	GND	AK
I/O L31N_4 INIT_B	VCCO_4	I/O L25N_4	I/O L21N_4	I/O L17N_4	I/O L14N_4	VCCO_4	I/O L09N_4	I/O L06N_4 VREF_4	I/O L38P_4	I/O L36N_4 ◆	I/O L33N_4	IO VREF_4	CCLK	VCCO_3	I/O L02P_3	I/O L02N_3 VREF_3	AL
I/O L31P_4 DOUT BUSY	I/O L28N_4	I/O L25P_4	I/O L21P_4	I/O L17P_4	I/O L14P_4	GND	I/O L09P_4	I/O L06P_4	VCCO_4	I/O L36P_4 ◆	I/O L33P_4	I/O L03N_4	VCCO_4	GND	I/O L01P_3 VRN_3	I/O L01N_3 VRP_3	AM
I/O L32N_4 GCLK1	I/O L28P_4	I/O L26N_4	I/O L22N_4 VREF_4	VCCO_4	I/O L15N_4	I/O L40N_4 ◆	I/O L10N_4	I/O	I/O L04N_4	I/O L37N_4 ◆	I/O L34N_4	I/O L03P_4	I/O L02N_4	I/O L01N_4 VRP_4	GND	GND	AN
I/O L32P_4 GCLK0	GND	I/O L26P_4 VREF_4	I/O L22P_4	GND	I/O L15P_4	I/O L40P_4 ◆	I/O L10P_4	GND	I/O L04P_4	I/O L37P_4 ◆	I/O L34P_4	GND	I/O L02P_4	I/O L01P_4 VRN_4	GND	GND	AP

Bank 3

Bank 4

DS099-4_14d_072903

Bottom Right Corner of FG1156 Package (Top View)

Figure 60: FG1156 Package Footprint (Top View) Continued

Revision History

Date	Version	Description
04/03/03	1.0	Initial Xilinx release.
04/21/03	1.1	Added information on the VQ100 package footprint, including a complete pinout table (Table 87) and footprint diagram (Figure 44). Updated Table 85 with final I/O counts for the VQ100 package. Also added final differential I/O pair counts for the TQ144 package. Added clarifying comments to HSWAP_EN pin description on page 119. Updated the footprint diagram for the FG900 package shown in Figure 55a and Figure 55b. Some thick lines separating I/O banks were incorrect. Made cosmetic changes to Figure 40, Figure 42, and Figure 43. Updated Xilinx hypertext links. Added XC3S200 and XC3S400 to Pin Name column in Table 91.
05/12/03	1.1.1	AM32 pin was missing GND label in FG1156 package diagram (Figure 53).
07/11/03	1.1.2	Corrected misspellings of GCLK in Table 69 and Table 70. Changed CMOS25 to LVCMOS25 in Dual-Purpose Pin I/O Standard During Configuration section. Clarified references to Module 2. For XC3S5000 in FG1156 package, corrected N.C. symbol to a black square in Table 110, key, and package drawing.
07/29/03	1.2	Corrected pin names on FG1156 package. Some package balls incorrectly included LVDS pair names. The affected balls on the FG1156 package include G1, G2, G33, G34, U9, U10, U25, U26, V9, V10, V25, V26, AH1, AH2, AH33, AH34. The number of LVDS pairs is unaffected. Modified affected balls and re-sorted rows in Table 110. Updated affected balls in Figure 53. Also updated ASCII and Excel electronic versions of FG1156 pinout.
08/19/03	1.2.1	Removed 100 MHz ConfigRate option in CCLK: Configuration Clock section and in Table 80. Added note that TDO is a totem-pole output in Table 77.
10/09/03	1.2.2	Some pins had incorrect bank designations and were improperly sorted in Table 93. No pin names or functions changed. Renamed DCI_IN to DCI and added black diamond to N.C. pins in Table 93. In Figure 47, removed some extraneous text from pin 106 and corrected spelling of pins 45, 48, and 81.
12/17/03	1.3	Added FG320 pin tables and pinout diagram (FG320: 320-lead Fine-pitch Ball Grid Array). Made cosmetic changes to the TQ144 footprint (Figure 46), the PQ208 footprint (Figure 47), the FG676 footprint (Figure 53), and the FG900 footprint (Figure 55). Clarified wording in Precautions When Using the JTAG Port in 3.3V Environments section.
02/27/04	1.4	Clarified wording in Using JTAG Port After Configuration section. In Table 81, reduced package height for FG320 and increased maximum I/O values for the FG676, FG900, and FG1156 packages.
07/13/04	1.5	Added information on lead-free (Pb-free) package options to the Package Overview section plus Table 81 and Table 83. Clarified the VRN_# reference resistor requirements for I/O standards that use single termination as described in the DCI Termination Types section and in Figure 42b. Graduated from Advance Product Specification to Product Specification.
08/24/04	1.5.1	Removed XC3S2000 references from FG1156: 1156-lead Fine-pitch Ball Grid Array.
01/17/05	1.6	Added XC3S50 in CP132 package option. Added XC3S2000 in FG456 package option. Added XC3S4000 in FG676 package option. Added Selecting the Right Package Option section. Modified or added Table 81, Table 83, Table 84, Table 85, Table 89, Table 90, Table 100, Table 102, Table 103, Table 106, Figure 45, and Figure 53.
08/19/05	1.7	Removed term “weak” from the description of pull-up and pull-down resistors. Added IDCODE Register values. Added signal integrity precautions to CCLK: Configuration Clock and indicated that CCLK should be treated as an I/O during Master mode in Table 79.
04/03/06	2.0	Added Package Thermal Characteristics. Updated Figure 41 to make it a more obvious example. Added detail about which pins have dedicated pull-up resistors during configuration, regardless of the HSWAP_EN value to Table 70 and to Pin Behavior During Configuration. Updated Precautions When Using the JTAG Port in 3.3V Environments.
04/26/06	2.1	Corrected swapped data row in Table 86. The Theta-JA with zero airflow column was swapped with the Theta-JC column. Made additional notations on CONFIG and JTAG pins that have pull-up resistors during configuration, regardless of the HSWAP_EN input.
05/25/07	2.2	Added link on page 128 to Material Declaration Data Sheets. Corrected units typo in Table 74. Added Note 1 to Table 103 about VREF for XC3S1500 in FG676.