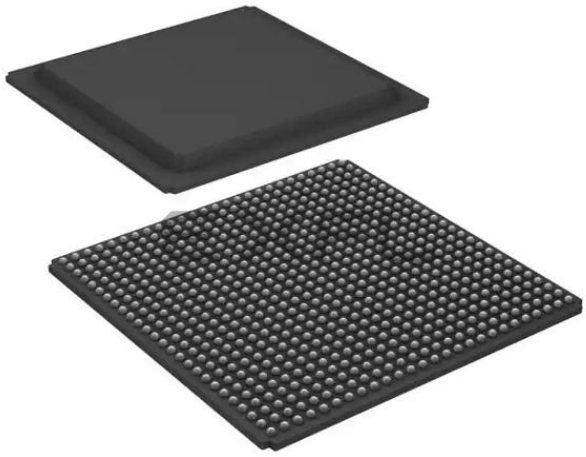
AMD Xilinx - XC3S2000-4FG676I Datasheet



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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	5120
Number of Logic Elements/Cells	46080
Total RAM Bits	737280
Number of I/O	489
Number of Gates	2000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s2000-4fg676i

In contrast, the 144-pin Thin Quad Flat Pack (TQ144) package and the 132-pin Chip-Scale Package (CP132) tie V_{CCO} together internally for the pair of banks on each side of the device. For example, the V_{CCO} Bank 0 and the V_{CCO} Bank 1 lines are tied together. The interconnected bank-pairs are 0/1, 2/3, 4/5, and 6/7. As a result, Spartan-3 devices in the CP132 and TQ144 packages support four independent V_{CCO} supplies.

Note: The CP132 package is discontinued. See http://www.xilinx.com/support/documentation /spartan-3_customer_notices.htm.

Spartan-3 FPGA Compatibility

Within the Spartan-3 family, all devices are pin-compatible by package. When the need for future logic resources outgrows the capacity of the Spartan-3 device in current use, a larger device in the same package can serve as a direct replacement. Larger devices may add extra V_{REF} and V_{CCO} lines to support a greater number of I/Os. In the larger device, more pins can convert from user I/Os to V_{REF} lines. Also, additional V_{CCO} lines are bonded out to pins that were “not connected” in the smaller device. Thus, it is important to plan for future upgrades at the time of the board’s initial design by laying out connections to the extra pins.

The Spartan-3 family is not pin-compatible with any previous Xilinx FPGA family or with other platforms among the Spartan-3 Generation FPGAs.

Rules Concerning Banks

When assigning I/Os to banks, it is important to follow the following V_{CCO} rules:

- Leave no V_{CCO} pins unconnected on the FPGA.
- Set all V_{CCO} lines associated with the (interconnected) bank to the same voltage level.
- The V_{CCO} levels used by all standards assigned to the I/Os of the (interconnected) bank(s) must agree. The Xilinx development software checks for this. Tables 8, 9, and 10 describe how different standards use the V_{CCO} supply.
- Only one of the following standards is allowed on outputs per bank: LVDS, LDT, LVDS_EXT, or RSDS. This restriction is for the eight banks in each device, even if the V_{CCO} levels are shared across banks, as in the CP132 and TQ144 packages.
- If none of the standards assigned to the I/Os of the (interconnected) bank(s) uses V_{CCO}, tie all associated V_{CCO} lines to 2.5V.
- In general, apply 2.5V to V_{CCO} Bank 4 from power-on to the end of configuration. Apply the same voltage to V_{CCO} Bank 5 during parallel configuration or a Readback operation. For information on how to program the FPGA using 3.3V signals and power, see the 3.3V-Tolerant Configuration Interface section.

If any of the standards assigned to the Inputs of the bank use V_{REF}, then observe the following additional rules:

- Connect *all* V_{REF} pins within the bank to the same voltage level.
- The V_{REF} levels used by all standards assigned to the Inputs of the bank must agree. The Xilinx development software checks for this. Tables 8 and 10 describe how different standards use the V_{REF} supply.

If none of the standards assigned to the Inputs of a bank use V_{REF} for biasing input switching thresholds, all associated V_{REF} pins function as User I/Os.

Exceptions to Banks Supporting I/O Standards

Bank 5 of any Spartan-3 device in a VQ100, CP132, or TQ144 package does not support DCI signal standards. In this case, bank 5 has neither VRN nor VRP pins.

Furthermore, banks 4 and 5 of any Spartan-3 device in a VQ100 package do not support signal standards using V_{REF} (see Table 8). In this case, the two banks do not have any V_{REF} pins.

upper path), enter the slice and connect directly to the LUT. Once inside the slice, the lower 4-bit path passes through a function generator ‘F’ (or ‘G’) that performs logic operations. The function generator’s Data output, ‘D’, offers five possible paths:

- Exit the slice via line ‘X’ (or ‘Y’) and return to interconnect.
- Inside the slice, ‘X’ (or ‘Y’) serves as an input to the DXMUX (DYMUX) which feeds the data input, ‘D’, of the FFX (FFY) storage element. The ‘Q’ output of the storage element drives the line XQ (or YQ) which exits the slice.
- Control the CYMUXF (or CYMUXG) multiplexer on the carry chain.
- With the carry chain, serve as an input to the XORF (or XORG) exclusive-OR gate that performs arithmetic operations, producing a result on ‘X’ (or ‘Y’).
- Drive the multiplexer F5MUX to implement logic functions wider than four bits. The ‘D’ outputs of both the F-LUT and G-LUT serve as data inputs to this multiplexer.

In addition to the main logic paths described above, there are two bypass paths that enter the slice as BX and BY. Once inside the FPGA, BX in the bottom half of the slice (or BY in the top half) can take any of several possible branches:

- Bypass both the LUT and the storage element, then exit the slice as BXOUT (or BYOUT) and return to interconnect.
- Bypass the LUT, then pass through a storage element via the D input before exiting as XQ (or YQ).
- Control the wide function multiplexer F5MUX (or F6MUX).
- Via multiplexers, serve as an input to the carry chain.
- Drives the DI input of the LUT.
- BY can control the REV inputs of both the FFY and FFX storage elements.
- Finally, the DIG_MUX multiplexer can switch BY onto the DIG line, which exits the slice.

Other slice signals shown in Figure 12 are discussed in the sections that follow.

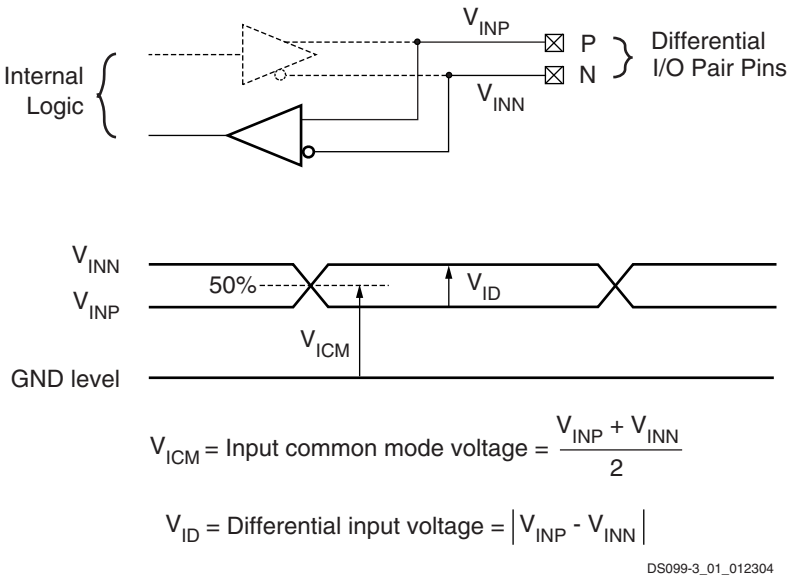


Figure 32: **Differential Input Voltages**

Table 37: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

Signal Standard (IOSTANDARD)	V_{CCO}(1)			V_{ID}(3)			V_{ICM}		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LDT_25 (ULVDS_25)	2.375	2.50	2.625	200	600	1000	0.44	0.60	0.78
LVDS_25, LVDS_25_DCI	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20
BLVDS_25	2.375	2.50	2.625	-	350	-	-	1.25	-
LVDSEXT_25, LVDSEXT_25_DCI	2.375	2.50	2.625	100	540	1000	0.30	1.20	2.20
LVPECL_25	2.375	2.50	2.625	100	-	-	0.30	1.20	2.00
RSDS_25	2.375	2.50	2.625	100	200	-	-	1.20	-
DIFF_HSTL_II_18, DIFF_HSTL_II_18_DCI	1.70	1.80	1.90	200	-	-	0.80	-	1.00
DIFF_SSTL2_II, DIFF_SSTL2_II_DCI	2.375	2.50	2.625	300	-	-	1.05	-	1.45

Notes:

1. V_{CCO} only supplies differential output drivers, not input circuits.
2. V_{REF} inputs are not used for any of the differential I/O standards.
3. V_{ID} is a differential measurement.

I/O Timing

Table 40: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max[2]	Speed Grade -4 Max[2]	Units
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25[3], 12 mA output drive, Fast slew rate, with DCM[4]	XC3S50	2.04	2.35	ns
			XC3S200	1.45	1.75	ns
			XC3S400	1.45	1.75	ns
			XC3S1000	2.07	2.39	ns
			XC3S1500	2.05	2.36	ns
			XC3S2000	2.03	2.34	ns
			XC3S4000	1.94	2.24	ns
			XC3S5000	2.00	2.30	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25[3], 12 mA output drive, Fast slew rate, without DCM	XC3S50	3.70	4.24	ns
			XC3S200	3.89	4.46	ns
			XC3S400	3.91	4.48	ns
			XC3S1000	4.00	4.59	ns
			XC3S1500	4.07	4.66	ns
			XC3S2000	4.19	4.80	ns
			XC3S4000	4.44	5.09	ns
			XC3S5000	4.38	5.02	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. For minimums, use the values reported by the Xilinx timing analyzer.
3. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 44. If the latter is true, *add* the appropriate Output adjustment from Table 47.
4. DCM output jitter is included in all measurements.

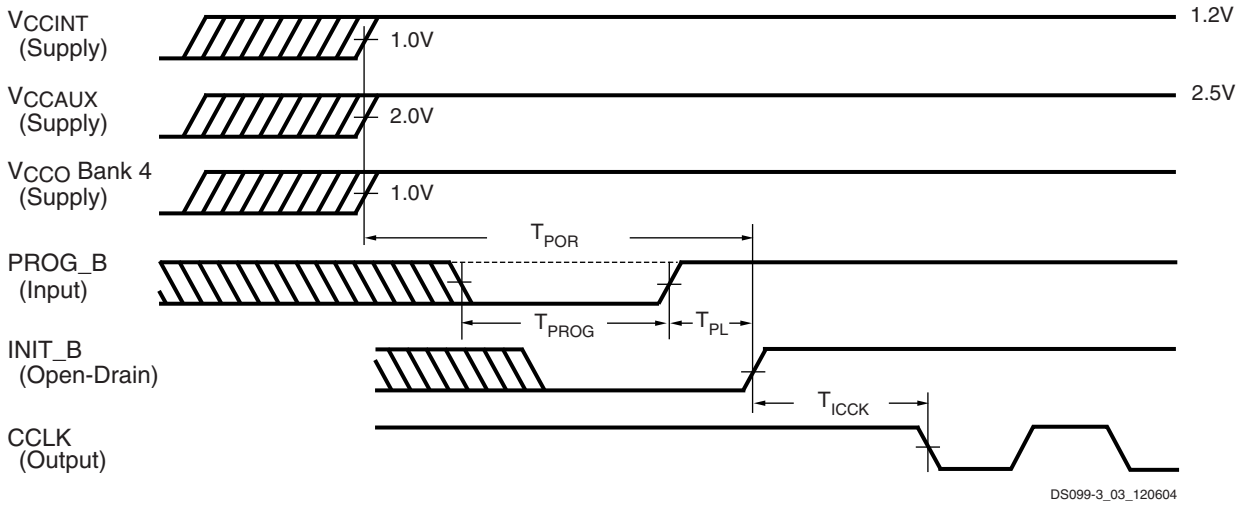
Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
HSLVDCI_25			0.27	0.31	ns
HSLVDCI_33			0.28	0.32	ns
HSTL_I			0.60	0.69	ns
HSTL_I_DCI			0.59	0.68	ns
HSTL_III			0.19	0.22	ns
HSTL_III_DCI			0.20	0.23	ns
HSTL_I_18			0.18	0.21	ns
HSTL_I_DCI_18			0.17	0.19	ns
HSTL_II_18			–0.02	–0.01	ns
HSTL_II_DCI_18			0.75	0.86	ns
HSTL_III_18			0.28	0.32	ns
HSTL_III_DCI_18			0.28	0.32	ns
LVCMOS12	Slow	2 mA	7.60	8.73	ns
		4 mA	7.42	8.53	ns
		6 mA	6.67	7.67	ns
	Fast	2 mA	3.16	3.63	ns
		4 mA	2.70	3.10	ns
		6 mA	2.41	2.77	ns
LVCMOS15	Slow	2 mA	4.55	5.23	ns
		4 mA	3.76	4.32	ns
		6 mA	3.57	4.11	ns
		8 mA	3.55	4.09	ns
		12 mA	3.00	3.45	ns
	Fast	2 mA	3.11	3.57	ns
		4 mA	1.71	1.96	ns
		6 mA	1.44	1.66	ns
		8 mA	1.26	1.44	ns
		12 mA	1.11	1.27	ns
LVDCI_15			1.51	1.74	ns
LVDCI_DV2_15			1.32	1.52	ns

Table 48: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
HSTL_III_DCI_18							
LVCMOS12		-	0	1.2	1M	0	0.6
LVCMOS15		-	0	1.5	1M	0	0.75
LVDCI_15							
LVDCI_DV2_15							
HSLVDCI_15							
LVCMOS18		-	0	1.8	1M	0	0.9
LVDCI_18							
LVDCI_DV2_18							
HSLVDCI_18							
LVCMOS25		-	0	2.5	1M	0	1.25
LVDCI_25							
LVDCI_DV2_25							
HSLVDCI_25							
LVCMOS33		-	0	3.3	1M	0	1.65
LVDCI_33							
LVDCI_DV2_33							
HSLVDCI_33							
LVTTL		-	0	3.3	1M	0	1.4
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_I_DCI							
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_I_DCI							
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL2_II_DCI					50	1.25	
Differential							
LDT_25 (ULVDS_25)		-	V_{ICM} – 0.125	V_{ICM} + 0.125	60	0.6	V_{ICM}
LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_25_DCI					N/A	N/A	
BLVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
LVDSEXT_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDSEXT_25_DCI					N/A	N/A	
LVPECL_25		-	V_{ICM} – 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25		-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
DIFF_HSTL_II_18		-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.8	V_{ICM}
DIFF_HSTL_II_18_DCI							

Configuration and JTAG Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 36: **Waveforms for Power-On and the Beginning of Configuration**

Table 65: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}[2]	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 4 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XC3S50	–	5	ms
		XC3S200	–	5	ms
		XC3S400	–	5	ms
		XC3S1000	–	5	ms
		XC3S1500	–	7	ms
		XC3S2000	–	7	ms
		XC3S4000	–	7	ms
		XC3S5000	–	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.3	–	µs
T_{PL}[2]	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S50	–	2	ms
		XC3S200	–	2	ms
		XC3S400	–	2	ms
		XC3S1000	–	2	ms
		XC3S1500	–	3	ms
		XC3S2000	–	3	ms
		XC3S4000	–	3	ms
		XC3S5000	–	3	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	–	ns
T_{ICCK}[3]	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.25	4.0	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only for the Master Serial and Master Parallel modes.

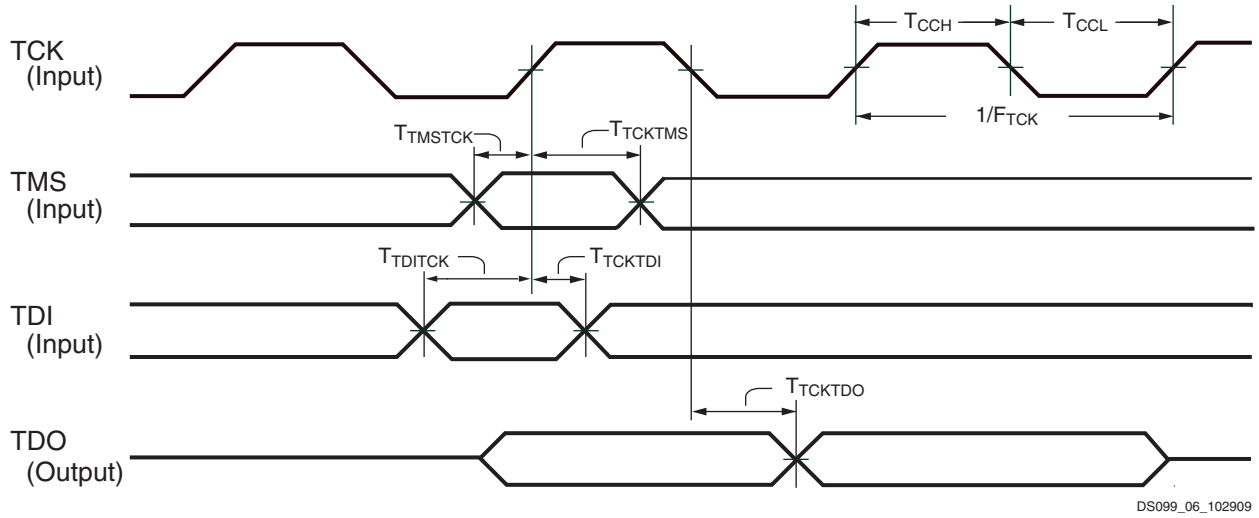


Figure 39: **JTAG Waveforms**

Table 68: **Timing for the JTAG Test Access Port**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin		1.0	11.0	ns
Setup Times					
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin		7.0	–	ns
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin		7.0	–	ns
Hold Times					
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin		0	–	ns
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin		0	–	ns
Clock Timing					
T_{TCKH}	TCK pin High pulse width		5	∞	ns
T_{TCKL}	TCK pin Low pulse width		5	∞	ns
F_{TCK}	Frequency of the TCK signal	JTAG Configuration	0	33	MHz
		Boundary-Scan	0	25	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.

Table 70: **Spartan-3 FPGA Pin Definitions *(Cont'd)***

Pin Name	Direction	Description
TDI	Input	**JTAG Test Data Input:** TDI is the serial data input for all JTAG instruction and data registers. This pin has an internal pull-up resistor to VCCAUX during configuration.
TMS	Input	**JTAG Test Mode Select:** The serial TMS input controls the operation of the JTAG port. This pin has an internal pull-up resistor to VCCAUX during configuration.
TDO	Output	**JTAG Test Data Output:** TDO is the serial data output for all JTAG instruction and data registers. This pin has an internal pull-up resistor to VCCAUX during configuration.
VCCO: I/O bank output voltage supply pins		
VCCO_#	Supply	**Power Supply for Output Buffer Drivers (per bank):** These pins power the output drivers within a specific I/O bank.
VCCAUX: Auxiliary voltage supply pins		
VCCAUX	Supply	**Power Supply for Auxiliary Circuits:** +2.5V power pins for auxiliary circuits, including the Digital Clock Managers (DCMs), the dedicated configuration pins (CONFIG), and the dedicated JTAG pins. All VCCAUX pins must be connected.
VCCINT: Internal core voltage supply pins		
VCCINT	Supply	**Power Supply for Internal Core Logic:** +1.2V power pins for the internal logic. All pins must be connected.
GND: Ground supply pins		
GND	Supply	**Ground:** Ground pins, which are connected to the power supply's return path. All pins must be connected.
N.C.: Unconnected package pins		
N.C.		**Unconnected Package Pin:** These package pins are unconnected.

Notes:

1. All unused inputs and bidirectional pins must be tied either High or Low. For unused enable inputs, apply the level that disables the associated function. One common approach is to activate internal pull-up or pull-down resistors. An alternative approach is to externally connect the pin to either VCCO or GND.
2. All outputs are of the totem-pole type — i.e., they can drive High as well as Low logic levels — except for the cases where "Open Drain" is indicated. The latter can only drive a Low logic level and require a pull-up resistor to produce a High logic level.

Detailed, Functional Pin Descriptions

I/O Type: Unrestricted, General-purpose I/O Pins

After configuration, I/O-type pins are inputs, outputs, bidirectional I/O, three-state outputs, open-drain outputs, or open-source outputs, as defined in the application

Pins labeled "IO" support all SelectIO™ interface signal standards except differential standards. A given device at most only has a few of these pins.

A majority of the general-purpose I/O pins are labeled in the format "IO_Lxxy_#". These pins support all SelectIO signal standards, including the differential standards such as LVDS, ULVDS, BLVDS, RSDS, or LDT.

For additional information, see IOBs, page 10

Table 72: **Dual-Purpose Configuration Pins for Parallel (SelectMAP) Configuration Modes *(Cont'd)***

Pin Name	Direction	Description
BUSY	Output	**Configuration Data Rate Control for Parallel Mode:** In the Slave and Master Parallel modes, BUSY throttles the rate at which configuration data is loaded. BUSY is only necessary if CCLK operates at greater than 50 MHz. Ignore BUSY for frequencies of 50 MHz and below. When BUSY is Low, the FPGA accepts the next configuration data byte on the next rising CCLK edge for which CS_B and RDWR_B are Low. When BUSY is High, the FPGA ignores the next configuration data byte. The next configuration data value must be held or reloaded until the next rising CCLK edge when BUSY is Low. When CS_B is High, BUSY is in a high impedance state. **BUSY** / **Function** 0 / The FPGA is ready to accept the next configuration data byte. 1 / The FPGA is busy processing the current configuration data byte and is not ready to accept the next byte. Hi-Z / If CS_B is High, then BUSY is high impedance. This signal is located in Bank 4 and its output voltage is determined by VCCO_4. The BitGen option Persist permits this pin to retain its configuration function in the User mode.
INIT_B	Bidirectional (open-drain)	**Initializing Configuration Memory/Configuration Error (active-Low):** See description under Serial Configuration Modes, page 112.

JTAG Configuration Mode

In the JTAG configuration mode all dual-purpose configuration pins are unused and behave exactly like user-I/O pins, as shown in Table 79. See Table 75 for Mode Select pin settings required for JTAG mode.

Dual-Purpose Pin I/O Standard During Configuration

During configuration, the dual-purpose pins default to CMOS input and output levels for the associated VCCO voltage supply pins. For example, in the Parallel configuration modes, both VCCO_4 and VCCO_5 are required. If connected to +2.5V, then the associated pins conform to the LVCMOS25 I/O standard. If connected to +3.3V, then the pins drive LVCMOS output levels and accept either LVTTL or LVCMOS input levels.

Dual-Purpose Pin Behavior After Configuration

After the configuration process completes, these pins, if they were borrowed during configuration, become user-I/O pins available to the application. If a dual-purpose configuration pin is not used during the configuration process—*i.e.*, the parallel configuration pins when using serial mode—then the pin behaves exactly like a general-purpose I/O. See I/O Type: Unrestricted, General-purpose I/O Pins section.

DCI: User I/O or Digitally Controlled Impedance Resistor Reference Input

These pins are individual user-I/O pins unless one of the I/O standards used in the bank requires the Digitally Controlled Impedance (DCI) feature. If DCI is used, then 1% precision resistors connected to the VRP_# and VRN_# pins match the impedance on the input or output buffers of the I/O standards that use DCI within the bank. The '#' character in the pin name indicates the associated I/O bank and is an integer, 0 through 7.

There are two DCI pins per I/O bank, except in the CP132 and TQ144 packages, which do not have any DCI inputs for Bank 5.

VRP and VRN Impedance Resistor Reference Inputs

The 1% precision impedance-matching resistor attached to the VRP_# pin controls the pull-up impedance of PMOS transistor in the input or output buffer. Consequently, the VRP_# pin must connect to ground. The 'P' character in "VRP" indicates that this pin controls the I/O buffer's PMOS transistor impedance. The VRP_# pin is used for both single and split termination.

Table 87: **VQ100 Package Pinout *(Cont'd)***

Bank	XC3S50 XC3S200 Pin Name	VQ100 Pin Number	Type
VCCAUX	TDO	P76	JTAG
VCCAUX	TMS	P78	JTAG

User I/Os by Bank

Table 88 indicates how the available user-I/O pins are distributed between the eight I/O banks on the VQ100 package.

Table 88: **User I/Os Per Bank in VQ100 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	6	1	0	2	1	2
	1	7	2	0	2	1	2
Right	2	8	5	0	2	1	0
	3	8	5	0	2	1	0
Bottom	4	10	0	6	2	0	2
	5	8	0	6	0	0	2
Left	6	8	4	0	2	2	0
	7	8	5	0	2	1	0

Table 93: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
N/A	GND	GND	P14	GND
N/A	GND	GND	P25	GND
N/A	VCCAUX	VCCAUX	P193	VCCAUX
N/A	VCCAUX	VCCAUX	P173	VCCAUX
N/A	VCCAUX	VCCAUX	P142	VCCAUX
N/A	VCCAUX	VCCAUX	P121	VCCAUX
N/A	VCCAUX	VCCAUX	P89	VCCAUX
N/A	VCCAUX	VCCAUX	P69	VCCAUX
N/A	VCCAUX	VCCAUX	P38	VCCAUX
N/A	VCCAUX	VCCAUX	P17	VCCAUX
N/A	VCCINT	VCCINT	P192	VCCINT
N/A	VCCINT	VCCINT	P174	VCCINT
N/A	VCCINT	VCCINT	P88	VCCINT
N/A	VCCINT	VCCINT	P70	VCCINT
VCCAUX	CCLK	CCLK	P104	CONFIG
VCCAUX	DONE	DONE	P103	CONFIG
VCCAUX	HSWAP_EN	HSWAP_EN	P206	CONFIG
VCCAUX	M0	M0	P55	CONFIG
VCCAUX	M1	M1	P54	CONFIG
VCCAUX	M2	M2	P56	CONFIG
VCCAUX	PROG_B	PROG_B	P207	CONFIG
VCCAUX	TCK	TCK	P159	JTAG
VCCAUX	TDI	TDI	P208	JTAG
VCCAUX	TDO	TDO	P158	JTAG
VCCAUX	TMS	TMS	P160	JTAG

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
N/A	GND	T16	GND
N/A	VCCAUX	A6	VCCAUX
N/A	VCCAUX	A11	VCCAUX
N/A	VCCAUX	F1	VCCAUX
N/A	VCCAUX	F16	VCCAUX
N/A	VCCAUX	L1	VCCAUX
N/A	VCCAUX	L16	VCCAUX
N/A	VCCAUX	T6	VCCAUX
N/A	VCCAUX	T11	VCCAUX
N/A	VCCINT	D4	VCCINT
N/A	VCCINT	D13	VCCINT
N/A	VCCINT	E5	VCCINT
N/A	VCCINT	E12	VCCINT
N/A	VCCINT	M5	VCCINT
N/A	VCCINT	M12	VCCINT
N/A	VCCINT	N4	VCCINT
N/A	VCCINT	N13	VCCINT
VCCAUX	CCLK	T15	CONFIG
VCCAUX	DONE	R14	CONFIG
VCCAUX	HSWAP_EN	C4	CONFIG
VCCAUX	M0	P3	CONFIG
VCCAUX	M1	T2	CONFIG
VCCAUX	M2	P4	CONFIG
VCCAUX	PROG_B	B3	CONFIG
VCCAUX	TCK	C14	JTAG
VCCAUX	TDI	A2	JTAG
VCCAUX	TDO	A15	JTAG
VCCAUX	TMS	C13	JTAG

FG320 Footprint

		Bank 0									Bank 1								
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
	A	GND	I/O L01N_0 VRP_0	I/O L01P_0 VRN_0	I/O L15N_0	I/O L15P_0	GND	I/O L30N_0	I/O L30P_0	I/O L31P_0 VREF_0	I/O L31N_1 VREF_1	I/O	I/O VREF_1	GND	I/O L16N_1	I/O L10N_1 VREF_1	I/O L01N_1 VRP_1	I/O L01P_1 VRN_1	GND
	B	I/O L16P_7 VREF_7	GND	I/O VREF_0	I/O L09N_0	I/O L25N_0	I/O L25P_0	VCCAUX	VCCO_0	I/O L31N_0	I/O L31P_1	VCCO_1	VCCAUX	I/O	I/O L16P_1	I/O L10P_1	TMS	GND	I/O L16N_2
	C	I/O L16N_7	I/O L01P_7 VRN_7	I/O L01N_7 VRP_7	I/O L09P_0	I/O L10N_0	VCCO_0	I/O L27N_0	I/O L28N_0	GND	GND	I/O L30N_1	I/O L28N_1	VCCO_1	I/O L15N_1	I/O L15P_1	I/O L01N_2 VRP_2	I/O L01P_2 VRN_2	I/O L16P_2
	D	I/O L17N_7	I/O L17P_7	I/O L19P_7	TDI	I/O L10P_0	I/O VREF_0	I/O L27P_0	I/O L28P_0	I/O	I/O	I/O L30P_1	I/O L28P_1	I/O L24P_1	I/O L24N_1	TDO	I/O L19N_2	I/O L17N_2	I/O L17P_2 VREF_2
Bank 7	E	I/O L20P_7	I/O L20N_7	I/O L19N_7 VREF_7	I/O L21N_7	PROG_B	HSWAP_ EN	I/O	I/O L29N_0	I/O L32N_0 GCLK7	I/O L32N_1 GCLK5	I/O L29P_1	I/O L27P_1	I/O L27N_1	TCK	I/O L21P_2	I/O L19P_2	I/O L20N_2	I/O L20P_2
	F	GND	I/O L23P_7	VCCO_7	I/O L21P_7	I/O L22P_7	VCCINT	VCCINT	I/O L29P_0	I/O L32P_0 GCLK6	I/O L32P_1 GCLK4	I/O L29N_1	VCCINT	VCCINT	I/O L22N_2	I/O L21N_2	VCCO_2	I/O L23P_2	GND
	G	I/O L23N_7	VCCAUX	I/O L24P_7	I/O L24N_7	I/O L22N_7	VCCINT	GND	VCCO_0	VCCO_0	VCCO_1	VCCO_1	GND	VCCINT	I/O L22P_2	I/O L24N_2	I/O L24P_2	VCCAUX	I/O L23N_2 VREF_2
	H	I/O L35N_7	I/O L35P_7	I/O L34P_7	I/O L34N_7	I/O L27N_7	I/O L27P_7 VREF_7	VCCO_7	GND	GND	GND	GND	VCCO_2	I/O L27N_2	I/O L27P_2	I/O L34P_2	I/O L34N_2 VREF_2	I/O L35N_2	I/O L35P_2
	J	I/O L39N_7	I/O L39P_7	GND	I/O L40P_7	I/O L40N_7 VREF_7	I/O	VCCO_7	GND			GND	VCCO_2	I/O	I/O L40P_2 VREF_2	I/O L40N_2	GND	I/O L39P_2	I/O L39N_2
	K	I/O L40N_6	I/O L40P_6 VREF_6	GND	I/O L39P_6	I/O L39N_6	I/O	VCCO_6	GND			GND	VCCO_3	I/O L39N_3	I/O L39P_3	I/O	GND	I/O L40N_3 VREF_3	I/O L40P_3
	L	I/O L35P_6	I/O L35N_6	I/O L34N_6 VREF_6	I/O L34P_6	I/O L27P_6	I/O L27N_6	VCCO_6	GND	GND	GND	GND	VCCO_3	I/O L27P_3	I/O L27N_3	I/O L34N_3	I/O L34P_3 VREF_3	I/O L35P_3	I/O L35N_3
	M	I/O L24P_6	VCCAUX	I/O L23N_6	I/O L23P_6	I/O L22P_6	VCCINT	GND	VCCO_5	VCCO_5	VCCO_4	VCCO_4	GND	VCCINT	I/O L22N_3	I/O L23N_3	I/O L23P_3 VREF_3	VCCAUX	I/O L24N_3
Bank 6	N	GND	I/O L24N_6 VREF_6	VCCO_6	I/O L21N_6	I/O L22N_6	VCCINT	VCCINT	I/O	I/O L32N_5 GCLK3	I/O L32N_4 GCLK1	I/O L30N_4 D2	VCCINT	VCCINT	I/O L22P_3	I/O L21P_3	VCCO_3	I/O L24P_3	GND
	P	I/O L20P_6	I/O L20N_6	I/O L19P_6	I/O L21P_6	M0	I/O L27N_5 VREF_5	I/O L27P_5	I/O	I/O L32P_5 GCLK2	I/O L32P_4 GCLK0	I/O L30P_4 D3	I/O	I/O L25P_4	I/O L06N_4 VREF_4	I/O L21N_3	I/O L17N_3	I/O L20P_3	I/O L20N_3
	R	I/O L17P_6 VREF_6	I/O L17N_6	I/O L19N_6	M2	I/O L15P_5	I/O L15N_5	I/O L28N_5 D6	I/O L30N_5	I/O VREF_5	I/O VREF_4	I/O L29N_4	I/O L27P_4 D1	I/O L25N_4	I/O L06P_4	DONE	I/O L17P_3 VREF_3	I/O L19N_3	I/O L19P_3
	T	I/O L16P_6	I/O L01P_6 VRN_6	I/O L01N_6 VRP_6	I/O L06P_5	I/O L06N_5	VCCO_5	I/O L28P_5 D7	I/O L30P_5	GND	GND	I/O L29P_4	I/O L27N_4 DIN D0	VCCO_4	I/O L10N_4	CCLK	I/O L01P_3 VRN_3	I/O L01N_3 VRP_3	I/O L16N_3
	U	I/O L16N_6	GND	M1	I/O L10P_5 VRN_5	I/O L16P_5	I/O	VCCAUX	VCCO_5	I/O L31N_5 D4	I/O L31N_4 INIT_B	VCCO_4	VCCAUX	I/O VREF_4	I/O L10P_4	I/O L09N_4	I/O L01N_4 VRP_4	GND	I/O L16P_3
	V	GND	I/O L01P_5 CS_B	I/O L01N_5 RDWR_B	I/O L10N_5 VRP_5	I/O L16N_5	GND	I/O L29P_5 VREF_5	I/O L29N_5	I/O L31P_5 D5	I/O L31P_4 DOUT BUSY	I/O L28P_4	I/O L28N_4	GND	I/O	I/O L09P_4	I/O L01P_4 VRN_4	I/O VREF_4	GND
		Bank 5									Bank 4								

Bank 2

Bank 3

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Figure 50: **FG320 Package Footprint (Top View)**

156	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	29	**VREF:** User I/O or input voltage reference for bank
16	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input	28	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	12	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	40	**GND:** Ground	8	**VCCAUX:** Auxiliary voltage supply (+2.5V)

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
N/A	GND	GND	P13	GND
N/A	GND	GND	P14	GND
N/A	GND	GND	P20	GND
N/A	GND	GND	Y9	GND
N/A	GND	GND	Y14	GND
N/A	VCCAUX	VCCAUX	A6	VCCAUX
N/A	VCCAUX	VCCAUX	A17	VCCAUX
N/A	VCCAUX	VCCAUX	AB6	VCCAUX
N/A	VCCAUX	VCCAUX	AB17	VCCAUX
N/A	VCCAUX	VCCAUX	F1	VCCAUX
N/A	VCCAUX	VCCAUX	F22	VCCAUX
N/A	VCCAUX	VCCAUX	U1	VCCAUX
N/A	VCCAUX	VCCAUX	U22	VCCAUX
N/A	VCCINT	VCCINT	G7	VCCINT
N/A	VCCINT	VCCINT	G8	VCCINT
N/A	VCCINT	VCCINT	G15	VCCINT
N/A	VCCINT	VCCINT	G16	VCCINT
N/A	VCCINT	VCCINT	H7	VCCINT
N/A	VCCINT	VCCINT	H16	VCCINT
N/A	VCCINT	VCCINT	R7	VCCINT
N/A	VCCINT	VCCINT	R16	VCCINT
N/A	VCCINT	VCCINT	T7	VCCINT
N/A	VCCINT	VCCINT	T8	VCCINT
N/A	VCCINT	VCCINT	T15	VCCINT
N/A	VCCINT	VCCINT	T16	VCCINT
VCCAUX	CCLK	CCLK	AA22	CONFIG
VCCAUX	DONE	DONE	AB21	CONFIG
VCCAUX	HSWAP_EN	HSWAP_EN	B3	CONFIG
VCCAUX	M0	M0	AB2	CONFIG
VCCAUX	M1	M1	AA1	CONFIG
VCCAUX	M2	M2	AB3	CONFIG
VCCAUX	PROG_B	PROG_B	A2	CONFIG
VCCAUX	TCK	TCK	A21	JTAG
VCCAUX	TDI	TDI	B1	JTAG
VCCAUX	TDO	TDO	B22	JTAG
VCCAUX	TMS	TMS	A20	JTAG

FG676: 676-lead Fine-pitch Ball Grid Array

The 676-lead fine-pitch ball grid array package, FG676, supports five different Spartan-3 devices, including the XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000. All five have nearly identical footprints but are slightly different, primarily due to unconnected pins on the XC3S1000 and XC3S1500. For example, because the XC3S1000 has fewer I/O pins, this device has 98 unconnected pins on the FG676 package, labeled as "N.C." In Table 103 and Figure 53, these unconnected pins are indicated with a black diamond symbol (◆). The XC3S1500, however, has only two unconnected pins, also labeled "N.C." in the pinout table but indicated with a black square symbol (■).

All the package pins appear in Table 103 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000 pinouts, then that difference is highlighted in Table 103. If the table entry is shaded grey, then there is an unconnected pin on either the XC3S1000 or XC3S1500 that maps to a user-I/O pin on the XC3S2000, XC3S4000, and XC3S5000. If the table entry is shaded tan, then the unconnected pin on either the XC3S1000 or XC3S1500 maps to a VREF-type pin on the XC3S2000, XC3S4000, and XC3S5000. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S1000 or XC3S1500 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S1000 through to the XC3S5000 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 103: **FG676 Package Pinout**

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
0	IO	IO	IO	IO	IO_L04N_0(3)	A3	I/O
0	IO	IO	IO	IO	IO	A5	I/O
0	IO	IO	IO	IO	IO	A6	I/O
0	IO	IO	IO	IO	IO_L04P_0(3)	C4	I/O
0	N.C. (◆)	IO	IO	IO	IO_L13N_0(3)	C8	I/O
0	IO	IO	IO	IO	IO	C12	I/O
0	IO	IO	IO	IO	IO	E13	I/O
0	IO	IO	IO	IO	IO	H11	I/O
0	IO	IO	IO	IO	IO	H12	I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	B3	VREF
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	F7	VREF
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	G10	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	E5	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	D5	DCI
0	IO_L05N_0	IO_L05N_0	IO_L05N_0	IO_L05N_0	IO_L05N_0	B4	I/O
0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	A4	VREF
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	IO_L06N_0	IO_L06N_0	C5	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	IO_L06P_0	IO_L06P_0	B5	I/O
0	IO_L07N_0	IO_L07N_0	IO_L07N_0	IO_L07N_0	IO_L07N_0	E6	I/O
0	IO_L07P_0	IO_L07P_0	IO_L07P_0	IO_L07P_0	IO_L07P_0	D6	I/O
0	IO_L08N_0	IO_L08N_0	IO_L08N_0	IO_L08N_0	IO_L08N_0	C6	I/O
0	IO_L08P_0	IO_L08P_0	IO_L08P_0	IO_L08P_0	IO_L08P_0	B6	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
0	IO_L09N_0	IO_L09N_0	IO_L09N_0	IO_L09N_0	IO_L09N_0	E7	I/O
0	IO_L09P_0	IO_L09P_0	IO_L09P_0	IO_L09P_0	IO_L09P_0	D7	I/O
0	IO_L10N_0	IO_L10N_0	IO_L10N_0	IO_L10N_0	IO_L10N_0	B7	I/O
0	IO_L10P_0	IO_L10P_0	IO_L10P_0	IO_L10P_0	IO_L10P_0	A7	I/O
0	N.C. (◆)	IO_L11N_0	IO_L11N_0	IO_L11N_0	IO_L11N_0	G8	I/O
0	N.C. (◆)	IO_L11P_0	IO_L11P_0	IO_L11P_0	IO_L11P_0	F8	I/O
0	N.C. (◆)	IO_L12N_0	IO_L12N_0	IO_L12N_0	IO(3)	E8	I/O
0	N.C. (◆)	IO_L12P_0	IO_L12P_0	IO_L12P_0	IO(3)	D8	I/O
0	IO_L15N_0	IO_L15N_0	IO_L15N_0	IO_L15N_0	IO_L13P_0(3)	B8	I/O
0	IO_L15P_0	IO_L15P_0	IO_L15P_0	IO_L15P_0	IO(3)	A8	I/O
0	IO_L16N_0	IO_L16N_0	IO_L16N_0	IO_L16N_0	IO_L16N_0	G9	I/O
0	IO_L16P_0	IO_L16P_0	IO_L16P_0	IO_L16P_0	IO_L16P_0	F9	I/O
0	N.C. (◆)	IO_L17N_0	IO_L17N_0	IO_L17N_0	IO_L17N_0	E9	I/O
0	N.C. (◆)	IO_L17P_0	IO_L17P_0	IO_L17P_0	IO_L17P_0	D9	I/O
0	N.C. (◆)	IO_L18N_0	IO_L18N_0	IO_L18N_0	IO_L18N_0	C9	I/O
0	N.C. (◆)	IO_L18P_0	IO_L18P_0	IO_L18P_0	IO_L18P_0	B9	I/O
0	IO_L19N_0	IO_L19N_0	IO_L19N_0	IO_L19N_0	IO_L19N_0	F10	I/O
0	IO_L19P_0	IO_L19P_0	IO_L19P_0	IO_L19P_0	IO_L19P_0	E10	I/O
0	IO_L22N_0	IO_L22N_0	IO_L22N_0	IO_L22N_0	IO_L22N_0	D10	I/O
0	IO_L22P_0	IO_L22P_0	IO_L22P_0	IO_L22P_0	IO_L22P_0	C10	I/O
0	N.C. (◆)	IO_L23N_0	IO_L23N_0	IO_L23N_0	IO_L23N_0	B10	I/O
0	N.C. (◆)	IO_L23P_0	IO_L23P_0	IO_L23P_0	IO_L23P_0	A10	I/O
0	IO_L24N_0	IO_L24N_0	IO_L24N_0	IO_L24N_0	IO_L24N_0	G11	I/O
0	IO_L24P_0	IO_L24P_0	IO_L24P_0	IO_L24P_0	IO_L24P_0	F11	I/O
0	IO_L25N_0	IO_L25N_0	IO_L25N_0	IO_L25N_0	IO_L25N_0	E11	I/O
0	IO_L25P_0	IO_L25P_0	IO_L25P_0	IO_L25P_0	IO_L25P_0	D11	I/O
0	N.C. (◆)	IO_L26N_0	IO_L26N_0	IO_L26N_0	IO_L26N_0	B11	I/O
0	N.C. (◆)	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	A11	VREF
0	IO_L27N_0	IO_L27N_0	IO_L27N_0	IO_L27N_0	IO_L27N_0	G12	I/O
0	IO_L27P_0	IO_L27P_0	IO_L27P_0	IO_L27P_0	IO_L27P_0	H13	I/O
0	IO_L28N_0	IO_L28N_0	IO_L28N_0	IO_L28N_0	IO_L28N_0	F12	I/O
0	IO_L28P_0	IO_L28P_0	IO_L28P_0	IO_L28P_0	IO_L28P_0	E12	I/O
0	IO_L29N_0	IO_L29N_0	IO_L29N_0	IO_L29N_0	IO_L29N_0	B12	I/O
0	IO_L29P_0	IO_L29P_0	IO_L29P_0	IO_L29P_0	IO_L29P_0	A12	I/O
0	IO_L30N_0	IO_L30N_0	IO_L30N_0	IO_L30N_0	IO_L30N_0	G13	I/O
0	IO_L30P_0	IO_L30P_0	IO_L30P_0	IO_L30P_0	IO_L30P_0	F13	I/O
0	IO_L31N_0	IO_L31N_0	IO_L31N_0	IO_L31N_0	IO_L31N_0	D13	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C13	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B13	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A13	GCLK
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	C7	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	C11	VCCO

User I/Os by Bank

Table 104 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1000 in the FG676 package. Similarly, Table 105 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1500 in the FG676 package. Finally, Table 106 shows the same information for the XC3S2000, XC3S4000, and XC3S5000 in the FG676 package.

Table 104: **User I/Os Per Bank for XC3S1000 in FG676 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	49	40	0	2	5	2
	1	50	41	0	2	5	2
Right	2	48	41	0	2	5	0
	3	48	41	0	2	5	0
Bottom	4	50	35	6	2	5	2
	5	50	35	6	2	5	2
Left	6	48	41	0	2	5	0
	7	48	41	0	2	5	0

Table 105: **User I/Os Per Bank for XC3S1500 in FG676 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	62	52	0	2	6	2
	1	61	51	0	2	6	2
Right	2	60	52	0	2	6	0
	3	60	52	0	2	6	0
Bottom	4	63	47	6	2	6	2
	5	61	45	6	2	6	2
Left	6	60	52	0	2	6	0
	7	60	52	0	2	6	0

Table 106: **User I/Os Per Bank for XC3S2000, XC3S4000, and XC3S5000 in FG676 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	62	52	0	2	6	2
	1	61	51	0	2	6	2
Right	2	61	53	0	2	6	0
	3	60	52	0	2	6	0
Bottom	4	63	47	6	2	6	2
	5	61	45	6	2	6	2
Left	6	61	53	0	2	6	0
	7	60	52	0	2	6	0

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	GND	GND	Y14	GND
N/A	GND	GND	Y15	GND
N/A	GND	GND	Y16	GND
N/A	GND	GND	Y17	GND
N/A	GND	GND	Y18	GND
N/A	GND	GND	Y19	GND
N/A	GND	GND	Y20	GND
N/A	GND	GND	Y21	GND
N/A	N.C. (◆)	N.C. (■)	AK31	N.C.
N/A	VCCAUX	VCCAUX	AD30	VCCAUX
N/A	VCCAUX	VCCAUX	AD5	VCCAUX
N/A	VCCAUX	VCCAUX	AG16	VCCAUX
N/A	VCCAUX	VCCAUX	AG19	VCCAUX
N/A	VCCAUX	VCCAUX	AJ30	VCCAUX
N/A	VCCAUX	VCCAUX	AJ5	VCCAUX
N/A	VCCAUX	VCCAUX	AK11	VCCAUX
N/A	VCCAUX	VCCAUX	AK15	VCCAUX
N/A	VCCAUX	VCCAUX	AK20	VCCAUX
N/A	VCCAUX	VCCAUX	AK24	VCCAUX
N/A	VCCAUX	VCCAUX	AK29	VCCAUX
N/A	VCCAUX	VCCAUX	AK6	VCCAUX
N/A	VCCAUX	VCCAUX	E11	VCCAUX
N/A	VCCAUX	VCCAUX	E15	VCCAUX
N/A	VCCAUX	VCCAUX	E20	VCCAUX
N/A	VCCAUX	VCCAUX	E24	VCCAUX
N/A	VCCAUX	VCCAUX	E29	VCCAUX
N/A	VCCAUX	VCCAUX	E6	VCCAUX
N/A	VCCAUX	VCCAUX	F30	VCCAUX
N/A	VCCAUX	VCCAUX	F5	VCCAUX
N/A	VCCAUX	VCCAUX	H16	VCCAUX
N/A	VCCAUX	VCCAUX	H19	VCCAUX
N/A	VCCAUX	VCCAUX	L30	VCCAUX
N/A	VCCAUX	VCCAUX	L5	VCCAUX
N/A	VCCAUX	VCCAUX	R30	VCCAUX
N/A	VCCAUX	VCCAUX	R5	VCCAUX
N/A	VCCAUX	VCCAUX	T27	VCCAUX
N/A	VCCAUX	VCCAUX	T8	VCCAUX
N/A	VCCAUX	VCCAUX	W27	VCCAUX
N/A	VCCAUX	VCCAUX	W8	VCCAUX
N/A	VCCAUX	VCCAUX	Y30	VCCAUX

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	VCCAUX	VCCAUX	Y5	VCCAUX
N/A	VCCINT	VCCINT	AA13	VCCINT
N/A	VCCINT	VCCINT	AA22	VCCINT
N/A	VCCINT	VCCINT	AB13	VCCINT
N/A	VCCINT	VCCINT	AB14	VCCINT
N/A	VCCINT	VCCINT	AB15	VCCINT
N/A	VCCINT	VCCINT	AB16	VCCINT
N/A	VCCINT	VCCINT	AB19	VCCINT
N/A	VCCINT	VCCINT	AB20	VCCINT
N/A	VCCINT	VCCINT	AB21	VCCINT
N/A	VCCINT	VCCINT	AB22	VCCINT
N/A	VCCINT	VCCINT	AC12	VCCINT
N/A	VCCINT	VCCINT	AC17	VCCINT
N/A	VCCINT	VCCINT	AC18	VCCINT
N/A	VCCINT	VCCINT	AC23	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	M23	VCCINT
N/A	VCCINT	VCCINT	N13	VCCINT
N/A	VCCINT	VCCINT	N14	VCCINT
N/A	VCCINT	VCCINT	N15	VCCINT
N/A	VCCINT	VCCINT	N16	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	N20	VCCINT
N/A	VCCINT	VCCINT	N21	VCCINT
N/A	VCCINT	VCCINT	N22	VCCINT
N/A	VCCINT	VCCINT	P13	VCCINT
N/A	VCCINT	VCCINT	P22	VCCINT
N/A	VCCINT	VCCINT	R13	VCCINT
N/A	VCCINT	VCCINT	R22	VCCINT
N/A	VCCINT	VCCINT	T13	VCCINT
N/A	VCCINT	VCCINT	T22	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT
N/A	VCCINT	VCCINT	U23	VCCINT
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	V23	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	W22	VCCINT
N/A	VCCINT	VCCINT	Y13	VCCINT