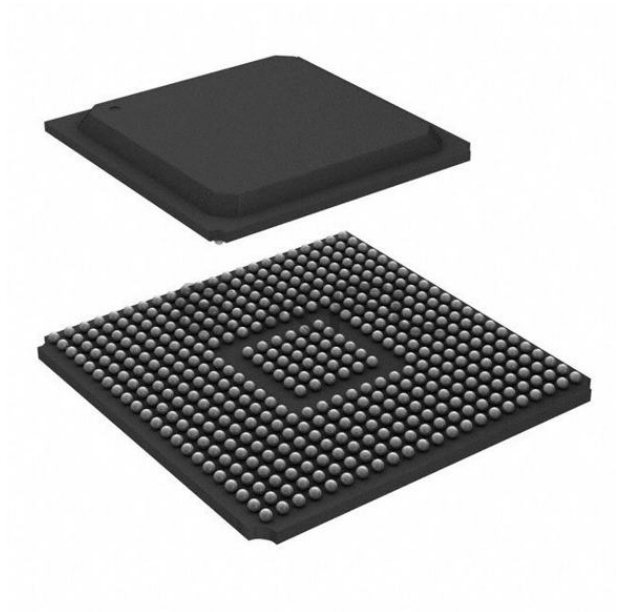
AMD Xilinx - XC3S2000-4FGG456I Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	5120
Number of Logic Elements/Cells	46080
Total RAM Bits	737280
Number of I/O	333
Number of Gates	2000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s2000-4fgg456i

IOBs

For additional information, refer to the chapter entitled “Using I/O Resources” in UG331: *Spartan-3 Generation FPGA User Guide*.

IOB Overview

The Input/Output Block (IOB) provides a programmable, bidirectional interface between an I/O pin and the FPGA’s internal logic.

A simplified diagram of the IOB’s internal structure appears in Figure 7. There are three main signal paths within the IOB: the output path, input path, and 3-state path. Each path has its own pair of storage elements that can act as either registers or latches. For more information, see the Storage Element Functions section. The three main signal paths are as follows:

- The input path carries data from the pad, which is bonded to a package pin, through an optional programmable delay element directly to the I line. There are alternate routes through a pair of storage elements to the IQ1 and IQ2 lines. The IOB outputs I, IQ1, and IQ2 all lead to the FPGA’s internal logic. The delay element can be set to ensure a hold time of zero.
- The output path, starting with the O1 and O2 lines, carries data from the FPGA’s internal logic through a multiplexer and then a three-state driver to the IOB pad. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.
- The 3-state path determines when the output driver is high impedance. The T1 and T2 lines carry data from the FPGA’s internal logic through a multiplexer to the output driver. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements. When the T1 or T2 lines are asserted High, the output driver is high-impedance (floating, hi-Z). The output driver is active-Low enabled.
- All signal paths entering the IOB, including those associated with the storage elements, have an inverter option. Any inverter placed on these paths is automatically absorbed into the IOB.

Storage Element Functions

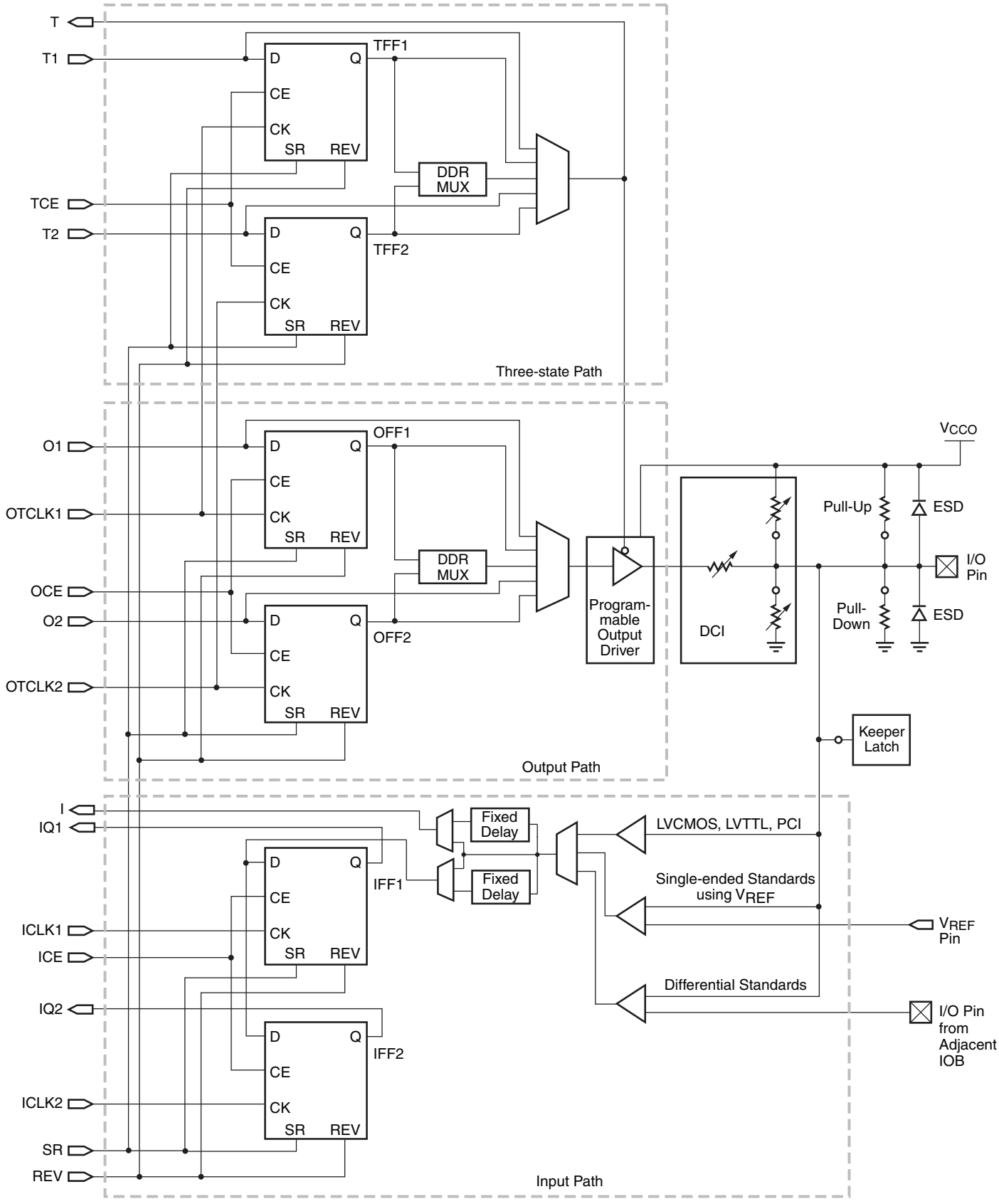
There are three pairs of storage elements in each IOB, one pair for each of the three paths. It is possible to configure each of these storage elements as an edge-triggered D-type flip-flop (FD) or a level-sensitive latch (LD).

The storage-element-pair on either the Output path or the Three-State path can be used together with a special multiplexer to produce Double-Data-Rate (DDR) transmission. This is accomplished by taking data synchronized to the clock signal’s rising edge and converting them to bits synchronized on both the rising and the falling edge. The combination of two registers and a multiplexer is referred to as a Double-Data-Rate D-type flip-flop (FDDR). See Double-Data-Rate Transmission, page 12 for more information.

The signal paths associated with the storage element are described in Table 5.

Table 5: **Storage Element Signal Description**

Storage Element Signal	Description	Function
D	Data input	Data at this input is stored on the active edge of CK enabled by CE. For latch operation when the input is enabled, data passes directly to the output Q.
Q	Data output	The data on this output reflects the state of the storage element. For operation as a latch in transparent mode, Q will mirror the data at D.
CK	Clock input	A signal’s active edge on this input with CE asserted, loads data into the storage element.
CE	Clock Enable input	When asserted, this input enables CK. If not connected, CE defaults to the asserted state.
SR	Set/Reset	Forces storage element into the state specified by the SRHIGH/SRLOW attributes. The SYNC/ASYNC attribute setting determines if the SR input is synchronized to the clock or not.
REV	Reverse	Used together with SR. Forces storage element into the state opposite from what SR does.



Note: All IOB signals originating from the FPGA's internal logic have an optional polarity inverter.

DS099-2_01_091410

Figure 7: **Simplified IOB Diagram**

The DLL component has two clock inputs, CLKIN and CLKFB, as well as seven clock outputs, CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV as described in Table 16. The clock outputs drive simultaneously; however, the High Frequency mode only supports a subset of the outputs available in the Low Frequency mode. See DLL Frequency Modes, page 35. Signals that initialize and report the state of the DLL are discussed in The Status Logic Component, page 41.

Table 16: **DLL Signals**

Signal	Direction	Description	Mode Support	
			Low Frequency	High Frequency
CLKIN	Input	Accepts original clock signal.	Yes	Yes
CLKFB	Input	Accepts either CLK0 or CLK2X as feed back signal. (Set CLK_FEEDBACK attribute accordingly).	Yes	Yes
CLK0	Output	Generates clock signal with same frequency and phase as CLKIN.	Yes	Yes
CLK90	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 90°.	Yes	No
CLK180	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 180°.	Yes	Yes
CLK270	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 270°.	Yes	No
CLK2X	Output	Generates clock signal with same phase as CLKIN, only twice the frequency.	Yes	No
CLK2X180	Output	Generates clock signal with twice the frequency of CLKIN, phase-shifted 180° with respect to CLKIN.	Yes	No
CLKDV	Output	Divides the CLKIN frequency by CLKDV_DIVIDE value to generate lower frequency clock signal that is phase-aligned to CLKIN.	Yes	Yes

The clock signal supplied to the CLKIN input serves as a reference waveform, with which the DLL seeks to align the feedback signal at the CLKFB input. When eliminating clock skew, the common approach to using the DLL is as follows: The CLK0 signal is passed through the clock distribution network to all the registers it synchronizes. These registers are either internal or external to the FPGA. After passing through the clock distribution network, the clock signal returns to the DLL via a feedback line called CLKFB. The control block inside the DLL measures the phase error between CLKFB and CLKIN. This phase error is a measure of the clock skew that the clock distribution network introduces. The control block activates the appropriate number of delay elements to cancel out the clock skew. Once the DLL has brought the CLK0 signal in phase with the CLKIN signal, it asserts the LOCKED output, indicating a “lock” on to the CLKIN signal.

DLL Attributes and Related Functions

A number of different functional options can be set for the DLL component through the use of the attributes described in Table 17. Each attribute is described in detail in the sections that follow:

Table 17: **DLL Attributes**

Attribute	Description	Values
CLK_FEEDBACK	Chooses either the CLK0 or CLK2X output to drive the CLKFB input	NONE, 1X, 2X
DLL_FREQUENCY_MODE	Chooses between High Frequency and Low Frequency modes	LOW, HIGH
CLKIN_DIVIDE_BY_2	Halves the frequency of the CLKIN signal just as it enters the DCM	TRUE, FALSE
CLKDV_DIVIDE	Selects constant used to divide the CLKIN input frequency to generate the CLKDV output frequency	1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6.0, 6.5, 7.0, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.
DUTY_CYCLE_CORRECTION	Enables 50% duty cycle correction for the CLK0, CLK90, CLK180, and CLK270 outputs	TRUE, FALSE

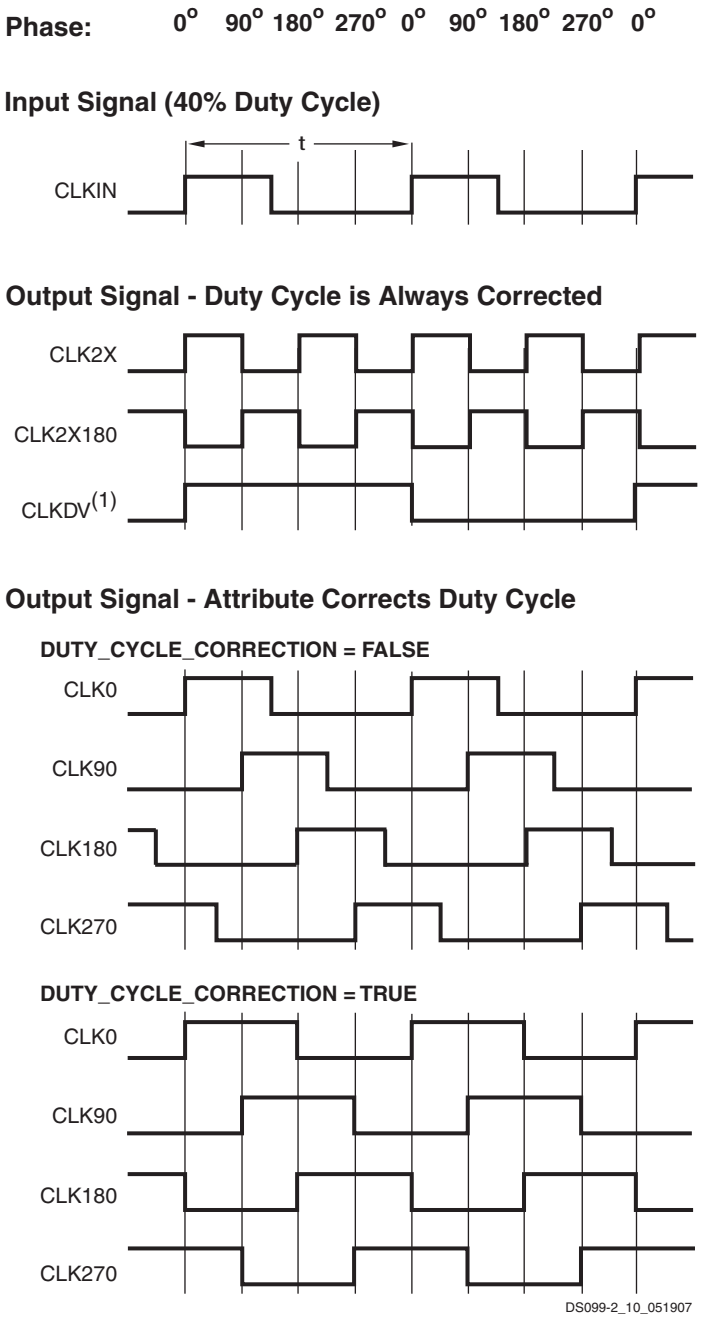


Figure 22: **Characteristics of the DLL Clock Outputs**

Digital Frequency Synthesizer (DFS)

The DFS component generates clock signals the frequency of which is a product of the clock frequency at the CLKIN input and a ratio of two user-determined integers. Because of the wide range of possible output frequencies such a ratio permits, the DFS feature provides still further flexibility than the DLL's basic synthesis options as described in the preceding section. The DFS component's two dedicated outputs, CLKFX and CLKFX180, are defined in Table 19.

The signal at the CLKFX180 output is essentially an inversion of the CLKFX signal. These two outputs always exhibit a 50% duty cycle. This is true even when the CLKIN signal does not. These DFS clock outputs are driven at the same time as the DLL's seven clock outputs.

The numerator of the ratio is the integer value assigned to the attribute CLKFX_MULTIPLY and the denominator is the integer value assigned to the attribute CLKFX_DIVIDE. These attributes are described in Table 18.

Switching Characteristics

All Spartan-3 devices are available in two speed grades: –4 and the higher performance –5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reported delays may still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Production-quality systems must use FPGA designs compiled using a Production status speed file. FPGAs designs using a less mature speed file designation may only be used during system prototyping or preproduction qualification. FPGA designs using Advance or Preliminary status speed files should never be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

Xilinx ISE Software Updates: http://www.xilinx.com/support/download/index.htm

All specified limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the following applies: Parameter values apply to all Spartan-3 devices. All parameters representing voltages are measured with respect to GND.

Selected timing parameters and their representative values are included below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3 FPGA v1.38 speed files are the original source for many but not all of the values. The v1.38 speed files are available in Xilinx Integrated Software Environment (ISE) software version 8.2i.

The speed grade designations for these files are shown in Table 39. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 39: **Spartan-3 FPGA Speed Grade Designations (ISE v8.2i or Later)**

Device	Advance	Preliminary	Production
XC3S50			-4, -5 (v1.37 and later)
XC3S200			
XC3S400			
XC3S1000			
XC3S1500			
XC3S2000			
XC3S4000			
XC3S5000			-4, -5 (v1.38 and later)

Table 43: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Propagation Times						
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2), IOBDELAY = NONE	XC3S50	2.01	2.31	ns
			XC3S200	1.50	1.72	ns
			XC3S400	1.50	1.72	ns
			XC3S1000	2.01	2.31	ns
			XC3S1500	2.01	2.31	ns
			XC3S2000	2.01	2.31	ns
			XC3S4000	2.09	2.41	ns
			XC3S5000	2.18	2.51	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2), IOBDELAY = IFD	XC3S50	4.75	5.46	ns
			XC3S200	4.89	5.62	ns
			XC3S400	4.76	5.48	ns
			XC3S1000	5.38	6.18	ns
			XC3S1500	5.76	6.62	ns
			XC3S2000	7.04	8.09	ns
			XC3S4000	7.52	8.65	ns
			XC3S5000	7.69	8.84	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 44.

Table 44: **Input Timing Adjustments for IOB**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
GTL, GTL_DCI	0.44	0.50	ns
GTLP, GTLP_DCI	0.36	0.42	ns
HSLVDCI_15	0.51	0.59	ns
HSLVDCI_18	0.29	0.33	ns
HSLVDCI_25	0.51	0.59	ns
HSLVDCI_33	0.51	0.59	ns
HSTL_I, HSTL_I_DCI	0.51	0.59	ns
HSTL_III, HSTL_III_DCI	0.37	0.42	ns
HSTL_I_18, HSTL_I_DCI_18	0.36	0.41	ns
HSTL_II_18, HSTL_II_DCI_18	0.39	0.45	ns
HSTL_III_18, HSTL_III_DCI_18	0.45	0.52	ns
LVCMOS12	0.63	0.72	ns

Table 48: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
DIFF_SSTL2_II	-	V_{ICM} – 0.75	V_{ICM} + 0.75	50	1.25	V_{ICM}
DIFF_SSTL2_II_DCI						

Notes:

1. Descriptions of the relevant symbols are as follows:
   VREF – The reference voltage for setting the input switching threshold
   VICM – The common mode input voltage
   VM – Voltage of measurement point on signal transition
   VL – Low-level test voltage at Input pin
   VH – High-level test voltage at Input pin
   RT – Effective termination resistance, which takes on a value of 1MW when no parallel termination is required
   VT – Termination voltage
2. The load capacitance (CL) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Using IBIS Models to Simulate Load Conditions in Application

IBIS Models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 48, V_T, R_T, and V_M. Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF}, is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link.

http://www.xilinx.com/support/download/index.htm

Simulate delays for a given application according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 35. Use parameter values V_T, R_T, and V_M from Table 48. C_{REF} is zero.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase (or decrease) in delay should be added to (or subtracted from) the appropriate Output standard adjustment (Table 47) to yield the worst-case delay of the PCB trace.

Table 59: **Switching Characteristics for the DLL *(Cont'd)***

Symbol	Description	Frequency Mode / FCLKIN Range	Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Lock Time								
LOCK_DLL	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	18 MHz ≤ F_{CLKIN} ≤ 30 MHz	All	–	2.88	–	2.88	ms
		30 MHz < F_{CLKIN} ≤ 40 MHz		–	2.16	–	2.16	ms
		40 MHz < F_{CLKIN} ≤ 50 MHz		–	1.20	–	1.20	ms
		50 MHz < F_{CLKIN} ≤ 60 MHz		–	0.60	–	0.60	ms
		F_{CLKIN} > 60 MHz		–	0.48	–	0.48	ms
Delay Lines								
DCM_TAP	Delay tap resolution	All	All	30.0	60.0	30.0	60.0	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32 and Table 58.
2. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
3. Only mask revision 'E' and later devices (see Mask and Fab Revisions, page 58) and all revisions of the XC3S50 and the XC3S1000 support DLL feedback using the CLK2X output. For all other Spartan-3 devices, use feedback from the CLK0 output (instead of the CLK2X output) and set the CLK_FEEDBACK attribute to 1X.
4. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
5. This specification only applies if the attribute DUTY_CYCLE_CORRECTION = TRUE.

Digital Frequency Synthesizer (DFS)

Table 60: **Recommended Operating Conditions for the DFS**

Symbol		Description	Frequency Mode	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input	All	1	280	1	280	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input	Low	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF			High	–	±150	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input	All	–	±1	–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 58.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.

Revision History

Date	Version	Description
04/11/03	1.0	Initial Xilinx release.
07/11/03	1.1	Extended Absolute Maximum Rating for junction temperature in Table 28. Added numbers for typical quiescent supply current (Table 34) and DLL timing.
02/06/04	1.2	Revised V_{IN} maximum rating (Table 28). Added power-on requirements (Table 30), leakage current number (Table 33), and differential output voltage levels (Table 38) for Rev. 0. Published new quiescent current numbers (Table 34). Updated pull-up and pull-down resistor strengths (Table 33). Added LVDCI_DV2 and LVPECL standards (Table 37 and Table 38). Changed CCLK setup time (Table 66 and Table 67).
03/04/04	1.3	Added timing numbers from v1.29 speed files as well as DCM timing (Table 58 through Table 63).
08/24/04	1.4	Added reference to errata documents on page 49. Clarified Absolute Maximum Ratings and added ESD information (Table 28). Explained V_{CCO} ramp time measurement (Table 30). Clarified I_L specification (Table 33). Updated quiescent current numbers and added information on power-on and surplus current (Table 34). Adjusted V_{REF} range for HSTL_III and HSTL_I_18 and changed V_{IH} min for LVCMOS12 (Table 35). Added note limiting V_{TT} range for SSTL2_II signal standards (Table 36). Calculated V_{OH} and V_{OL} levels for differential standards (Table 38). Updated Switching Characteristics with speed file v1.32 (Table 40 through Table 48 and Table 51 through Table 56). Corrected IOB test conditions (Table 41). Updated DCM timing with latest characterization data (Table 58 through Table 62). Improved DCM CLKIN pulse width specification (Table 58). Recommended use of Virtex-II FPGA Jitter calculator (Table 61). Improved DCM PSCLK pulse width specification (Table 62). Changed Phase Shifter lock time parameter (Table 63). Because the BitGen option Centered_x#_y# is not necessary for Variable Phase Shift mode, removed BitGen command table and referring text. Adjusted maximum CCLK frequency for the slave serial and parallel configuration modes (Table 66). Inverted CCLK waveform (Figure 37). Adjusted JTAG setup times (Table 68).
12/17/04	1.5	Updated timing parameters to match v1.35 speed file. Improved V_{CCO} ramp time specification (Table 30). Added a note limiting the rate of change of V_{CCAUX} (Table 32). Added typical quiescent current values for the XC3S2000, XC3S4000, and XC3S5000 (Table 34). Increased I_{OH} and I_{OL} for SSTL2-I and SSTL2-II standards (Table 36). Added SSO guidelines for the VQ, TQ, and PQ packages as well as edited SSO guidelines for the FT and FG packages (Table 50). Added maximum CCLK frequencies for configuration using compressed bitstreams (Table 66 and Table 67). Added specifications for the HSLVDCI standards (Table 35, Table 36, Table 44, Table 47, Table 48, and Table 50).
08/19/05	1.6	Updated timing parameters to match v1.37 speed file. All Spartan-3 FPGA part types, except XC3S5000, promoted to Production status. Removed V_{CCO} ramp rate restriction from all mask revision 'E' and later devices (Table 30). Added equivalent resistance values for internal pull-up and pull-down resistors (Table 33). Added worst-case quiescent current values for XC3S2000, XC3S4000, XC3S5000 (Table 34). Added industrial temperature range specification and improved typical quiescent current values (Table 34). Improved the DLL minimum clock input frequency specification from 24 MHz down to 18 MHz (Table 58). Improved the DFS minimum and maximum clock output frequency specifications (Table 60, Table 61). Added new miscellaneous DCM specifications (Table 64), primarily affecting Industrial temperature range applications. Updated Simultaneously Switching Output Guidelines and Table 50 for QFP packages. Added information on SSTL18_II I/O standard and timing to support DDR2 SDRAM interfaces. Added differential (or complementary single-ended) DIFF_HSTL_II_18 and DIFF_SSTL2_II I/O standards, including DCI terminated versions. Added electro-static discharge (ESD) data for the XC3S2000 and larger FPGAs (Table 28). Added link to Spartan-3 FPGA errata notices and how to receive automatic notifications of data sheet or errata changes.
04/03/06	2.0	Upgraded Module 3, removing Preliminary status. Moved XC3S5000 to Production status in Table 39. Finalized I/O timing on XC3S5000 for v1.38 speed files. Added minimum timing values for various logic and I/O paths. Corrected labels for R_{PU} and R_{PD} and updated R_{PD} conditions for in Table 33. Added final mask revision 'E' specifications for LVDS_25, RSDS_25, LVDSEXT_25 differential outputs to Table 38. Added BLVDS termination requirements to Figure 34. Improved recommended Simultaneous Switching Outputs (SSOs) limits in Table 50 for quad-flat packaged based on silicon testing using devices soldered on a printed circuit board. Updated Note 2 in Table 63. Updated Note 6 in Table 30. Added INIT_B minimum pulse width specification, T_{INIT}, to Table 65.
04/26/06	2.1	Updated document links.

Differential Pair Labeling

A pin supports differential standards if the pin is labeled in the format “Lxxy_#”. The pin name suffix has the following significance. Figure 40 provides a specific example showing a differential input to and a differential output from Bank 2.

- ‘L’ indicates differential capability.
- "xx" is a two-digit integer, unique for each bank, that identifies a differential pin-pair.
- ‘y’ is replaced by ‘P’ for the true signal or ‘N’ for the inverted. These two pins form one differential pin-pair.
- ‘#’ is an integer, 0 through 7, indicating the associated I/O bank.

If unused, these pins are in a high impedance state. The Bitstream generator option UnusedPin enables a pull-up or pull-down resistor on all unused I/O pins.

Behavior from Power-On through End of Configuration

During the configuration process, all pins that are not actively involved in the configuration process are in a high-impedance state. The CONFIG- and JTAG-type pins have an internal pull-up resistor to VCCAUX during configuration. For all other I/O pins, the HSWAP_EN input determines whether or not pull-up resistors are activated during configuration. HSWAP_EN = 0 enables the pull-up resistors. HSWAP_EN = 1 disables the pull-up resistors allowing the pins to float, which is the desired state for hot-swap applications.

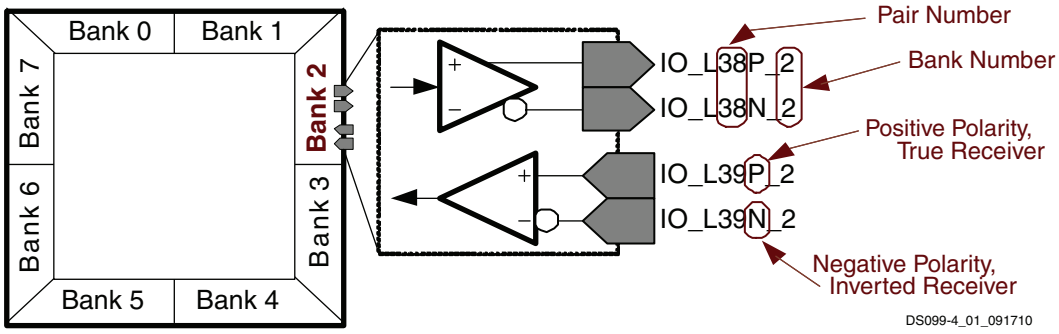


Figure 40: **Differential Pair Labelling**

DUAL Type: Dual-Purpose Configuration and I/O Pins

These pins serve dual purposes. The user-I/O pins are temporarily borrowed during the configuration process to load configuration data into the FPGA. After configuration, these pins are then usually available as a user I/O in the application. If a pin is not applicable to the specific configuration mode—controlled by the mode select pins M2, M1, and M0—then the pin behaves as an I/O-type pin.

There are 12 dual-purpose configuration pins on every package, six of which are part of I/O Bank 4, the other six part of I/O Bank 5. Only a few of the pins in Bank 4 are used in the Serial configuration modes.

See Pin Behavior During Configuration, page 122.

Serial Configuration Modes

This section describes the dual-purpose pins used during either Master or Slave Serial mode. See Table 75 for Mode Select pin settings required for Serial modes. All such pins are in Bank 4 and powered by VCCO_4.

In both the Master and Slave Serial modes, DIN is the serial configuration data input. The D1-D7 inputs are unused in serial mode and behave like general-purpose I/O pins.

In all the cases, the configuration data is synchronized to the rising edge of the CCLK clock signal.

The DIN, DOUT, and INIT_B pins can be retained in the application to support reconfiguration by setting the Persist bitstream generation option. However, the serial modes do not support device readback.

CP132: 132-Ball Chip-Scale Package

Note: The CP132 and CPG132 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

The pinout and footprint for the XC3S50 in the 132-ball chip-scale package, CP132, appear in Table 89 and Figure 45.

All the package pins appear in Table 89 and are sorted by bank number, then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The CP132 footprint has eight I/O banks. However, the voltage supplies for the two I/O banks along an edge are connected together internally. Consequently, there are four output voltage supplies, labeled VCCO_TOP, VCCO_RIGHT, VCCO_BOTTOM, and VCCO_LEFT.

Pinout Table

Table 89: **CP132 Package Pinout**

Bank	XC3S50 Pin Name	CP132 Ball	Type
0	IO_L01N_0/VRP_0	A3	DCI
0	IO_L01P_0/VRN_0	C4	DCI
0	IO_L27N_0	C5	I/O
0	IO_L27P_0	B5	I/O
0	IO_L30N_0	B6	I/O
0	IO_L30P_0	A6	I/O
0	IO_L31N_0	C7	I/O
0	IO_L31P_0/VREF_0	B7	VREF
0	IO_L32N_0/GCLK7	A7	GCLK
0	IO_L32P_0/GCLK6	C8	GCLK
1	IO_L01N_1/VRP_1	A13	DCI
1	IO_L01P_1/VRN_1	B13	DCI
1	IO_L27N_1	C11	I/O
1	IO_L27P_1	A12	I/O
1	IO_L28N_1	A11	I/O
1	IO_L28P_1	B11	I/O
1	IO_L31N_1/VREF_1	C9	VREF
1	IO_L31P_1	A10	I/O
1	IO_L32N_1/GCLK5	A8	GCLK
1	IO_L32P_1/GCLK4	A9	GCLK
2	IO_L01N_2/VRP_2	D12	DCI
2	IO_L01P_2/VRN_2	C14	DCI
2	IO_L20N_2	E12	I/O
2	IO_L20P_2	E13	I/O
2	IO_L21N_2	E14	I/O
2	IO_L21P_2	F12	I/O
2	IO_L23N_2/VREF_2	F13	VREF
2	IO_L23P_2	F14	I/O
2	IO_L24N_2	G12	I/O

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
4	IO_L31P_4/ DOUT/BUSY	V10	DUAL
4	IO_L32N_4/GCLK1	N10	GCLK
4	IO_L32P_4/GCLK0	P10	GCLK
4	VCCO_4	M10	VCCO
4	VCCO_4	M11	VCCO
4	VCCO_4	T13	VCCO
4	VCCO_4	U11	VCCO
5	IO	N8	I/O
5	IO	P8	I/O
5	IO	U6	I/O
5	IO/VREF_5	R9	VREF
5	IO_L01N_5/RDWR_B	V3	DUAL
5	IO_L01P_5/CS_B	V2	DUAL
5	IO_L06N_5	T5	I/O
5	IO_L06P_5	T4	I/O
5	IO_L10N_5/VRP_5	V4	DCI
5	IO_L10P_5/VRN_5	U4	DCI
5	IO_L15N_5	R6	I/O
5	IO_L15P_5	R5	I/O
5	IO_L16N_5	V5	I/O
5	IO_L16P_5	U5	I/O
5	IO_L27N_5/VREF_5	P6	VREF
5	IO_L27P_5	P7	I/O
5	IO_L28N_5/D6	R7	DUAL
5	IO_L28P_5/D7	T7	DUAL
5	IO_L29N_5	V8	I/O
5	IO_L29P_5/VREF_5	V7	VREF
5	IO_L30N_5	R8	I/O
5	IO_L30P_5	T8	I/O
5	IO_L31N_5/D4	U9	DUAL
5	IO_L31P_5/D5	V9	DUAL
5	IO_L32N_5/GCLK3	N9	GCLK
5	IO_L32P_5/GCLK2	P9	GCLK
5	VCCO_5	M8	VCCO
5	VCCO_5	M9	VCCO
5	VCCO_5	T6	VCCO
5	VCCO_5	U8	VCCO
6	IO	K6	I/O
6	IO_L01N_6/VRP_6	T3	DCI

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
1	IO_L15P_1	IO_L15P_1	E17	I/O
1	IO_L16N_1	IO_L16N_1	B17	I/O
1	IO_L16P_1	IO_L16P_1	C17	I/O
1	N.C. (◆)	IO_L19N_1	C16	I/O
1	N.C. (◆)	IO_L19P_1	D16	I/O
1	N.C. (◆)	IO_L22N_1	A16	I/O
1	N.C. (◆)	IO_L22P_1	B16	I/O
1	IO_L24N_1	IO_L24N_1	D15	I/O
1	IO_L24P_1	IO_L24P_1	E15	I/O
1	IO_L25N_1	IO_L25N_1	B15	I/O
1	IO_L25P_1	IO_L25P_1	A15	I/O
1	IO_L27N_1	IO_L27N_1	D14	I/O
1	IO_L27P_1	IO_L27P_1	E14	I/O
1	IO_L28N_1	IO_L28N_1	A14	I/O
1	IO_L28P_1	IO_L28P_1	B14	I/O
1	IO_L29N_1	IO_L29N_1	C13	I/O
1	IO_L29P_1	IO_L29P_1	D13	I/O
1	IO_L30N_1	IO_L30N_1	A13	I/O
1	IO_L30P_1	IO_L30P_1	B13	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D12	VREF
1	IO_L31P_1	IO_L31P_1	E12	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B12	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C12	GCLK
1	VCCO_1	VCCO_1	C15	VCCO
1	VCCO_1	VCCO_1	F15	VCCO
1	VCCO_1	VCCO_1	G12	VCCO
1	VCCO_1	VCCO_1	G13	VCCO
1	VCCO_1	VCCO_1	G14	VCCO
2	IO	IO	C22	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C20	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C21	DCI
2	IO_L16N_2	IO_L16N_2	D20	I/O
2	IO_L16P_2	IO_L16P_2	D19	I/O
2	IO_L17N_2	IO_L17N_2	D21	I/O
2	IO_L17P_2/VREF_2	IO_L17P_2/VREF_2	D22	VREF
2	IO_L19N_2	IO_L19N_2	E18	I/O
2	IO_L19P_2	IO_L19P_2	F18	I/O
2	IO_L20N_2	IO_L20N_2	E19	I/O
2	IO_L20P_2	IO_L20P_2	E20	I/O
2	IO_L21N_2	IO_L21N_2	E21	I/O

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
4	IO_L30N_4/D2	IO_L30N_4/D2	U12	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	V12	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	W12	DUAL
4	IO_L31P_4/DOUT/BUSY	IO_L31P_4/DOUT/BUSY	Y12	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	AA12	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	AB12	GCLK
4	VCCO_4	VCCO_4	T12	VCCO
4	VCCO_4	VCCO_4	T13	VCCO
4	VCCO_4	VCCO_4	T14	VCCO
4	VCCO_4	VCCO_4	U15	VCCO
4	VCCO_4	VCCO_4	Y15	VCCO
5	IO	IO	U7	I/O
5	N.C. (◆)	IO	U9	I/O
5	IO	IO	U10	I/O
5	IO	IO	U11	I/O
5	IO	IO	V7	I/O
5	IO	IO	V10	I/O
5	IO/VREF_5	IO/VREF_5	AB11	VREF
5	IO/VREF_5	IO/VREF_5	U6	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	Y4	DUAL
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AA3	DUAL
5	IO_L06N_5	IO_L06N_5	AB4	I/O
5	IO_L06P_5	IO_L06P_5	AA4	I/O
5	IO_L09N_5	IO_L09N_5	Y5	I/O
5	IO_L09P_5	IO_L09P_5	W5	I/O
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	AB5	DCI
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	AA5	DCI
5	IO_L15N_5	IO_L15N_5	W6	I/O
5	IO_L15P_5	IO_L15P_5	V6	I/O
5	IO_L16N_5	IO_L16N_5	AA6	I/O
5	IO_L16P_5	IO_L16P_5	Y6	I/O
5	N.C. (◆)	IO_L19N_5	Y7	I/O
5	N.C. (◆)	IO_L19P_5/ VREF_5	W7	VREF
5	N.C. (◆)	IO_L22N_5	AB7	I/O
5	N.C. (◆)	IO_L22P_5	AA7	I/O
5	IO_L24N_5	IO_L24N_5	W8	I/O
5	IO_L24P_5	IO_L24P_5	V8	I/O
5	IO_L25N_5	IO_L25N_5	AB8	I/O
5	IO_L25P_5	IO_L25P_5	AA8	I/O

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
N/A	GND	GND	P13	GND
N/A	GND	GND	P14	GND
N/A	GND	GND	P20	GND
N/A	GND	GND	Y9	GND
N/A	GND	GND	Y14	GND
N/A	VCCAUX	VCCAUX	A6	VCCAUX
N/A	VCCAUX	VCCAUX	A17	VCCAUX
N/A	VCCAUX	VCCAUX	AB6	VCCAUX
N/A	VCCAUX	VCCAUX	AB17	VCCAUX
N/A	VCCAUX	VCCAUX	F1	VCCAUX
N/A	VCCAUX	VCCAUX	F22	VCCAUX
N/A	VCCAUX	VCCAUX	U1	VCCAUX
N/A	VCCAUX	VCCAUX	U22	VCCAUX
N/A	VCCINT	VCCINT	G7	VCCINT
N/A	VCCINT	VCCINT	G8	VCCINT
N/A	VCCINT	VCCINT	G15	VCCINT
N/A	VCCINT	VCCINT	G16	VCCINT
N/A	VCCINT	VCCINT	H7	VCCINT
N/A	VCCINT	VCCINT	H16	VCCINT
N/A	VCCINT	VCCINT	R7	VCCINT
N/A	VCCINT	VCCINT	R16	VCCINT
N/A	VCCINT	VCCINT	T7	VCCINT
N/A	VCCINT	VCCINT	T8	VCCINT
N/A	VCCINT	VCCINT	T15	VCCINT
N/A	VCCINT	VCCINT	T16	VCCINT
VCCAUX	CCLK	CCLK	AA22	CONFIG
VCCAUX	DONE	DONE	AB21	CONFIG
VCCAUX	HSWAP_EN	HSWAP_EN	B3	CONFIG
VCCAUX	M0	M0	AB2	CONFIG
VCCAUX	M1	M1	AA1	CONFIG
VCCAUX	M2	M2	AB3	CONFIG
VCCAUX	PROG_B	PROG_B	A2	CONFIG
VCCAUX	TCK	TCK	A21	JTAG
VCCAUX	TDI	TDI	B1	JTAG
VCCAUX	TDO	TDO	B22	JTAG
VCCAUX	TMS	TMS	A20	JTAG

FG676: 676-lead Fine-pitch Ball Grid Array

The 676-lead fine-pitch ball grid array package, FG676, supports five different Spartan-3 devices, including the XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000. All five have nearly identical footprints but are slightly different, primarily due to unconnected pins on the XC3S1000 and XC3S1500. For example, because the XC3S1000 has fewer I/O pins, this device has 98 unconnected pins on the FG676 package, labeled as "N.C." In Table 103 and Figure 53, these unconnected pins are indicated with a black diamond symbol (◆). The XC3S1500, however, has only two unconnected pins, also labeled "N.C." in the pinout table but indicated with a black square symbol (■).

All the package pins appear in Table 103 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000 pinouts, then that difference is highlighted in Table 103. If the table entry is shaded grey, then there is an unconnected pin on either the XC3S1000 or XC3S1500 that maps to a user-I/O pin on the XC3S2000, XC3S4000, and XC3S5000. If the table entry is shaded tan, then the unconnected pin on either the XC3S1000 or XC3S1500 maps to a VREF-type pin on the XC3S2000, XC3S4000, and XC3S5000. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S1000 or XC3S1500 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S1000 through to the XC3S5000 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 103: **FG676 Package Pinout**

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
0	IO	IO	IO	IO	IO_L04N_0(3)	A3	I/O
0	IO	IO	IO	IO	IO	A5	I/O
0	IO	IO	IO	IO	IO	A6	I/O
0	IO	IO	IO	IO	IO_L04P_0(3)	C4	I/O
0	N.C. (◆)	IO	IO	IO	IO_L13N_0(3)	C8	I/O
0	IO	IO	IO	IO	IO	C12	I/O
0	IO	IO	IO	IO	IO	E13	I/O
0	IO	IO	IO	IO	IO	H11	I/O
0	IO	IO	IO	IO	IO	H12	I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	B3	VREF
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	F7	VREF
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	G10	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	E5	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	D5	DCI
0	IO_L05N_0	IO_L05N_0	IO_L05N_0	IO_L05N_0	IO_L05N_0	B4	I/O
0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	A4	VREF
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	IO_L06N_0	IO_L06N_0	C5	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	IO_L06P_0	IO_L06P_0	B5	I/O
0	IO_L07N_0	IO_L07N_0	IO_L07N_0	IO_L07N_0	IO_L07N_0	E6	I/O
0	IO_L07P_0	IO_L07P_0	IO_L07P_0	IO_L07P_0	IO_L07P_0	D6	I/O
0	IO_L08N_0	IO_L08N_0	IO_L08N_0	IO_L08N_0	IO_L08N_0	C6	I/O
0	IO_L08P_0	IO_L08P_0	IO_L08P_0	IO_L08P_0	IO_L08P_0	B6	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
6	IO_L28P_6	IO_L28P_6	W1	I/O
6	IO_L29N_6	IO_L29N_6	W10	I/O
6	IO_L29P_6	IO_L29P_6	V10	I/O
6	N.C. (◆)	IO_L30N_6	V9	I/O
6	N.C. (◆)	IO_L30P_6	V8	I/O
6	IO_L31N_6	IO_L31N_6	W5	I/O
6	IO_L31P_6	IO_L31P_6	V6	I/O
6	IO_L32N_6	IO_L32N_6	V5	I/O
6	IO_L32P_6	IO_L32P_6	V4	I/O
6	IO_L33N_6	IO_L33N_6	V2	I/O
6	IO_L33P_6	IO_L33P_6	V1	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	U10	VREF
6	IO_L34P_6	IO_L34P_6	U9	I/O
6	IO_L35N_6	IO_L35N_6	U7	I/O
6	IO_L35P_6	IO_L35P_6	U6	I/O
6	N.C. (◆)	IO_L36N_6	U3	I/O
6	N.C. (◆)	IO_L36P_6	U2	I/O
6	IO_L37N_6	IO_L37N_6	T10	I/O
6	IO_L37P_6	IO_L37P_6	T9	I/O
6	IO_L38N_6	IO_L38N_6	T6	I/O
6	IO_L38P_6	IO_L38P_6	T5	I/O
6	IO_L39N_6	IO_L39N_6	T4	I/O
6	IO_L39P_6	IO_L39P_6	T3	I/O
6	IO_L40N_6	IO_L40N_6	T2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	T1	VREF
6	N.C. (◆)	IO_L45N_6	Y4	I/O
6	N.C. (◆)	IO_L45P_6	Y3	I/O
6	N.C. (◆)	IO_L52N_6	T8	I/O
6	N.C. (◆)	IO_L52P_6	T7	I/O
6	VCCO_6	VCCO_6	V3	VCCO
6	VCCO_6	VCCO_6	AB3	VCCO
6	VCCO_6	VCCO_6	AF3	VCCO
6	VCCO_6	VCCO_6	AD5	VCCO
6	VCCO_6	VCCO_6	V7	VCCO
6	VCCO_6	VCCO_6	AB7	VCCO
6	VCCO_6	VCCO_6	Y9	VCCO
6	VCCO_6	VCCO_6	U11	VCCO
6	VCCO_6	VCCO_6	V11	VCCO
6	VCCO_6	VCCO_6	W11	VCCO
7	IO	IO	J6	I/O

User I/Os by Bank

Table 108 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S2000 in the FG900 package. Similarly, Table 109 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S4000 and XC3S5000 in the FG900 package.

Table 108: **User I/Os Per Bank for XC3S2000 in FG900 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	71	62	0	2	5	2
	1	71	62	0	2	5	2
Right	2	69	61	0	2	6	0
	3	71	62	0	2	7	0
Bottom	4	72	57	6	2	5	2
	5	71	55	6	2	6	2
Left	6	69	60	0	2	7	0
	7	71	62	0	2	7	0

Table 109: **User I/Os Per Bank for XC3S4000 and XC3S5000 in FG900 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	79	70	0	2	5	2
	1	79	70	0	2	5	2
Right	2	79	71	0	2	6	0
	3	79	70	0	2	7	0
Bottom	4	80	65	6	2	5	2
	5	79	63	6	2	6	2
Left	6	79	70	0	2	7	0
	7	79	70	0	2	7	0

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
0	VCCO_0	VCCO_0	F13	VCCO
0	VCCO_0	VCCO_0	G8	VCCO
0	VCCO_0	VCCO_0	H11	VCCO
0	VCCO_0	VCCO_0	H15	VCCO
0	VCCO_0	VCCO_0	M13	VCCO
0	VCCO_0	VCCO_0	M14	VCCO
0	VCCO_0	VCCO_0	M15	VCCO
0	VCCO_0	VCCO_0	M16	VCCO
1	IO	IO	B26	I/O
1	IO	IO	A18	I/O
1	IO	IO	C23	I/O
1	IO	IO	E21	I/O
1	IO	IO	E25	I/O
1	IO	IO	F18	I/O
1	IO	IO	F27	I/O
1	IO	IO	F29	I/O
1	IO	IO	H23	I/O
1	IO	IO	H26	I/O
1	N.C. (◆)	IO	J26	I/O
1	IO	IO	K19	I/O
1	IO	IO	L19	I/O
1	IO	IO	L20	I/O
1	IO	IO	L21	I/O
1	N.C. (◆)	IO	L23	I/O
1	IO	IO	L24	I/O
1	IO/VREF_1	IO/VREF_1	D30	VREF
1	IO/VREF_1	IO/VREF_1	K21	VREF
1	IO/VREF_1	IO/VREF_1	L18	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	A32	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B32	DCI
1	IO_L02N_1	IO_L02N_1	A31	I/O
1	IO_L02P_1	IO_L02P_1	B31	I/O
1	IO_L03N_1	IO_L03N_1	B30	I/O
1	IO_L03P_1	IO_L03P_1	C30	I/O
1	IO_L04N_1	IO_L04N_1	C29	I/O
1	IO_L04P_1	IO_L04P_1	D29	I/O
1	IO_L05N_1	IO_L05N_1	A29	I/O
1	IO_L05P_1	IO_L05P_1	B29	I/O
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	E28	VREF
1	IO_L06P_1	IO_L06P_1	F28	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	VCCAUX	VCCAUX	Y5	VCCAUX
N/A	VCCINT	VCCINT	AA13	VCCINT
N/A	VCCINT	VCCINT	AA22	VCCINT
N/A	VCCINT	VCCINT	AB13	VCCINT
N/A	VCCINT	VCCINT	AB14	VCCINT
N/A	VCCINT	VCCINT	AB15	VCCINT
N/A	VCCINT	VCCINT	AB16	VCCINT
N/A	VCCINT	VCCINT	AB19	VCCINT
N/A	VCCINT	VCCINT	AB20	VCCINT
N/A	VCCINT	VCCINT	AB21	VCCINT
N/A	VCCINT	VCCINT	AB22	VCCINT
N/A	VCCINT	VCCINT	AC12	VCCINT
N/A	VCCINT	VCCINT	AC17	VCCINT
N/A	VCCINT	VCCINT	AC18	VCCINT
N/A	VCCINT	VCCINT	AC23	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	M23	VCCINT
N/A	VCCINT	VCCINT	N13	VCCINT
N/A	VCCINT	VCCINT	N14	VCCINT
N/A	VCCINT	VCCINT	N15	VCCINT
N/A	VCCINT	VCCINT	N16	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	N20	VCCINT
N/A	VCCINT	VCCINT	N21	VCCINT
N/A	VCCINT	VCCINT	N22	VCCINT
N/A	VCCINT	VCCINT	P13	VCCINT
N/A	VCCINT	VCCINT	P22	VCCINT
N/A	VCCINT	VCCINT	R13	VCCINT
N/A	VCCINT	VCCINT	R22	VCCINT
N/A	VCCINT	VCCINT	T13	VCCINT
N/A	VCCINT	VCCINT	T22	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT
N/A	VCCINT	VCCINT	U23	VCCINT
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	V23	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	W22	VCCINT
N/A	VCCINT	VCCINT	Y13	VCCINT