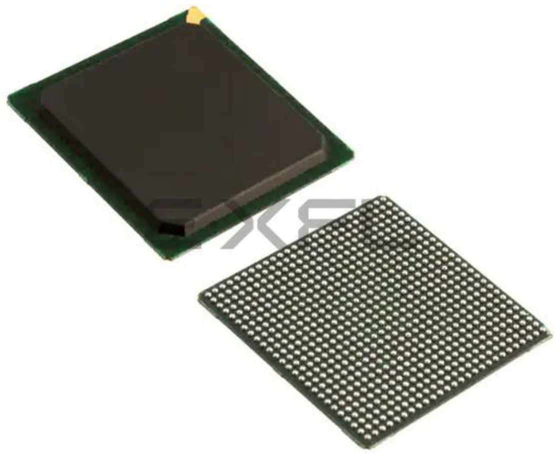

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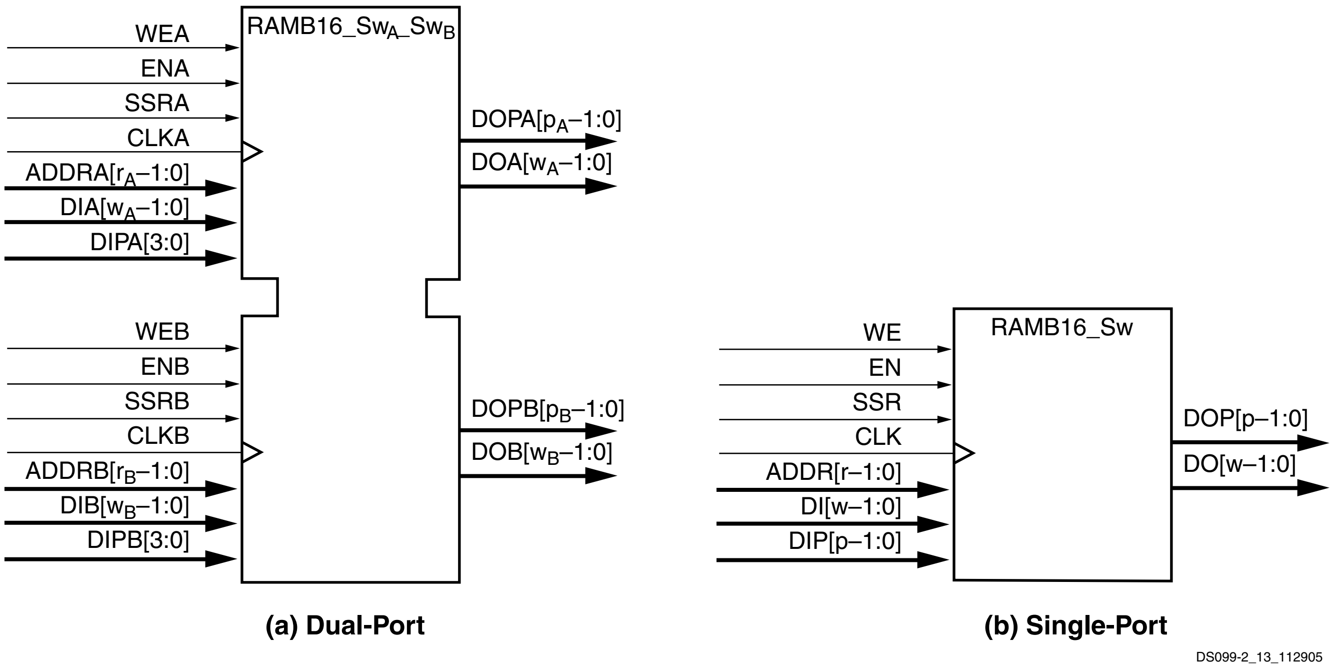
Details	
Product Status	Active
Number of LABs/CLBs	5120
Number of Logic Elements/Cells	46080
Total RAM Bits	737280
Number of I/O	489
Number of Gates	2000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s2000-4fgg676c



Notes:

1. w_A and w_B are integers representing the total data path width (i.e., data bits plus parity bits) at ports A and B, respectively.
2. p_A and p_B are integers that indicate the number of data path lines serving as parity bits.
3. r_A and r_B are integers representing the address bus width at ports A and B, respectively.
4. The control signals CLK, WE, EN, and SSR on both ports have the option of inverted polarity.

Figure 14: **Block RAM Primitives**

Table 13: **Block RAM Port Signals**

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Address Bus	ADDRA	ADDRB	Input	The Address Bus selects a memory location for read or write operations. The width (w) of the port's associated data path determines the number of available address lines (r). Whenever a port is enabled (ENA or ENB = High), address transitions must meet the data sheet setup and hold times with respect to the port clock (CLKA or CLKB). This requirement must be met, even if the RAM read output is of no interest.
Data Input Bus	DIA	DIB	Input	Data at the DI input bus is written to the addressed memory location addressed on an enabled active CLK edge. It is possible to configure a port's total data path width (w) to be 1, 2, 4, 9, 18, or 36 bits. This selection applies to both the DI and DO paths of a given port. Each port is independent. For a port assigned a width (w), the number of addressable locations is 16,384/(w-p) where "p" is the number of parity bits. Each memory location has a width of "w" (including parity bits). See the DIP signal description for more information of parity.
Parity Data Input(s)	DIPA	DIPB	Input	Parity inputs represent additional bits included in the data input path to support error detection. The number of parity bits "p" included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 14.

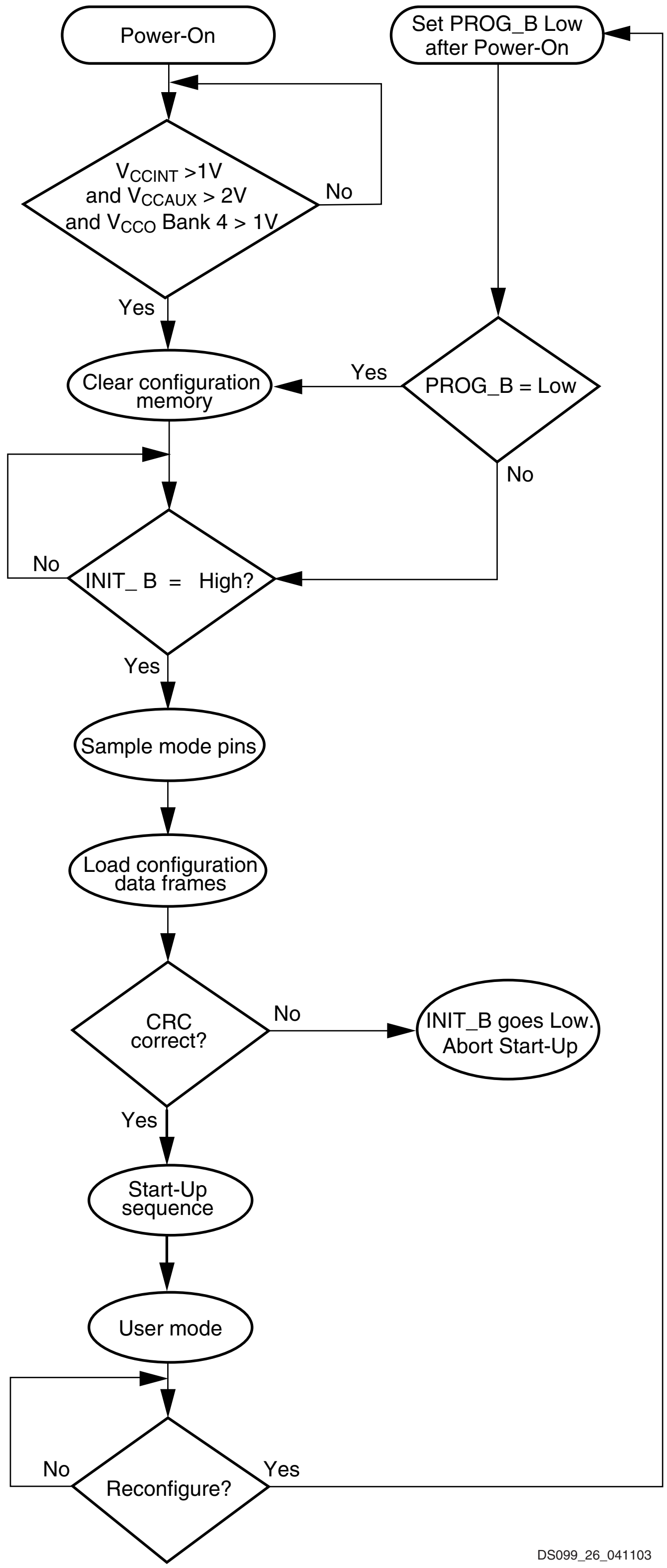


Figure 29: **Configuration Flow Diagram for the Serial and Parallel Modes**

Initial Spartan-3 FPGA mask revisions have a limit on how fast the V_{CCO} supply can ramp. The minimum allowed V_{CCO} ramp rate appears as T_{CCO} in Table 30, page 60. The minimum rate is affected by the package inductance. Consequently, the ball grid array and chip-scale packages (CP132, FT256, FG456, FG676, and FG900) allow a faster ramp rate than the quad-flat packages (VQ100, TQ144, and PQ208).

Configuration Data Retention, Brown-Out

The FPGA's configuration data is stored in robust CMOS configuration latches. The data in these latches is retained even when the voltages drop to the minimum levels necessary to preserve RAM contents. This is specified in Table 31, page 60.

If, after configuration, the V_{CCAUX} or V_{CCINT} supply drops below its data retention voltage, clear the current device configuration using one of the following methods:

- Force the V_{CCAUX} or V_{CCINT} supply voltage below the minimum Power On Reset (POR) voltage threshold Table 29, page 59).
- Assert PROG_B Low.

The POR circuit does not monitor the VCCO_4 supply after configuration. Consequently, dropping the VCCO_4 voltage does not reset the device by triggering a Power-On Reset (POR) event.

No Internal Charge Pumps or Free-Running Oscillators

Some system applications are sensitive to sources of analog noise. Spartan-3 FPGA circuitry is fully static and does not employ internal charge pumps.

The CCLK configuration clock is active during the FPGA configuration process. After configuration completes, the CCLK oscillator is automatically disabled unless the Bitstream Generator (BitGen) option ***Persist=Yes***. See Module 4: Table 80, page 125.

Spartan-3 FPGAs optionally support a featured called Digitally Controlled Impedance (DCI). When used in an application, the DCI logic uses an internal oscillator. The DCI logic is only enabled if the FPGA application specifies an I/O standard that requires DCI (LVDCI_33, LVDCI_25, etc.). If DCI is not used, the associated internal oscillator is also disabled.

In summary, unless an application uses the ***Persist=Yes*** option or specifies a DCI I/O standard, an FPGA with no external switching remains fully static.

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair**

Signal Standard (IOSTANDARD)			Package				
			VQ100	TQ144	PQ208	CP132	FT256, FG320, FG456, FG676, FG900, FG1156
Single-Ended Standards							
GTL			0	0	0	1	14
GTL_DCI			0	0	0	1	14
GTLP			0	0	0	1	19
GTLP_DCI			0	0	0	1	19
HSLVDCI_15			6	6	6	6	14
HSLVDCI_18			7	7	7	7	10
HSLVDCI_25			7	7	7	7	11
HSLVDCI_33			10	10	10	10	10
HSTL_I			11	11	11	11	17
HSTL_I_DCI			11	11	11	11	17
HSTL_III			7	7	7	7	7
HSTL_III_DCI			7	7	7	7	7
HSTL_I_18			13	13	13	13	17
HSTL_I_DCI_18			13	13	13	13	17
HSTL_II_18			9	9	9	9	9
HSTL_II_DCI_18			9	9	9	9	9
HSTL_III_18			8	8	8	8	8
HSTL_III_DCI_18			8	8	8	8	8
LVCMOS12	Slow	2	17	17	17	17	55
		4	13	13	13	13	32
		6	10	10	10	10	18
	Fast	2	12	12	12	12	31
		4	11	11	11	11	13
		6	9	9	9	9	9
LVCMOS15	Slow	2	16	12	12	19	55
		4	8	7	7	9	31
		6	7	7	7	9	18
		8	6	6	6	6	15
		12	5	5	5	5	10
	Fast	2	10	10	10	13	25
		4	6	7	7	7	16
		6	7	7	7	7	13
		8	6	6	6	6	11
		12	6	6	6	6	7

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package				
			VQ100	TQ144	PQ208	CP132	FT256, FG320, FG456, FG676, FG900, FG1156
LVCMOS33	Slow	2	34	24	24	52	76
		4	17	14	14	26	46
		6	17	11	11	26	27
		8	10	10	10	13	20
		12	9	9	9	13	13
		16	8	8	8	8	10
		24	8	8	8	8	9
	Fast	2	20	20	20	26	44
		4	15	15	15	15	26
		6	11	11	11	13	16
		8	10	10	10	10	12
		12	8	8	8	8	10
		16	8	8	8	8	8
		24	7	7	7	7	7
LVDCI_33			10	10	10	10	10
LVDCI_DV2_33			10	10	10	10	10
HSLVDCI_33			10	10	10	10	10
LVTTL	Slow	2	34	25	25	52	60
		4	17	16	16	26	41
		6	17	15	15	26	29
		8	12	12	12	13	22
		12	10	10	10	13	13
		16	10	10	10	10	11
		24	8	8	8	8	9
	Fast	2	20	20	20	26	34
		4	13	13	13	13	20
		6	11	11	11	13	15
		8	10	10	10	10	12
		12	9	9	9	9	10
		16	8	8	8	8	9
		24	7	7	7	7	7

Miscellaneous DCM Timing

Table 64: **Miscellaneous DCM Timing**

Symbol	Description	DLL Frequency Mode	Temperature Range		Units
			Commercial	Industrial	
DCM_INPUT_CLOCK_STOP	Maximum duration that the CLKIN and CLKFB signals can be stopped[1,2]	Any	100	100	ms
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	Any	3	3	CLKIN cycles
DCM_RST_PW_MAX[3]	Maximum duration of a RST pulse width[1,2]	Low	N/A	N/A	seconds
		High	N/A	10	seconds
DCM_CONFIG_LAG_TIME[4]	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL[1,2]	Low	N/A	N/A	minutes
		High	N/A	10	minutes

Notes:

1. These limits only apply to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected. Required due to effects of device cooling: see “Momentarily Stopping CLKIN” in Chapter 3 of UG331.
2. Industrial-temperature applications that use the DLL in High-Frequency mode must use a continuous or increasing operating frequency. The DLL under these conditions does not support reducing the operating frequency once establishing an initial operating frequency.
3. This specification is equivalent to the Virtex-4 FPGA DCM_RESET specification.
4. This specification is equivalent to the Virtex-4 FPGA TCONFIG specification.

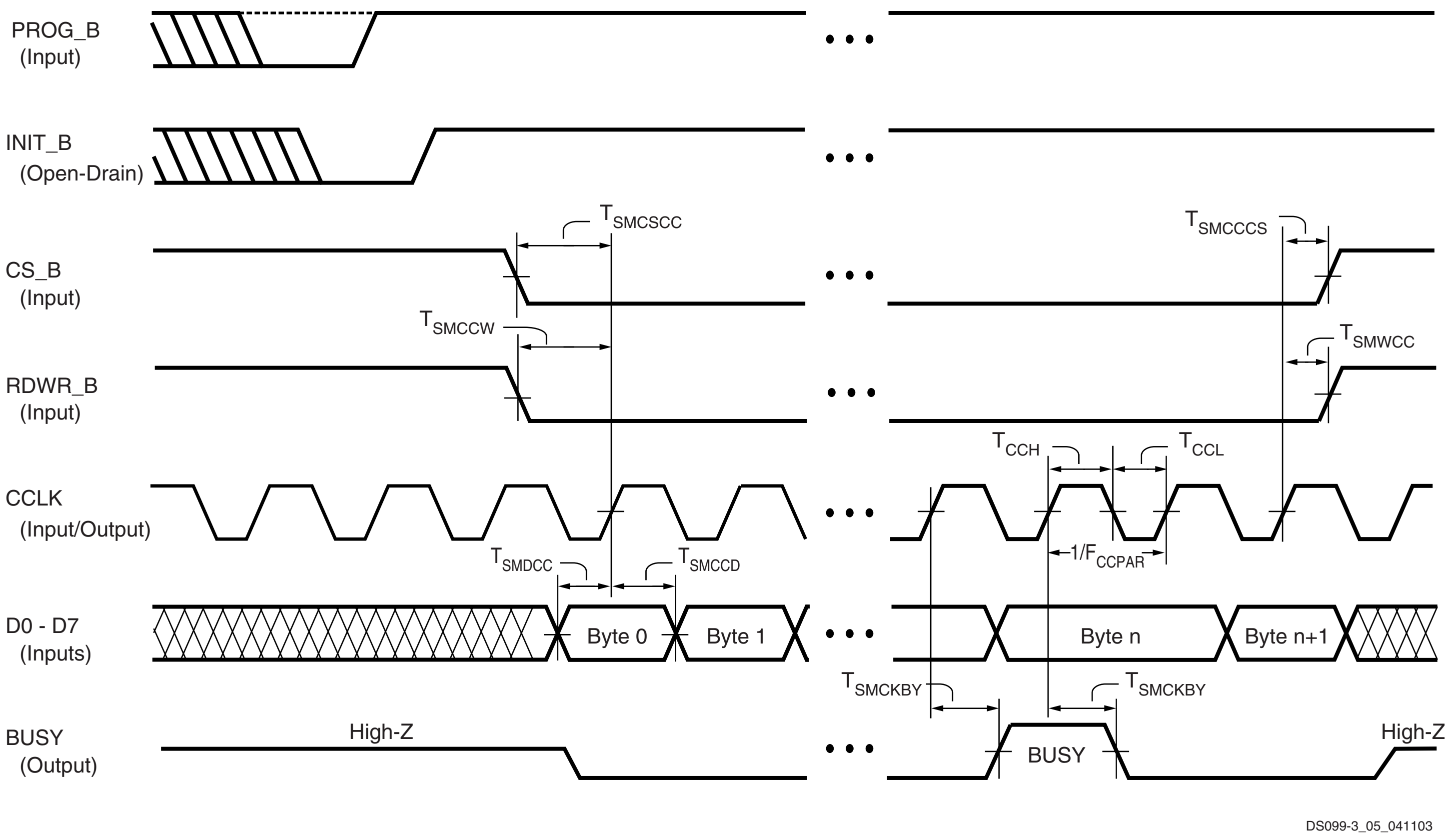


Figure 38: **Waveforms for Master and Slave Parallel Configuration**

Table 67: **Timing for the Master and Slave Parallel Configuration Modes**

Symbol	Description	Slave/ Master	All Speed Grades Min	All Speed Grades Max	Units
Clock-to-Output Times					
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin	Slave	–	12.0	ns
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	Both	10.0	–	ns
T_{SMCSCC}	The time from the setup of a logic level at the CS_B pin to the rising transition at the CCLK pin		10.0	–	ns
T_{SMCCW}(3)	The time from the setup of a logic level at the RDWR_B pin to the rising transition at the CCLK pin		10.0	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins	Both	0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CS_B pin		0	–	ns
T_{SMWCC}(3)	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns

Table 67: **Timing for the Master and Slave Parallel Configuration Modes *(Cont'd)***

Symbol	Description			Slave/ Master	All Speed Grades		Units
					Min	Max	
Clock Timing							
T_{CCH}	CCLK input pin High pulse width			Slave	5	∞	ns
T_{CCL}	CCLK input pin Low pulse width				5	∞	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Not using the BUSY pin(4)		0	50	MHz
			Using the BUSY pin		0	66	MHz
		With bitstream compression			0	20	MHz
		During STARTUP phase			0	50	MHz
ΔF_{CCPAR}	Variation from the CCLK output frequency set using the BitGen option ConfigRate			Master	–50%	+50%	–

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. Some Xilinx documents may refer to Parallel modes as "SelectMAP" modes.
3. RDWR_B is synchronized to CCLK for the purpose of performing the Abort operation. The same pin asynchronously controls the driver impedance of the D0 - D7 pins. To avoid contention when writing configuration data to the D0 - D7 bus, do not bring RDWR_B High when CS_B is Low.
4. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.

Table 70: **Spartan-3 FPGA Pin Definitions**

Pin Name	Direction	Description
I/O: General-purpose I/O pins		
I/O	User-defined as input, output, bidirectional, three-state output, open-drain output, open-source output	**User I/O:** Unrestricted single-ended user-I/O pin. Supports all I/O standards except the differential standards.
I/O_Lxxy_#	User-defined as input, output, bidirectional, three-state output, open-drain output, open-source output	**User I/O, Half of Differential Pair:** Unrestricted single-ended user-I/O pin or half of a differential pair. Supports all I/O standards including the differential standards.
DUAL: Dual-purpose configuration pins		
IO_Lxxy_#/DIN/D0, IO_Lxxy_#/D1, IO_Lxxy_#/D2, IO_Lxxy_#/D3, IO_Lxxy_#/D4, IO_Lxxy_#/D5, IO_Lxxy_#/D6, IO_Lxxy_#/D7	Input during configuration Possible bidirectional I/O after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Configuration Data Port:** In Parallel (SelectMAP) modes, D0-D7 are byte-wide configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained via the Persist bitstream option. In Serial modes, DIN (D0) serves as the single configuration data input. This pin becomes a user I/O after configuration unless retained by the Persist bitstream option.
IO_Lxxy_#/CS_B	Input during Parallel mode configuration Possible input after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Chip Select for Parallel Mode Configuration:** In Parallel (SelectMAP) modes, this is the active-Low Chip Select signal. This pin becomes a user I/O after configuration unless the SelectMAP port is retained via the Persist bitstream option.
IO_Lxxy_#/RDWR_B	Input during Parallel mode configuration Possible input after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Read/Write Control for Parallel Mode Configuration:** In Parallel (SelectMAP) modes, this is the active-Low Write Enable, active-High Read Enable signal. This pin becomes a user I/O after configuration unless the SelectMAP port is retained via the Persist bitstream option.
IO_Lxxy_#/ BUSY/DOUT	Output during configuration Possible output after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Configuration Data Rate Control for Parallel Mode, Serial Data Output for Serial Mode:** In Parallel (SelectMAP) modes, BUSY throttles the rate at which configuration data is loaded. This pin becomes a user I/O after configuration unless the SelectMAP port is retained via the Persist bitstream option. In Serial modes, DOUT provides preamble and configuration data to downstream devices in a multi-FPGA daisy-chain. This pin becomes a user I/O after configuration.
IO_Lxxy_#/INIT_B	Bidirectional (open-drain) during configuration User I/O after configuration	**Initializing Configuration Memory/Detected Configuration Error:** When Low, this pin indicates that configuration memory is being cleared. When held Low, this pin delays the start of configuration. After this pin is released or configuration memory is cleared, the pin goes High. During configuration, a Low on this output indicates that a configuration data error occurred. This pin always has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM during configuration, regardless of the HSWAP_EN pin. This pin becomes a user I/O after configuration.
DCI: Digitally Controlled Impedance reference resistor input pins		
IO_Lxxy_#/VRN_# or IO/VRN_#	Input when using DCI Otherwise, same as I/O	**DCI Reference Resistor for NMOS I/O Transistor (per bank):** If using DCI, a 1% precision impedance-matching resistor is connected between this pin and the VCCO supply for this bank. Otherwise, this pin is a user I/O.
IO_Lxxy_#/VRP_# or IO/VRP_#	Input when using DCI Otherwise, same as I/O	**DCI Reference Resistor for PMOS I/O Transistor (per bank):** If using DCI, a 1% precision impedance-matching resistor is connected between this pin and the ground supply. Otherwise, this pin is a user I/O.

The 1% precision impedance-matching resistor attached to the VRN_# pin controls the pull-down impedance of NMOS transistor in the input or output buffer. Consequently, the VRN_# pin must connect to VCCO. The 'N' character in "VRN" indicates that this pin controls the I/O buffer's NMOS transistor impedance. The VRN_# pin is only used for split termination.

Each VRN or VRP reference input requires its own resistor. A single resistor cannot be shared between VRN or VRP pins associated with different banks.

During configuration, these pins behave exactly like user-I/O pins. The associated DCI behavior is not active or valid until after configuration completes.

Also see Digitally Controlled Impedance (DCI), page 16.

DCI Termination Types

If the I/O in an I/O bank do not use the DCI feature, then no external resistors are required and both the VRP_# and VRN_# pins are available for user I/O, as shown in section [a] of Figure 42.

If the I/O standards within the associated I/O bank require single termination—such as GTL_DCI, GTLP_DCI, or HSTL_III_DCI—then only the VRP_# signal connects to a 1% precision impedance-matching resistor, as shown in section [b] of Figure 42. A resistor is not required for the VRN_# pin.

Finally, if the I/O standards with the associated I/O bank require split termination—such as HSTL_I_DCI, SSTL2_I_DCI, SSTL2_II_DCI, or LVDS_25_DCI and LVDSEXT_25_DCI receivers—then both the VRP_# and VRN_# pins connect to separate 1% precision impedance-matching resistors, as shown in section [c] of Figure 42. Neither pin is available for user I/O.

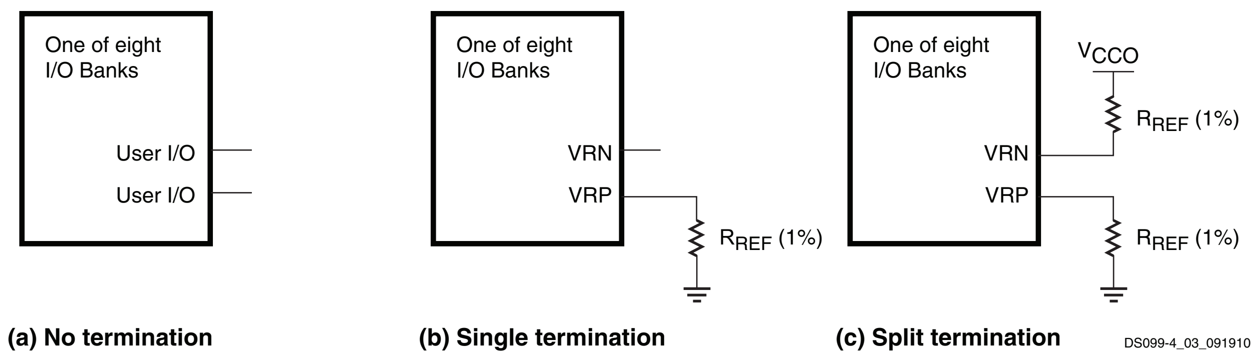


Figure 42: **DCI Termination Types**

GCLK: Global Clock Buffer Inputs or General-Purpose I/O Pins

These pins are user-I/O pins unless they specifically connect to one of the eight low-skew global clock buffers on the device, specified using the IBUFG primitive.

There are eight GCLK pins per device and two each appear in the top-edge banks, Bank 0 and 1, and the bottom-edge banks, Banks 4 and 5. See Figure 40 for a picture of bank labeling.

During configuration, these pins behave exactly like user-I/O pins.

Also see Global Clock Network, page 42.

CONFIG: Dedicated Configuration Pins

The dedicated configuration pins control the configuration process and are not available as user-I/O pins. Every package has seven dedicated configuration pins. All CONFIG-type pins are powered by the +2.5V VCCAUX supply.

Also see Configuration, page 46.

HSWAP_EN: Disable Pull-up Resistors During Configuration

As shown in Table 76, a Low on this asynchronous pin enables pull-up resistors on all user I/Os not actively involved in the configuration process, although only until device configuration completes. A High disables the pull-up resistors during configuration, which is the desired state for some applications.

The dedicated configuration CONFIG pins (CCLK, DONE, PROG_B, HSWAP_EN, M2, M1, M0), the JTAG pins (TDI, TMS, TCK, TDO) and the INIT_B always have active pull-up resistors during configuration, regardless of the value on HSWAP_EN.

After configuration, HSWAP_EN becomes a "don't care" input and any pull-up resistors previously enabled by HSWAP_EN are disabled. If a user I/O in the application requires a pull-up resistor after configuration, place a PULLUP primitive on the associated I/O pin or, for some pins, set the associated bitstream generator option.

Table 76: **HSWAP_EN Encoding**

HSWAP_EN	Function
During Configuration	
0	Enable pull-up resistors on all pins not actively involved in the configuration process. Pull-ups are only active until configuration completes. See Table 79.
1	No pull-up resistors during configuration.
After Configuration, User Mode	
X	This pin has no function except during device configuration.

Notes:
1. X = don't care, either 0 or 1.

The Bitstream generator option HswapenPin determines whether a pull-up resistor to VCCAUX, a pull-down resistor, or no resistor is present on HSWAP_EN after configuration.

JTAG: Dedicated JTAG Port Pins

Table 77: **JTAG Pin Descriptions**

Pin Name	Direction	Description	Bitstream Generation Option
TCK	Input	**Test Clock:** The TCK clock signal synchronizes all boundary scan operations on its rising edge.	The BitGen option **TckPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.
TDI	Input	**Test Data Input:** TDI is the serial data input for all JTAG instruction and data registers. This input is sampled on the rising edge of TCK.	The BitGen option **TdiPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.
TMS	Input	**Test Mode Select:** The TMS input controls the sequence of states through which the JTAG TAP state machine passes. This input is sampled on the rising edge of TCK.	The BitGen option **TmsPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.
TDO	Output	**Test Data Output:** The TDO pin is the data output for all JTAG instruction and data registers. This output is sampled on the rising edge of TCK. The TDO output is an active totem-pole driver and is not like the open-collector TDO output on Virtex®-II Pro FPGAs.	The BitGen option **TdoPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.

These pins are dedicated connections to the four-wire IEEE 1532/IEEE 1149.1 JTAG port, shown in Figure 43 and described in Table 77. The JTAG port is used for boundary-scan testing, device configuration, application debugging, and possibly an additional serial port for the application. These pins are dedicated and are not available as user-I/O pins. Every package has four dedicated JTAG pins and these pins are powered by the +2.5V VCCAUX supply.

For additional information on JTAG configuration, see Boundary-Scan (JTAG) Mode, page 50.

Table 89: **CP132 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	CP132 Ball	Type
N/A	GND	M3	GND
N/A	GND	M13	GND
N/A	GND	N6	GND
N/A	GND	N11	GND
N/A	VCCAUX	A5	VCCAUX
N/A	VCCAUX	C10	VCCAUX
N/A	VCCAUX	M5	VCCAUX
N/A	VCCAUX	P10	VCCAUX
N/A	VCCINT	B10	VCCINT
N/A	VCCINT	C6	VCCINT
N/A	VCCINT	M9	VCCINT
N/A	VCCINT	N5	VCCINT
VCCAUX	CCLK	P14	CONFIG
VCCAUX	DONE	P13	CONFIG
VCCAUX	HSWAP_EN	B3	CONFIG
VCCAUX	M0	N1	CONFIG
VCCAUX	M1	M2	CONFIG
VCCAUX	M2	P1	CONFIG
VCCAUX	PROG_B	A2	CONFIG
VCCAUX	TCK	B14	JTAG
VCCAUX	TDI	A1	JTAG
VCCAUX	TDO	C13	JTAG
VCCAUX	TMS	A14	JTAG

User I/Os by Bank

Table 90 indicates how the 89 available user-I/O pins are distributed between the eight I/O banks on the CP132 package. There are only four output banks, each with its own VCCO voltage input.

Table 90: **User I/Os Per Bank for XC3S50 in CP132 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	10	5	0	2	1	2
	1	10	5	0	2	1	2
Right	2	12	8	0	2	2	0
	3	12	8	0	2	2	0
Bottom	4	11	0	6	2	1	2
	5	10	1	6	0	1	2
Left	6	12	8	0	2	2	0
	7	12	9	0	2	1	0

Notes:

1. The CP132 and CPG132 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

Table 91: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
5	IO_L32P_5/GCLK2	P52	GCLK
6	IO_L01N_6/VRP_6	P36	DCI
6	IO_L01P_6/VRN_6	P35	DCI
6	IO_L20N_6	P33	I/O
6	IO_L20P_6	P32	I/O
6	IO_L21N_6	P31	I/O
6	IO_L21P_6	P30	I/O
6	IO_L22N_6	P28	I/O
6	IO_L22P_6	P27	I/O
6	IO_L23N_6	P26	I/O
6	IO_L23P_6	P25	I/O
6	IO_L24N_6/VREF_6	P24	VREF
6	IO_L24P_6	P23	I/O
6	IO_L40N_6	P21	I/O
6	IO_L40P_6/VREF_6	P20	VREF
7	IO/VREF_7	P4	VREF
7	IO_L01N_7/VRP_7	P2	DCI
7	IO_L01P_7/VRN_7	P1	DCI
7	IO_L20N_7	P6	I/O
7	IO_L20P_7	P5	I/O
7	IO_L21N_7	P8	I/O
7	IO_L21P_7	P7	I/O
7	IO_L22N_7	P11	I/O
7	IO_L22P_7	P10	I/O
7	IO_L23N_7	P13	I/O
7	IO_L23P_7	P12	I/O
7	IO_L24N_7	P15	I/O
7	IO_L24P_7	P14	I/O
7	IO_L40N_7/VREF_7	P18	VREF
7	IO_L40P_7	P17	I/O
0,1	VCCO_TOP	P126	VCCO
0,1	VCCO_TOP	P138	VCCO
0,1	VCCO_TOP	P115	VCCO
2,3	VCCO_RIGHT	P106	VCCO
2,3	VCCO_RIGHT	P75	VCCO
2,3	VCCO_RIGHT	P91	VCCO
4,5	VCCO_BOTTOM	P54	VCCO
4,5	VCCO_BOTTOM	P43	VCCO
4,5	VCCO_BOTTOM	P66	VCCO
6,7	VCCO_LEFT	P19	VCCO

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
4	IO_L31P_4/ DOUT/BUSY	V10	DUAL
4	IO_L32N_4/GCLK1	N10	GCLK
4	IO_L32P_4/GCLK0	P10	GCLK
4	VCCO_4	M10	VCCO
4	VCCO_4	M11	VCCO
4	VCCO_4	T13	VCCO
4	VCCO_4	U11	VCCO
5	IO	N8	I/O
5	IO	P8	I/O
5	IO	U6	I/O
5	IO/VREF_5	R9	VREF
5	IO_L01N_5/RDWR_B	V3	DUAL
5	IO_L01P_5/CS_B	V2	DUAL
5	IO_L06N_5	T5	I/O
5	IO_L06P_5	T4	I/O
5	IO_L10N_5/VRP_5	V4	DCI
5	IO_L10P_5/VRN_5	U4	DCI
5	IO_L15N_5	R6	I/O
5	IO_L15P_5	R5	I/O
5	IO_L16N_5	V5	I/O
5	IO_L16P_5	U5	I/O
5	IO_L27N_5/VREF_5	P6	VREF
5	IO_L27P_5	P7	I/O
5	IO_L28N_5/D6	R7	DUAL
5	IO_L28P_5/D7	T7	DUAL
5	IO_L29N_5	V8	I/O
5	IO_L29P_5/VREF_5	V7	VREF
5	IO_L30N_5	R8	I/O
5	IO_L30P_5	T8	I/O
5	IO_L31N_5/D4	U9	DUAL
5	IO_L31P_5/D5	V9	DUAL
5	IO_L32N_5/GCLK3	N9	GCLK
5	IO_L32P_5/GCLK2	P9	GCLK
5	VCCO_5	M8	VCCO
5	VCCO_5	M9	VCCO
5	VCCO_5	T6	VCCO
5	VCCO_5	U8	VCCO
6	IO	K6	I/O
6	IO_L01N_6/VRP_6	T3	DCI

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
7	IO_L20P_7	E1	I/O
7	IO_L21N_7	E4	I/O
7	IO_L21P_7	F4	I/O
7	IO_L22N_7	G5	I/O
7	IO_L22P_7	F5	I/O
7	IO_L23N_7	G1	I/O
7	IO_L23P_7	F2	I/O
7	IO_L24N_7	G4	I/O
7	IO_L24P_7	G3	I/O
7	IO_L27N_7	H5	I/O
7	IO_L27P_7/VREF_7	H6	VREF
7	IO_L34N_7	H4	I/O
7	IO_L34P_7	H3	I/O
7	IO_L35N_7	H1	I/O
7	IO_L35P_7	H2	I/O
7	IO_L39N_7	J1	I/O
7	IO_L39P_7	J2	I/O
7	IO_L40N_7/VREF_7	J5	VREF
7	IO_L40P_7	J4	I/O
7	VCCO_7	F3	VCCO
7	VCCO_7	H7	VCCO
7	VCCO_7	J7	VCCO
N/A	GND	A1	GND
N/A	GND	A13	GND
N/A	GND	A18	GND
N/A	GND	A6	GND
N/A	GND	B17	GND
N/A	GND	B2	GND
N/A	GND	C10	GND
N/A	GND	C9	GND
N/A	GND	F1	GND
N/A	GND	F18	GND
N/A	GND	G12	GND
N/A	GND	G7	GND
N/A	GND	H10	GND
N/A	GND	H11	GND
N/A	GND	H8	GND
N/A	GND	H9	GND
N/A	GND	J11	GND
N/A	GND	J16	GND

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
0	N.C. (◆)	IO_L22N_0	E8	I/O
0	N.C. (◆)	IO_L22P_0	D8	I/O
0	IO_L24N_0	IO_L24N_0	B8	I/O
0	IO_L24P_0	IO_L24P_0	A8	I/O
0	IO_L25N_0	IO_L25N_0	F9	I/O
0	IO_L25P_0	IO_L25P_0	E9	I/O
0	IO_L27N_0	IO_L27N_0	B9	I/O
0	IO_L27P_0	IO_L27P_0	A9	I/O
0	IO_L28N_0	IO_L28N_0	F10	I/O
0	IO_L28P_0	IO_L28P_0	E10	I/O
0	IO_L29N_0	IO_L29N_0	C10	I/O
0	IO_L29P_0	IO_L29P_0	B10	I/O
0	IO_L30N_0	IO_L30N_0	F11	I/O
0	IO_L30P_0	IO_L30P_0	E11	I/O
0	IO_L31N_0	IO_L31N_0	D11	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C11	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B11	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A11	GCLK
0	VCCO_0	VCCO_0	C8	VCCO
0	VCCO_0	VCCO_0	F8	VCCO
0	VCCO_0	VCCO_0	G9	VCCO
0	VCCO_0	VCCO_0	G10	VCCO
0	VCCO_0	VCCO_0	G11	VCCO
1	IO	IO	A12	I/O
1	IO	IO	E16	I/O
1	IO	IO	F12	I/O
1	IO	IO	F13	I/O
1	IO	IO	F16	I/O
1	IO	IO	F17	I/O
1	IO/VREF_1	IO/VREF_1	E13	VREF
1	N.C. (◆)	IO/VREF_1	F14	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	C19	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B20	DCI
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	A19	VREF
1	IO_L06P_1	IO_L06P_1	B19	I/O
1	IO_L09N_1	IO_L09N_1	C18	I/O
1	IO_L09P_1	IO_L09P_1	D18	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	A18	VREF
1	IO_L10P_1	IO_L10P_1	B18	I/O
1	IO_L15N_1	IO_L15N_1	D17	I/O

User I/Os by Bank

Table 101 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S400 in the FG456 package. Similarly, Table 102 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1000, XC3S1500, and XC3S2000 in the FG456 package.

Table 101: **User I/Os Per Bank for XC3S400 in FG456 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	35	27	0	2	4	2
	1	35	27	0	2	4	2
Right	2	31	25	0	2	4	0
	3	31	25	0	2	4	0
Bottom	4	35	21	6	2	4	2
	5	35	21	6	2	4	2
Left	6	31	25	0	2	4	0
	7	31	25	0	2	4	0

Table 102: **User I/Os Per Bank for XC3S1000, XC3S1500, and XC3S2000 in FG456 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	40	31	0	2	5	2
	1	40	31	0	2	5	2
Right	2	43	37	0	2	4	0
	3	43	37	0	2	4	0
Bottom	4	41	26	6	2	5	2
	5	40	25	6	2	5	2
Left	6	43	37	0	2	4	0
	7	43	37	0	2	4	0

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO_L10N_0	IO_L10N_0	J9	I/O
0	IO_L10P_0	IO_L10P_0	H9	I/O
0	IO_L11N_0	IO_L11N_0	G10	I/O
0	IO_L11P_0	IO_L11P_0	F10	I/O
0	IO_L12N_0	IO_L12N_0	C10	I/O
0	IO_L12P_0	IO_L12P_0	B10	I/O
0	IO_L13N_0	IO_L13N_0	J10	I/O
0	IO_L13P_0	IO_L13P_0	K11	I/O
0	IO_L14N_0	IO_L14N_0	H11	I/O
0	IO_L14P_0	IO_L14P_0	G11	I/O
0	IO_L15N_0	IO_L15N_0	F11	I/O
0	IO_L15P_0	IO_L15P_0	E11	I/O
0	IO_L16N_0	IO_L16N_0	D11	I/O
0	IO_L16P_0	IO_L16P_0	C11	I/O
0	IO_L17N_0	IO_L17N_0	B11	I/O
0	IO_L17P_0	IO_L17P_0	A11	I/O
0	IO_L18N_0	IO_L18N_0	K12	I/O
0	IO_L18P_0	IO_L18P_0	J12	I/O
0	IO_L19N_0	IO_L19N_0	H12	I/O
0	IO_L19P_0	IO_L19P_0	G12	I/O
0	IO_L20N_0	IO_L20N_0	F12	I/O
0	IO_L20P_0	IO_L20P_0	E12	I/O
0	IO_L21N_0	IO_L21N_0	D12	I/O
0	IO_L21P_0	IO_L21P_0	C12	I/O
0	IO_L22N_0	IO_L22N_0	B12	I/O
0	IO_L22P_0	IO_L22P_0	A12	I/O
0	IO_L23N_0	IO_L23N_0	J13	I/O
0	IO_L23P_0	IO_L23P_0	H13	I/O
0	IO_L24N_0	IO_L24N_0	F13	I/O
0	IO_L24P_0	IO_L24P_0	E13	I/O
0	IO_L25N_0	IO_L25N_0	B13	I/O
0	IO_L25P_0	IO_L25P_0	A13	I/O
0	IO_L26N_0	IO_L26N_0	K14	I/O
0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	J14	VREF
0	IO_L27N_0	IO_L27N_0	G14	I/O
0	IO_L27P_0	IO_L27P_0	F14	I/O
0	IO_L28N_0	IO_L28N_0	C14	I/O
0	IO_L28P_0	IO_L28P_0	B14	I/O
0	IO_L29N_0	IO_L29N_0	J15	I/O
0	IO_L29P_0	IO_L29P_0	H15	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
6	IO_L16N_6	IO_L16N_6	AE2	I/O
6	IO_L16P_6	IO_L16P_6	AE1	I/O
6	IO_L17N_6	IO_L17N_6	AD10	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	AD9	VREF
6	IO_L19N_6	IO_L19N_6	AD2	I/O
6	IO_L19P_6	IO_L19P_6	AD1	I/O
6	IO_L20N_6	IO_L20N_6	AC11	I/O
6	IO_L20P_6	IO_L20P_6	AC10	I/O
6	IO_L21N_6	IO_L21N_6	AC8	I/O
6	IO_L21P_6	IO_L21P_6	AC7	I/O
6	IO_L22N_6	IO_L22N_6	AC6	I/O
6	IO_L22P_6	IO_L22P_6	AC5	I/O
6	IO_L23N_6	IO_L23N_6	AC2	I/O
6	IO_L23P_6	IO_L23P_6	AC1	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	AC9	VREF
6	IO_L24P_6	IO_L24P_6	AB10	I/O
6	IO_L25N_6	IO_L25N_6	AB8	I/O
6	IO_L25P_6	IO_L25P_6	AB7	I/O
6	IO_L26N_6	IO_L26N_6	AB4	I/O
6	IO_L26P_6	IO_L26P_6	AB3	I/O
6	IO_L27N_6	IO_L27N_6	AB11	I/O
6	IO_L27P_6	IO_L27P_6	AA11	I/O
6	IO_L28N_6	IO_L28N_6	AA8	I/O
6	IO_L28P_6	IO_L28P_6	AA7	I/O
6	IO_L29N_6	IO_L29N_6	AA6	I/O
6	IO_L29P_6	IO_L29P_6	AA5	I/O
6	IO_L30N_6	IO_L30N_6	AA4	I/O
6	IO_L30P_6	IO_L30P_6	AA3	I/O
6	IO_L31N_6	IO_L31N_6	AA2	I/O
6	IO_L31P_6	IO_L31P_6	AA1	I/O
6	IO_L32N_6	IO_L32N_6	Y11	I/O
6	IO_L32P_6	IO_L32P_6	Y10	I/O
6	IO_L33N_6	IO_L33N_6	Y4	I/O
6	IO_L33P_6	IO_L33P_6	Y3	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	Y2	VREF
6	IO_L34P_6	IO_L34P_6	Y1	I/O
6	IO_L35N_6	IO_L35N_6	Y9	I/O
6	IO_L35P_6	IO_L35P_6	W10	I/O
6	IO_L36N_6	IO_L36N_6	W7	I/O
6	IO_L36P_6	IO_L36P_6	W6	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
7	IO_L45P_7	IO_L45P_7	M2	I/O
7	IO_L46N_7	IO_L46N_7	N7	I/O
7	IO_L46P_7	IO_L46P_7	N8	I/O
7	N.C. (◆)	IO_L47N_7	P9	I/O
7	N.C. (◆)	IO_L47P_7	P10	I/O
7	IO_L49N_7	IO_L49N_7	P1	I/O
7	IO_L49P_7	IO_L49P_7	P2	I/O
7	IO_L50N_7	IO_L50N_7	R10	I/O
7	IO_L50P_7	IO_L50P_7	R11	I/O
7	N.C. (◆)	IO_L51N_7	U11	I/O
7	N.C. (◆)	IO_L51P_7	T11	I/O
7	VCCO_7	VCCO_7	D3	VCCO
7	VCCO_7	VCCO_7	H3	VCCO
7	VCCO_7	VCCO_7	H7	VCCO
7	VCCO_7	VCCO_7	L4	VCCO
7	VCCO_7	VCCO_7	L8	VCCO
7	VCCO_7	VCCO_7	N12	VCCO
7	VCCO_7	VCCO_7	N2	VCCO
7	VCCO_7	VCCO_7	N6	VCCO
7	VCCO_7	VCCO_7	P12	VCCO
7	VCCO_7	VCCO_7	R12	VCCO
7	VCCO_7	VCCO_7	R8	VCCO
7	VCCO_7	VCCO_7	T12	VCCO
7	VCCO_7	VCCO_7	T4	VCCO
N/A	GND	GND	A1	GND
N/A	GND	GND	A13	GND
N/A	GND	GND	A16	GND
N/A	GND	GND	A19	GND
N/A	GND	GND	A2	GND
N/A	GND	GND	A22	GND
N/A	GND	GND	A26	GND
N/A	GND	GND	A30	GND
N/A	GND	GND	A33	GND
N/A	GND	GND	A34	GND
N/A	GND	GND	A5	GND
N/A	GND	GND	A9	GND
N/A	GND	GND	AA14	GND
N/A	GND	GND	AA15	GND
N/A	GND	GND	AA16	GND
N/A	GND	GND	AA17	GND