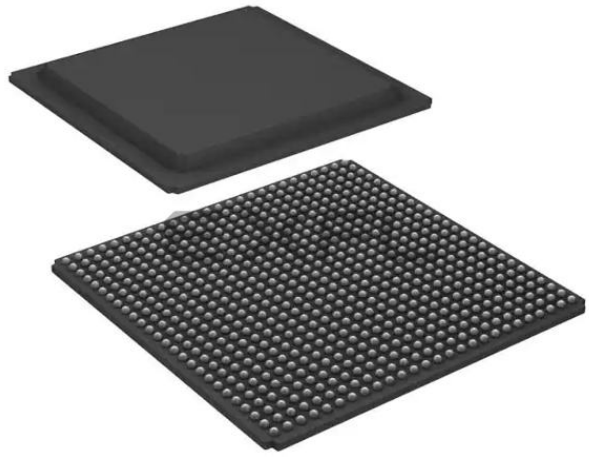

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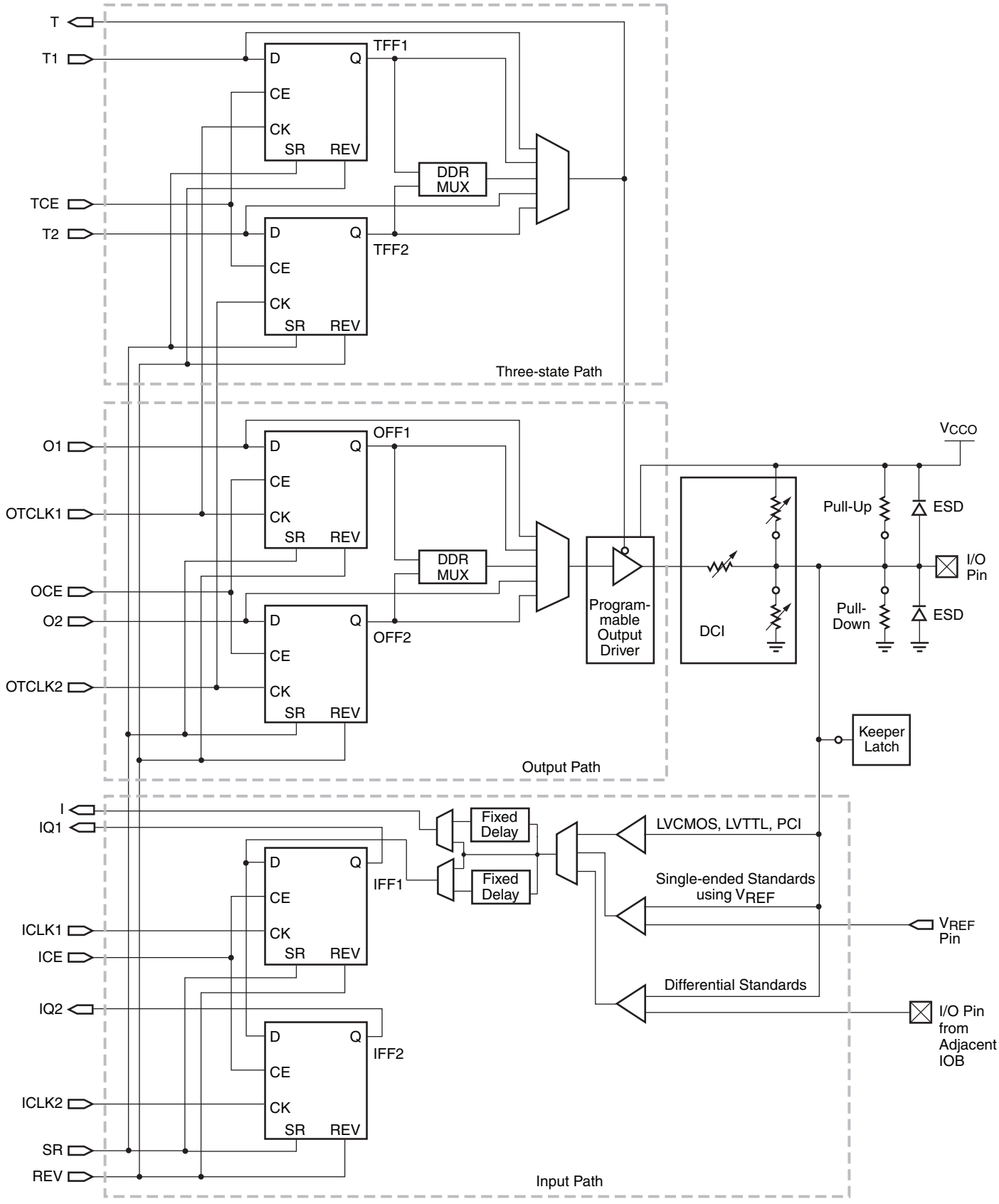
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	5120
Number of Logic Elements/Cells	46080
Total RAM Bits	737280
Number of I/O	489
Number of Gates	2000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s2000-5fg676c



Note: All IOB signals originating from the FPGA's internal logic have an optional polarity inverter.

DS099-2_01_091410

Figure 7: **Simplified IOB Diagram**

Supply Voltages for the IOBs

Three different supplies power the IOBs:

- The V_{CCO} supplies, one for each of the FPGA's I/O banks, power the output drivers, except when using the GTL and GTLP signal standards. The voltage on the V_{CCO} pins determines the voltage swing of the output signal.
- V_{CCINT} is the main power supply for the FPGA's internal logic.
- The V_{CCAUX} is an auxiliary source of power, primarily to optimize the performance of various FPGA functions such as I/O switching.

The I/Os During Power-On, Configuration, and User Mode

With no power applied to the FPGA, all I/Os are in a high-impedance state. The V_{CCINT} (1.2V), V_{CCAUX} (2.5V), and V_{CCO} supplies may be applied in any order. Before power-on can finish, V_{CCINT}, V_{CCO} Bank 4, and V_{CCAUX} must have reached their respective minimum recommended operating levels (see Table 29, page 59). At this time, all I/O drivers also will be in a high-impedance state. V_{CCO} Bank 4, V_{CCINT}, and V_{CCAUX} serve as inputs to the internal Power-On Reset circuit (POR).

A Low level applied to the HSWAP_EN input enables pull-up resistors on User I/Os from power-on throughout configuration. A High level on HSWAP_EN disables the pull-up resistors, allowing the I/Os to float. If the HSWAP_EN pin is floating, then an internal pull-up resistor pulls HSWAP_EN High. As soon as power is applied, the FPGA begins initializing its configuration memory. At the same time, the FPGA internally asserts the Global Set-Reset (GSR), which asynchronously resets all IOB storage elements to a Low state.

Upon the completion of initialization, INIT_B goes High, sampling the M0, M1, and M2 inputs to determine the configuration mode. At this point, the configuration data is loaded into the FPGA. The I/O drivers remain in a high-impedance state (with or without pull-up resistors, as determined by the HSWAP_EN input) throughout configuration.

The Global Three State (GTS) net is released during Start-Up, marking the end of configuration and the beginning of design operation in the User mode. At this point, those I/Os to which signals have been assigned go active while all unused I/Os remain in a high-impedance state. The release of the GSR net, also part of Start-up, leaves the IOB registers in a Low state by default, unless the loaded design reverses the polarity of their respective RS inputs.

In User mode, all internal pull-up resistors on the I/Os are disabled and HSWAP_EN becomes a "don't care" input. If it is desirable to have pull-up or pull-down resistors on I/Os carrying signals, the appropriate symbol—e.g., PULLUP, PULLDOWN—must be placed at the appropriate pads in the design. The Bitstream Generator (Bitgen) option UnusedPin available in the Xilinx development software determines whether unused I/Os collectively have pull-up resistors, pull-down resistors, or no resistors in User mode.

CLB Overview

For more details on the CLBs, refer to the chapter entitled "Using Configurable Logic Blocks" in UG331.

The Configurable Logic Blocks (CLBs) constitute the main logic resource for implementing synchronous as well as combinatorial circuits. Each CLB comprises four interconnected slices, as shown in Figure 11. These slices are grouped in pairs. Each pair is organized as a column with an independent carry chain.

The nomenclature that the FPGA Editor—part of the Xilinx development software—uses to designate slices is as follows: The letter 'X' followed by a number identifies columns of slices. The 'X' number counts up in sequence from the left side of the die to the right. The letter 'Y' followed by a number identifies the position of each slice in a pair as well as indicating the CLB row. The 'Y' number counts slices starting from the bottom of the die according to the sequence: 0, 1, 0, 1 (the first CLB row); 2, 3, 2, 3 (the second CLB row); etc. Figure 11 shows the CLB located in the lower left-hand corner of the die. Slices X0Y0 and X0Y1 make up the column-pair on the left where as slices X1Y0 and X1Y1 make up the column-pair on the right. For each CLB, the term "left-hand" (or SLICEM) indicates the pair of slices labeled with an even 'X' number, such as X0, and the term "right-hand" (or SLICEL) designates the pair of slices with an odd 'X' number, e.g., X1.

Function Generator

Each of the two LUTs (F and G) in a slice have four logic inputs (A1-A4) and a single output (D). This permits any four-variable Boolean logic operation to be programmed into them. Furthermore, wide function multiplexers can be used to effectively combine LUTs within the same CLB or across different CLBs, making logic functions with still more input variables possible.

The LUTs in both the right-hand and left-hand slice-pairs not only support the logic functions described above, but also can function as ROM that is initialized with data at the time of configuration.

The LUTs in the left-hand slice-pair (even-numbered columns such as X0 in Figure 11) of each CLB support two additional functions that the right-hand slice-pair (odd-numbered columns such as X1) do not.

First, it is possible to program the “left-hand LUTs” as distributed RAM. This type of memory affords moderate amounts of data buffering anywhere along a data path. One left-hand LUT stores 16 bits. Multiple left-hand LUTs can be combined in various ways to store larger amounts of data. A dual port option combines two LUTs so that memory access is possible from two independent data lines. A Distributed ROM option permits pre-loading the memory with data during FPGA configuration.

Second, it is possible to program each left-hand LUT as a 16-bit shift register. Used in this way, each LUT can delay serial data anywhere from one to 16 clock cycles. The four left-hand LUTs of a single CLB can be combined to produce delays up to 64 clock cycles. The SHIFTIN and SHIFTOUT lines cascade LUTs to form larger shift registers. It is also possible to combine shift registers across more than one CLB. The resulting programmable delays can be used to balance the timing of data pipelines.

Block RAM Overview

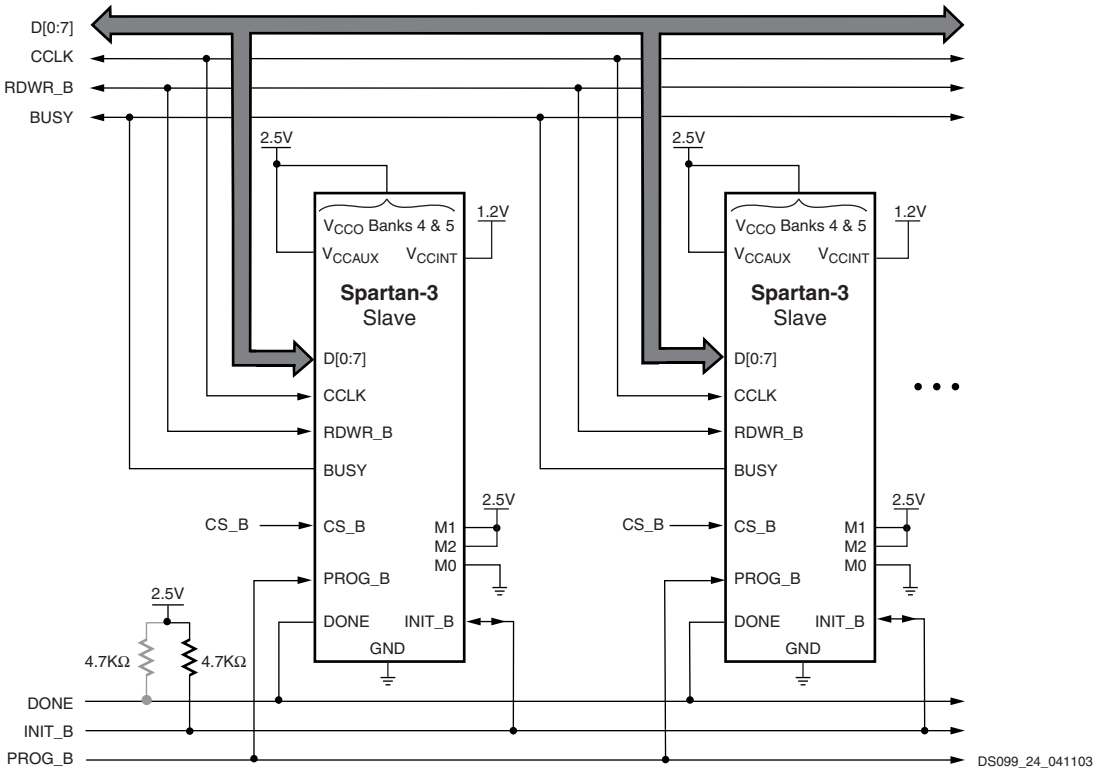
All Spartan-3 devices support block RAM, which is organized as configurable, synchronous 18Kbit blocks. Block RAM stores relatively large amounts of data more efficiently than the distributed RAM feature described earlier. (The latter is better suited for buffering small amounts of data anywhere along signal paths.) This section describes basic Block RAM functions. For more information, refer to the chapter entitled “Using Block RAM” in UG331.

The aspect ratio—i.e., width vs. depth—of each block RAM is configurable. Furthermore, multiple blocks can be cascaded to create still wider and/or deeper memories.

A choice among primitives determines whether the block RAM functions as dual- or single-port memory. A name of the form RAMB16_S[w_A]_S[w_B] calls out the dual-port primitive, where the integers w_A and w_B specify the total data path width at ports w_A and w_B, respectively. Thus, a RAMB16_S9_S18 is a dual-port RAM with a 9-bit-wide Port A and an 18-bit-wide Port B. A name of the form RAMB16_S[w] identifies the single-port primitive, where the integer w specifies the total data path width of the lone port. A RAMB16_S18 is a single-port RAM with an 18-bit-wide port. Other memory functions—e.g., FIFOs, data path width conversion, ROM, etc.—are readily available using the CORE Generator™ software, part of the Xilinx development software.

(e.g. all configuration pins taken together) when operating in the User mode. This is accomplished by setting the *Persist* option to *Yes*.

Multiple FPGAs can be configured using the Slave Parallel mode and can be made to start-up simultaneously. Figure 27 shows the device connections. To configure multiple devices in this way, wire the individual CCLK, Data, RDWR_B, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by deasserting the CS_B pin of each device in turn and writing the appropriate data.



Notes:

1. There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.
2. If the FPGAs use different configuration data files, configure them in sequence by first asserting the CS_B of one FPGA then asserting the CS_B of the other FPGA.
3. For information on how to program the FPGA using 3.3V signals and power, see 3.3V-Tolerant Configuration Interface.

Figure 27: **Connection Diagram for Slave Parallel Configuration**

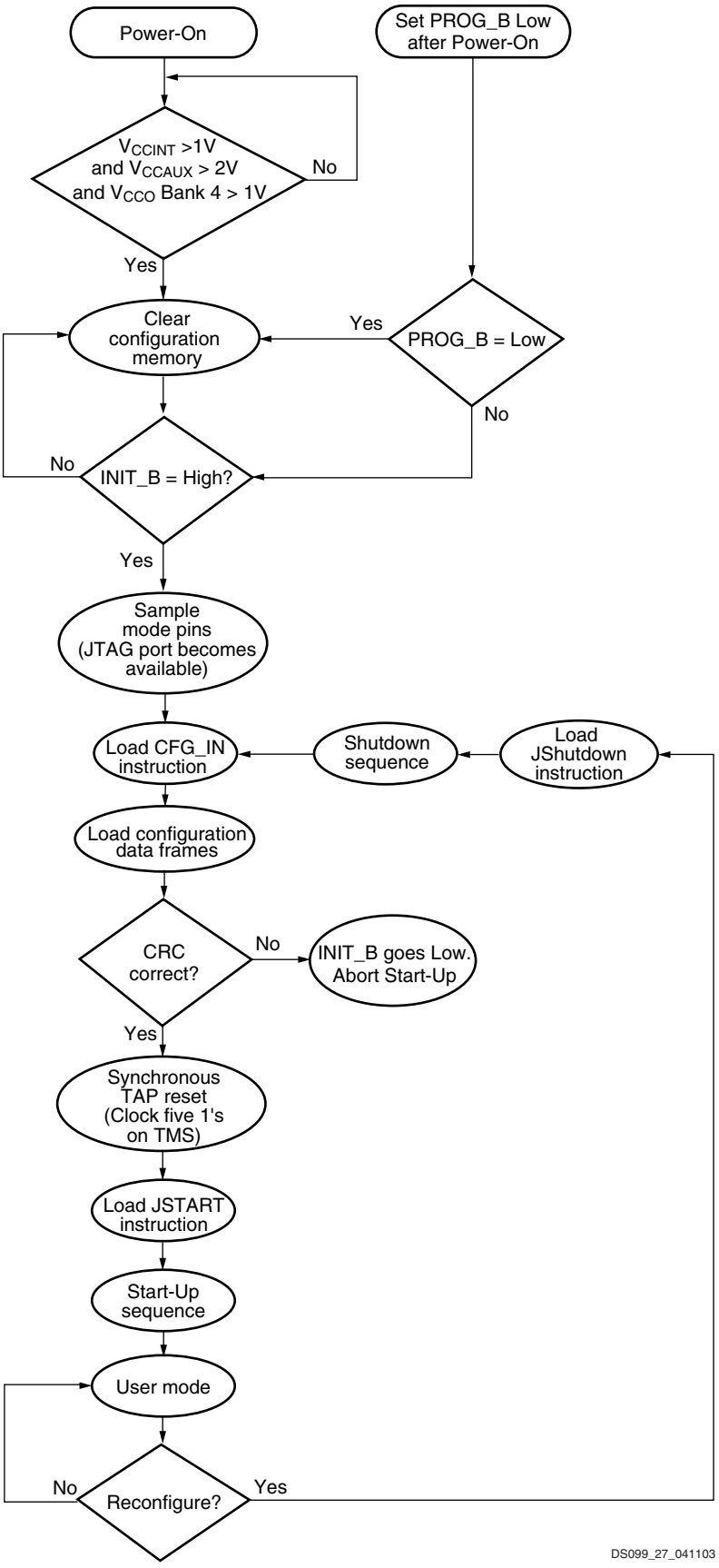


Figure 30: **Boundary-Scan Configuration Flow Diagram**

Configuration is automatically initiated after power-on unless it is delayed by the user. INIT_B is an open-drain line that the FPGA holds Low during the clearing of the configuration memory. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High. At this point, the configuration data is written to the FPGA. The FPGA pulses the Global Set/Reset (GSR) signal at the end of configuration, resetting all flip-flops. The completion of the entire process is signaled by the DONE pin going High.

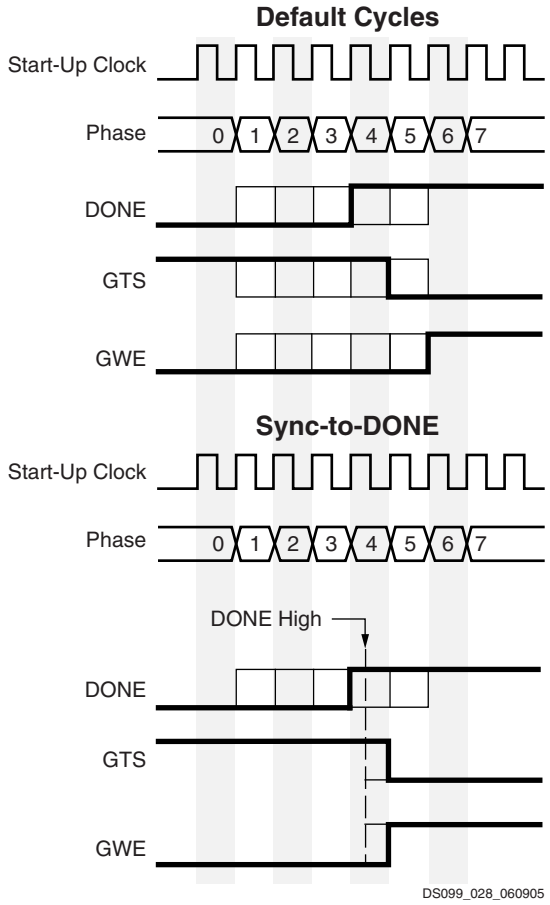


Figure 31: **Default Start-Up Sequence**

The default start-up sequence, shown in Figure 31, serves as a transition to the User mode. The default start-up sequence is that one CCLK cycle after DONE goes High, the Global Three-State signal (GTS) is released. This permits device outputs to which signals have been assigned to become active. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage elements to begin changing state in response to the design logic and the user clock.

The relative timing of configuration events can be changed via the BitGen options in the Xilinx development software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start synchronously. The sequence can also be paused at any stage, until lock has been achieved on any DCM.

Readback

Using Slave Parallel mode, configuration data from the FPGA can be read back. Readback is supported only in the Slave Parallel and Boundary-Scan modes.

Along with the configuration data, it is possible to read back the contents of all registers, distributed RAM, and block RAM resources. This capability is used for real-time debugging.

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Table 28: **Absolute Maximum Ratings *(Cont'd)***

Symbol	Description	Conditions	Min	Max	Units
I_{IK}	Input clamp current per I/O pin	–0.5 V < V_{IN} < (V_{CCO} + 0.5 V)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage pins relative to GND	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{SOL}	Soldering temperature(4)		–	220	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. All User I/O and Dual-Purpose pins (DIN/D0, D1–D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B) draw power from the V_{CCO} power rail of the associated bank. Keeping VIN within 500 mV of the associated V_{CCO} rails or ground rail ensures that the internal diode junctions that exist between each of these pins and the V_{CCO} and GND rails do not turn on. Table 32 specifies the V_{CCO} range used to determine the max limit. Input voltages outside the –0.5V to V_{CCO}+0.5V voltage range are permissible provided that the I_{IK} input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Prolonged exposure to such current may compromise device reliability. A sustained current of 10 mA will not compromise device reliability. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Generation FPGAs* for more details. The VIN limits apply to both the DC and AC components of signals. Simple application solutions are available that show how to handle overshoot/undershoot as well as achieve PCI compliance. Refer to the following application notes: XAPP457, *Powering and Configuring Spartan-3 Generation FPGAs in Compliant PCI Applications* and XAPP659, *Virtex®-II Pro / Virtex-II Pro X 3.3V I/O Design Guidelines*.
3. All Dedicated pins (M0–M2, CCLK, PROG_B, DONE, HSWAP_EN, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} rail do not turn on. Table 32 specifies the V_{CCAUX} range used to determine the max limit. When V_{CCAUX} is at its maximum recommended operating level (2.625V), V_{IN} max < 3.125V. As long as the V_{IN} max specification is met, oxide stress is not possible. For information concerning the use of 3.3V signals, see the 3.3V-Tolerant Configuration Interface, page 47. See also XAPP459.
4. For soldering guidelines, see UG112, *Device Packaging and Thermal Characteristics* and XAPP427, *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Table 29: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO4T}	Threshold for the V_{CCO} Bank 4 supply	0.4	1.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order. When applying V_{CCINT} power before V_{CCAUX} power, the FPGA may draw a *surplus* current in addition to the quiescent current levels specified in Table 34. Applying V_{CCAUX} eliminates the surplus current. The FPGA does not use any of the surplus current for the power-on process. For this power sequence, make sure that regulators with foldback features will not shut down inadvertently.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 4, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.
3. If a brown-out condition occurs where V_{CCAUX} or V_{CCINT} drops below the retention voltage indicated in Table 31, then V_{CCAUX} or V_{CCINT} must drop below the minimum power-on reset voltage in order to clear out the device configuration content.

Table 36: **DC Characteristics of User I/Os Using Single-Ended Standards *(Cont'd)***

Signal Standard (IOSTANDARD) and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVCMOS33[4]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_33, LVDCI_DV2_33		Note 3	Note 3		
LVTTL[4]	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
PCI33_3		Note 6	Note 6	$0.10V_{CCO}$	$0.90V_{CCO}$
SSTL18_I		6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475
SSTL18_I_DCI		Note 3	Note 3		
SSTL18_II		13.4	–13.4	V_{TT} – 0.475	V_{TT} + 0.475
SSTL2_I		8.1	–8.1	V_{TT} – 0.61	V_{TT} + 0.61
SSTL2_I_DCI		Note 3	Note 3		
SSTL2_II[7]		16.2	–16.2	V_{TT} – 0.81	V_{TT} + 0.81
SSTL2_II_DCI[7]		Note 3	Note 3		

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32 and Table 35.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL} – the output current condition under which VOL is tested
   I_{OH} – the output current condition under which VOH is tested
   V_{OL} – the output voltage that indicates a Low logic level
   V_{OH} – the output voltage that indicates a High logic level
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
   V_{CCO} – the supply voltage for output drivers as well as LVCMOS, LVTTL, and PCI inputs
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{TT} – the voltage applied to a resistor termination
3. Tested according to the standard's relevant specifications. When using the DCI version of a standard on a given I/O bank, that bank will consume more power than if the non-DCI version had been used instead. The additional power is drawn for the purpose of impedance-matching at the I/O pins. A portion of this power is dissipated in the two RREF resistors.
4. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for both the Fast and Slow slew attributes.
5. All dedicated output pins (CCLK, DONE, and TDO) and dual-purpose totem-pole output pins (D0-D7 and BUSY/DOUT) exhibit the characteristics of LVCMOS25 with 12 mA drive and slow slew rate. For information concerning the use of 3.3V signals, see 3.3V-Tolerant Configuration Interface, page 47.
6. Tested according to the relevant PCI specifications. For more information, see XAPP457.
7. The minimum usable V_{TT} voltage is 1.25V.

Table 41: **System-Synchronous Pin-to-Pin Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IOBDELAY = IFD, without DCM	XC3S50	–0.98	–0.93	ns
			XC3S200	–0.40	–0.35	ns
			XC3S400	–0.27	–0.22	ns
			XC3S1000	–1.19	–1.14	ns
			XC3S1500	–1.43	–1.38	ns
			XC3S2000	–2.33	–2.28	ns
			XC3S4000	–2.47	–2.42	ns
			XC3S5000	–2.66	–2.61	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *subtract* the appropriate adjustment from Table 44. If this is true of the data Input, *add* the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *add* the appropriate Input adjustment from Table 44. If this is true of the data Input, *subtract* the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Table 42: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Setup Times						
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2), IOBDELAY = NONE	XC3S50	1.65	1.89	ns
			XC3S200	1.37	1.57	ns
			XC3S400	1.37	1.57	ns
			XC3S1000	1.65	1.89	ns
			XC3S1500	1.65	1.89	ns
			XC3S2000	1.65	1.89	ns
			XC3S4000	1.73	1.99	ns
			XC3S5000	1.82	2.09	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the IFF's ICLK input. The Input Delay is programmed.	LVCMOS25(2), IOBDELAY = IFD	XC3S50	4.39	5.04	ns
			XC3S200	4.76	5.47	ns
			XC3S400	4.63	5.32	ns
			XC3S1000	5.02	5.76	ns
			XC3S1500	5.40	6.20	ns
			XC3S2000	6.68	7.68	ns
			XC3S4000	7.16	8.24	ns
			XC3S5000	7.33	8.42	ns

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
HSLVDCI_25			0.27	0.31	ns
HSLVDCI_33			0.28	0.32	ns
HSTL_I			0.60	0.69	ns
HSTL_I_DCI			0.59	0.68	ns
HSTL_III			0.19	0.22	ns
HSTL_III_DCI			0.20	0.23	ns
HSTL_I_18			0.18	0.21	ns
HSTL_I_DCI_18			0.17	0.19	ns
HSTL_II_18			–0.02	–0.01	ns
HSTL_II_DCI_18			0.75	0.86	ns
HSTL_III_18			0.28	0.32	ns
HSTL_III_DCI_18			0.28	0.32	ns
LVCMOS12	Slow	2 mA	7.60	8.73	ns
		4 mA	7.42	8.53	ns
		6 mA	6.67	7.67	ns
	Fast	2 mA	3.16	3.63	ns
		4 mA	2.70	3.10	ns
		6 mA	2.41	2.77	ns
LVCMOS15	Slow	2 mA	4.55	5.23	ns
		4 mA	3.76	4.32	ns
		6 mA	3.57	4.11	ns
		8 mA	3.55	4.09	ns
		12 mA	3.00	3.45	ns
	Fast	2 mA	3.11	3.57	ns
		4 mA	1.71	1.96	ns
		6 mA	1.44	1.66	ns
		8 mA	1.26	1.44	ns
		12 mA	1.11	1.27	ns
LVDCI_15			1.51	1.74	ns
LVDCI_DV2_15			1.32	1.52	ns

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package				
			VQ100	TQ144	PQ208	CP132	FT256, FG320, FG456, FG676, FG900, FG1156
LVCMOS33	Slow	2	34	24	24	52	76
		4	17	14	14	26	46
		6	17	11	11	26	27
		8	10	10	10	13	20
		12	9	9	9	13	13
		16	8	8	8	8	10
		24	8	8	8	8	9
	Fast	2	20	20	20	26	44
		4	15	15	15	15	26
		6	11	11	11	13	16
		8	10	10	10	10	12
		12	8	8	8	8	10
		16	8	8	8	8	8
		24	7	7	7	7	7
LVDCI_33			10	10	10	10	10
LVDCI_DV2_33			10	10	10	10	10
HSLVDCI_33			10	10	10	10	10
LVTTL	Slow	2	34	25	25	52	60
		4	17	16	16	26	41
		6	17	15	15	26	29
		8	12	12	12	13	22
		12	10	10	10	13	13
		16	10	10	10	10	11
		24	8	8	8	8	9
	Fast	2	20	20	20	26	34
		4	13	13	13	13	20
		6	11	11	11	13	15
		8	10	10	10	10	12
		12	9	9	9	9	10
		16	8	8	8	8	9
		24	7	7	7	7	7

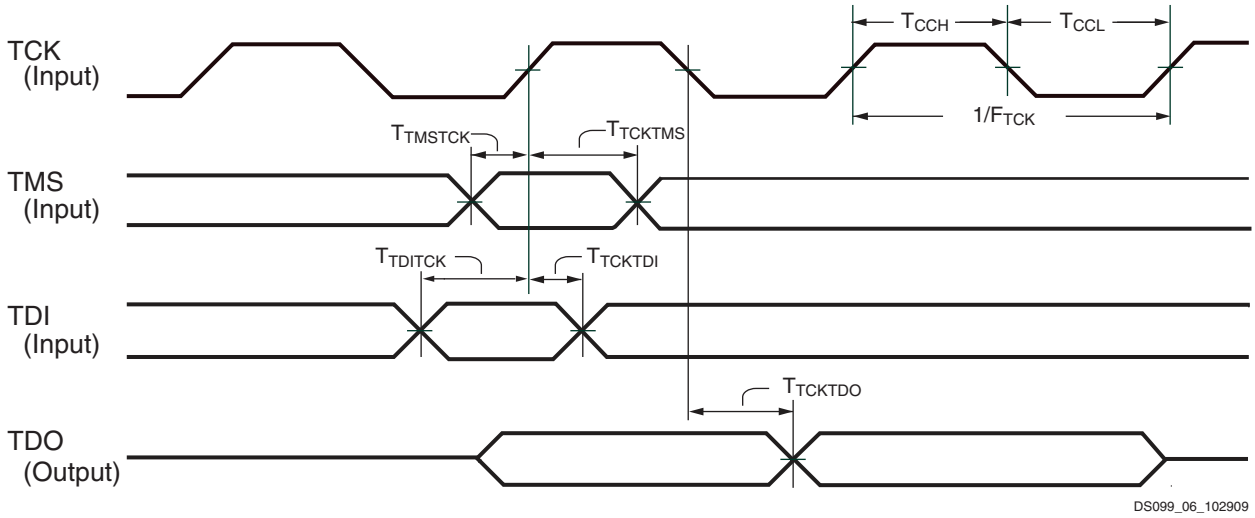

Figure 39: **JTAG Waveforms**

Table 68: **Timing for the JTAG Test Access Port**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin		1.0	11.0	ns
Setup Times					
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin		7.0	–	ns
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin		7.0	–	ns
Hold Times					
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin		0	–	ns
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin		0	–	ns
Clock Timing					
T_{TCKH}	TCK pin High pulse width		5	∞	ns
T_{TCKL}	TCK pin Low pulse width		5	∞	ns
F_{TCK}	Frequency of the TCK signal	JTAG Configuration	0	33	MHz
		Boundary-Scan	0	25	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.

Revision History

Date	Version	Description
04/11/03	1.0	Initial Xilinx release.
07/11/03	1.1	Extended Absolute Maximum Rating for junction temperature in Table 28. Added numbers for typical quiescent supply current (Table 34) and DLL timing.
02/06/04	1.2	Revised V_{IN} maximum rating (Table 28). Added power-on requirements (Table 30), leakage current number (Table 33), and differential output voltage levels (Table 38) for Rev. 0. Published new quiescent current numbers (Table 34). Updated pull-up and pull-down resistor strengths (Table 33). Added LVDCI_DV2 and LVPECL standards (Table 37 and Table 38). Changed CCLK setup time (Table 66 and Table 67).
03/04/04	1.3	Added timing numbers from v1.29 speed files as well as DCM timing (Table 58 through Table 63).
08/24/04	1.4	Added reference to errata documents on page 49. Clarified Absolute Maximum Ratings and added ESD information (Table 28). Explained V_{CCO} ramp time measurement (Table 30). Clarified I_L specification (Table 33). Updated quiescent current numbers and added information on power-on and surplus current (Table 34). Adjusted V_{REF} range for HSTL_III and HSTL_I_18 and changed V_{IH} min for LVCMOS12 (Table 35). Added note limiting V_{TT} range for SSTL2_II signal standards (Table 36). Calculated V_{OH} and V_{OL} levels for differential standards (Table 38). Updated Switching Characteristics with speed file v1.32 (Table 40 through Table 48 and Table 51 through Table 56). Corrected IOB test conditions (Table 41). Updated DCM timing with latest characterization data (Table 58 through Table 62). Improved DCM CLKIN pulse width specification (Table 58). Recommended use of Virtex-II FPGA Jitter calculator (Table 61). Improved DCM PSCLK pulse width specification (Table 62). Changed Phase Shifter lock time parameter (Table 63). Because the BitGen option Centered_x#_y# is not necessary for Variable Phase Shift mode, removed BitGen command table and referring text. Adjusted maximum CCLK frequency for the slave serial and parallel configuration modes (Table 66). Inverted CCLK waveform (Figure 37). Adjusted JTAG setup times (Table 68).
12/17/04	1.5	Updated timing parameters to match v1.35 speed file. Improved V_{CCO} ramp time specification (Table 30). Added a note limiting the rate of change of V_{CCAUX} (Table 32). Added typical quiescent current values for the XC3S2000, XC3S4000, and XC3S5000 (Table 34). Increased I_{OH} and I_{OL} for SSTL2-I and SSTL2-II standards (Table 36). Added SSO guidelines for the VQ, TQ, and PQ packages as well as edited SSO guidelines for the FT and FG packages (Table 50). Added maximum CCLK frequencies for configuration using compressed bitstreams (Table 66 and Table 67). Added specifications for the HSLVDCI standards (Table 35, Table 36, Table 44, Table 47, Table 48, and Table 50).
08/19/05	1.6	Updated timing parameters to match v1.37 speed file. All Spartan-3 FPGA part types, except XC3S5000, promoted to Production status. Removed V_{CCO} ramp rate restriction from all mask revision 'E' and later devices (Table 30). Added equivalent resistance values for internal pull-up and pull-down resistors (Table 33). Added worst-case quiescent current values for XC3S2000, XC3S4000, XC3S5000 (Table 34). Added industrial temperature range specification and improved typical quiescent current values (Table 34). Improved the DLL minimum clock input frequency specification from 24 MHz down to 18 MHz (Table 58). Improved the DFS minimum and maximum clock output frequency specifications (Table 60, Table 61). Added new miscellaneous DCM specifications (Table 64), primarily affecting Industrial temperature range applications. Updated Simultaneously Switching Output Guidelines and Table 50 for QFP packages. Added information on SSTL18_II I/O standard and timing to support DDR2 SDRAM interfaces. Added differential (or complementary single-ended) DIFF_HSTL_II_18 and DIFF_SSTL2_II I/O standards, including DCI terminated versions. Added electro-static discharge (ESD) data for the XC3S2000 and larger FPGAs (Table 28). Added link to Spartan-3 FPGA errata notices and how to receive automatic notifications of data sheet or errata changes.
04/03/06	2.0	Upgraded Module 3, removing Preliminary status. Moved XC3S5000 to Production status in Table 39. Finalized I/O timing on XC3S5000 for v1.38 speed files. Added minimum timing values for various logic and I/O paths. Corrected labels for R_{PU} and R_{PD} and updated R_{PD} conditions for in Table 33. Added final mask revision 'E' specifications for LVDS_25, RSDS_25, LVDSEXT_25 differential outputs to Table 38. Added BLVDS termination requirements to Figure 34. Improved recommended Simultaneous Switching Outputs (SSOs) limits in Table 50 for quad-flat packaged based on silicon testing using devices soldered on a printed circuit board. Updated Note 2 in Table 63. Updated Note 6 in Table 30. Added INIT_B minimum pulse width specification, T_{INIT}, to Table 65.
04/26/06	2.1	Updated document links.

Once the FPGA enters User mode after completing configuration, the DONE pin no longer drives the DONE pin Low. The bitstream generator option DonePin determines whether or not a pull-up resistor is present on the DONE pin to pull the pin to VCCAUX. If the pull-up resistor is eliminated, then the DONE pin must be pulled High using an external pull-up resistor or one of the FPGAs in the design must actively drive the DONE pin High via the DriveDone bitstream generator option.

The bitstream generator option DriveDone causes the FPGA to actively drive the DONE output High after configuration. This option should only be used in single-FPGA designs or on the last FPGA in a multi-FPGA daisy-chain.

By default, the bitstream generator software retains the pull-up resistor and does not actively drive the DONE pin as highlighted in Table 74, which shows the interaction of these bitstream options in single- and multi-FPGA designs.

Table 74: **DonePin and DriveDone Bitstream Option Interaction**

DonePin	DriveDone	Single- or Multi-FPGA Design	Comments
Pullnone	No	Single	External pull-up resistor, with value between 330Ω to 3.3kΩ, required on DONE.
Pullnone	No	Multi	External pull-up resistor, with value between 330Ω to 3.3kΩ, required on common node connecting to all DONE pins.
Pullnone	Yes	Single	OK, no external requirements.
Pullnone	Yes	Multi	DriveDone on last device in daisy-chain only. No external requirements.
Pullup	No	Single	OK, but pull-up on DONE pin has slow rise time. May require 330Ω pull-up resistor for high CCLK frequencies.
Pullup	No	Multi	External pull-up resistor, with value between 330Ω to 3.3kΩ, required on common node connecting to all DONE pins.
Pullup	Yes	Single	OK, no external requirements.
Pullup	Yes	Multi	DriveDone on last device in daisy-chain only. No external requirements.

M2, M1, M0: Configuration Mode Selection

The M2, M1, and M0 inputs select the FPGA configuration mode, as described in Table 75. The logic levels applied to the mode pins are sampled on the rising edge of INIT_B.

Table 75: **Spartan-3 FPGA Mode Select Settings**

Configuration Mode	M2	M1	M0
Master Serial	0	0	0
Slave Serial	1	1	1
Master Parallel	0	1	1
Slave Parallel	1	1	0
JTAG	1	0	1
Reserved	0	0	1
Reserved	0	1	0
Reserved	1	0	0
After Configuration	X	X	X

Notes:

1. X = don't care, either 0 or 1.

Before and during configuration, the mode pins have an internal pull-up resistor to VCCAUX, regardless of the HSWAP_EN pin. If the mode pins are unconnected, then the FPGA defaults to the Slave Serial configuration mode. After configuration successfully completes, any levels applied to these input are ignored. Furthermore, the bitstream generator options M0Pin, M1Pin, and M2Pin determines whether a pull-up resistor, pull-down resistor, or no resistor is present on its respective mode pin, M0, M1, or M2.

VQ100 Footprint

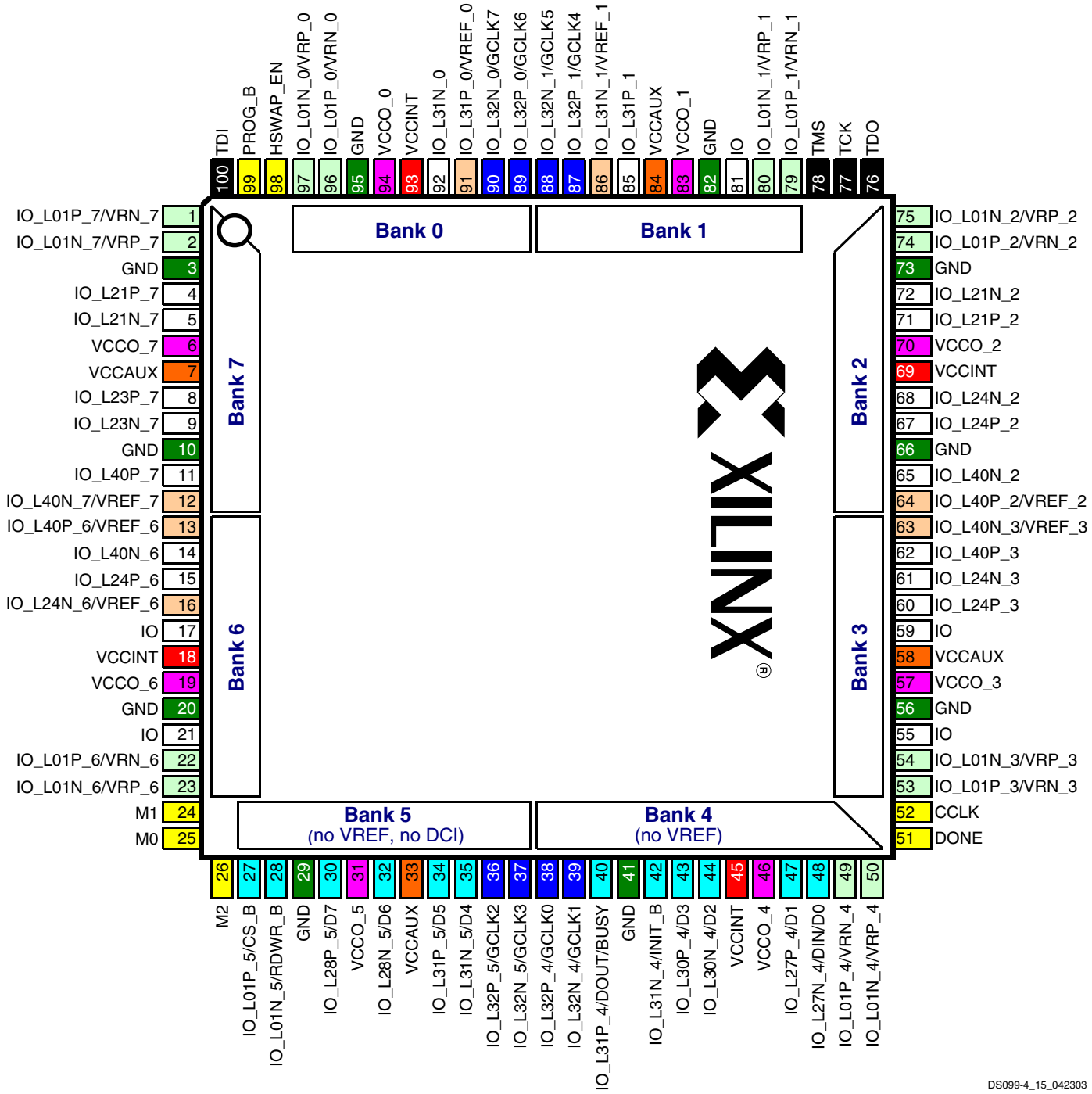

Figure 44: **VQ100 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

22	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	7	**VREF:** User I/O or input voltage reference for bank
14	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input	8	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	10	**GND:** Ground	4	**VCCAUX:** Auxiliary voltage supply (+2.5V)

Table 91: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
5	IO_L32P_5/GCLK2	P52	GCLK
6	IO_L01N_6/VRP_6	P36	DCI
6	IO_L01P_6/VRN_6	P35	DCI
6	IO_L20N_6	P33	I/O
6	IO_L20P_6	P32	I/O
6	IO_L21N_6	P31	I/O
6	IO_L21P_6	P30	I/O
6	IO_L22N_6	P28	I/O
6	IO_L22P_6	P27	I/O
6	IO_L23N_6	P26	I/O
6	IO_L23P_6	P25	I/O
6	IO_L24N_6/VREF_6	P24	VREF
6	IO_L24P_6	P23	I/O
6	IO_L40N_6	P21	I/O
6	IO_L40P_6/VREF_6	P20	VREF
7	IO/VREF_7	P4	VREF
7	IO_L01N_7/VRP_7	P2	DCI
7	IO_L01P_7/VRN_7	P1	DCI
7	IO_L20N_7	P6	I/O
7	IO_L20P_7	P5	I/O
7	IO_L21N_7	P8	I/O
7	IO_L21P_7	P7	I/O
7	IO_L22N_7	P11	I/O
7	IO_L22P_7	P10	I/O
7	IO_L23N_7	P13	I/O
7	IO_L23P_7	P12	I/O
7	IO_L24N_7	P15	I/O
7	IO_L24P_7	P14	I/O
7	IO_L40N_7/VREF_7	P18	VREF
7	IO_L40P_7	P17	I/O
0,1	VCCO_TOP	P126	VCCO
0,1	VCCO_TOP	P138	VCCO
0,1	VCCO_TOP	P115	VCCO
2,3	VCCO_RIGHT	P106	VCCO
2,3	VCCO_RIGHT	P75	VCCO
2,3	VCCO_RIGHT	P91	VCCO
4,5	VCCO_BOTTOM	P54	VCCO
4,5	VCCO_BOTTOM	P43	VCCO
4,5	VCCO_BOTTOM	P66	VCCO
6,7	VCCO_LEFT	P19	VCCO

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
1	IO_L15P_1	IO_L15P_1	E17	I/O
1	IO_L16N_1	IO_L16N_1	B17	I/O
1	IO_L16P_1	IO_L16P_1	C17	I/O
1	N.C. (◆)	IO_L19N_1	C16	I/O
1	N.C. (◆)	IO_L19P_1	D16	I/O
1	N.C. (◆)	IO_L22N_1	A16	I/O
1	N.C. (◆)	IO_L22P_1	B16	I/O
1	IO_L24N_1	IO_L24N_1	D15	I/O
1	IO_L24P_1	IO_L24P_1	E15	I/O
1	IO_L25N_1	IO_L25N_1	B15	I/O
1	IO_L25P_1	IO_L25P_1	A15	I/O
1	IO_L27N_1	IO_L27N_1	D14	I/O
1	IO_L27P_1	IO_L27P_1	E14	I/O
1	IO_L28N_1	IO_L28N_1	A14	I/O
1	IO_L28P_1	IO_L28P_1	B14	I/O
1	IO_L29N_1	IO_L29N_1	C13	I/O
1	IO_L29P_1	IO_L29P_1	D13	I/O
1	IO_L30N_1	IO_L30N_1	A13	I/O
1	IO_L30P_1	IO_L30P_1	B13	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D12	VREF
1	IO_L31P_1	IO_L31P_1	E12	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B12	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C12	GCLK
1	VCCO_1	VCCO_1	C15	VCCO
1	VCCO_1	VCCO_1	F15	VCCO
1	VCCO_1	VCCO_1	G12	VCCO
1	VCCO_1	VCCO_1	G13	VCCO
1	VCCO_1	VCCO_1	G14	VCCO
2	IO	IO	C22	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C20	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C21	DCI
2	IO_L16N_2	IO_L16N_2	D20	I/O
2	IO_L16P_2	IO_L16P_2	D19	I/O
2	IO_L17N_2	IO_L17N_2	D21	I/O
2	IO_L17P_2/VREF_2	IO_L17P_2/VREF_2	D22	VREF
2	IO_L19N_2	IO_L19N_2	E18	I/O
2	IO_L19P_2	IO_L19P_2	F18	I/O
2	IO_L20N_2	IO_L20N_2	E19	I/O
2	IO_L20P_2	IO_L20P_2	E20	I/O
2	IO_L21N_2	IO_L21N_2	E21	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
3	IO_L21P_3	IO_L21P_3	Y23	I/O
3	IO_L22N_3	IO_L22N_3	Y26	I/O
3	IO_L22P_3	IO_L22P_3	Y25	I/O
3	IO_L23N_3	IO_L23N_3	Y28	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	Y27	VREF
3	IO_L24N_3	IO_L24N_3	Y30	I/O
3	IO_L24P_3	IO_L24P_3	Y29	I/O
3	IO_L26N_3	IO_L26N_3	W30	I/O
3	IO_L26P_3	IO_L26P_3	W29	I/O
3	IO_L27N_3	IO_L27N_3	V21	I/O
3	IO_L27P_3	IO_L27P_3	W21	I/O
3	IO_L28N_3	IO_L28N_3	V23	I/O
3	IO_L28P_3	IO_L28P_3	V22	I/O
3	IO_L29N_3	IO_L29N_3	V25	I/O
3	IO_L29P_3	IO_L29P_3	W26	I/O
3	IO_L31N_3	IO_L31N_3	V30	I/O
3	IO_L31P_3	IO_L31P_3	V29	I/O
3	IO_L32N_3	IO_L32N_3	U22	I/O
3	IO_L32P_3	IO_L32P_3	U21	I/O
3	IO_L33N_3	IO_L33N_3	U25	I/O
3	IO_L33P_3	IO_L33P_3	U24	I/O
3	IO_L34N_3	IO_L34N_3	U29	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	U28	VREF
3	IO_L35N_3	IO_L35N_3	T22	I/O
3	IO_L35P_3	IO_L35P_3	T21	I/O
3	IO_L37N_3	IO_L37N_3	T24	I/O
3	IO_L37P_3	IO_L37P_3	T23	I/O
3	IO_L38N_3	IO_L38N_3	T26	I/O
3	IO_L38P_3	IO_L38P_3	T25	I/O
3	IO_L39N_3	IO_L39N_3	T28	I/O
3	IO_L39P_3	IO_L39P_3	T27	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	T30	VREF
3	IO_L40P_3	IO_L40P_3	T29	I/O
3	N.C. (◆)	IO_L46N_3	W23	I/O
3	N.C. (◆)	IO_L46P_3	W22	I/O
3	N.C. (◆)	IO_L47N_3	W25	I/O
3	N.C. (◆)	IO_L47P_3	W24	I/O
3	N.C. (◆)	IO_L48N_3	W28	I/O
3	N.C. (◆)	IO_L48P_3	W27	I/O
3	N.C. (◆)	IO_L50N_3	V27	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
7	VCCO_7	VCCO_7	N3	VCCO
7	VCCO_7	VCCO_7	G5	VCCO
7	VCCO_7	VCCO_7	J7	VCCO
7	VCCO_7	VCCO_7	N7	VCCO
7	VCCO_7	VCCO_7	L9	VCCO
7	VCCO_7	VCCO_7	M11	VCCO
7	VCCO_7	VCCO_7	N11	VCCO
7	VCCO_7	VCCO_7	P11	VCCO
N/A	GND	GND	A1	GND
N/A	GND	GND	B1	GND
N/A	GND	GND	F1	GND
N/A	GND	GND	K1	GND
N/A	GND	GND	P1	GND
N/A	GND	GND	U1	GND
N/A	GND	GND	AA1	GND
N/A	GND	GND	AE1	GND
N/A	GND	GND	AJ1	GND
N/A	GND	GND	AK1	GND
N/A	GND	GND	A2	GND
N/A	GND	GND	B2	GND
N/A	GND	GND	AJ2	GND
N/A	GND	GND	E5	GND
N/A	GND	GND	K5	GND
N/A	GND	GND	P5	GND
N/A	GND	GND	U5	GND
N/A	GND	GND	AA5	GND
N/A	GND	GND	AF5	GND
N/A	GND	GND	A6	GND
N/A	GND	GND	AK6	GND
N/A	GND	GND	K8	GND
N/A	GND	GND	P8	GND
N/A	GND	GND	U8	GND
N/A	GND	GND	AA8	GND
N/A	GND	GND	A10	GND
N/A	GND	GND	E10	GND
N/A	GND	GND	H10	GND
N/A	GND	GND	AC10	GND
N/A	GND	GND	AF10	GND
N/A	GND	GND	AK10	GND
N/A	GND	GND	R12	GND