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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	5120
Number of Logic Elements/Cells	46080
Total RAM Bits	737280
Number of I/O	333
Number of Gates	2000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s2000-5fgg456c

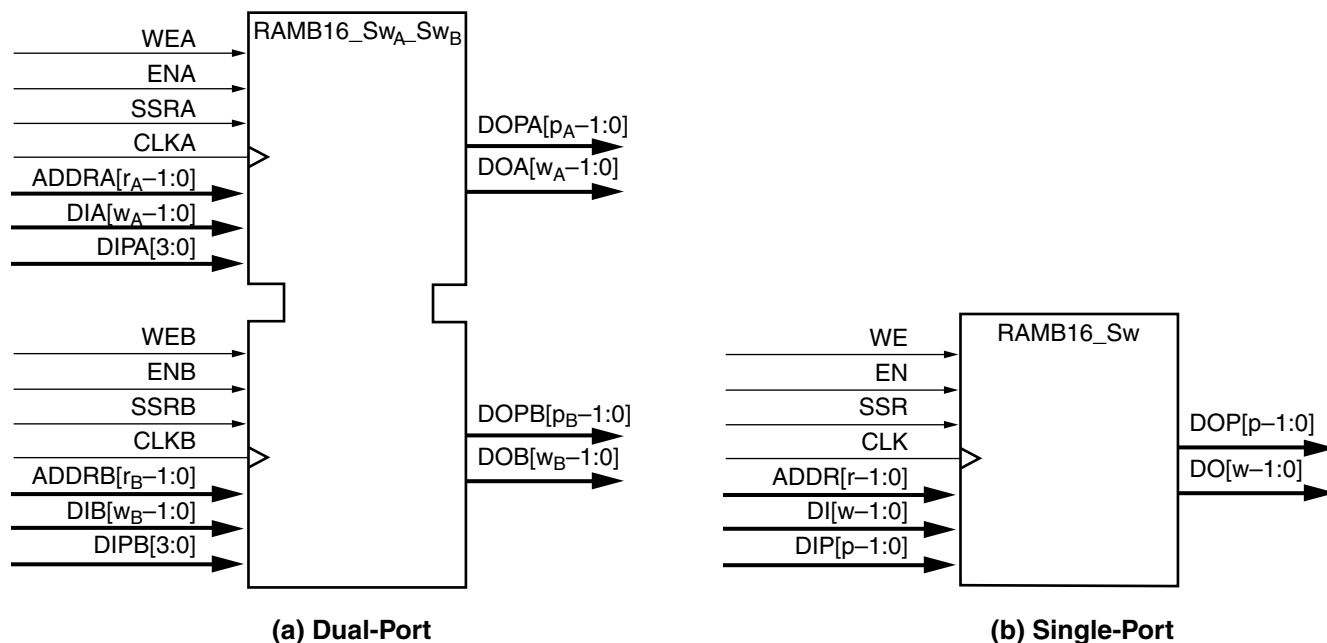
upper path), enter the slice and connect directly to the LUT. Once inside the slice, the lower 4-bit path passes through a function generator 'F' (or 'G') that performs logic operations. The function generator's Data output, 'D', offers five possible paths:

- Exit the slice via line 'X' (or 'Y') and return to interconnect.
- Inside the slice, 'X' (or 'Y') serves as an input to the DXMUX (DYMUX) which feeds the data input, 'D', of the FFX (FFY) storage element. The 'Q' output of the storage element drives the line XQ (or YQ) which exits the slice.
- Control the CYMUXF (or CYMUXG) multiplexer on the carry chain.
- With the carry chain, serve as an input to the XORF (or XORG) exclusive-OR gate that performs arithmetic operations, producing a result on 'X' (or 'Y').
- Drive the multiplexer F5MUX to implement logic functions wider than four bits. The 'D' outputs of both the F-LUT and G-LUT serve as data inputs to this multiplexer.

In addition to the main logic paths described above, there are two bypass paths that enter the slice as BX and BY. Once inside the FPGA, BX in the bottom half of the slice (or BY in the top half) can take any of several possible branches:

- Bypass both the LUT and the storage element, then exit the slice as BXOUT (or BYOUT) and return to interconnect.
- Bypass the LUT, then pass through a storage element via the D input before exiting as XQ (or YQ).
- Control the wide function multiplexer F5MUX (or F6MUX).
- Via multiplexers, serve as an input to the carry chain.
- Drives the DI input of the LUT.
- BY can control the REV inputs of both the FFY and FFX storage elements.
- Finally, the DIG_MUX multiplexer can switch BY onto the DIG line, which exits the slice.

Other slice signals shown in [Figure 12](#) are discussed in the sections that follow.



DS099-2_13_112905

Notes:

1. w_A and w_B are integers representing the total data path width (i.e., data bits plus parity bits) at ports A and B, respectively.
2. p_A and p_B are integers that indicate the number of data path lines serving as parity bits.
3. r_A and r_B are integers representing the address bus width at ports A and B, respectively.
4. The control signals CLK, WE, EN, and SSR on both ports have the option of inverted polarity.

Figure 14: Block RAM Primitives

Table 13: Block RAM Port Signals

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Address Bus	ADDRA	ADDRB	Input	The Address Bus selects a memory location for read or write operations. The width (w) of the port's associated data path determines the number of available address lines (r). Whenever a port is enabled (ENA or ENB = High), address transitions must meet the data sheet setup and hold times with respect to the port clock (CLKA or CLKB). This requirement must be met, even if the RAM read output is of no interest.
Data Input Bus	DIA	DIB	Input	Data at the DI input bus is written to the addressed memory location addressed on an enabled active CLK edge. It is possible to configure a port's total data path width (w) to be 1, 2, 4, 9, 18, or 36 bits. This selection applies to both the DI and DO paths of a given port. Each port is independent. For a port assigned a width (w), the number of addressable locations is $16,384/(w-p)$ where "p" is the number of parity bits. Each memory location has a width of "w" (including parity bits). See the DIP signal description for more information of parity.
Parity Data Input(s)	DIPA	DIPB	Input	Parity inputs represent additional bits included in the data input path to support error detection. The number of parity bits "p" included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 14.

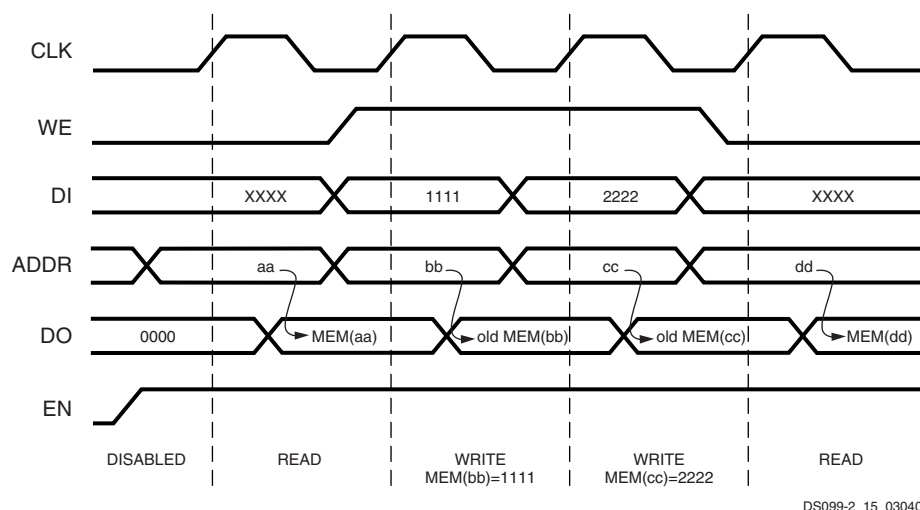


Figure 16: Waveforms of Block RAM Data Operations with READ_FIRST Selected

Choosing a third attribute called NO_CHANGE puts the DO outputs in a latched state when asserting WE. Under this condition, the DO outputs will retain the data driven just before WE was asserted. NO_CHANGE timing is shown in the portion of Figure 17 during which WE is High.

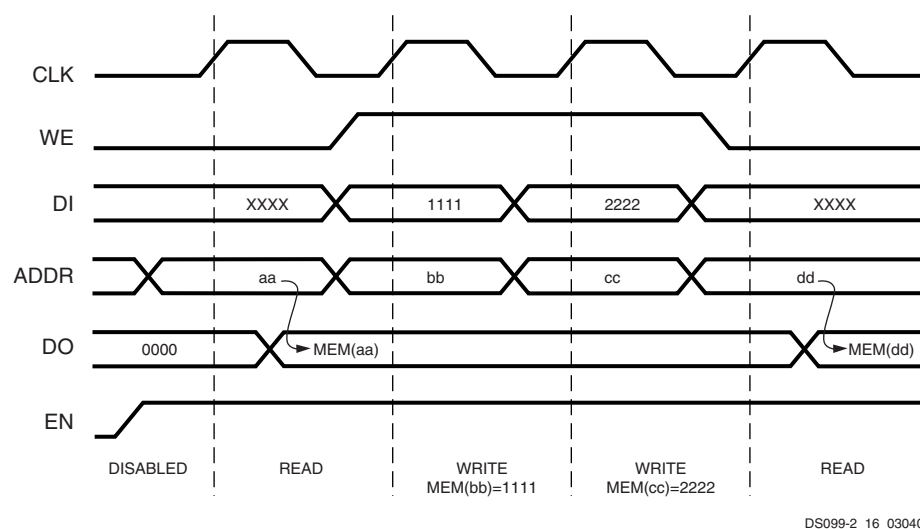


Figure 17: Waveforms of Block RAM Data Operations with NO_CHANGE Selected

Dedicated Multipliers

All Spartan-3 devices provide embedded multipliers that accept two 18-bit words as inputs to produce a 36-bit product. This section provides an introduction to multipliers. For further details, refer to the chapter entitled “Using Embedded Multipliers” in [UG331](#).

The input buses to the multiplier accept data in two’s-complement form (either 18-bit signed or 17-bit unsigned). One such multiplier is matched to each block RAM on the die. The close physical proximity of the two ensures efficient data handling. Cascading multipliers permits multiplicands more than three in number as well as wider than 18-bits. The multiplier is placed in a design using one of two primitives: an asynchronous version called MULT18X18 and a version with a register called MULT18X18S, as shown in [Figure 18](#). The signals for these primitives are defined in [Table 15](#).

The CORE Generator system produces multipliers based on these primitives that can be configured to suit a wide range of requirements.

The output frequency (f_{CLKFX}) can be expressed as a function of the incoming clock frequency (f_{CLKIN}) as follows:

$$f_{\text{CLKFX}} = f_{\text{CLKIN}}(\text{CLKFX_MULTIPLY}/\text{CLKFX_DIVIDE}) \quad \text{Equation 3}$$

Regarding the two attributes, it is possible to assign any combination of integer values, provided that two conditions are met:

- The two values fall within their corresponding ranges, as specified in [Table 18](#).
- The f_{CLKFX} frequency calculated from the above expression accords with the DCM's operating frequency specifications.

For example, if $\text{CLKFX_MULTIPLY} = 5$ and $\text{CLKFX_DIVIDE} = 3$, then the frequency of the output clock signal would be 5/3 that of the input clock signal.

DFS Frequency Modes

The DFS supports two operating modes, High Frequency and Low Frequency, with each specified over a different clock frequency range. The $\text{DFS_FREQUENCY_MODE}$ attribute chooses between the two modes. When the attribute is set to LOW, the Low Frequency mode permits the two DFS outputs to operate over a low-to-moderate frequency range. When the attribute is set to HIGH, the High Frequency mode allows both these outputs to operate at the highest possible frequencies.

DFS With or Without the DLL

The DFS component can be used with or without the DLL component:

Without the DLL, the DFS component multiplies or divides the CLKIN signal frequency according to the respective CLKFX_MULTIPLY and CLKFX_DIVIDE values, generating a clock with the new target frequency on the CLKFX and CLKFX180 outputs. Though classified as belonging to the DLL component, the CLKIN input is shared with the DFS component. This case does not employ feedback loop; therefore, it cannot correct for clock distribution delay.

With the DLL, the DFS operates as described in the preceding case, only with the additional benefit of eliminating the clock distribution delay. In this case, a feedback loop from the CLK0 output to the CLKFB input must be present.

The DLL and DFS components work together to achieve this phase correction as follows: Given values for the CLKFX_MULTIPLY and CLKFX_DIVIDE attributes, the DLL selects the delay element for which the output clock edge coincides with the input clock edge whenever mathematically possible. For example, when $\text{CLKFX_MULTIPLY} = 5$ and $\text{CLKFX_DIVIDE} = 3$, the input and output clock edges will coincide every three input periods, which is equivalent in time to five output periods.

Smaller CLKFX_MULTIPLY and CLKFX_DIVIDE values achieve faster lock times. With no factors common to the two attributes, alignment will occur once with every number of cycles equal to the CLKFX_DIVIDE value. Therefore, it is recommended that the user reduce these values by factoring wherever possible. For example, given $\text{CLKFX_MULTIPLY} = 9$ and $\text{CLKFX_DIVIDE} = 6$, removing a factor of three yields $\text{CLKFX_MULTIPLY} = 3$ and $\text{CLKFX_DIVIDE} = 2$. While both value-pairs will result in the multiplication of clock frequency by 3/2, the latter value-pair will enable the DLL to lock more quickly.

Table 18: DFS Attributes

Attribute	Description	Values
$\text{DFS_FREQUENCY_MODE}$	Chooses between High Frequency and Low Frequency modes	Low, High
CLKFX_MULTIPLY	Frequency multiplier constant	Integer from 2 to 32
CLKFX_DIVIDE	Frequency divisor constant	Integer from 1 to 32

Table 19: DFS Signals

Signal	Direction	Description
CLKFX	Output	Multiplies the CLKIN frequency by the attribute-value ratio ($\text{CLKFX_MULTIPLY}/\text{CLKFX_DIVIDE}$) to generate a clock signal with a new target frequency.
CLKFX180	Output	Generates a clock signal with same frequency as CLKFX, only shifted 180° out-of-phase.

Table 22: Status Logic Signals

Signal	Direction	Description
RST	Input	A High resets the entire DCM to its initial power-on state. Initializes the DLL taps for a delay of zero. Sets the LOCKED output Low. This input is asynchronous.
STATUS[7:0]	Output	The bit values on the STATUS bus provide information regarding the state of DLL and PS operation
LOCKED	Output	Indicates that the CLKIN and CLKFB signals are in phase by going High. The two signals are out-of-phase when Low.

Table 23: DCM STATUS Bus

Bit	Name	Description
0	Phase Shift Overflow	A value of 1 indicates a phase shift overflow when one of two conditions occurs: Incrementing (or decrementing) TPS beyond 255/256 of a CLKIN cycle. The DLL is producing its maximum possible phase shift (i.e., all delay taps are active). ⁽¹⁾
1	CLKIN Input Stopped Toggling	A value of 1 indicates that the CLKIN input signal is not toggling. A value of 0 indicates toggling. This bit functions only when the CLKFB input is connected. ⁽²⁾
2	CLKFX/CLKFX180 Output Stopped Toggling	A value of 1 indicates that the CLKFX or CLKFX180 output signals are not toggling. A value of 0 indicates toggling. This bit functions only when using the Digital Frequency Synthesizer (DFS).
3:7	Reserved	—

Notes:

1. The DLL phase shift with all delay taps active is specified as the parameter FINE_SHIFT_RANGE.
2. If only the DFS clock outputs are used, but none of the DLL clock outputs, this bit will not go High when the CLKIN signal stops.

Table 24: Status Attributes

Attribute	Description	Values
STARTUP_WAIT	Delays transition from configuration to user mode until lock condition is achieved.	TRUE, FALSE

Stabilizing DCM Clocks Before User Mode

It is possible to delay the completion of device configuration until after the DLL has achieved a lock condition using the STARTUP_WAIT attribute described in [Table 24](#). This option ensures that the FPGA does not enter user mode—i.e., begin functional operation—until all system clocks generated by the DCM are stable. In order to achieve the delay, it is necessary to set the attribute to TRUE as well as set the BitGen option LCK_cycle to one of the six cycles making up the Startup phase of configuration. The selected cycle defines the point at which configuration will halt until the LOCKED output goes High.

Global Clock Network

Spartan-3 devices have eight Global Clock inputs called GCLK0 - GCLK7. These inputs provide access to a low-capacitance, low-skew network that is well-suited to carrying high-frequency signals. The Spartan-3 FPGAs clock network is shown in [Figure 23](#). GCLK0 through GCLK3 are located in the center of the bottom edge. GCLK4 through GCLK7 are located in the center of the top edge.

Eight Global Clock Multiplexers (also called BUFGMUX elements) are provided that accept signals from Global Clock inputs and route them to the internal clock network as well as DCMs. Four BUFGMUX elements are located in the center of the bottom edge, just above the GCLK0 - GCLK3 inputs. The remaining four BUFGMUX elements are located in the center of the top edge, just below the GCLK4 - GCLK7 inputs.

Pairs of BUFGMUX elements share global inputs, as shown in [Figure 24](#). For example, the GCLK4 and GCLK5 inputs both potentially connect to BUFGMUX4 and BUFGMUX5 located in the upper right center. A differential clock input uses a pair of GCLK inputs to connect to a single BUFGMUX element.

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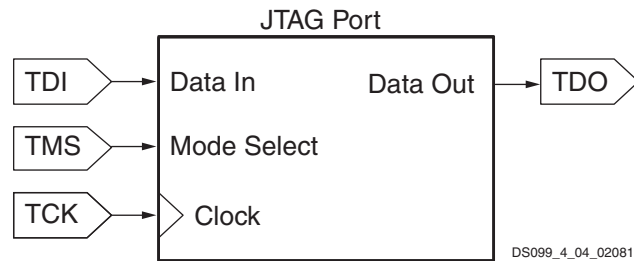


Figure 43: JTAG Port

IDCODE Register

Spartan-3 FPGAs contain a 32-bit identification register called the IDCODE register, as defined in the IEEE 1149.1 JTAG standard. The fixed value electrically identifies the manufacture (Xilinx) and the type of device being addressed over a JTAG chain. This register allows the JTAG host to identify the device being tested or programmed via JTAG. See [Table 78](#).

Using JTAG Port After Configuration

The JTAG port is always active and available before, during, and after FPGA configuration. Add the BSCAN_SPARTAN3 primitive to the design to create user-defined JTAG instructions and JTAG chains to communicate with internal logic.

Furthermore, the contents of the User ID register within the JTAG port can be specified as a Bitstream Generation option. By default, the 32-bit User ID register contains 0xFFFFFFFF.

Table 78: Spartan-3 JTAG IDCODE Register Values (hexadecimal)

Part Number	IDCODE Register
XC3S50	0x0140C093
XC3S200	0x01414093
XC3S400	0x0141C093
XC3S1000	0x01428093
XC3S1500	0x01434093
XC3S2000	0x01440093
XC3S4000	0x01448093
XC3S5000	0x01450093

Precautions When Using the JTAG Port in 3.3V Environments

The JTAG port is powered by the +2.5V VCCAUX power supply. When connecting to a 3.3V interface, the JTAG input pins must be current-limited using a series resistor. Similarly, the TDO pin is a CMOS output powered from +2.5V. The TDO output can directly drive a 3.3V input but with reduced noise immunity. See [3.3V-Tolerant Configuration Interface, page 47](#). See also [XAPP453: The 3.3V Configuration of Spartan-3 FPGAs](#) for additional details.

The following interface precautions are recommended when connecting the JTAG port to a 3.3V interface.

- Avoid actively driving the JTAG input signals High with 3.3V signal levels. If required in the application, use series current-limiting resistors to keep the current below 10 mA per pin.
- If possible, drive the FPGA JTAG inputs with drivers that can be placed in high-impedance (Hi-Z) after using the JTAG port. Alternatively, drive the FPGA JTAG inputs with open-drain outputs, which only drive Low. In both cases, pull-up resistors are required. The FPGA JTAG pins have pull-up resistors to VCCAUX before configuration and optional pull-up resistors after configuration, controlled by [Bitstream Options, page 125](#).

PQ208: 208-lead Plastic Quad Flat Pack

The 208-lead plastic quad flat package, PQ208, supports three different Spartan-3 devices, including the XC3S50, the XC3S200, and the XC3S400. The footprints for the XC3S200 and XC3S400 are identical, as shown in [Table 93](#) and [Figure 47](#). The XC3S50, however, has fewer I/O pins resulting in 17 unconnected pins on the PQ208 package, labeled as “N.C.” In [Table 93](#) and [Figure 47](#), these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in [Table 93](#) and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S50 pinout and the pinout for the XC3S200 and XC3S400, then that difference is highlighted in [Table 93](#). If the table entry is shaded grey, then there is an unconnected pin on the XC3S50 that maps to a user-I/O pin on the XC3S200 and XC3S400. If the table entry is shaded tan, then the unconnected pin on the XC3S50 maps to a VREF-type pin on the XC3S200 and XC3S400. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S50 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S50 device to an XC3S200 or XC3S400 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_sheets/s3_pin.zip

Pinout Table

Table 93: PQ208 Package Pinout

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
0	IO	IO	P189	I/O
0	IO	IO	P197	I/O
0	N.C. (◆)	IO/VREF_0	P200	VREF
0	IO/VREF_0	IO/VREF_0	P205	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	P204	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	P203	DCI
0	IO_L25N_0	IO_L25N_0	P199	I/O
0	IO_L25P_0	IO_L25P_0	P198	I/O
0	IO_L27N_0	IO_L27N_0	P196	I/O
0	IO_L27P_0	IO_L27P_0	P194	I/O
0	IO_L30N_0	IO_L30N_0	P191	I/O
0	IO_L30P_0	IO_L30P_0	P190	I/O
0	IO_L31N_0	IO_L31N_0	P187	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	P185	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	P184	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	P183	GCLK
0	VCCO_0	VCCO_0	P188	VCCO
0	VCCO_0	VCCO_0	P201	VCCO
1	IO	IO	P167	I/O
1	IO	IO	P175	I/O
1	IO	IO	P182	I/O
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	P162	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	P161	DCI

Table 96: FT256 Package Pinout (Cont'd)

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
7	IO_L24P_7	G4	I/O
7	IO_L39N_7	H3	I/O
7	IO_L39P_7	H4	I/O
7	IO_L40N_7/VREF_7	H1	VREF
7	IO_L40P_7	G1	I/O
7	VCCO_7	G6	VCCO
7	VCCO_7	H5	VCCO
7	VCCO_7	H6	VCCO
N/A	GND	A1	GND
N/A	GND	A16	GND
N/A	GND	B2	GND
N/A	GND	B9	GND
N/A	GND	B15	GND
N/A	GND	F6	GND
N/A	GND	F11	GND
N/A	GND	G7	GND
N/A	GND	G8	GND
N/A	GND	G9	GND
N/A	GND	G10	GND
N/A	GND	H2	GND
N/A	GND	H7	GND
N/A	GND	H8	GND
N/A	GND	H9	GND
N/A	GND	H10	GND
N/A	GND	J7	GND
N/A	GND	J8	GND
N/A	GND	J9	GND
N/A	GND	J10	GND
N/A	GND	J15	GND
N/A	GND	K7	GND
N/A	GND	K8	GND
N/A	GND	K9	GND
N/A	GND	K10	GND
N/A	GND	L6	GND
N/A	GND	L11	GND
N/A	GND	R2	GND
N/A	GND	R8	GND
N/A	GND	R15	GND
N/A	GND	T1	GND

Table 98: FG320 Package Pinout (Cont'd)

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
4	IO_L31P_4/ DOUT/BUSY	V10	DUAL
4	IO_L32N_4/GCLK1	N10	GCLK
4	IO_L32P_4/GCLK0	P10	GCLK
4	VCCO_4	M10	VCCO
4	VCCO_4	M11	VCCO
4	VCCO_4	T13	VCCO
4	VCCO_4	U11	VCCO
5	IO	N8	I/O
5	IO	P8	I/O
5	IO	U6	I/O
5	IO/VREF_5	R9	VREF
5	IO_L01N_5/RDWR_B	V3	DUAL
5	IO_L01P_5/CS_B	V2	DUAL
5	IO_L06N_5	T5	I/O
5	IO_L06P_5	T4	I/O
5	IO_L10N_5/VRP_5	V4	DCI
5	IO_L10P_5/VRN_5	U4	DCI
5	IO_L15N_5	R6	I/O
5	IO_L15P_5	R5	I/O
5	IO_L16N_5	V5	I/O
5	IO_L16P_5	U5	I/O
5	IO_L27N_5/VREF_5	P6	VREF
5	IO_L27P_5	P7	I/O
5	IO_L28N_5/D6	R7	DUAL
5	IO_L28P_5/D7	T7	DUAL
5	IO_L29N_5	V8	I/O
5	IO_L29P_5/VREF_5	V7	VREF
5	IO_L30N_5	R8	I/O
5	IO_L30P_5	T8	I/O
5	IO_L31N_5/D4	U9	DUAL
5	IO_L31P_5/D5	V9	DUAL
5	IO_L32N_5/GCLK3	N9	GCLK
5	IO_L32P_5/GCLK2	P9	GCLK
5	VCCO_5	M8	VCCO
5	VCCO_5	M9	VCCO
5	VCCO_5	T6	VCCO
5	VCCO_5	U8	VCCO
6	IO	K6	I/O
6	IO_L01N_6/VRP_6	T3	DCI

Table 100: FG456 Package Pinout (Cont'd)

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	W9	VREF
5	IO_L27P_5	IO_L27P_5	V9	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	AB9	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	AA9	DUAL
5	IO_L29N_5	IO_L29N_5	Y10	I/O
5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	W10	VREF
5	IO_L30N_5	IO_L30N_5	AB10	I/O
5	IO_L30P_5	IO_L30P_5	AA10	I/O
5	IO_L31N_5/D4	IO_L31N_5/D4	W11	DUAL
5	IO_L31P_5/D5	IO_L31P_5/D5	V11	DUAL
5	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	AA11	GCLK
5	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	Y11	GCLK
5	VCCO_5	VCCO_5	T9	VCCO
5	VCCO_5	VCCO_5	T10	VCCO
5	VCCO_5	VCCO_5	T11	VCCO
5	VCCO_5	VCCO_5	U8	VCCO
5	VCCO_5	VCCO_5	Y8	VCCO
6	IO	IO	Y1	I/O
6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	Y3	DCI
6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	Y2	DCI
6	IO_L16N_6	IO_L16N_6	W4	I/O
6	IO_L16P_6	IO_L16P_6	W3	I/O
6	IO_L17N_6	IO_L17N_6	W2	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	W1	VREF
6	IO_L19N_6	IO_L19N_6	V5	I/O
6	IO_L19P_6	IO_L19P_6	U5	I/O
6	IO_L20N_6	IO_L20N_6	V4	I/O
6	IO_L20P_6	IO_L20P_6	V3	I/O
6	IO_L21N_6	IO_L21N_6	V2	I/O
6	IO_L21P_6	IO_L21P_6	V1	I/O
6	IO_L22N_6	IO_L22N_6	T6	I/O
6	IO_L22P_6	IO_L22P_6	T5	I/O
6	IO_L23N_6	IO_L23N_6	U4	I/O
6	IO_L23P_6	IO_L23P_6	T4	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	U3	VREF
6	IO_L24P_6	IO_L24P_6	U2	I/O
6	N.C. (◆)	IO_L26N_6	T3	I/O
6	N.C. (◆)	IO_L26P_6	R4	I/O
6	IO_L27N_6	IO_L27N_6	T2	I/O
6	IO_L27P_6	IO_L27P_6	T1	I/O

Table 103: FG676 Package Pinout (Cont'd)

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	H9	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	H10	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	J11	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	J12	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	J13	VCCO
0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	VCCO_0	K13	VCCO
1	IO	IO	IO	IO	IO	A14	I/O
1	IO	IO	IO	IO	IO	A22	I/O
1	IO	IO	IO	IO	IO	A23	I/O
1	IO	IO	IO	IO	IO	D16	I/O
1	IO	IO	IO	IO	IO_L17P_1 ⁽³⁾	E18	I/O
1	IO	IO	IO	IO	IO	F14	I/O
1	IO	IO	IO	IO	IO	F20	I/O
1	IO	IO	IO	IO	IO	G19	I/O
1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	C15	VREF
1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO/VREF_1	C17	VREF
1	N.C. (◆)	IO/VREF_1	IO/VREF_1	IO/VREF_1	IO_L17N_1/VREF_1 ⁽³⁾	D18	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	D22	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	E22	DCI
1	IO_L04N_1	IO_L04N_1	IO_L04N_1	IO_L04N_1	IO_L04N_1	B23	I/O
1	IO_L04P_1	IO_L04P_1	IO_L04P_1	IO_L04P_1	IO_L04P_1	C23	I/O
1	IO_L05N_1	IO_L05N_1	IO_L05N_1	IO_L05N_1	IO_L05N_1	E21	I/O
1	IO_L05P_1	IO_L05P_1	IO_L05P_1	IO_L05P_1	IO_L05P_1	F21	I/O
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	B22	VREF
1	IO_L06P_1	IO_L06P_1	IO_L06P_1	IO_L06P_1	IO_L06P_1	C22	I/O
1	IO_L07N_1	IO_L07N_1	IO_L07N_1	IO_L07N_1	IO_L07N_1	C21	I/O
1	IO_L07P_1	IO_L07P_1	IO_L07P_1	IO_L07P_1	IO_L07P_1	D21	I/O
1	IO_L08N_1	IO_L08N_1	IO_L08N_1	IO_L08N_1	IO_L08N_1	A21	I/O
1	IO_L08P_1	IO_L08P_1	IO_L08P_1	IO_L08P_1	IO_L08P_1	B21	I/O
1	IO_L09N_1	IO_L09N_1	IO_L09N_1	IO_L09N_1	IO_L09N_1	D20	I/O
1	IO_L09P_1	IO_L09P_1	IO_L09P_1	IO_L09P_1	IO_L09P_1	E20	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	A20	VREF
1	IO_L10P_1	IO_L10P_1	IO_L10P_1	IO_L10P_1	IO_L10P_1	B20	I/O
1	N.C. (◆)	IO_L11N_1	IO_L11N_1	IO_L11N_1	IO_L11N_1	E19	I/O
1	N.C. (◆)	IO_L11P_1	IO_L11P_1	IO_L11P_1	IO_L11P_1	F19	I/O
1	N.C. (◆)	IO_L12N_1	IO_L12N_1	IO_L12N_1	IO_L12N_1	C19	I/O
1	N.C. (◆)	IO_L12P_1	IO_L12P_1	IO_L12P_1	IO_L12P_1	D19	I/O
1	IO_L15N_1	IO_L15N_1	IO_L15N_1	IO_L15N_1	IO_L15N_1	A19	I/O
1	IO_L15P_1	IO_L15P_1	IO_L15P_1	IO_L15P_1	IO_L15P_1	B19	I/O
1	IO_L16N_1	IO_L16N_1	IO_L16N_1	IO_L16N_1	IO_L16N_1	F18	I/O
1	IO_L16P_1	IO_L16P_1	IO_L16P_1	IO_L16P_1	IO_L16P_1	G18	I/O
1	N.C. (◆)	IO_L18N_1	IO_L18N_1	IO_L18N_1	IO ⁽³⁾	B18	I/O

Table 103: FG676 Package Pinout (Cont'd)

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
2	N.C. (◆)	IO_L06N_2	IO_L06N_2	IO_L06N_2	IO_L06N_2	G20	I/O
2	N.C. (◆)	IO_L06P_2	IO_L06P_2	IO_L06P_2	IO_L06P_2	G21	I/O
2	N.C. (◆)	IO_L07N_2	IO_L07N_2	IO_L07N_2	IO_L07N_2	F23	I/O
2	N.C. (◆)	IO_L07P_2	IO_L07P_2	IO_L07P_2	IO_L07P_2	F24	I/O
2	N.C. (◆)	IO_L08N_2	IO_L08N_2	IO_L08N_2	IO_L08N_2	G22	I/O
2	N.C. (◆)	IO_L08P_2	IO_L08P_2	IO_L08P_2	IO_L08P_2	G23	I/O
2	N.C. (◆)	IO_L09N_2/VREF_2 ⁽¹⁾	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	F25	VREF ⁽¹⁾
2	N.C. (◆)	IO_L09P_2	IO_L09P_2	IO_L09P_2	IO_L09P_2	F26	I/O
2	N.C. (◆)	IO_L10N_2	IO_L10N_2	IO_L10N_2	IO_L10N_2	G25	I/O
2	N.C. (◆)	IO_L10P_2	IO_L10P_2	IO_L10P_2	IO_L10P_2	G26	I/O
2	IO_L14N_2	IO_L14N_2	IO_L14N_2 ⁽²⁾	IO_L11N_2 ⁽²⁾	IO_L11N_2	H20	I/O
2	IO_L14P_2	IO_L14P_2	IO_L14P_2 ⁽²⁾	IO_L11P_2 ⁽²⁾	IO_L11P_2	H21	I/O
2	IO_L16N_2	IO_L16N_2	IO_L16N_2 ⁽²⁾	IO_L12N_2 ⁽²⁾	IO_L12N_2	H22	I/O
2	IO_L16P_2	IO_L16P_2	IO_L16P_2 ⁽²⁾	IO_L12P_2 ⁽²⁾	IO_L12P_2	J21	I/O
2	IO_L17N_2	IO_L17N_2	IO_L17N_2 ⁽²⁾	IO_L13N_2 ⁽²⁾	IO ⁽³⁾	H23	I/O
2	IO_L17P_2/VREF_2	IO_L17P_2/VREF_2	IO_L17P_2 ⁽²⁾ /VREF_2	IO_L13P_2 ⁽²⁾ /VREF_2	IO/VREF_2 ⁽³⁾	H24	VREF
2	IO_L19N_2	IO_L19N_2	IO_L19N_2	IO_L19N_2	IO_L19N_2	H25	I/O
2	IO_L19P_2	IO_L19P_2	IO_L19P_2	IO_L19P_2	IO_L19P_2	H26	I/O
2	IO_L20N_2	IO_L20N_2	IO_L20N_2	IO_L20N_2	IO_L20N_2	J20	I/O
2	IO_L20P_2	IO_L20P_2	IO_L20P_2	IO_L20P_2	IO_L20P_2	K20	I/O
2	IO_L21N_2	IO_L21N_2	IO_L21N_2	IO_L21N_2	IO_L21N_2	J22	I/O
2	IO_L21P_2	IO_L21P_2	IO_L21P_2	IO_L21P_2	IO_L21P_2	J23	I/O
2	IO_L22N_2	IO_L22N_2	IO_L22N_2	IO_L22N_2	IO_L22N_2	J24	I/O
2	IO_L22P_2	IO_L22P_2	IO_L22P_2	IO_L22P_2	IO_L22P_2	J25	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	K21	VREF
2	IO_L23P_2	IO_L23P_2	IO_L23P_2	IO_L23P_2	IO_L23P_2	K22	I/O
2	IO_L24N_2	IO_L24N_2	IO_L24N_2	IO_L24N_2	IO_L24N_2	K23	I/O
2	IO_L24P_2	IO_L24P_2	IO_L24P_2	IO_L24P_2	IO_L24P_2	K24	I/O
2	IO_L26N_2	IO_L26N_2	IO_L26N_2	IO_L26N_2	IO_L26N_2	K25	I/O
2	IO_L26P_2	IO_L26P_2	IO_L26P_2	IO_L26P_2	IO_L26P_2	K26	I/O
2	IO_L27N_2	IO_L27N_2	IO_L27N_2	IO_L27N_2	IO_L27N_2	L19	I/O
2	IO_L27P_2	IO_L27P_2	IO_L27P_2	IO_L27P_2	IO_L27P_2	L20	I/O
2	IO_L28N_2	IO_L28N_2	IO_L28N_2	IO_L28N_2	IO_L28N_2	L21	I/O
2	IO_L28P_2	IO_L28P_2	IO_L28P_2	IO_L28P_2	IO_L28P_2	L22	I/O
2	IO_L29N_2	IO_L29N_2	IO_L29N_2	IO_L29N_2	IO_L29N_2	L25	I/O
2	IO_L29P_2	IO_L29P_2	IO_L29P_2	IO_L29P_2	IO_L29P_2	L26	I/O
2	IO_L31N_2	IO_L31N_2	IO_L31N_2	IO_L31N_2	IO_L31N_2	M19	I/O
2	IO_L31P_2	IO_L31P_2	IO_L31P_2	IO_L31P_2	IO_L31P_2	M20	I/O
2	IO_L32N_2	IO_L32N_2	IO_L32N_2	IO_L32N_2	IO_L32N_2	M21	I/O
2	IO_L32P_2	IO_L32P_2	IO_L32P_2	IO_L32P_2	IO_L32P_2	M22	I/O
2	IO_L33N_2	IO_L33N_2	IO_L33N_2	IO_L33N_2	IO_L33N_2	L23	I/O
2	IO_L33P_2	IO_L33P_2	IO_L33P_2	IO_L33P_2	IO_L33P_2	M24	I/O

Table 103: FG676 Package Pinout (Cont'd)

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
3	IO_L19N_3	IO_L19N_3	IO_L19N_3	IO_L19N_3	IO_L19N_3	W26	I/O
3	IO_L19P_3	IO_L19P_3	IO_L19P_3	IO_L19P_3	IO_L19P_3	W25	I/O
3	IO_L20N_3	IO_L20N_3	IO_L20N_3	IO_L20N_3	IO_L20N_3	U20	I/O
3	IO_L20P_3	IO_L20P_3	IO_L20P_3	IO_L20P_3	IO_L20P_3	V20	I/O
3	IO_L21N_3	IO_L21N_3	IO_L21N_3	IO_L21N_3	IO_L21N_3	V23	I/O
3	IO_L21P_3	IO_L21P_3	IO_L21P_3	IO_L21P_3	IO_L21P_3	V22	I/O
3	IO_L22N_3	IO_L22N_3	IO_L22N_3	IO_L22N_3	IO_L22N_3	V25	I/O
3	IO_L22P_3	IO_L22P_3	IO_L22P_3	IO_L22P_3	IO_L22P_3	V24	I/O
3	IO_L23N_3	IO_L23N_3	IO_L23N_3	IO_L23N_3	IO_L23N_3	U22	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	U21	VREF
3	IO_L24N_3	IO_L24N_3	IO_L24N_3	IO_L24N_3	IO_L24N_3	U24	I/O
3	IO_L24P_3	IO_L24P_3	IO_L24P_3	IO_L24P_3	IO_L24P_3	U23	I/O
3	IO_L26N_3	IO_L26N_3	IO_L26N_3	IO_L26N_3	IO_L26N_3	U26	I/O
3	IO_L26P_3	IO_L26P_3	IO_L26P_3	IO_L26P_3	IO_L26P_3	U25	I/O
3	IO_L27N_3	IO_L27N_3	IO_L27N_3	IO_L27N_3	IO_L27N_3	T20	I/O
3	IO_L27P_3	IO_L27P_3	IO_L27P_3	IO_L27P_3	IO_L27P_3	T19	I/O
3	IO_L28N_3	IO_L28N_3	IO_L28N_3	IO_L28N_3	IO_L28N_3	T22	I/O
3	IO_L28P_3	IO_L28P_3	IO_L28P_3	IO_L28P_3	IO_L28P_3	T21	I/O
3	IO_L29N_3	IO_L29N_3	IO_L29N_3	IO_L29N_3	IO_L29N_3	T26	I/O
3	IO_L29P_3	IO_L29P_3	IO_L29P_3	IO_L29P_3	IO_L29P_3	T25	I/O
3	IO_L31N_3	IO_L31N_3	IO_L31N_3	IO_L31N_3	IO_L31N_3	R20	I/O
3	IO_L31P_3	IO_L31P_3	IO_L31P_3	IO_L31P_3	IO_L31P_3	R19	I/O
3	IO_L32N_3	IO_L32N_3	IO_L32N_3	IO_L32N_3	IO_L32N_3	R22	I/O
3	IO_L32P_3	IO_L32P_3	IO_L32P_3	IO_L32P_3	IO_L32P_3	R21	I/O
3	IO_L33N_3	IO_L33N_3	IO_L33N_3	IO_L33N_3	IO_L33N_3	R24	I/O
3	IO_L33P_3	IO_L33P_3	IO_L33P_3	IO_L33P_3	IO_L33P_3	T23	I/O
3	IO_L34N_3	IO_L34N_3	IO_L34N_3	IO_L34N_3	IO_L34N_3	R26	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	R25	VREF
3	IO_L35N_3	IO_L35N_3	IO_L35N_3	IO_L35N_3	IO_L35N_3	P20	I/O
3	IO_L35P_3	IO_L35P_3	IO_L35P_3	IO_L35P_3	IO_L35P_3	P19	I/O
3	IO_L38N_3	IO_L38N_3	IO_L38N_3	IO_L38N_3	IO_L38N_3	P22	I/O
3	IO_L38P_3	IO_L38P_3	IO_L38P_3	IO_L38P_3	IO_L38P_3	P21	I/O
3	IO_L39N_3	IO_L39N_3	IO_L39N_3	IO_L39N_3	IO_L39N_3	P24	I/O
3	IO_L39P_3	IO_L39P_3	IO_L39P_3	IO_L39P_3	IO_L39P_3	P23	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	P26	VREF
3	IO_L40P_3	IO_L40P_3	IO_L40P_3	IO_L40P_3	IO_L40P_3	P25	I/O
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	P17	VCCO
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	P18	VCCO
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	R18	VCCO
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	T18	VCCO
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	T24	VCCO
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	U19	VCCO
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	V19	VCCO

Table 103: FG676 Package Pinout (Cont'd)

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	IO_L29P_5/VREF_5	AE12	VREF
5	IO_L30N_5	IO_L30N_5	IO_L30N_5	IO_L30N_5	IO_L30N_5	Y13	I/O
5	IO_L30P_5	IO_L30P_5	IO_L30P_5	IO_L30P_5	IO_L30P_5	W13	I/O
5	IO_L31N_5/D4	IO_L31N_5/D4	IO_L31N_5/D4	IO_L31N_5/D4	IO_L31N_5/D4	AC13	DUAL
5	IO_L31P_5/D5	IO_L31P_5/D5	IO_L31P_5/D5	IO_L31P_5/D5	IO_L31P_5/D5	AB13	DUAL
5	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	IO_L32N_5/GCLK3	AE13	GCLK
5	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	IO_L32P_5/GCLK2	AD13	GCLK
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	AD7	VCCO
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	AD11	VCCO
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	U13	VCCO
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	V11	VCCO
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	V12	VCCO
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	V13	VCCO
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	W9	VCCO
5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	VCCO_5	W10	VCCO
6	N.C. (◆)	N.C. (■)	IO	IO	IO	AA5	I/O
6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	IO_L01N_6/VRP_6	AD2	DCI
6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	IO_L01P_6/VRN_6	AD1	DCI
6	IO_L02N_6	IO_L02N_6	IO_L02N_6	IO_L02N_6	IO_L02N_6	AB4	I/O
6	IO_L02P_6	IO_L02P_6	IO_L02P_6	IO_L02P_6	IO_L02P_6	AB3	I/O
6	IO_L03N_6/VREF_6	IO_L03N_6/VREF_6	IO_L03N_6/VREF_6	IO_L03N_6/VREF_6	IO_L03N_6/VREF_6	AC2	VREF
6	IO_L03P_6	IO_L03P_6	IO_L03P_6	IO_L03P_6	IO_L03P_6	AC1	I/O
6	N.C. (◆)	IO_L05N_6	IO_L05N_6	IO_L05N_6	IO_L05N_6	AB2	I/O
6	N.C. (◆)	IO_L05P_6	IO_L05P_6	IO_L05P_6	IO_L05P_6	AB1	I/O
6	N.C. (◆)	IO_L06N_6	IO_L06N_6	IO_L06N_6	IO_L06N_6	Y7	I/O
6	N.C. (◆)	IO_L06P_6	IO_L06P_6	IO_L06P_6	IO_L06P_6	Y6	I/O
6	N.C. (◆)	IO_L07N_6	IO_L07N_6	IO_L07N_6	IO_L07N_6	AA4	I/O
6	N.C. (◆)	IO_L07P_6	IO_L07P_6	IO_L07P_6	IO_L07P_6	AA3	I/O
6	N.C. (◆)	IO_L08N_6	IO_L08N_6	IO_L08N_6	IO_L08N_6	Y5	I/O
6	N.C. (◆)	IO_L08P_6	IO_L08P_6	IO_L08P_6	IO_L08P_6	Y4	I/O
6	N.C. (◆)	IO_L09N_6/VREF_6	IO_L09N_6/VREF_6	IO_L09N_6/VREF_6	IO_L09N_6/VREF_6	AA2	VREF
6	N.C. (◆)	IO_L09P_6	IO_L09P_6	IO_L09P_6	IO_L09P_6	AA1	I/O
6	N.C. (◆)	IO_L10N_6	IO_L10N_6	IO_L10N_6	IO_L10N_6	Y2	I/O
6	N.C. (◆)	IO_L10P_6	IO_L10P_6	IO_L10P_6	IO_L10P_6	Y1	I/O
6	IO_L14N_6	IO_L14N_6	IO_L14N_6	IO_L14N_6	IO_L14N_6	W7	I/O
6	IO_L14P_6	IO_L14P_6	IO_L14P_6	IO_L14P_6	IO_L14P_6	W6	I/O
6	IO_L16N_6	IO_L16N_6	IO_L16N_6	IO_L16N_6	IO_L16N_6	V6	I/O
6	IO_L16P_6	IO_L16P_6	IO_L16P_6	IO_L16P_6	IO_L16P_6	W5	I/O
6	IO_L17N_6	IO_L17N_6	IO_L17N_6	IO_L17N_6	IO_L17N_6	W4	I/O
6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	IO_L17P_6/VREF_6	W3	VREF
6	IO_L19N_6	IO_L19N_6	IO_L19N_6	IO_L19N_6	IO_L19N_6	W2	I/O
6	IO_L19P_6	IO_L19P_6	IO_L19P_6	IO_L19P_6	IO_L19P_6	W1	I/O

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO_L30N_0	IO_L30N_0	G15	I/O
0	IO_L30P_0	IO_L30P_0	F15	I/O
0	IO_L31N_0	IO_L31N_0	D15	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C15	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B15	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A15	GCLK
0	N.C. (◆)	IO_L35N_0	B7	I/O
0	N.C. (◆)	IO_L35P_0	A7	I/O
0	N.C. (◆)	IO_L36N_0	G7	I/O
0	N.C. (◆)	IO_L36P_0	H8	I/O
0	N.C. (◆)	IO_L37N_0	E9	I/O
0	N.C. (◆)	IO_L37P_0	D9	I/O
0	N.C. (◆)	IO_L38N_0	B9	I/O
0	N.C. (◆)	IO_L38P_0	A9	I/O
0	VCCO_0	VCCO_0	C5	VCCO
0	VCCO_0	VCCO_0	E7	VCCO
0	VCCO_0	VCCO_0	C9	VCCO
0	VCCO_0	VCCO_0	G9	VCCO
0	VCCO_0	VCCO_0	J11	VCCO
0	VCCO_0	VCCO_0	L12	VCCO
0	VCCO_0	VCCO_0	C13	VCCO
0	VCCO_0	VCCO_0	G13	VCCO
0	VCCO_0	VCCO_0	L13	VCCO
0	VCCO_0	VCCO_0	L14	VCCO
1	IO	IO	E25	I/O
1	IO	IO	J21	I/O
1	IO	IO	K20	I/O
1	IO	IO	F18	I/O
1	IO	IO	F16	I/O
1	IO	IO	A16	I/O
1	IO/VREF_1	IO/VREF_1	J17	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	A27	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B27	DCI
1	IO_L02N_1	IO_L02N_1	D26	I/O
1	IO_L02P_1	IO_L02P_1	C27	I/O
1	IO_L03N_1	IO_L03N_1	A26	I/O
1	IO_L03P_1	IO_L03P_1	B26	I/O
1	IO_L04N_1	IO_L04N_1	B25	I/O
1	IO_L04P_1	IO_L04P_1	C25	I/O
1	IO_L05N_1	IO_L05N_1	F24	I/O

**Right Half of FG900
Package (Top View)**

Figure 56: FG900 Package Footprint (Top View) Continued

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
2	IO_L19N_2	IO_L19N_2	M29	I/O
2	IO_L19P_2	IO_L19P_2	M30	I/O
2	IO_L20N_2	IO_L20N_2	M31	I/O
2	IO_L20P_2	IO_L20P_2	M32	I/O
2	IO_L21N_2	IO_L21N_2	M26	I/O
2	IO_L21P_2	IO_L21P_2	N25	I/O
2	IO_L22N_2	IO_L22N_2	N27	I/O
2	IO_L22P_2	IO_L22P_2	N28	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	N31	VREF
2	IO_L23P_2	IO_L23P_2	N32	I/O
2	IO_L24N_2	IO_L24N_2	N24	I/O
2	IO_L24P_2	IO_L24P_2	P24	I/O
2	IO_L26N_2	IO_L26N_2	P29	I/O
2	IO_L26P_2	IO_L26P_2	P30	I/O
2	IO_L27N_2	IO_L27N_2	P31	I/O
2	IO_L27P_2	IO_L27P_2	P32	I/O
2	IO_L28N_2	IO_L28N_2	P33	I/O
2	IO_L28P_2	IO_L28P_2	P34	I/O
2	IO_L29N_2	IO_L29N_2	R24	I/O
2	IO_L29P_2	IO_L29P_2	R25	I/O
2	IO_L30N_2	IO_L30N_2	R28	I/O
2	IO_L30P_2	IO_L30P_2	R29	I/O
2	IO_L31N_2	IO_L31N_2	R31	I/O
2	IO_L31P_2	IO_L31P_2	R32	I/O
2	IO_L32N_2	IO_L32N_2	R33	I/O
2	IO_L32P_2	IO_L32P_2	R34	I/O
2	IO_L33N_2	IO_L33N_2	R26	I/O
2	IO_L33P_2	IO_L33P_2	T25	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	T28	VREF
2	IO_L34P_2	IO_L34P_2	T29	I/O
2	IO_L35N_2	IO_L35N_2	T32	I/O
2	IO_L35P_2	IO_L35P_2	T33	I/O
2	IO_L37N_2	IO_L37N_2	U27	I/O
2	IO_L37P_2	IO_L37P_2	U28	I/O
2	IO_L38N_2	IO_L38N_2	U29	I/O
2	IO_L38P_2	IO_L38P_2	U30	I/O
2	IO_L39N_2	IO_L39N_2	U31	I/O
2	IO_L39P_2	IO_L39P_2	U32	I/O
2	IO_L40N_2	IO_L40N_2	U33	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	U34	VREF

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	GND	GND	Y14	GND
N/A	GND	GND	Y15	GND
N/A	GND	GND	Y16	GND
N/A	GND	GND	Y17	GND
N/A	GND	GND	Y18	GND
N/A	GND	GND	Y19	GND
N/A	GND	GND	Y20	GND
N/A	GND	GND	Y21	GND
N/A	N.C. (◆)	N.C. (■)	AK31	N.C.
N/A	VCCAUX	VCCAUX	AD30	VCCAUX
N/A	VCCAUX	VCCAUX	AD5	VCCAUX
N/A	VCCAUX	VCCAUX	AG16	VCCAUX
N/A	VCCAUX	VCCAUX	AG19	VCCAUX
N/A	VCCAUX	VCCAUX	AJ30	VCCAUX
N/A	VCCAUX	VCCAUX	AJ5	VCCAUX
N/A	VCCAUX	VCCAUX	AK11	VCCAUX
N/A	VCCAUX	VCCAUX	AK15	VCCAUX
N/A	VCCAUX	VCCAUX	AK20	VCCAUX
N/A	VCCAUX	VCCAUX	AK24	VCCAUX
N/A	VCCAUX	VCCAUX	AK29	VCCAUX
N/A	VCCAUX	VCCAUX	AK6	VCCAUX
N/A	VCCAUX	VCCAUX	E11	VCCAUX
N/A	VCCAUX	VCCAUX	E15	VCCAUX
N/A	VCCAUX	VCCAUX	E20	VCCAUX
N/A	VCCAUX	VCCAUX	E24	VCCAUX
N/A	VCCAUX	VCCAUX	E29	VCCAUX
N/A	VCCAUX	VCCAUX	E6	VCCAUX
N/A	VCCAUX	VCCAUX	F30	VCCAUX
N/A	VCCAUX	VCCAUX	F5	VCCAUX
N/A	VCCAUX	VCCAUX	H16	VCCAUX
N/A	VCCAUX	VCCAUX	H19	VCCAUX
N/A	VCCAUX	VCCAUX	L30	VCCAUX
N/A	VCCAUX	VCCAUX	L5	VCCAUX
N/A	VCCAUX	VCCAUX	R30	VCCAUX
N/A	VCCAUX	VCCAUX	R5	VCCAUX
N/A	VCCAUX	VCCAUX	T27	VCCAUX
N/A	VCCAUX	VCCAUX	T8	VCCAUX
N/A	VCCAUX	VCCAUX	W27	VCCAUX
N/A	VCCAUX	VCCAUX	W8	VCCAUX
N/A	VCCAUX	VCCAUX	Y30	VCCAUX

User I/Os by Bank

Note: The FG(G)1156 package is discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Table 111 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S4000 in the FG1156 package. Similarly, Table 112 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S5000 in the FG1156 package.

Table 111: User I/Os Per Bank for XC3S4000 in FG1156 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	90	79	0	2	7	2
	1	90	79	0	2	7	2
Right	2	88	80	0	2	6	0
	3	88	79	0	2	7	0
Bottom	4	90	73	6	2	7	2
	5	90	73	6	2	7	2
Left	6	88	79	0	2	7	0
	7	88	79	0	2	7	0

Notes:

- The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

Table 112: User I/Os Per Bank for XC3S5000 in FG1156 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	100	89	0	2	7	2
	1	100	89	0	2	7	2
Right	2	96	87	0	2	7	0
	3	96	87	0	2	7	0
Bottom	4	100	83	6	2	7	2
	5	100	83	6	2	7	2
Left	6	96	87	0	2	7	0
	7	96	87	0	2	7	0

Notes:

- The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.