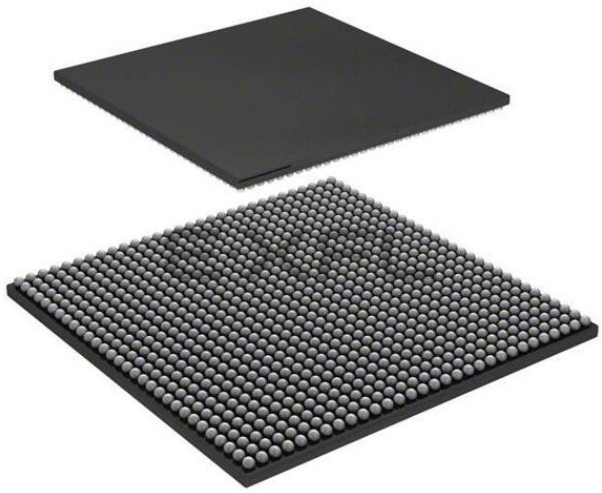
AMD Xilinx - XC3S2000-5FGG900C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	5120
Number of Logic Elements/Cells	46080
Total RAM Bits	737280
Number of I/O	565
Number of Gates	2000000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s2000-5fgg900c

Spartan-3 FPGA Family: Introduction and Ordering Information

DS099 (v3.0) October 29, 2012 **Product Specification**

Introduction

The Spartan®-3 family of Field-Programmable Gate Arrays is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The eight-member family offers densities ranging from 50,000 to 5,000,000 system gates, as shown in Table 1.

The Spartan-3 family builds on the success of the earlier Spartan-IIE family by increasing the amount of logic resources, the capacity of internal RAM, the total number of I/Os, and the overall level of performance as well as by improving clock management functions. Numerous enhancements derive from the Virtex®-II platform technology. These Spartan-3 FPGA enhancements, combined with advanced process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3 FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection and digital television equipment.

The Spartan-3 family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

Features

- Low-cost, high-performance logic solution for high-volume, consumer-oriented applications
  - Densities up to 74,880 logic cells
- SelectIO™ interface signaling
  - Up to 633 I/O pins
  - 622+ Mb/s data transfer rate per I/O
  - 18 single-ended signal standards
  - 8 differential I/O standards including LVDS, RSDS
  - Termination by Digitally Controlled Impedance
  - Signal swing ranging from 1.14V to 3.465V
  - Double Data Rate (DDR) support
  - DDR, DDR2 SDRAM support up to 333 Mb/s
- Logic resources
  - Abundant logic cells with shift register capability
  - Wide, fast multiplexers
  - Fast look-ahead carry logic
  - Dedicated 18 x 18 multipliers
  - JTAG logic compatible with IEEE 1149.1/1532
- SelectRAM™ hierarchical memory
  - Up to 1,872 Kbits of total block RAM
  - Up to 520 Kbits of total distributed RAM
- Digital Clock Manager (up to four DCMs)
  - Clock skew elimination
  - Frequency synthesis
  - High resolution phase shifting
- Eight global clock lines and abundant routing
- Fully supported by Xilinx ISE® and WebPACK™ software development systems
- MicroBlaze™ and PicoBlaze™ processor, PCI®, PCI Express® PIPE Endpoint, and other IP cores
- Pb-free packaging options
- Automotive Spartan-3 XA Family variant

Table 1: **Summary of Spartan-3 FPGA Attributes**

Device	System Gates	Equivalent Logic Cells[1]	CLB Array (One CLB = Four Slices)			Distributed RAM Bits (K=1024)	Block RAM Bits (K=1024)	Dedicated Multipliers	DCMs	Max. User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs						
XC3S50[2]	50K	1,728	16	12	192	12K	72K	4	2	124	56
XC3S200[2]	200K	4,320	24	20	480	30K	216K	12	4	173	76
XC3S400[2]	400K	8,064	32	28	896	56K	288K	16	4	264	116
XC3S1000[2]	1M	17,280	48	40	1,920	120K	432K	24	4	391	175
XC3S1500	1.5M	29,952	64	52	3,328	208K	576K	32	4	487	221
XC3S2000	2M	46,080	80	64	5,120	320K	720K	40	4	565	270
XC3S4000	4M	62,208	96	72	6,912	432K	1,728K	96	4	633	300
XC3S5000	5M	74,880	104	80	8,320	520K	1,872K	104	4	633	300

Notes:

1. Logic Cell = 4-input Look-Up Table (LUT) plus a 'D' flip-flop. "Equivalent Logic Cells" equals "Total CLBs" x 8 Logic Cells/CLB x 1.125 effectiveness.
2. These devices are available in Xilinx Automotive versions as described in DS314: *Spartan-3 Automotive XA FPGA Family.*

The DLL component has two clock inputs, CLKIN and CLKFB, as well as seven clock outputs, CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV as described in Table 16. The clock outputs drive simultaneously; however, the High Frequency mode only supports a subset of the outputs available in the Low Frequency mode. See DLL Frequency Modes, page 35. Signals that initialize and report the state of the DLL are discussed in The Status Logic Component, page 41.

Table 16: **DLL Signals**

Signal	Direction	Description	Mode Support	
			Low Frequency	High Frequency
CLKIN	Input	Accepts original clock signal.	Yes	Yes
CLKFB	Input	Accepts either CLK0 or CLK2X as feed back signal. (Set CLK_FEEDBACK attribute accordingly).	Yes	Yes
CLK0	Output	Generates clock signal with same frequency and phase as CLKIN.	Yes	Yes
CLK90	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 90°.	Yes	No
CLK180	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 180°.	Yes	Yes
CLK270	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 270°.	Yes	No
CLK2X	Output	Generates clock signal with same phase as CLKIN, only twice the frequency.	Yes	No
CLK2X180	Output	Generates clock signal with twice the frequency of CLKIN, phase-shifted 180° with respect to CLKIN.	Yes	No
CLKDV	Output	Divides the CLKIN frequency by CLKDV_DIVIDE value to generate lower frequency clock signal that is phase-aligned to CLKIN.	Yes	Yes

The clock signal supplied to the CLKIN input serves as a reference waveform, with which the DLL seeks to align the feedback signal at the CLKFB input. When eliminating clock skew, the common approach to using the DLL is as follows: The CLK0 signal is passed through the clock distribution network to all the registers it synchronizes. These registers are either internal or external to the FPGA. After passing through the clock distribution network, the clock signal returns to the DLL via a feedback line called CLKFB. The control block inside the DLL measures the phase error between CLKFB and CLKIN. This phase error is a measure of the clock skew that the clock distribution network introduces. The control block activates the appropriate number of delay elements to cancel out the clock skew. Once the DLL has brought the CLK0 signal in phase with the CLKIN signal, it asserts the LOCKED output, indicating a “lock” on to the CLKIN signal.

DLL Attributes and Related Functions

A number of different functional options can be set for the DLL component through the use of the attributes described in Table 17. Each attribute is described in detail in the sections that follow:

Table 17: **DLL Attributes**

Attribute	Description	Values
CLK_FEEDBACK	Chooses either the CLK0 or CLK2X output to drive the CLKFB input	NONE, 1X, 2X
DLL_FREQUENCY_MODE	Chooses between High Frequency and Low Frequency modes	LOW, HIGH
CLKIN_DIVIDE_BY_2	Halves the frequency of the CLKIN signal just as it enters the DCM	TRUE, FALSE
CLKDV_DIVIDE	Selects constant used to divide the CLKIN input frequency to generate the CLKDV output frequency	1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6.0, 6.5, 7.0, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.
DUTY_CYCLE_CORRECTION	Enables 50% duty cycle correction for the CLK0, CLK90, CLK180, and CLK270 outputs	TRUE, FALSE

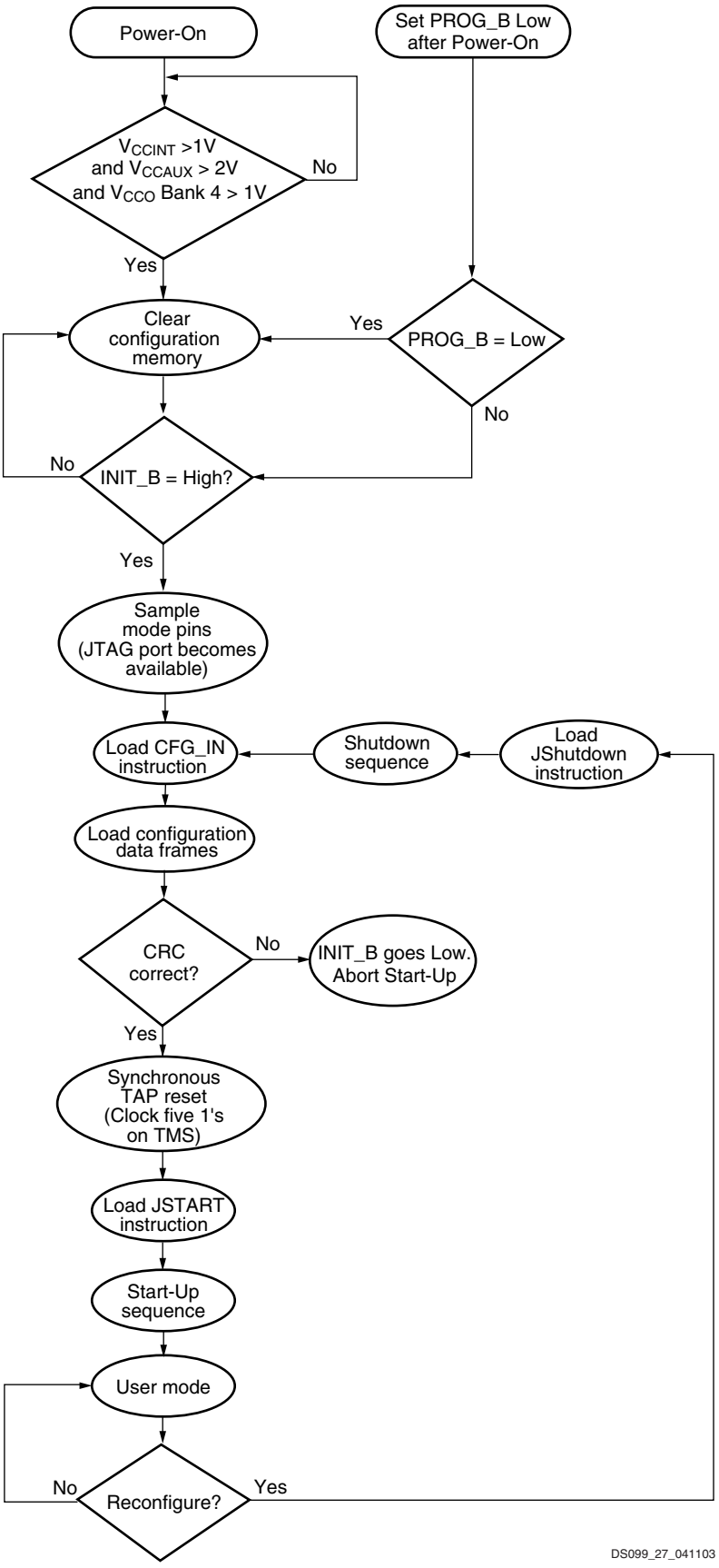

Figure 30: **Boundary-Scan Configuration Flow Diagram**

Table 33: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**

Symbol	Description	Test Conditions		Min	Typ	Max	Units
I_L (2)(4)	Leakage current at User I/O, Dual-Purpose, and Dedicated pins	Driver is Hi-Z, V_{IN} = 0V or V_{CCO} max, sample-tested	$V_{CCO} \geq 3.0V$	–	-	±25	µA
			$V_{CCO} < 3.0V$	–	-	±10	µA
I_{RPU} (3)	Current through pull-up resistor at User I/O, Dual-Purpose, and Dedicated pins	V_{IN} = 0V, V_{CCO} = 3.3V		–0.84	-	–2.35	mA
		V_{IN} = 0V, V_{CCO} = 3.0V		–0.69	-	–1.99	mA
		V_{IN} = 0V, V_{CCO} = 2.5V		–0.47	-	–1.41	mA
		V_{IN} = 0V, V_{CCO} = 1.8V		–0.21	-	–0.69	mA
		V_{IN} = 0V, V_{CCO} = 1.5V		–0.13	-	–0.43	mA
		V_{IN} = 0V, V_{CCO} = 1.2V		–0.06	-	–0.22	mA
R_{PU} (3)	Equivalent resistance of pull-up resistor at User I/O, Dual-Purpose, and Dedicated pins, derived from I_{RPU}	V_{CCO} = 3.0V to 3.465V		1.27	-	4.11	kΩ
		V_{CCO} = 2.3V to 2.7V		1.15	-	3.25	kΩ
		V_{CCO} = 1.7V to 1.9V		2.45	-	9.10	kΩ
		V_{CCO} = 1.4V to 1.6V		3.25	-	12.10	kΩ
		V_{CCO} = 1.14 to 1.26V		5.15	-	21.00	kΩ
I_{RPD} (3)	Current through pull-down resistor at User I/O, Dual-Purpose, and Dedicated pins	$V_{IN} = V_{CCO}$		0.37	-	1.67	mA
R_{PD} (3)	Equivalent resistance of pull-down resistor at User I/O, Dual-Purpose, and Dedicated pins, driven from I_{RPD}	$V_{IN} = V_{CCO}$ = 3.0V to 3.465V		1.75	-	9.35	kΩ
		$V_{IN} = V_{CCO}$ = 2.3V to 2.7V		1.35	-	7.30	kΩ
		$V_{IN} = V_{CCO}$ = 1.7V to 1.9V		1.00	-	5.15	kΩ
		$V_{IN} = V_{CCO}$ = 1.4V to 1.6V		0.85	-	4.35	kΩ
		$V_{IN} = V_{CCO}$ = 1.14 to 1.26V		0.68	-	3.465	kΩ
R_{DCI}	Value of external reference resistor to support DCI I/O standards			20	-	100	Ω
I_{REF}	V_{REF} current per pin	$V_{CCO} \geq 3.0V$		–	-	±25	µA
		$V_{CCO} < 3.0V$		–	-	±10	µA
C_{IN}	Input capacitance			3	-	10	pF

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32.
2. The I_L specification applies to every I/O pin throughout power-on as long as the voltage on that pin stays between the absolute V_{IN} minimum and maximum values (Table 28). For hot-swap applications, at the time of card connection, be sure to keep all I/O voltages within this range before applying V_{CCO} power. Consider applying V_{CCO} power before connecting the signal lines, to avoid turning on the ESD protection diodes, shown in Module 2: Figure 7, page 11. When the FPGA is completely unpowered, the I/O pins are high impedance, but there is a path through the upper and lower ESD protection diodes.
3. This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPU}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$. Spartan-3 family values for both resistances are stronger than they have been for previous FPGA families.
4. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.3V is supported but can cause increased leakage between the two pins. See the *Parasitic Leakage* section in UG331, *Spartan-3 Generation FPGA User Guide*.

Table 42: **Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Hold Times						
T_{IOICKP}	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(3), IOBDELAY = NONE	XC3S50	-0.55	-0.55	ns
			XC3S200	-0.29	-0.29	ns
			XC3S400	-0.29	-0.29	ns
			XC3S1000	-0.55	-0.55	ns
			XC3S1500	-0.55	-0.55	ns
			XC3S2000	-0.55	-0.55	ns
			XC3S4000	-0.61	-0.61	ns
			XC3S5000	-0.68	-0.68	ns
$T_{IOICKPD}$	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(3), IOBDELAY = IFD	XC3S50	-2.74	-2.74	ns
			XC3S200	-3.00	-3.00	ns
			XC3S400	-2.90	-2.90	ns
			XC3S1000	-3.24	-3.24	ns
			XC3S1500	-3.55	-3.55	ns
			XC3S2000	-4.57	-4.57	ns
			XC3S4000	-4.96	-4.96	ns
			XC3S5000	-5.09	-5.09	ns
Set/Reset Pulse Width						
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB		All	0.66	0.76	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 44.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 44. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 44: **Input Timing Adjustments for IOB *(Cont'd)***

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
LVCMOS15	0.42	0.49	ns
LVDCI_15	0.38	0.43	ns
LVDCI_DV2_15	0.38	0.44	ns
LVCMOS18	0.24	0.28	ns
LVDCI_18	0.29	0.33	ns
LVDCI_DV2_18	0.28	0.33	ns
LVCMOS25	0	0	ns
LVDCI_25	0.05	0.05	ns
LVDCI_DV2_25	0.04	0.04	ns
LVCMOS33, LVDCI_33, LVDCI_DV2_33	–0.05	–0.02	ns
LVTTL	0.18	0.21	ns
PCI33_3	0.20	0.22	ns
SSTL18_I, SSTL18_I_DCI	0.39	0.45	ns
SSTL18_II	0.39	0.45	ns
SSTL2_I, SSTL2_I_DCI	0.40	0.46	ns
SSTL2_II, SSTL2_II_DCI	0.36	0.41	ns
Differential Standards			
LDT_25 (ULVDS_25)	0.76	0.88	ns
LVDS_25, LVDS_25_DCI	0.65	0.75	ns
BLVDS_25	0.34	0.39	ns
LVDSEXT_25, LVDSEXT_25_DCI	0.80	0.92	ns
LVPECL_25	0.18	0.21	ns
RSDS_25	0.43	0.50	ns
DIFF_HSTL_II_18, DIFF_HSTL_II_18_DCI	0.34	0.39	ns
DIFF_SSTL2_II, DIFF_SSTL2_II_DCI	0.65	0.75	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32, Table 35, and Table 37.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Table 59: **Switching Characteristics for the DLL**

Symbol	Description	Frequency Mode / FCLKIN Range	Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_1X_LF	Frequency for the CLK0, CLK90, CLK180, and CLK270 outputs	Low	All	18	167	18	167	MHz
CLKOUT_FREQ_1X_HF	Frequency for the CLK0 and CLK180 outputs	High		48	280	48	280	MHz
CLKOUT_FREQ_2X_LF(3)	Frequency for the CLK2X and CLK2X180 outputs	Low		36	334	36	334	MHz
CLKOUT_FREQ_DV_LF	Frequency for the CLKDV output	Low		1.125	110	1.125	110	MHz
CLKOUT_FREQ_DV_HF		High		3	185	3	185	MHz
Output Clock Jitter(4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output	All	All	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			–	±200	–	±200	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			–	±300	–	±300	ps
Duty Cycle								
CLKOUT_DUTY_CYCLE_DLL(5)	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs	All	XC3S50	–	±150	–	±150	ps
			XC3S200	–	±150	–	±150	ps
			XC3S400	–	±250	–	±250	ps
			XC3S1000	–	±400	–	±400	ps
			XC3S1500	–	±400	–	±400	ps
			XC3S2000	–	±400	–	±400	ps
			XC3S4000	–	±400	–	±400	ps
			XC3S5000	–	±400	–	±400	ps
Phase Alignment								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs	All	All	–	±150	–	±150	ps
CLKOUT_PHASE	Phase offset between any two DLL outputs (except CLK2X and CLK0)			–	±140	–	±140	ps
	Phase offset between the CLK2X and CLK0 outputs			–	±250	–	±250	ps

Table 70: **Spartan-3 FPGA Pin Definitions**

Pin Name	Direction	Description
I/O: General-purpose I/O pins		
I/O	User-defined as input, output, bidirectional, three-state output, open-drain output, open-source output	**User I/O:** Unrestricted single-ended user-I/O pin. Supports all I/O standards except the differential standards.
I/O_Lxxy_#	User-defined as input, output, bidirectional, three-state output, open-drain output, open-source output	**User I/O, Half of Differential Pair:** Unrestricted single-ended user-I/O pin or half of a differential pair. Supports all I/O standards including the differential standards.
DUAL: Dual-purpose configuration pins		
IO_Lxxy_#/DIN/D0, IO_Lxxy_#/D1, IO_Lxxy_#/D2, IO_Lxxy_#/D3, IO_Lxxy_#/D4, IO_Lxxy_#/D5, IO_Lxxy_#/D6, IO_Lxxy_#/D7	Input during configuration Possible bidirectional I/O after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Configuration Data Port:** In Parallel (SelectMAP) modes, D0-D7 are byte-wide configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained via the Persist bitstream option. In Serial modes, DIN (D0) serves as the single configuration data input. This pin becomes a user I/O after configuration unless retained by the Persist bitstream option.
IO_Lxxy_#/CS_B	Input during Parallel mode configuration Possible input after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Chip Select for Parallel Mode Configuration:** In Parallel (SelectMAP) modes, this is the active-Low Chip Select signal. This pin becomes a user I/O after configuration unless the SelectMAP port is retained via the Persist bitstream option.
IO_Lxxy_#/RDWR_B	Input during Parallel mode configuration Possible input after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Read/Write Control for Parallel Mode Configuration:** In Parallel (SelectMAP) modes, this is the active-Low Write Enable, active-High Read Enable signal. This pin becomes a user I/O after configuration unless the SelectMAP port is retained via the Persist bitstream option.
IO_Lxxy_#/ BUSY/DOUT	Output during configuration Possible output after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Configuration Data Rate Control for Parallel Mode, Serial Data Output for Serial Mode:** In Parallel (SelectMAP) modes, BUSY throttles the rate at which configuration data is loaded. This pin becomes a user I/O after configuration unless the SelectMAP port is retained via the Persist bitstream option. In Serial modes, DOUT provides preamble and configuration data to downstream devices in a multi-FPGA daisy-chain. This pin becomes a user I/O after configuration.
IO_Lxxy_#/INIT_B	Bidirectional (open-drain) during configuration User I/O after configuration	**Initializing Configuration Memory/Detected Configuration Error:** When Low, this pin indicates that configuration memory is being cleared. When held Low, this pin delays the start of configuration. After this pin is released or configuration memory is cleared, the pin goes High. During configuration, a Low on this output indicates that a configuration data error occurred. This pin always has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM during configuration, regardless of the HSWAP_EN pin. This pin becomes a user I/O after configuration.
DCI: Digitally Controlled Impedance reference resistor input pins		
IO_Lxxy_#/VRN_# or IO/VRN_#	Input when using DCI Otherwise, same as I/O	**DCI Reference Resistor for NMOS I/O Transistor (per bank):** If using DCI, a 1% precision impedance-matching resistor is connected between this pin and the VCCO supply for this bank. Otherwise, this pin is a user I/O.
IO_Lxxy_#/VRP_# or IO/VRP_#	Input when using DCI Otherwise, same as I/O	**DCI Reference Resistor for PMOS I/O Transistor (per bank):** If using DCI, a 1% precision impedance-matching resistor is connected between this pin and the ground supply. Otherwise, this pin is a user I/O.

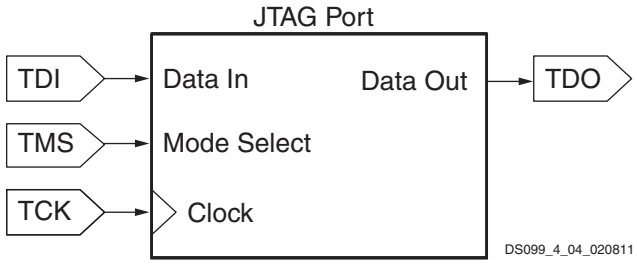

Figure 43: **JTAG Port**

IDCODE Register

Spartan-3 FPGAs contain a 32-bit identification register called the IDCODE register, as defined in the IEEE 1149.1 JTAG standard. The fixed value electrically identifies the manufacture (Xilinx) and the type of device being addressed over a JTAG chain. This register allows the JTAG host to identify the device being tested or programmed via JTAG. See Table 78.

Using JTAG Port After Configuration

The JTAG port is always active and available before, during, and after FPGA configuration. Add the BSCAN_SPARTAN3 primitive to the design to create user-defined JTAG instructions and JTAG chains to communicate with internal logic.

Furthermore, the contents of the User ID register within the JTAG port can be specified as a Bitstream Generation option. By default, the 32-bit User ID register contains `0xFFFFFFFF`.

Table 78: **Spartan-3 JTAG IDCODE Register Values (hexadecimal)**

Part Number	IDCODE Register
XC3S50	0x0140C093
XC3S200	0x01414093
XC3S400	0x0141C093
XC3S1000	0x01428093
XC3S1500	0x01434093
XC3S2000	0x01440093
XC3S4000	0x01448093
XC3S5000	0x01450093

Precautions When Using the JTAG Port in 3.3V Environments

The JTAG port is powered by the +2.5V VCCAUX power supply. When connecting to a 3.3V interface, the JTAG input pins must be current-limited using a series resistor. Similarly, the TDO pin is a CMOS output powered from +2.5V. The TDO output can directly drive a 3.3V input but with reduced noise immunity. See 3.3V-Tolerant Configuration Interface, page 47. See also XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional details.

The following interface precautions are recommended when connecting the JTAG port to a 3.3V interface.

- Avoid actively driving the JTAG input signals High with 3.3V signal levels. If required in the application, use series current-limiting resistors to keep the current below 10 mA per pin.
- If possible, drive the FPGA JTAG inputs with drivers that can be placed in high-impedance (Hi-Z) after using the JTAG port. Alternatively, drive the FPGA JTAG inputs with open-drain outputs, which only drive Low. In both cases, pull-up resistors are required. The FPGA JTAG pins have pull-up resistors to VCCAUX before configuration and optional pull-up resistors after configuration, controlled by Bitstream Options, page 125.

CP132: 132-Ball Chip-Scale Package

Note: The CP132 and CPG132 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

The pinout and footprint for the XC3S50 in the 132-ball chip-scale package, CP132, appear in Table 89 and Figure 45.

All the package pins appear in Table 89 and are sorted by bank number, then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The CP132 footprint has eight I/O banks. However, the voltage supplies for the two I/O banks along an edge are connected together internally. Consequently, there are four output voltage supplies, labeled VCCO_TOP, VCCO_RIGHT, VCCO_BOTTOM, and VCCO_LEFT.

Pinout Table

Table 89: **CP132 Package Pinout**

Bank	XC3S50 Pin Name	CP132 Ball	Type
0	IO_L01N_0/VRP_0	A3	DCI
0	IO_L01P_0/VRN_0	C4	DCI
0	IO_L27N_0	C5	I/O
0	IO_L27P_0	B5	I/O
0	IO_L30N_0	B6	I/O
0	IO_L30P_0	A6	I/O
0	IO_L31N_0	C7	I/O
0	IO_L31P_0/VREF_0	B7	VREF
0	IO_L32N_0/GCLK7	A7	GCLK
0	IO_L32P_0/GCLK6	C8	GCLK
1	IO_L01N_1/VRP_1	A13	DCI
1	IO_L01P_1/VRN_1	B13	DCI
1	IO_L27N_1	C11	I/O
1	IO_L27P_1	A12	I/O
1	IO_L28N_1	A11	I/O
1	IO_L28P_1	B11	I/O
1	IO_L31N_1/VREF_1	C9	VREF
1	IO_L31P_1	A10	I/O
1	IO_L32N_1/GCLK5	A8	GCLK
1	IO_L32P_1/GCLK4	A9	GCLK
2	IO_L01N_2/VRP_2	D12	DCI
2	IO_L01P_2/VRN_2	C14	DCI
2	IO_L20N_2	E12	I/O
2	IO_L20P_2	E13	I/O
2	IO_L21N_2	E14	I/O
2	IO_L21P_2	F12	I/O
2	IO_L23N_2/VREF_2	F13	VREF
2	IO_L23P_2	F14	I/O
2	IO_L24N_2	G12	I/O

Table 91: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
2	IO_L23N_2/VREF_2	P98	VREF
2	IO_L23P_2	P97	I/O
2	IO_L24N_2	P96	I/O
2	IO_L24P_2	P95	I/O
2	IO_L40N_2	P93	I/O
2	IO_L40P_2/VREF_2	P92	VREF
3	IO	P76	I/O
3	IO_L01N_3/VRP_3	P74	DCI
3	IO_L01P_3/VRN_3	P73	DCI
3	IO_L20N_3	P78	I/O
3	IO_L20P_3	P77	I/O
3	IO_L21N_3	P80	I/O
3	IO_L21P_3	P79	I/O
3	IO_L22N_3	P83	I/O
3	IO_L22P_3	P82	I/O
3	IO_L23N_3	P85	I/O
3	IO_L23P_3/VREF_3	P84	VREF
3	IO_L24N_3	P87	I/O
3	IO_L24P_3	P86	I/O
3	IO_L40N_3/VREF_3	P90	VREF
3	IO_L40P_3	P89	I/O
4	IO/VREF_4	P70	VREF
4	IO_L01N_4/VRP_4	P69	DCI
4	IO_L01P_4/VRN_4	P68	DCI
4	IO_L27N_4/DIN/D0	P65	DUAL
4	IO_L27P_4/D1	P63	DUAL
4	IO_L30N_4/D2	P60	DUAL
4	IO_L30P_4/D3	P59	DUAL
4	IO_L31N_4/INIT_B	P58	DUAL
4	IO_L31P_4/DOUT/BUSY	P57	DUAL
4	IO_L32N_4/GCLK1	P56	GCLK
4	IO_L32P_4/GCLK0	P55	GCLK
5	IO/VREF_5	P44	VREF
5	IO_L01N_5/RDWR_B	P41	DUAL
5	IO_L01P_5/CS_B	P40	DUAL
5	IO_L28N_5/D6	P47	DUAL
5	IO_L28P_5/D7	P46	DUAL
5	IO_L31N_5/D4	P51	DUAL
5	IO_L31P_5/D5	P50	DUAL
5	IO_L32N_5/GCLK3	P53	GCLK

PQ208: 208-lead Plastic Quad Flat Pack

The 208-lead plastic quad flat package, PQ208, supports three different Spartan-3 devices, including the XC3S50, the XC3S200, and the XC3S400. The footprints for the XC3S200 and XC3S400 are identical, as shown in Table 93 and Figure 47. The XC3S50, however, has fewer I/O pins resulting in 17 unconnected pins on the PQ208 package, labeled as "N.C." In Table 93 and Figure 47, these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in Table 93 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S50 pinout and the pinout for the XC3S200 and XC3S400, then that difference is highlighted in Table 93. If the table entry is shaded grey, then there is an unconnected pin on the XC3S50 that maps to a user-I/O pin on the XC3S200 and XC3S400. If the table entry is shaded tan, then the unconnected pin on the XC3S50 maps to a VREF-type pin on the XC3S200 and XC3S400. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S50 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S50 device to an XC3S200 or XC3S400 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip

Pinout Table

Table 93: **PQ208 Package Pinout**

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
0	IO	IO	P189	I/O
0	IO	IO	P197	I/O
0	N.C. (◆)	IO/VREF_0	P200	VREF
0	IO/VREF_0	IO/VREF_0	P205	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	P204	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	P203	DCI
0	IO_L25N_0	IO_L25N_0	P199	I/O
0	IO_L25P_0	IO_L25P_0	P198	I/O
0	IO_L27N_0	IO_L27N_0	P196	I/O
0	IO_L27P_0	IO_L27P_0	P194	I/O
0	IO_L30N_0	IO_L30N_0	P191	I/O
0	IO_L30P_0	IO_L30P_0	P190	I/O
0	IO_L31N_0	IO_L31N_0	P187	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	P185	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	P184	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	P183	GCLK
0	VCCO_0	VCCO_0	P188	VCCO
0	VCCO_0	VCCO_0	P201	VCCO
1	IO	IO	P167	I/O
1	IO	IO	P175	I/O
1	IO	IO	P182	I/O
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	P162	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	P161	DCI

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
4	IO_L30N_4/D2	IO_L30N_4/D2	U12	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	V12	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	W12	DUAL
4	IO_L31P_4/DOUT/BUSY	IO_L31P_4/DOUT/BUSY	Y12	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	AA12	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	AB12	GCLK
4	VCCO_4	VCCO_4	T12	VCCO
4	VCCO_4	VCCO_4	T13	VCCO
4	VCCO_4	VCCO_4	T14	VCCO
4	VCCO_4	VCCO_4	U15	VCCO
4	VCCO_4	VCCO_4	Y15	VCCO
5	IO	IO	U7	I/O
5	N.C. (◆)	IO	U9	I/O
5	IO	IO	U10	I/O
5	IO	IO	U11	I/O
5	IO	IO	V7	I/O
5	IO	IO	V10	I/O
5	IO/VREF_5	IO/VREF_5	AB11	VREF
5	IO/VREF_5	IO/VREF_5	U6	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	Y4	DUAL
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AA3	DUAL
5	IO_L06N_5	IO_L06N_5	AB4	I/O
5	IO_L06P_5	IO_L06P_5	AA4	I/O
5	IO_L09N_5	IO_L09N_5	Y5	I/O
5	IO_L09P_5	IO_L09P_5	W5	I/O
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	AB5	DCI
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	AA5	DCI
5	IO_L15N_5	IO_L15N_5	W6	I/O
5	IO_L15P_5	IO_L15P_5	V6	I/O
5	IO_L16N_5	IO_L16N_5	AA6	I/O
5	IO_L16P_5	IO_L16P_5	Y6	I/O
5	N.C. (◆)	IO_L19N_5	Y7	I/O
5	N.C. (◆)	IO_L19P_5/ VREF_5	W7	VREF
5	N.C. (◆)	IO_L22N_5	AB7	I/O
5	N.C. (◆)	IO_L22P_5	AA7	I/O
5	IO_L24N_5	IO_L24N_5	W8	I/O
5	IO_L24P_5	IO_L24P_5	V8	I/O
5	IO_L25N_5	IO_L25N_5	AB8	I/O
5	IO_L25P_5	IO_L25P_5	AA8	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO_L30N_0	IO_L30N_0	G15	I/O
0	IO_L30P_0	IO_L30P_0	F15	I/O
0	IO_L31N_0	IO_L31N_0	D15	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C15	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B15	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A15	GCLK
0	N.C. (◆)	IO_L35N_0	B7	I/O
0	N.C. (◆)	IO_L35P_0	A7	I/O
0	N.C. (◆)	IO_L36N_0	G7	I/O
0	N.C. (◆)	IO_L36P_0	H8	I/O
0	N.C. (◆)	IO_L37N_0	E9	I/O
0	N.C. (◆)	IO_L37P_0	D9	I/O
0	N.C. (◆)	IO_L38N_0	B9	I/O
0	N.C. (◆)	IO_L38P_0	A9	I/O
0	VCCO_0	VCCO_0	C5	VCCO
0	VCCO_0	VCCO_0	E7	VCCO
0	VCCO_0	VCCO_0	C9	VCCO
0	VCCO_0	VCCO_0	G9	VCCO
0	VCCO_0	VCCO_0	J11	VCCO
0	VCCO_0	VCCO_0	L12	VCCO
0	VCCO_0	VCCO_0	C13	VCCO
0	VCCO_0	VCCO_0	G13	VCCO
0	VCCO_0	VCCO_0	L13	VCCO
0	VCCO_0	VCCO_0	L14	VCCO
1	IO	IO	E25	I/O
1	IO	IO	J21	I/O
1	IO	IO	K20	I/O
1	IO	IO	F18	I/O
1	IO	IO	F16	I/O
1	IO	IO	A16	I/O
1	IO/VREF_1	IO/VREF_1	J17	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	A27	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B27	DCI
1	IO_L02N_1	IO_L02N_1	D26	I/O
1	IO_L02P_1	IO_L02P_1	C27	I/O
1	IO_L03N_1	IO_L03N_1	A26	I/O
1	IO_L03P_1	IO_L03P_1	B26	I/O
1	IO_L04N_1	IO_L04N_1	B25	I/O
1	IO_L04P_1	IO_L04P_1	C25	I/O
1	IO_L05N_1	IO_L05N_1	F24	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	VCCO_2	VCCO_2	J28	VCCO
2	VCCO_2	VCCO_2	N28	VCCO
3	IO	IO	AB25	I/O
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	AH30	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	AH29	DCI
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	AG28	VREF
3	IO_L02P_3	IO_L02P_3	AG27	I/O
3	IO_L03N_3	IO_L03N_3	AG30	I/O
3	IO_L03P_3	IO_L03P_3	AG29	I/O
3	IO_L04N_3	IO_L04N_3	AF30	I/O
3	IO_L04P_3	IO_L04P_3	AF29	I/O
3	IO_L05N_3	IO_L05N_3	AE26	I/O
3	IO_L05P_3	IO_L05P_3	AF27	I/O
3	IO_L06N_3	IO_L06N_3	AE29	I/O
3	IO_L06P_3	IO_L06P_3	AE28	I/O
3	IO_L07N_3	IO_L07N_3	AD28	I/O
3	IO_L07P_3	IO_L07P_3	AD27	I/O
3	IO_L08N_3	IO_L08N_3	AD30	I/O
3	IO_L08P_3	IO_L08P_3	AD29	I/O
3	IO_L09N_3	IO_L09N_3	AC24	I/O
3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	AD25	VREF
3	IO_L10N_3	IO_L10N_3	AC26	I/O
3	IO_L10P_3	IO_L10P_3	AC25	I/O
3	IO_L11N_3	IO_L11N_3	AC28	I/O
3	IO_L11P_3	IO_L11P_3	AC27	I/O
3	IO_L13N_3/VREF_3	IO_L13N_3/VREF_3	AC30	VREF
3	IO_L13P_3	IO_L13P_3	AC29	I/O
3	IO_L14N_3	IO_L14N_3	AB27	I/O
3	IO_L14P_3	IO_L14P_3	AB26	I/O
3	IO_L15N_3	IO_L15N_3	AB30	I/O
3	IO_L15P_3	IO_L15P_3	AB29	I/O
3	IO_L16N_3	IO_L16N_3	AA22	I/O
3	IO_L16P_3	IO_L16P_3	AB23	I/O
3	IO_L17N_3	IO_L17N_3	AA25	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	AA24	VREF
3	IO_L19N_3	IO_L19N_3	AA29	I/O
3	IO_L19P_3	IO_L19P_3	AA28	I/O
3	IO_L20N_3	IO_L20N_3	Y21	I/O
3	IO_L20P_3	IO_L20P_3	AA21	I/O
3	IO_L21N_3	IO_L21N_3	Y24	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	GND	GND	R17	GND
N/A	GND	GND	T17	GND
N/A	GND	GND	U17	GND
N/A	GND	GND	V17	GND
N/A	GND	GND	AC17	GND
N/A	GND	GND	AF17	GND
N/A	GND	GND	AK17	GND
N/A	GND	GND	N18	GND
N/A	GND	GND	P18	GND
N/A	GND	GND	R18	GND
N/A	GND	GND	T18	GND
N/A	GND	GND	U18	GND
N/A	GND	GND	V18	GND
N/A	GND	GND	R19	GND
N/A	GND	GND	T19	GND
N/A	GND	GND	A21	GND
N/A	GND	GND	E21	GND
N/A	GND	GND	H21	GND
N/A	GND	GND	AC21	GND
N/A	GND	GND	AF21	GND
N/A	GND	GND	AK21	GND
N/A	GND	GND	K23	GND
N/A	GND	GND	P23	GND
N/A	GND	GND	U23	GND
N/A	GND	GND	AA23	GND
N/A	GND	GND	A25	GND
N/A	GND	GND	AK25	GND
N/A	GND	GND	E26	GND
N/A	GND	GND	K26	GND
N/A	GND	GND	P26	GND
N/A	GND	GND	U26	GND
N/A	GND	GND	AA26	GND
N/A	GND	GND	AF26	GND
N/A	GND	GND	A29	GND
N/A	GND	GND	B29	GND
N/A	GND	GND	AJ29	GND
N/A	GND	GND	AK29	GND
N/A	GND	GND	A30	GND
N/A	GND	GND	B30	GND
N/A	GND	GND	F30	GND

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	GND	GND	K30	GND
N/A	GND	GND	P30	GND
N/A	GND	GND	U30	GND
N/A	GND	GND	AA30	GND
N/A	GND	GND	AE30	GND
N/A	GND	GND	AJ30	GND
N/A	GND	GND	AK30	GND
N/A	GND	GND	AK2	GND
N/A	VCCAUX	VCCAUX	F4	VCCAUX
N/A	VCCAUX	VCCAUX	K4	VCCAUX
N/A	VCCAUX	VCCAUX	P4	VCCAUX
N/A	VCCAUX	VCCAUX	U4	VCCAUX
N/A	VCCAUX	VCCAUX	AA4	VCCAUX
N/A	VCCAUX	VCCAUX	AE4	VCCAUX
N/A	VCCAUX	VCCAUX	D6	VCCAUX
N/A	VCCAUX	VCCAUX	AG6	VCCAUX
N/A	VCCAUX	VCCAUX	D10	VCCAUX
N/A	VCCAUX	VCCAUX	AG10	VCCAUX
N/A	VCCAUX	VCCAUX	D14	VCCAUX
N/A	VCCAUX	VCCAUX	AG14	VCCAUX
N/A	VCCAUX	VCCAUX	D17	VCCAUX
N/A	VCCAUX	VCCAUX	AG17	VCCAUX
N/A	VCCAUX	VCCAUX	D21	VCCAUX
N/A	VCCAUX	VCCAUX	AG21	VCCAUX
N/A	VCCAUX	VCCAUX	D25	VCCAUX
N/A	VCCAUX	VCCAUX	AG25	VCCAUX
N/A	VCCAUX	VCCAUX	F27	VCCAUX
N/A	VCCAUX	VCCAUX	K27	VCCAUX
N/A	VCCAUX	VCCAUX	P27	VCCAUX
N/A	VCCAUX	VCCAUX	U27	VCCAUX
N/A	VCCAUX	VCCAUX	AA27	VCCAUX
N/A	VCCAUX	VCCAUX	AE27	VCCAUX
N/A	VCCINT	VCCINT	L11	VCCINT
N/A	VCCINT	VCCINT	R11	VCCINT
N/A	VCCINT	VCCINT	T11	VCCINT
N/A	VCCINT	VCCINT	Y11	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	N12	VCCINT
N/A	VCCINT	VCCINT	P12	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
4	VCCO_4	VCCO_4	AC19	VCCO
4	VCCO_4	VCCO_4	AC20	VCCO
4	VCCO_4	VCCO_4	AC21	VCCO
4	VCCO_4	VCCO_4	AC22	VCCO
4	VCCO_4	VCCO_4	AG20	VCCO
4	VCCO_4	VCCO_4	AG24	VCCO
4	VCCO_4	VCCO_4	AH27	VCCO
4	VCCO_4	VCCO_4	AJ22	VCCO
4	VCCO_4	VCCO_4	AL19	VCCO
4	VCCO_4	VCCO_4	AL24	VCCO
4	VCCO_4	VCCO_4	AM27	VCCO
4	VCCO_4	VCCO_4	AM31	VCCO
4	VCCO_4	VCCO_4	AN22	VCCO
5	IO	IO	AD11	I/O
5	N.C. (◆)	IO	AD12	I/O
5	IO	IO	AD14	I/O
5	IO	IO	AD15	I/O
5	IO	IO	AD16	I/O
5	IO	IO	AD17	I/O
5	IO	IO	AE14	I/O
5	IO	IO	AE16	I/O
5	N.C. (◆)	IO	AF9	I/O
5	IO	IO	AG9	I/O
5	IO	IO	AG12	I/O
5	IO	IO	AJ6	I/O
5	IO	IO	AJ17	I/O
5	IO	IO	AK10	I/O
5	IO	IO	AK14	I/O
5	IO	IO	AM12	I/O
5	IO	IO	AN9	I/O
5	IO/VREF_5	IO/VREF_5	AJ8	VREF
5	IO/VREF_5	IO/VREF_5	AL5	VREF
5	IO/VREF_5	IO/VREF_5	AP17	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	AP3	DUAL
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AN3	DUAL
5	IO_L02N_5	IO_L02N_5	AP4	I/O
5	IO_L02P_5	IO_L02P_5	AN4	I/O
5	IO_L03N_5	IO_L03N_5	AN5	I/O
5	IO_L03P_5	IO_L03P_5	AM5	I/O
5	IO_L04N_5	IO_L04N_5	AM6	I/O

User I/Os by Bank

Note: The FG(G)1156 package is discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

Table 111 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S4000 in the FG1156 package. Similarly, Table 112 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S5000 in the FG1156 package.

Table 111: **User I/Os Per Bank for XC3S4000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	90	79	0	2	7	2
	1	90	79	0	2	7	2
Right	2	88	80	0	2	6	0
	3	88	79	0	2	7	0
Bottom	4	90	73	6	2	7	2
	5	90	73	6	2	7	2
Left	6	88	79	0	2	7	0
	7	88	79	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

Table 112: **User I/Os Per Bank for XC3S5000 in FG1156 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	100	89	0	2	7	2
	1	100	89	0	2	7	2
Right	2	96	87	0	2	7	0
	3	96	87	0	2	7	0
Bottom	4	100	83	6	2	7	2
	5	100	83	6	2	7	2
Left	6	96	87	0	2	7	0
	7	96	87	0	2	7	0

Notes:

1. The FG1156 and FGG1156 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

Date	Version	Description
11/30/07	2.3	Added XC3S5000 FG(G)676 package. Noted that the FG(G)1156 package is being discontinued. Updated Table 86 with latest thermal characteristics data.
06/25/08	2.4	Updated formatting and links.
12/04/09	2.5	Added link to UG332 in CCLK: Configuration Clock. Noted that the CP132, CPG132, FG1156, and FGG1156 packages are being discontinued in Table 81, Table 83, Table 84, Table 85, and Table 86. Updated CP132: 132-Ball Chip-Scale Package to indicate that the CP132 and CPG132 packages are being discontinued.
10/29/12	3.0	Added Notice of Disclaimer. Per XCN07022, updated the FG1156 and FGG1156 package discussion throughout document including in Table 81, Table 83, Table 84, Table 85, and Table 86. Per XCN08011, updated CP132 and CPG132 package discussion throughout document including in Table 81, Table 83, Table 84, Table 85, and Table 86. This product is not recommended for new designs.

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