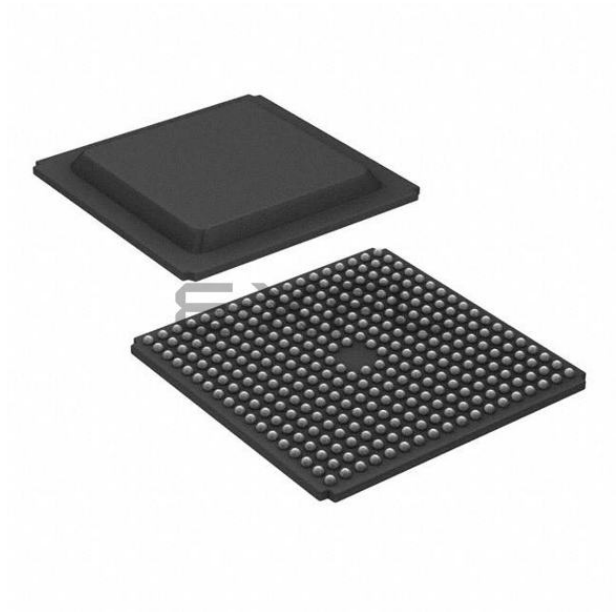
AMD Xilinx - XC3S400-4FG320I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	294912
Number of I/O	221
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s400-4fg320i

The DLL component has two clock inputs, CLKIN and CLKFB, as well as seven clock outputs, CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV as described in Table 16. The clock outputs drive simultaneously; however, the High Frequency mode only supports a subset of the outputs available in the Low Frequency mode. See DLL Frequency Modes, page 35. Signals that initialize and report the state of the DLL are discussed in The Status Logic Component, page 41.

Table 16: **DLL Signals**

Signal	Direction	Description	Mode Support	
			Low Frequency	High Frequency
CLKIN	Input	Accepts original clock signal.	Yes	Yes
CLKFB	Input	Accepts either CLK0 or CLK2X as feed back signal. (Set CLK_FEEDBACK attribute accordingly).	Yes	Yes
CLK0	Output	Generates clock signal with same frequency and phase as CLKIN.	Yes	Yes
CLK90	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 90°.	Yes	No
CLK180	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 180°.	Yes	Yes
CLK270	Output	Generates clock signal with same frequency as CLKIN, only phase-shifted 270°.	Yes	No
CLK2X	Output	Generates clock signal with same phase as CLKIN, only twice the frequency.	Yes	No
CLK2X180	Output	Generates clock signal with twice the frequency of CLKIN, phase-shifted 180° with respect to CLKIN.	Yes	No
CLKDV	Output	Divides the CLKIN frequency by CLKDV_DIVIDE value to generate lower frequency clock signal that is phase-aligned to CLKIN.	Yes	Yes

The clock signal supplied to the CLKIN input serves as a reference waveform, with which the DLL seeks to align the feedback signal at the CLKFB input. When eliminating clock skew, the common approach to using the DLL is as follows: The CLK0 signal is passed through the clock distribution network to all the registers it synchronizes. These registers are either internal or external to the FPGA. After passing through the clock distribution network, the clock signal returns to the DLL via a feedback line called CLKFB. The control block inside the DLL measures the phase error between CLKFB and CLKIN. This phase error is a measure of the clock skew that the clock distribution network introduces. The control block activates the appropriate number of delay elements to cancel out the clock skew. Once the DLL has brought the CLK0 signal in phase with the CLKIN signal, it asserts the LOCKED output, indicating a “lock” on to the CLKIN signal.

DLL Attributes and Related Functions

A number of different functional options can be set for the DLL component through the use of the attributes described in Table 17. Each attribute is described in detail in the sections that follow:

Table 17: **DLL Attributes**

Attribute	Description	Values
CLK_FEEDBACK	Chooses either the CLK0 or CLK2X output to drive the CLKFB input	NONE, 1X, 2X
DLL_FREQUENCY_MODE	Chooses between High Frequency and Low Frequency modes	LOW, HIGH
CLKIN_DIVIDE_BY_2	Halves the frequency of the CLKIN signal just as it enters the DCM	TRUE, FALSE
CLKDV_DIVIDE	Selects constant used to divide the CLKIN input frequency to generate the CLKDV output frequency	1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6.0, 6.5, 7.0, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.
DUTY_CYCLE_CORRECTION	Enables 50% duty cycle correction for the CLK0, CLK90, CLK180, and CLK270 outputs	TRUE, FALSE

The Standard Configuration Interface

Configuration signals belong to one of two different categories: Dedicated or Dual-Purpose. Which category determines which of the FPGA's power rails supplies the signal's driver and, thus, helps describe the electrical characteristics at the pin.

The Dedicated configuration pins include PROG_B, HSWAP_EN, TDI, TMS, TCK, TDO, CCLK, DONE, and M0-M2. These pins are powered by the V_{CCAUX} supply.

The Dual-Purpose configuration pins comprise INIT_B, DOUT, BUSY, RDWR_B, CS_B, and DIN/D0-D7. Each of these pins, according to its bank placement, uses the V_{CCO} lines for either Bank 4 (VCCO_4 on most packages, VCCO_BOTTOM on TQ144 and CP132 packages) or Bank 5 (VCCO_5). All the signals used in the serial configuration modes rely on VCCO_4 power. Signals used in the parallel configuration modes and Readback require from VCCO_5 as well as from VCCO_4.

Both the Dedicated signals described above and the Dual-Purpose signals constitute the configuration interface. The Dedicated pins, powered by the 2.5V V_{CCAUX} supply, always use the LVCMOS25 I/O standard. The Dual-Purpose signals, however, are powered by the VCCO_4 supply and also by the VCCO_5 supply in the Parallel configuration modes. The simplest configuration interface uses 2.5V for VCCO_4 and VCCO_5, if required. However, VCCO_4 and, if needed, VCCO_5 can be voltages other than 2.5V but then the configuration interface will have two voltage levels: 2.5V for V_{CCAUX} and a separate V_{CCO} supply. The Dual-Purpose signals default to the LVCMOS input and output levels for the associated V_{CCO} voltage supply.

3.3V-Tolerant Configuration Interface

A 3.3V-tolerant configuration interface simply requires adding a few external resistors as described in detail in XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs*.

The 3.3V-tolerance is implemented as follows (a similar approach can be used for other supply voltage levels):

Apply 3.3V to VCCO_4 and, in some configuration modes, to VCCO_5 to power the Dual-Purpose configuration pins. This scales the output voltages and input thresholds associated with these pins so that they become 3.3V-compatible.

Apply 2.5V to V_{CCAUX} to power the Dedicated configuration pins. For 3.3V-tolerance, the Dedicated inputs require series resistors to limit the incoming current to 10 mA or less. The Dedicated outputs have reduced noise margin when the FPGA drives a High logic level into another device's 3.3V receiver. Choose a power regulator or supply that can tolerate reverse current on the V_{CCAUX} lines.

Configuration Modes

Spartan-3 FPGAs support the following five configuration modes:

- Slave Serial mode
- Master Serial mode
- Slave Parallel (SelectMAP) mode
- Master Parallel (SelectMAP) mode
- Boundary-Scan (JTAG) mode (IEEE 1532/IEEE 1149.1)

Slave Serial Mode

In Slave Serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other serial source of configuration data. The FPGA on the far right of Figure 26 is set for the Slave Serial mode. The CCLK pin on the FPGA is an input in this mode. The serial bitstream must be set up at the DIN input pin a short time before each rising edge of the externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the DOUT pin. The data on the DOUT pin changes on the falling edge of CCLK.

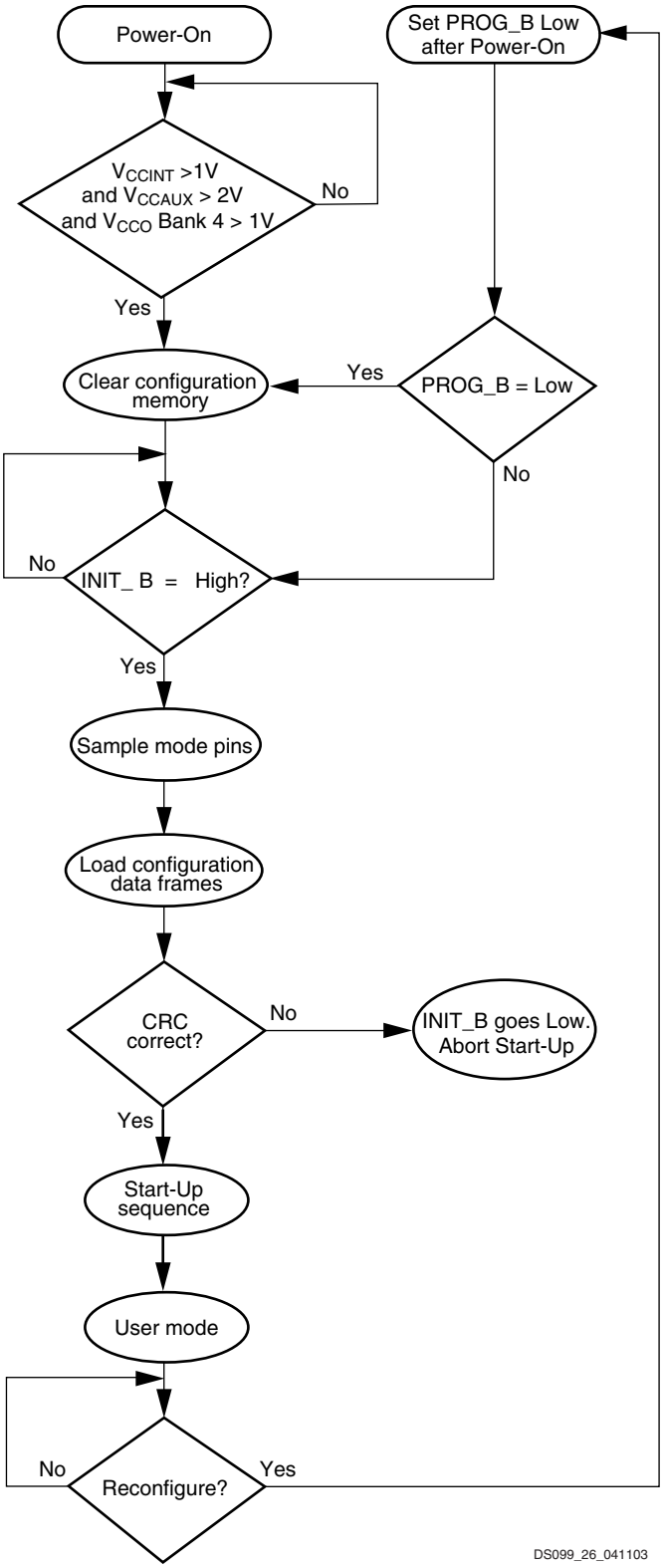

Figure 29: **Configuration Flow Diagram for the Serial and Parallel Modes**

Revision History

Date	Version No.	Description
04/11/03	1.0	Initial Xilinx release
05/19/03	1.1	Added Block RAM column, DCMs, and multipliers to XC3S50 descriptions.
07/11/03	1.2	Explained the configuration port *Persist* option in Slave Parallel Mode (SelectMAP) section. Updated Figure 8 and Double-Data-Rate Transmission section to indicate that DDR clocking for the XC3S50 is the same as that for all other Spartan-3 devices. Updated description of I/O voltage tolerance in ESD Protection section. In Table 10, changed input termination type for DCI version of the LVCMOS standard to *None*. Added additional flexibility for making DLL connections in Figure 21 and accompanying text. In the Configuration section, inserted an explanation of how to choose power supplies for the configuration interface, including guidelines for achieving 3.3V-tolerance.
08/24/04	1.3	Showed inversion of 3-state signal (Figure 7). Clarified description of pull-up and pull-down resistors (Table 6 and page 13). Added information on operating block RAM with multipliers to page 26. Corrected output buffer name in Figure 21. Corrected description of how DOUT is synchronized to CCLK (page 47).
08/19/05	1.4	Corrected description of WRITE_FIRST and READ_FIRST in Table 13. Added note regarding address setup and hold time requirements whenever a block RAM port is enabled (Table 13). Added information in the maximum length of a Configuration daisy-chain. Added reference to XAPP453 in 3.3V-Tolerant Configuration Interface section. Added information on the STATUS[2] DCM output (Table 23). Added information on CCLK behavior and termination recommendations to Configuration. Added Additional Configuration Details section. Added Powering Spartan-3 FPGAs section. Removed GSR from Figure 31 because its timing is not programmable.
04/03/06	2.0	Updated Figure 7. Updated Figure 14. Updated Table 10. Updated Figure 22. Corrected Platform Flash supply voltage name and value in Figure 26 and Figure 28. Added No Internal Charge Pumps or Free-Running Oscillators. Corrected a few minor typographical errors.
04/26/06	2.1	Added more information on the pull-up resistors that are active during configuration to Configuration. Added information to Boundary-Scan (JTAG) Mode about potential interactions when configuring via JTAG if the mode select pins are set for other than JTAG.
05/25/07	2.2	Added Spartan-3 FPGA Design Documentation. Noted SSTL2_I_DCI 25-Ohm driver in Table 10 and Table 11. Added note that pull-down is active during boundary scan tests.
11/30/07	2.3	Updated links to documentation on xilinx.com.
06/25/08	2.4	Added HSLVDCI to Table 10. Updated formatting and links.
12/04/09	2.5	Updated HSLVDCI description in Digitally Controlled Impedance (DCI). Updated the low-voltage differential signaling V_{CCO} values in Table 10. Noted that the CP132 package is being discontinued in The Organization of IOBs into Banks. Updated rule 4 in Rules Concerning Banks. Added software version requirement in The Fixed Phase Mode.
10/29/12	3.0	Added Notice of Disclaimer. Per XCN07022, updated the discontinued FG1156 and FGG1156 package discussion throughout document. Per XCN08011, updated the discontinued CP132 and CPG132 package discussion throughout document. This product is not recommended for new designs.

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

- **Advance:** Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur. Use as estimates, not for production.
- **Preliminary:** Based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reported delays is greatly reduced compared to Advance data. Use as estimates, not for production.
- **Production:** These specifications are approved only after silicon has been characterized over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Parameter values are considered stable with no future changes expected.

  Production-quality systems must only use FPGA designs compiled with a Production status speed file. FPGA designs using a less mature speed file designation should only be used during system prototyping or preproduction qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **The following applies unless otherwise noted: The parameter values published in this module apply to all Spartan®-3 devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.** All parameters representing voltages are measured with respect to GND.

Mask and Fab Revisions

Some specifications list different values for one or more mask or fab revisions, indicated by the device top marking (see Package Marking, page 5). The revision differences involve the power ramp rates, differential DC specifications, and DCM characteristics. The most recent revision (mask rev E and GQ fab/geometry code) is errata-free with improved specifications than earlier revisions.

Mask rev E with fab rev GQ has been shipping since 2005 (see XCN05009) and has been 100% of Xilinx Spartan-3 device shipments since 2006. SCD 0974 was provided to ensure the receipt of the rev E silicon, but it is no longer needed. Parts ordered under the SCD appended “0974” to the standard part number. For example, “XC3S50-4VQ100C” became “XC3S50-4VQ100C0974”.

Table 28: **Absolute Maximum Ratings**

Symbol	Description	Conditions		Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND			–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage relative to GND			–0.5	3.00	V
V_{CCO}	Output driver supply voltage relative to GND			–0.5	3.75	V
V_{REF}	Input reference voltage relative to GND			–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND(2,4)	Driver in a high-impedance state	Commercial	–0.95	4.4	V
			Industrial	–0.85	4.3	
	Voltage applied to all Dedicated pins relative to GND(3)		All temp. ranges	–0.5	V_{CCAUX} + 0.5	V

Table 30: **Power Voltage Ramp Time Requirements**

Symbol	Description	Device	Package	Min	Max	Units
T_{CCO}	V_{CCO} ramp time for all eight banks	All	All	No limit(4)	–	N/A
T_{CCINT}	V_{CCINT} ramp time, only if V_{CCINT} is last in three-rail power-on sequence	All	All	No limit	No limit(5)	N/A

Notes:

1. If a limit exists, this specification is based on characterization.
2. The ramp time is measured from 10% to 90% of the full nominal voltage swing for all I/O standards.
3. For information on power-on current needs, see Power-On Behavior, page 54
4. For mask revisions earlier than revision E (see Mask and Fab Revisions, page 58), T_{CCO} min is limited to 2.0 ms for the XC3S200 and XC3S400 devices in QFP packages, and limited to 0.6 ms for the XC3S200, XC3S400, XC3S1500, and XC3S4000 devices in the FT and FG packages.
5. For earlier device versions with the FQ fabrication/process code (see Mask and Fab Revisions, page 58), T_{CCINT} max is limited to 500 µs.

Table 31: **Power Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:

1. RAM contents include data stored in CMOS configuration latches.
2. The level of the V_{CCO} supply has no effect on data retention.
3. If a brown-out condition occurs where V_{CCAUX} or V_{CCINT} drops below the retention voltage, then V_{CCAUX} or V_{CCINT} must drop below the minimum power-on reset voltage indicated in Table 29 in order to clear out the device configuration content.

Table 32: **General Recommended Operating Conditions**

Symbol	Description		Min	Nom	Max	Units
T_J	Junction temperature	Commercial	0	25	85	°C
		Industrial	–40	25	100	°C
V_{CCINT}	Internal supply voltage		1.140	1.200	1.260	V
V_{CCO}(1)	Output driver supply voltage		1.140	–	3.465	V
V_{CCAUX}	Auxiliary supply voltage		2.375	2.500	2.625	V
ΔV_{CCAUX}(2)	Voltage variance on VCCAUX when using a DCM		–	–	10	mV/ms
V_{IN}(3)	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND(4)(6)	V_{CCO} = 3.3V, IO	–0.3	–	3.75	V
		V_{CCO} = 3.3V, IO_Lxxy(7)	–0.3	–	3.75	V
		$V_{CCO} \le$ 2.5V, IO	–0.3	–	V_{CCO} + 0.3(4)	V
		$V_{CCO} \le$ 2.5V, IO_Lxxy(7)	–0.3	–	V_{CCO} + 0.3(4)	V
	Voltage applied to all Dedicated pins relative to GND(5)		–0.3	–	V_{CCAUX} + 0.3(5)	V

Notes:

1. The V_{CCO} range given here spans the lowest and highest operating voltages of all supported I/O standards. The recommended V_{CCO} range specific to each of the single-ended I/O standards is given in Table 35, and that specific to the differential standards is given in Table 37.
2. Only during DCM operation is it recommended that the rate of change of V_{CCAUX} not exceed 10 mV/ms.
3. Input voltages outside the recommended range are permissible provided that the I_{IK} input diode clamp diode rating is met. Refer to Table 28.
4. Each of the User I/O and Dual-Purpose pins is associated with one of the V_{CCO} rails. Meeting the V_{IN} limit ensures that the internal diode junctions that exist between these pins and their associated V_{CCO} and GND rails do not turn on. The absolute maximum rating is provided in Table 28.
5. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} and GND rails do not turn on.
6. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Generation FPGAs*.
7. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.3V is supported but can cause increased leakage between the two pins. See the *Parasitic Leakage* section in UG331, *Spartan-3 Generation FPGA User Guide*.

Table 44: **Input Timing Adjustments for IOB *(Cont'd)***

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
LVCMOS15	0.42	0.49	ns
LVDCI_15	0.38	0.43	ns
LVDCI_DV2_15	0.38	0.44	ns
LVCMOS18	0.24	0.28	ns
LVDCI_18	0.29	0.33	ns
LVDCI_DV2_18	0.28	0.33	ns
LVCMOS25	0	0	ns
LVDCI_25	0.05	0.05	ns
LVDCI_DV2_25	0.04	0.04	ns
LVCMOS33, LVDCI_33, LVDCI_DV2_33	–0.05	–0.02	ns
LVTTL	0.18	0.21	ns
PCI33_3	0.20	0.22	ns
SSTL18_I, SSTL18_I_DCI	0.39	0.45	ns
SSTL18_II	0.39	0.45	ns
SSTL2_I, SSTL2_I_DCI	0.40	0.46	ns
SSTL2_II, SSTL2_II_DCI	0.36	0.41	ns
Differential Standards			
LDT_25 (ULVDS_25)	0.76	0.88	ns
LVDS_25, LVDS_25_DCI	0.65	0.75	ns
BLVDS_25	0.34	0.39	ns
LVDSEXT_25, LVDSEXT_25_DCI	0.80	0.92	ns
LVPECL_25	0.18	0.21	ns
RSDS_25	0.43	0.50	ns
DIFF_HSTL_II_18, DIFF_HSTL_II_18_DCI	0.34	0.39	ns
DIFF_SSTL2_II, DIFF_SSTL2_II_DCI	0.65	0.75	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32, Table 35, and Table 37.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
HSLVDCI_25			0.27	0.31	ns
HSLVDCI_33			0.28	0.32	ns
HSTL_I			0.60	0.69	ns
HSTL_I_DCI			0.59	0.68	ns
HSTL_III			0.19	0.22	ns
HSTL_III_DCI			0.20	0.23	ns
HSTL_I_18			0.18	0.21	ns
HSTL_I_DCI_18			0.17	0.19	ns
HSTL_II_18			–0.02	–0.01	ns
HSTL_II_DCI_18			0.75	0.86	ns
HSTL_III_18			0.28	0.32	ns
HSTL_III_DCI_18			0.28	0.32	ns
LVCMOS12	Slow	2 mA	7.60	8.73	ns
		4 mA	7.42	8.53	ns
		6 mA	6.67	7.67	ns
	Fast	2 mA	3.16	3.63	ns
		4 mA	2.70	3.10	ns
		6 mA	2.41	2.77	ns
LVCMOS15	Slow	2 mA	4.55	5.23	ns
		4 mA	3.76	4.32	ns
		6 mA	3.57	4.11	ns
		8 mA	3.55	4.09	ns
		12 mA	3.00	3.45	ns
	Fast	2 mA	3.11	3.57	ns
		4 mA	1.71	1.96	ns
		6 mA	1.44	1.66	ns
		8 mA	1.26	1.44	ns
		12 mA	1.11	1.27	ns
LVDCI_15			1.51	1.74	ns
LVDCI_DV2_15			1.32	1.52	ns

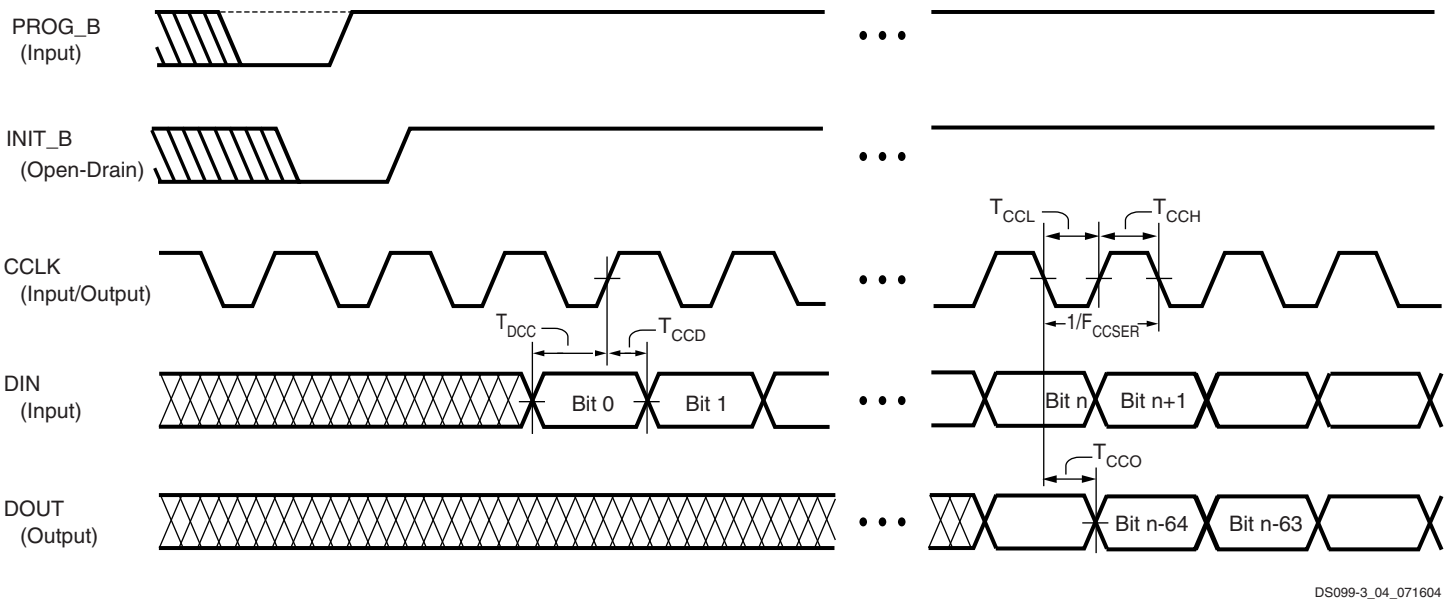

Figure 37: **Waveforms for Master and Slave Serial Configuration**

Table 66: **Timing for the Master and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	12.0	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		Both	10.0	–	ns
Hold Times						
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		Both	0	–	ns
Clock Timing						
T_{CCH}	CCLK input pin High pulse width		Slave	5.0	∞	ns
T_{CCL}	CCLK input pin Low pulse width			5.0	∞	ns
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression		0	66(2)	MHz
		With bitstream compression		0	20	MHz
		During STARTUP phase		0	50	MHz
ΔF_{CCSER}	Variation from the CCLK output frequency set using the ConfigRate BitGen option		Master	–50%	+50%	–

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

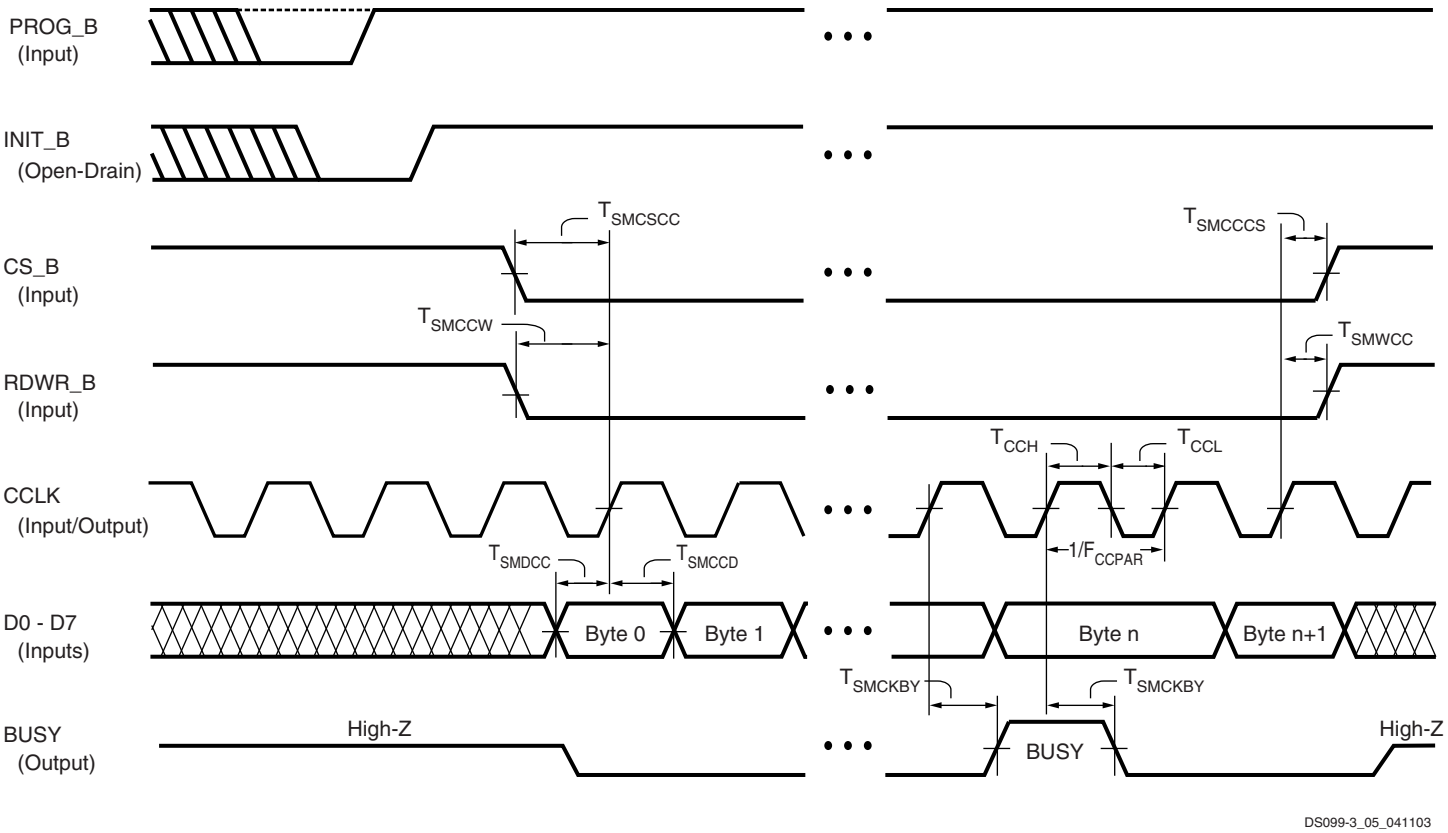

Figure 38: **Waveforms for Master and Slave Parallel Configuration**

Table 67: **Timing for the Master and Slave Parallel Configuration Modes**

Symbol	Description	Slave/ Master	All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin	Slave	–	12.0	ns
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	Both	10.0	–	ns
T_{SMCSCC}	The time from the setup of a logic level at the CS_B pin to the rising transition at the CCLK pin		10.0	–	ns
T_{SMCCW}(3)	The time from the setup of a logic level at the RDWR_B pin to the rising transition at the CCLK pin		10.0	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins	Both	0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CS_B pin		0	–	ns
T_{SMWCC}(3)	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns

Once the FPGA enters User mode after completing configuration, the DONE pin no longer drives the DONE pin Low. The bitstream generator option DonePin determines whether or not a pull-up resistor is present on the DONE pin to pull the pin to VCCAUX. If the pull-up resistor is eliminated, then the DONE pin must be pulled High using an external pull-up resistor or one of the FPGAs in the design must actively drive the DONE pin High via the DriveDone bitstream generator option.

The bitstream generator option DriveDone causes the FPGA to actively drive the DONE output High after configuration. This option should only be used in single-FPGA designs or on the last FPGA in a multi-FPGA daisy-chain.

By default, the bitstream generator software retains the pull-up resistor and does not actively drive the DONE pin as highlighted in Table 74, which shows the interaction of these bitstream options in single- and multi-FPGA designs.

Table 74: **DonePin and DriveDone Bitstream Option Interaction**

DonePin	DriveDone	Single- or Multi-FPGA Design	Comments
Pullnone	No	Single	External pull-up resistor, with value between 330Ω to 3.3kΩ, required on DONE.
Pullnone	No	Multi	External pull-up resistor, with value between 330Ω to 3.3kΩ, required on common node connecting to all DONE pins.
Pullnone	Yes	Single	OK, no external requirements.
Pullnone	Yes	Multi	DriveDone on last device in daisy-chain only. No external requirements.
Pullup	No	Single	OK, but pull-up on DONE pin has slow rise time. May require 330Ω pull-up resistor for high CCLK frequencies.
Pullup	No	Multi	External pull-up resistor, with value between 330Ω to 3.3kΩ, required on common node connecting to all DONE pins.
Pullup	Yes	Single	OK, no external requirements.
Pullup	Yes	Multi	DriveDone on last device in daisy-chain only. No external requirements.

M2, M1, M0: Configuration Mode Selection

The M2, M1, and M0 inputs select the FPGA configuration mode, as described in Table 75. The logic levels applied to the mode pins are sampled on the rising edge of INIT_B.

Table 75: **Spartan-3 FPGA Mode Select Settings**

Configuration Mode	M2	M1	M0
Master Serial	0	0	0
Slave Serial	1	1	1
Master Parallel	0	1	1
Slave Parallel	1	1	0
JTAG	1	0	1
Reserved	0	0	1
Reserved	0	1	0
Reserved	1	0	0
After Configuration	X	X	X

Notes:

1. X = don't care, either 0 or 1.

Before and during configuration, the mode pins have an internal pull-up resistor to VCCAUX, regardless of the HSWAP_EN pin. If the mode pins are unconnected, then the FPGA defaults to the Slave Serial configuration mode. After configuration successfully completes, any levels applied to these input are ignored. Furthermore, the bitstream generator options M0Pin, M1Pin, and M2Pin determines whether a pull-up resistor, pull-down resistor, or no resistor is present on its respective mode pin, M0, M1, or M2.

HSWAP_EN: Disable Pull-up Resistors During Configuration

As shown in Table 76, a Low on this asynchronous pin enables pull-up resistors on all user I/Os not actively involved in the configuration process, although only until device configuration completes. A High disables the pull-up resistors during configuration, which is the desired state for some applications.

The dedicated configuration CONFIG pins (CCLK, DONE, PROG_B, HSWAP_EN, M2, M1, M0), the JTAG pins (TDI, TMS, TCK, TDO) and the INIT_B always have active pull-up resistors during configuration, regardless of the value on HSWAP_EN.

After configuration, HSWAP_EN becomes a "don't care" input and any pull-up resistors previously enabled by HSWAP_EN are disabled. If a user I/O in the application requires a pull-up resistor after configuration, place a PULLUP primitive on the associated I/O pin or, for some pins, set the associated bitstream generator option.

Table 76: **HSWAP_EN Encoding**

HSWAP_EN	Function
During Configuration	
0	Enable pull-up resistors on all pins not actively involved in the configuration process. Pull-ups are only active until configuration completes. See Table 79.
1	No pull-up resistors during configuration.
After Configuration, User Mode	
X	This pin has no function except during device configuration.

Notes:

1. X = don't care, either 0 or 1.

The Bitstream generator option HswapenPin determines whether a pull-up resistor to VCCAUX, a pull-down resistor, or no resistor is present on HSWAP_EN after configuration.

JTAG: Dedicated JTAG Port Pins

Table 77: **JTAG Pin Descriptions**

Pin Name	Direction	Description	Bitstream Generation Option
TCK	Input	**Test Clock:** The TCK clock signal synchronizes all boundary scan operations on its rising edge.	The BitGen option **TckPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.
TDI	Input	**Test Data Input:** TDI is the serial data input for all JTAG instruction and data registers. This input is sampled on the rising edge of TCK.	The BitGen option **TdiPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.
TMS	Input	**Test Mode Select:** The TMS input controls the sequence of states through which the JTAG TAP state machine passes. This input is sampled on the rising edge of TCK.	The BitGen option **TmsPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.
TDO	Output	**Test Data Output:** The TDO pin is the data output for all JTAG instruction and data registers. This output is sampled on the rising edge of TCK. The TDO output is an active totem-pole driver and is not like the open-collector TDO output on Virtex®-II Pro FPGAs.	The BitGen option **TdoPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present.

These pins are dedicated connections to the four-wire IEEE 1532/IEEE 1149.1 JTAG port, shown in Figure 43 and described in Table 77. The JTAG port is used for boundary-scan testing, device configuration, application debugging, and possibly an additional serial port for the application. These pins are dedicated and are not available as user-I/O pins. Every package has four dedicated JTAG pins and these pins are powered by the +2.5V VCCAUX supply.

For additional information on JTAG configuration, see Boundary-Scan (JTAG) Mode, page 50.

VREF: User I/O or Input Buffer Reference Voltage for Special Interface Standards

These pins are individual user-I/O pins unless collectively they supply an input reference voltage, VREF_#, for any SSTL, HSTL, GTL, or GTLP I/Os implemented in the associated I/O bank. The '#' character in the pin name represents an integer, 0 through 7, that indicates the associated I/O bank.

The VREF function becomes active for this pin whenever a signal standard requiring a reference voltage is used in the associated bank. If used as a user I/O, then each pin behaves as an independent I/O described in the I/O type section. If used for a reference voltage within a bank, then *all* VREF pins within the bank must be connected to the same reference voltage.

Spartan-3 devices are designed and characterized to support certain I/O standards when VREF is connected to +1.25V, +1.10V, +1.00V, +0.90V, +0.80V, and +0.75V. During configuration, the VREF pins behave exactly like user-I/O pins.

If designing for footprint compatibility across the range of devices in a specific package, and if the VREF_# pins within a bank connect to an input reference voltage, then also connect any N.C. (not connected) pins on the smaller devices in that package to the input reference voltage. More details are provided later for each package type.

N.C. Type: Unconnected Package Pins

Pins marked as "N.C." are unconnected for the specific device/package combination. For other devices in this same package, this pin may be used as an I/O or VREF connection. In both the pinout tables and the footprint diagrams, unconnected pins are noted with either a black diamond symbol (◆) or a black square symbol (■).

If designing for footprint compatibility across multiple device densities, check the pin types of the other Spartan-3 devices available in the same footprint. If the N.C. pin matches to VREF pins in other devices, and the VREF pins are used in the associated I/O bank, then connect the N.C. to the VREF voltage source.

VCCO Type: Output Voltage Supply for I/O Bank

Each I/O bank has its own set of voltage supply pins that determines the output voltage for the output buffers in the I/O bank. Furthermore, for some I/O standards such as LVCMOS, LVCMOS25, LVTTL, etc., VCCO sets the input threshold voltage on the associated input buffers.

Spartan-3 devices are designed and characterized to support various I/O standards for VCCO values of +1.2V, +1.5V, +1.8V, +2.5V, and +3.3V.

Most VCCO pins are labeled as VCCO_# where the '#' symbol represents the associated I/O bank number, an integer ranging from 0 to 7. In the 144-pin TQFP package (TQ144) however, the VCCO pins along an edge of the device are combined into a single VCCO input. For example, the VCCO inputs for Bank 0 and Bank 1 along the top edge of the package are combined and relabeled VCCO_TOP. The bottom, left, and right edges are similarly combined.

In Serial configuration mode, VCCO_4 must be at a level compatible with the attached configuration memory or data source. In Parallel configuration mode, both VCCO_4 and VCCO_5 must be at the same compatible voltage level.

All VCCO inputs to a bank must be connected together and to the voltage supply. Furthermore, there must be sufficient supply decoupling to guarantee problem-free operation, as described in XAPP623: *Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors*.

VCCINT Type: Voltage Supply for Internal Core Logic

Internal core logic circuits such as the configurable logic blocks (CLBs) and programmable interconnect operate from the VCCINT voltage supply inputs. VCCINT must be +1.2V.

All VCCINT inputs must be connected together and to the +1.2V voltage supply. Furthermore, there must be sufficient supply decoupling to guarantee problem-free operation, as described in XAPP623.

VCCAUX Type: Voltage Supply for Auxiliary Logic

The VCCAUX pins supply power to various auxiliary circuits, such as to the Digital Clock Managers (DCMs), the JTAG pins, and to the dedicated configuration pins (CONFIG type). VCCAUX must be +2.5V.

Table 93: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
7	IO_L21N_7	IO_L21N_7	P13	I/O
7	IO_L21P_7	IO_L21P_7	P12	I/O
7	IO_L22N_7	IO_L22N_7	P16	I/O
7	IO_L22P_7	IO_L22P_7	P15	I/O
7	IO_L23N_7	IO_L23N_7	P19	I/O
7	IO_L23P_7	IO_L23P_7	P18	I/O
7	IO_L24N_7	IO_L24N_7	P21	I/O
7	IO_L24P_7	IO_L24P_7	P20	I/O
7	N.C. (◆)	IO_L39N_7	P24	I/O
7	N.C. (◆)	IO_L39P_7	P22	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	P27	VREF
7	IO_L40P_7	IO_L40P_7	P26	I/O
7	VCCO_7	VCCO_7	P6	VCCO
7	VCCO_7	VCCO_7	P23	VCCO
N/A	GND	GND	P1	GND
N/A	GND	GND	P186	GND
N/A	GND	GND	P195	GND
N/A	GND	GND	P202	GND
N/A	GND	GND	P163	GND
N/A	GND	GND	P170	GND
N/A	GND	GND	P179	GND
N/A	GND	GND	P134	GND
N/A	GND	GND	P145	GND
N/A	GND	GND	P151	GND
N/A	GND	GND	P157	GND
N/A	GND	GND	P112	GND
N/A	GND	GND	P118	GND
N/A	GND	GND	P129	GND
N/A	GND	GND	P82	GND
N/A	GND	GND	P91	GND
N/A	GND	GND	P99	GND
N/A	GND	GND	P105	GND
N/A	GND	GND	P53	GND
N/A	GND	GND	P59	GND
N/A	GND	GND	P66	GND
N/A	GND	GND	P75	GND
N/A	GND	GND	P30	GND
N/A	GND	GND	P41	GND
N/A	GND	GND	P47	GND
N/A	GND	GND	P8	GND

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
1	IO_L10N_1/VREF_1	A13	VREF
1	IO_L10P_1	B13	I/O
1	IO_L27N_1	B12	I/O
1	IO_L27P_1	C12	I/O
1	IO_L28N_1	D11	I/O
1	IO_L28P_1	E11	I/O
1	IO_L29N_1	B11	I/O
1	IO_L29P_1	C11	I/O
1	IO_L30N_1	D10	I/O
1	IO_L30P_1	E10	I/O
1	IO_L31N_1/VREF_1	A10	VREF
1	IO_L31P_1	B10	I/O
1	IO_L32N_1/GCLK5	C9	GCLK
1	IO_L32P_1/GCLK4	D9	GCLK
1	VCCO_1	E9	VCCO
1	VCCO_1	F9	VCCO
1	VCCO_1	F10	VCCO
2	IO	G16	I/O
2	IO_L01N_2/VRP_2	B16	DCI
2	IO_L01P_2/VRN_2	C16	DCI
2	IO_L16N_2	C15	I/O
2	IO_L16P_2	D14	I/O
2	IO_L17N_2	D15	I/O
2	IO_L17P_2/VREF_2	D16	VREF
2	IO_L19N_2	E13	I/O
2	IO_L19P_2	E14	I/O
2	IO_L20N_2	E15	I/O
2	IO_L20P_2	E16	I/O
2	IO_L21N_2	F12	I/O
2	IO_L21P_2	F13	I/O
2	IO_L22N_2	F14	I/O
2	IO_L22P_2	F15	I/O
2	IO_L23N_2/VREF_2	G12	VREF
2	IO_L23P_2	G13	I/O
2	IO_L24N_2	G14	I/O
2	IO_L24P_2	G15	I/O
2	IO_L39N_2	H13	I/O
2	IO_L39P_2	H14	I/O
2	IO_L40N_2	H15	I/O
2	IO_L40P_2/VREF_2	H16	VREF

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
7	IO_L24P_7	G4	I/O
7	IO_L39N_7	H3	I/O
7	IO_L39P_7	H4	I/O
7	IO_L40N_7/VREF_7	H1	VREF
7	IO_L40P_7	G1	I/O
7	VCCO_7	G6	VCCO
7	VCCO_7	H5	VCCO
7	VCCO_7	H6	VCCO
N/A	GND	A1	GND
N/A	GND	A16	GND
N/A	GND	B2	GND
N/A	GND	B9	GND
N/A	GND	B15	GND
N/A	GND	F6	GND
N/A	GND	F11	GND
N/A	GND	G7	GND
N/A	GND	G8	GND
N/A	GND	G9	GND
N/A	GND	G10	GND
N/A	GND	H2	GND
N/A	GND	H7	GND
N/A	GND	H8	GND
N/A	GND	H9	GND
N/A	GND	H10	GND
N/A	GND	J7	GND
N/A	GND	J8	GND
N/A	GND	J9	GND
N/A	GND	J10	GND
N/A	GND	J15	GND
N/A	GND	K7	GND
N/A	GND	K8	GND
N/A	GND	K9	GND
N/A	GND	K10	GND
N/A	GND	L6	GND
N/A	GND	L11	GND
N/A	GND	R2	GND
N/A	GND	R8	GND
N/A	GND	R15	GND
N/A	GND	T1	GND

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
0	VCCO_0	G9	VCCO
1	IO	A11	I/O
1	IO	B13	I/O
1	IO	D10	I/O
1	IO/VREF_1	A12	VREF
1	IO_L01N_1/VRP_1	A16	DCI
1	IO_L01P_1/VRN_1	A17	DCI
1	IO_L10N_1/VREF_1	A15	VREF
1	IO_L10P_1	B15	I/O
1	IO_L15N_1	C14	I/O
1	IO_L15P_1	C15	I/O
1	IO_L16N_1	A14	I/O
1	IO_L16P_1	B14	I/O
1	IO_L24N_1	D14	I/O
1	IO_L24P_1	D13	I/O
1	IO_L27N_1	E13	I/O
1	IO_L27P_1	E12	I/O
1	IO_L28N_1	C12	I/O
1	IO_L28P_1	D12	I/O
1	IO_L29N_1	F11	I/O
1	IO_L29P_1	E11	I/O
1	IO_L30N_1	C11	I/O
1	IO_L30P_1	D11	I/O
1	IO_L31N_1/VREF_1	A10	VREF
1	IO_L31P_1	B10	I/O
1	IO_L32N_1/GCLK5	E10	GCLK
1	IO_L32P_1/GCLK4	F10	GCLK
1	VCCO_1	B11	VCCO
1	VCCO_1	C13	VCCO
1	VCCO_1	G10	VCCO
1	VCCO_1	G11	VCCO
2	IO	J13	I/O
2	IO_L01N_2/VRP_2	C16	DCI
2	IO_L01P_2/VRN_2	C17	DCI
2	IO_L16N_2	B18	I/O
2	IO_L16P_2	C18	I/O
2	IO_L17N_2	D17	I/O
2	IO_L17P_2/VREF_2	D18	VREF
2	IO_L19N_2	D16	I/O
2	IO_L19P_2	E16	I/O

User I/Os by Bank

Table 101 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S400 in the FG456 package. Similarly, Table 102 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1000, XC3S1500, and XC3S2000 in the FG456 package.

Table 101: **User I/Os Per Bank for XC3S400 in FG456 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	35	27	0	2	4	2
	1	35	27	0	2	4	2
Right	2	31	25	0	2	4	0
	3	31	25	0	2	4	0
Bottom	4	35	21	6	2	4	2
	5	35	21	6	2	4	2
Left	6	31	25	0	2	4	0
	7	31	25	0	2	4	0

Table 102: **User I/Os Per Bank for XC3S1000, XC3S1500, and XC3S2000 in FG456 Package**

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	40	31	0	2	5	2
	1	40	31	0	2	5	2
Right	2	43	37	0	2	4	0
	3	43	37	0	2	4	0
Bottom	4	41	26	6	2	5	2
	5	40	25	6	2	5	2
Left	6	43	37	0	2	4	0
	7	43	37	0	2	4	0

FG676: 676-lead Fine-pitch Ball Grid Array

The 676-lead fine-pitch ball grid array package, FG676, supports five different Spartan-3 devices, including the XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000. All five have nearly identical footprints but are slightly different, primarily due to unconnected pins on the XC3S1000 and XC3S1500. For example, because the XC3S1000 has fewer I/O pins, this device has 98 unconnected pins on the FG676 package, labeled as "N.C." In Table 103 and Figure 53, these unconnected pins are indicated with a black diamond symbol (◆). The XC3S1500, however, has only two unconnected pins, also labeled "N.C." in the pinout table but indicated with a black square symbol (■).

All the package pins appear in Table 103 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000 pinouts, then that difference is highlighted in Table 103. If the table entry is shaded grey, then there is an unconnected pin on either the XC3S1000 or XC3S1500 that maps to a user-I/O pin on the XC3S2000, XC3S4000, and XC3S5000. If the table entry is shaded tan, then the unconnected pin on either the XC3S1000 or XC3S1500 maps to a VREF-type pin on the XC3S2000, XC3S4000, and XC3S5000. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S1000 or XC3S1500 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S1000 through to the XC3S5000 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 103: **FG676 Package Pinout**

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
0	IO	IO	IO	IO	IO_L04N_0(3)	A3	I/O
0	IO	IO	IO	IO	IO	A5	I/O
0	IO	IO	IO	IO	IO	A6	I/O
0	IO	IO	IO	IO	IO_L04P_0(3)	C4	I/O
0	N.C. (◆)	IO	IO	IO	IO_L13N_0(3)	C8	I/O
0	IO	IO	IO	IO	IO	C12	I/O
0	IO	IO	IO	IO	IO	E13	I/O
0	IO	IO	IO	IO	IO	H11	I/O
0	IO	IO	IO	IO	IO	H12	I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	B3	VREF
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	F7	VREF
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	IO/VREF_0	G10	VREF
0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	IO_L01N_0/VRP_0	E5	DCI
0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	IO_L01P_0/VRN_0	D5	DCI
0	IO_L05N_0	IO_L05N_0	IO_L05N_0	IO_L05N_0	IO_L05N_0	B4	I/O
0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	IO_L05P_0/VREF_0	A4	VREF
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	IO_L06N_0	IO_L06N_0	C5	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	IO_L06P_0	IO_L06P_0	B5	I/O
0	IO_L07N_0	IO_L07N_0	IO_L07N_0	IO_L07N_0	IO_L07N_0	E6	I/O
0	IO_L07P_0	IO_L07P_0	IO_L07P_0	IO_L07P_0	IO_L07P_0	D6	I/O
0	IO_L08N_0	IO_L08N_0	IO_L08N_0	IO_L08N_0	IO_L08N_0	C6	I/O
0	IO_L08P_0	IO_L08P_0	IO_L08P_0	IO_L08P_0	IO_L08P_0	B6	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
5	IO_L07N_5	IO_L07N_5	AK8	I/O
5	IO_L07P_5	IO_L07P_5	AJ8	I/O
5	IO_L08N_5	IO_L08N_5	AC9	I/O
5	IO_L08P_5	IO_L08P_5	AB9	I/O
5	IO_L09N_5	IO_L09N_5	AG9	I/O
5	IO_L09P_5	IO_L09P_5	AF9	I/O
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	AK9	DCI
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	AJ9	DCI
5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	AE10	VREF
5	IO_L11P_5	IO_L11P_5	AE9	I/O
5	IO_L12N_5	IO_L12N_5	AJ10	I/O
5	IO_L12P_5	IO_L12P_5	AH10	I/O
5	IO_L13N_5	IO_L13N_5	AD11	I/O
5	IO_L13P_5	IO_L13P_5	AD10	I/O
5	IO_L14N_5	IO_L14N_5	AF11	I/O
5	IO_L14P_5	IO_L14P_5	AE11	I/O
5	IO_L15N_5	IO_L15N_5	AH11	I/O
5	IO_L15P_5	IO_L15P_5	AG11	I/O
5	IO_L16N_5	IO_L16N_5	AK11	I/O
5	IO_L16P_5	IO_L16P_5	AJ11	I/O
5	IO_L17N_5	IO_L17N_5	AB12	I/O
5	IO_L17P_5	IO_L17P_5	AC11	I/O
5	IO_L18N_5	IO_L18N_5	AD12	I/O
5	IO_L18P_5	IO_L18P_5	AC12	I/O
5	IO_L19N_5	IO_L19N_5	AF12	I/O
5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	AE12	VREF
5	IO_L20N_5	IO_L20N_5	AH12	I/O
5	IO_L20P_5	IO_L20P_5	AG12	I/O
5	IO_L21N_5	IO_L21N_5	AK12	I/O
5	IO_L21P_5	IO_L21P_5	AJ12	I/O
5	IO_L22N_5	IO_L22N_5	AA13	I/O
5	IO_L22P_5	IO_L22P_5	AA12	I/O
5	IO_L23N_5	IO_L23N_5	AC13	I/O
5	IO_L23P_5	IO_L23P_5	AB13	I/O
5	IO_L24N_5	IO_L24N_5	AG13	I/O
5	IO_L24P_5	IO_L24P_5	AF13	I/O
5	IO_L25N_5	IO_L25N_5	AK13	I/O
5	IO_L25P_5	IO_L25P_5	AJ13	I/O
5	IO_L26N_5	IO_L26N_5	AB14	I/O
5	IO_L26P_5	IO_L26P_5	AA14	I/O