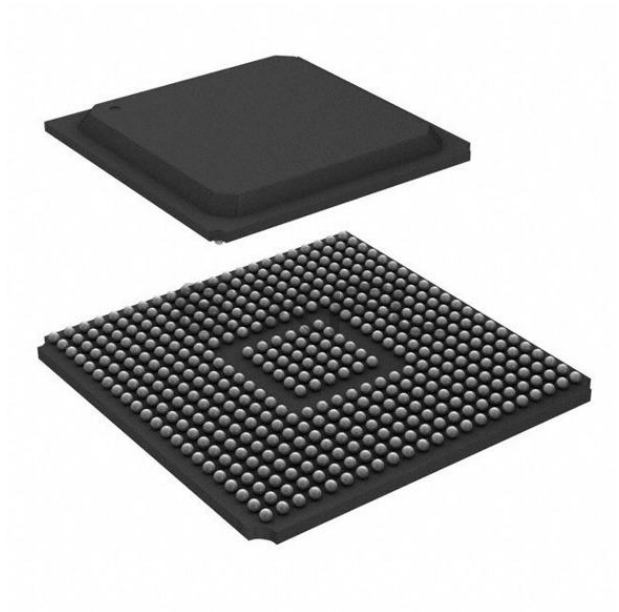
# AMD Xilinx - XC3S400-4FG456C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 896 |
| Number of Logic Elements/Cells | 8064 |
| Total RAM Bits | 294912 |
| Number of I/O | 264 |
| Number of Gates | 400000 |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 456-BBGA |
| Supplier Device Package | 456-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc3s400-4fg456c |

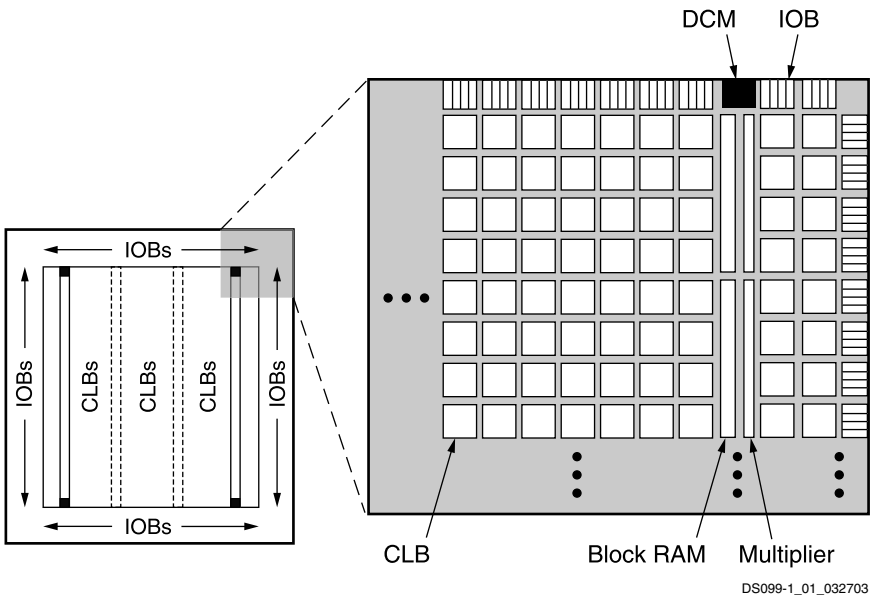
## Architectural Overview

The Spartan-3 family architecture consists of five fundamental programmable functional elements:

- Configurable Logic Blocks (CLBs) contain RAM-based Look-Up Tables (LUTs) to implement logic and storage elements that can be used as flip-flops or latches. CLBs can be programmed to perform a wide variety of logical functions as well as to store data.
- Input/Output Blocks (IOBs) control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Twenty-six different signal standards, including eight high-performance differential standards, are available as shown in Table 2. Double Data-Rate (DDR) registers are included. The Digitally Controlled Impedance (DCI) feature provides automatic on-chip terminations, simplifying board designs.
- Block RAM provides data storage in the form of 18-Kbit dual-port blocks.
- Multiplier blocks accept two 18-bit binary numbers as inputs and calculate the product.
- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. The XC3S50 has a single column of block RAM embedded in the array. Those devices ranging from the XC3S200 to the XC3S2000 have two columns of block RAM. The XC3S4000 and XC3S5000 devices have four RAM columns. Each column is made up of several 18-Kbit RAM blocks; each block is associated with a dedicated multiplier. The DCMs are positioned at the ends of the outer block RAM columns.

The Spartan-3 family features a rich network of traces and switches that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.




**Notes:**

1. The two additional block RAM columns of the XC3S4000 and XC3S5000 devices are shown with dashed lines. The XC3S50 has only the block RAM column on the far left.

*Figure 1:* **Spartan-3 Family Architecture**

## Configuration

Spartan-3 FPGAs are programmed by loading configuration data into robust reprogrammable static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. Before powering on the FPGA, configuration data is stored externally in a PROM or some other nonvolatile medium either on or off the board. After applying

Table 3 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

*Table 3:* **Spartan-3 Device I/O Chart**

| Available User I/Os and Differential (Diff) I/O Pairs by Package Type | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Package** | **VQ100 VQG100** | | **CP132(1) CPG132** | | **TQ144 TQG144** | | **PQ208 PQG208** | | **FT256 FTG256** | | **FG320 FGG320** | | **FG456 FGG456** | | **FG676 FGG676** | | **FG900 FGG900** | | **FG1156(1) FGG1156** | |
| **Footprint (mm)** | **16 x 16** | | **8 x 8** | | **22 x 22** | | **30.6 x 30.6** | | **17 x 17** | | **19 x 19** | | **23 x 23** | | **27 x 27** | | **31 x 31** | | **35 x 35** | |
| **Device** | **User** | **Diff** | **User** | **Diff** | **User** | **Diff** | **User** | **Diff** | **User** | **Diff** | **User** | **Diff** | **User** | **Diff** | **User** | **Diff** | **User** | **Diff** | **User** | **Diff** |
| XC3S50 | 63 | 29 | 89(1) | 44(1) | 97 | 46 | 124 | 56 | – | – | – | – | – | – | – | – | – | – | – | – |
| XC3S200 | 63 | 29 | – | – | 97 | 46 | 141 | 62 | 173 | 76 | – | – | – | – | – | – | – | – | – | – |
| XC3S400 | – | – | – | – | 97 | 46 | 141 | 62 | 173 | 76 | 221 | 100 | 264 | 116 | – | – | – | – | – | – |
| XC3S1000 | – | – | – | – | – | – | – | – | 173 | 76 | 221 | 100 | 333 | 149 | 391 | 175 | – | – | – | – |
| XC3S1500 | – | – | – | – | – | – | – | – | – | – | 221 | 100 | 333 | 149 | 487 | 221 | – | – | – | – |
| XC3S2000 | – | – | – | – | – | – | – | – | – | – | – | – | 333 | 149 | 489 | 221 | 565 | 270 | – | – |
| XC3S4000 | – | – | – | – | – | – | – | – | – | – | – | – | – | – | 489 | 221 | 633 | 300 | 712(1) | 312(1) |
| XC3S5000 | – | – | – | – | – | – | – | – | – | – | – | – | – | – | 489 | 221 | 633 | 300 | 784(1) | 344(1) |

**Notes:**

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.
2. All device options listed in a given package column are pin-compatible.
3. User = Single-ended user I/O pins. Diff = Differential I/O pairs.

## Package Marking

Figure 2 shows the top marking for Spartan-3 FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3 FPGAs in BGA packages except the 132-ball chip-scale package (CP132 and CPG132). The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for Spartan-3 FPGAs in the CP132 and CPG132 packages.

The "5C" and "4I" part combinations may be dual marked as "5C/4I". Devices with the dual mark can be used as either -5C or -4I devices. Devices with a single mark are only guaranteed for the marked speed grade and temperature range. Some specifications vary according to mask revision. Mask revision E devices are errata-free. All shipments since 2006 have been mask revision E.

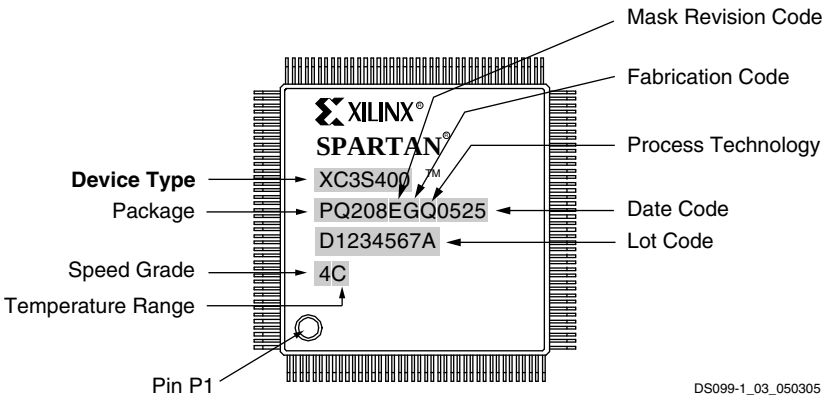



*Figure 2:* **Spartan-3 FPGA QFP Package Marking Example for Part Number XC3S400-4PQ208C**

## Function Generator

Each of the two LUTs (F and G) in a slice have four logic inputs (A1-A4) and a single output (D). This permits any four-variable Boolean logic operation to be programmed into them. Furthermore, wide function multiplexers can be used to effectively combine LUTs within the same CLB or across different CLBs, making logic functions with still more input variables possible.

The LUTs in both the right-hand and left-hand slice-pairs not only support the logic functions described above, but also can function as ROM that is initialized with data at the time of configuration.

The LUTs in the left-hand slice-pair (even-numbered columns such as X0 in Figure 11) of each CLB support two additional functions that the right-hand slice-pair (odd-numbered columns such as X1) do not.

First, it is possible to program the “left-hand LUTs” as distributed RAM. This type of memory affords moderate amounts of data buffering anywhere along a data path. One left-hand LUT stores 16 bits. Multiple left-hand LUTs can be combined in various ways to store larger amounts of data. A dual port option combines two LUTs so that memory access is possible from two independent data lines. A Distributed ROM option permits pre-loading the memory with data during FPGA configuration.

Second, it is possible to program each left-hand LUT as a 16-bit shift register. Used in this way, each LUT can delay serial data anywhere from one to 16 clock cycles. The four left-hand LUTs of a single CLB can be combined to produce delays up to 64 clock cycles. The SHIFTIN and SHIFTOUT lines cascade LUTs to form larger shift registers. It is also possible to combine shift registers across more than one CLB. The resulting programmable delays can be used to balance the timing of data pipelines.

# Block RAM Overview

All Spartan-3 devices support block RAM, which is organized as configurable, synchronous 18Kbit blocks. Block RAM stores relatively large amounts of data more efficiently than the distributed RAM feature described earlier. (The latter is better suited for buffering small amounts of data anywhere along signal paths.) This section describes basic Block RAM functions. For more information, refer to the chapter entitled “Using Block RAM” in UG331.

The aspect ratio—i.e., width vs. depth—of each block RAM is configurable. Furthermore, multiple blocks can be cascaded to create still wider and/or deeper memories.

A choice among primitives determines whether the block RAM functions as dual- or single-port memory. A name of the form RAMB16_S[$w_A$]_S[$w_B$] calls out the dual-port primitive, where the integers $w_A$ and $w_B$ specify the total data path width at ports $w_A$ and $w_B$, respectively. Thus, a RAMB16_S9_S18 is a dual-port RAM with a 9-bit-wide Port A and an 18-bit-wide Port B. A name of the form RAMB16_S[w] identifies the single-port primitive, where the integer w specifies the total data path width of the lone port. A RAMB16_S18 is a single-port RAM with an 18-bit-wide port. Other memory functions—e.g., FIFOs, data path width conversion, ROM, etc.—are readily available using the CORE Generator™ software, part of the Xilinx development software.

- **Phase Shifting:** The DCM provides the ability to shift the phase of all its output clock signals with respect to its input clock signal.

The DCM has four functional components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), the Phase Shifter (PS), and the Status Logic. Each component has its associated signals, as shown in Figure 19.

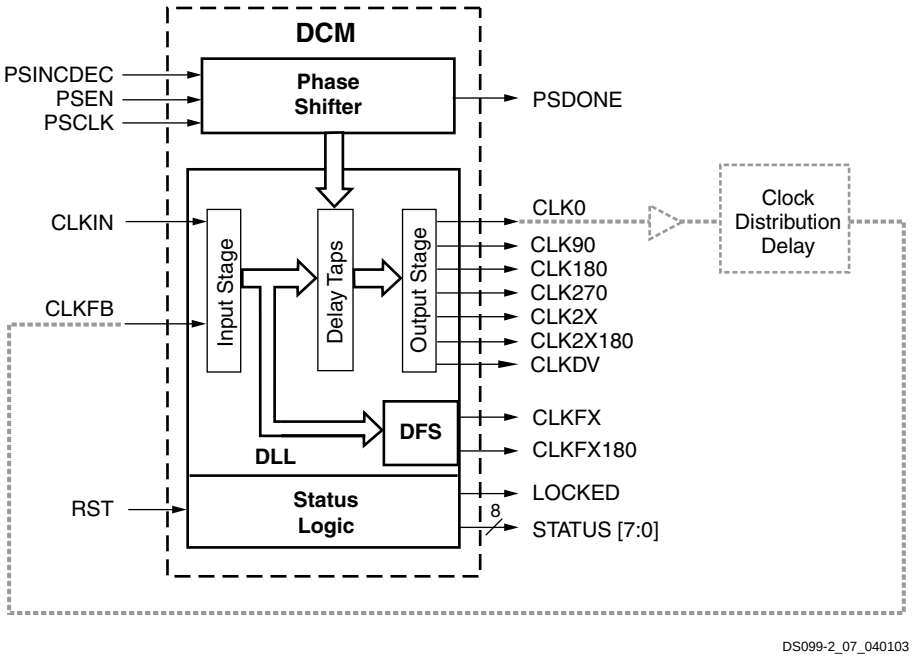



*Figure 19:* **DCM Functional Blocks and Associated Signals**

## Delay-Locked Loop (DLL)

The most basic function of the DLL component is to eliminate clock skew. The main signal path of the DLL consists of an input stage, followed by a series of discrete delay elements or *taps,* which in turn leads to an output stage. This path together with logic for phase detection and control forms a system complete with feedback as shown in Figure 20.

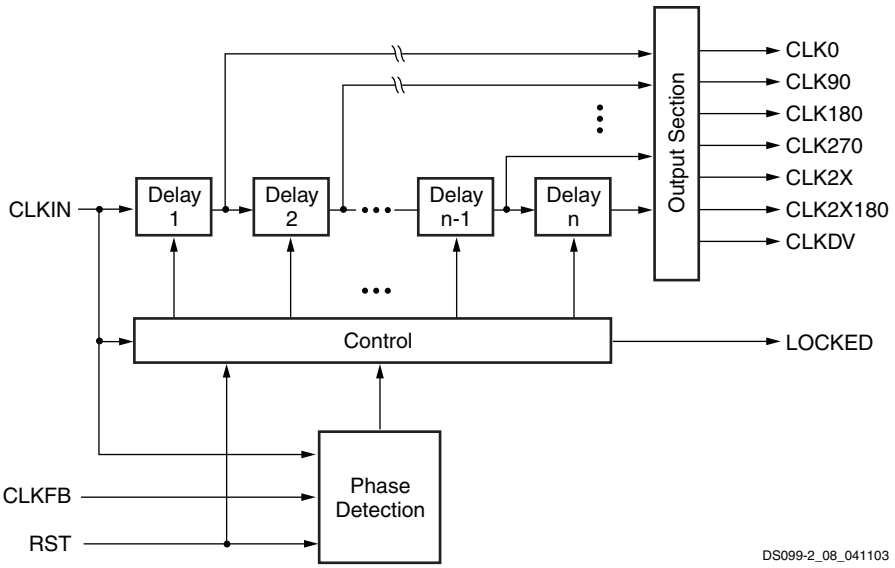



*Figure 20:* **Simplified Functional Diagram of DLL**

The output frequency ($f_{CLKFX}$) can be expressed as a function of the incoming clock frequency ($f_{CLKIN}$) as follows:

$$f_{CLKFX} = f_{CLKIN}(CLKFX\_MULTIPLY/CLKFX\_DIVIDE) \quad \textit{Equation 3}$$

Regarding the two attributes, it is possible to assign any combination of integer values, provided that two conditions are met:

- The two values fall within their corresponding ranges, as specified in Table 18.
- The $f_{CLKFX}$ frequency calculated from the above expression accords with the DCM's operating frequency specifications.

For example, if CLKFX_MULTIPLY = 5 and CLKFX_DIVIDE = 3, then the frequency of the output clock signal would be 5/3 that of the input clock signal.

### DFS Frequency Modes

The DFS supports two operating modes, High Frequency and Low Frequency, with each specified over a different clock frequency range. The DFS_FREQUENCY_MODE attribute chooses between the two modes. When the attribute is set to LOW, the Low Frequency mode permits the two DFS outputs to operate over a low-to-moderate frequency range. When the attribute is set to HIGH, the High Frequency mode allows both these outputs to operate at the highest possible frequencies.

### DFS With or Without the DLL

The DFS component can be used with or without the DLL component:

Without the DLL, the DFS component multiplies or divides the CLKIN signal frequency according to the respective CLKFX_MULTIPLY and CLKFX_DIVIDE values, generating a clock with the new target frequency on the CLKFX and CLKFX180 outputs. Though classified as belonging to the DLL component, the CLKIN input is shared with the DFS component. This case does not employ feedback loop; therefore, it cannot correct for clock distribution delay.

With the DLL, the DFS operates as described in the preceding case, only with the additional benefit of eliminating the clock distribution delay. In this case, a feedback loop from the CLK0 output to the CLKFB input must be present.

The DLL and DFS components work together to achieve this phase correction as follows: Given values for the CLKFX_MULTIPLY and CLKFX_DIVIDE attributes, the DLL selects the delay element for which the output clock edge coincides with the input clock edge whenever mathematically possible. For example, when CLKFX_MULTIPLY = 5 and CLKFX_DIVIDE = 3, the input and output clock edges will coincide every three input periods, which is equivalent in time to five output periods.

Smaller CLKFX_MULTIPLY and CLKFX_DIVIDE values achieve faster lock times. With no factors common to the two attributes, alignment will occur once with every number of cycles equal to the CLKFX_DIVIDE value. Therefore, it is recommended that the user reduce these values by factoring wherever possible. For example, given CLKFX_MULTIPLY = 9 and CLKFX_DIVIDE = 6, removing a factor of three yields CLKFX_MULTIPLY = 3 and CLKFX_DIVIDE = 2. While both value-pairs will result in the multiplication of clock frequency by 3/2, the latter value-pair will enable the DLL to lock more quickly.

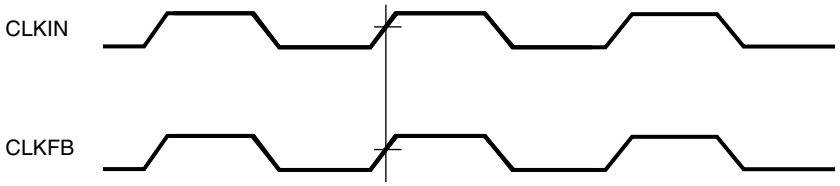
*Table 18:* **DFS Attributes**

| Attribute | Description | Values |
|---|---|---|
| DFS_FREQUENCY_MODE | Chooses between High Frequency and Low Frequency modes | Low, High |
| CLKFX_MULTIPLY | Frequency multiplier constant | Integer from 2 to 32 |
| CLKFX_DIVIDE | Frequency divisor constant | Integer from 1 to 32 |

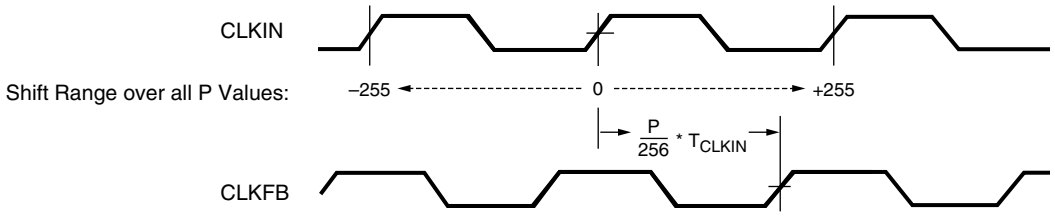
*Table 19:* **DFS Signals**

| Signal | Direction | Description |
|---|---|---|
| CLKFX | Output | Multiplies the CLKIN frequency by the attribute-value ratio (CLKFX_MULTIPLY/CLKFX_DIVIDE) to generate a clock signal with a new target frequency. |
| CLKFX180 | Output | Generates a clock signal with same frequency as CLKFX, only shifted 180° out-of-phase. |

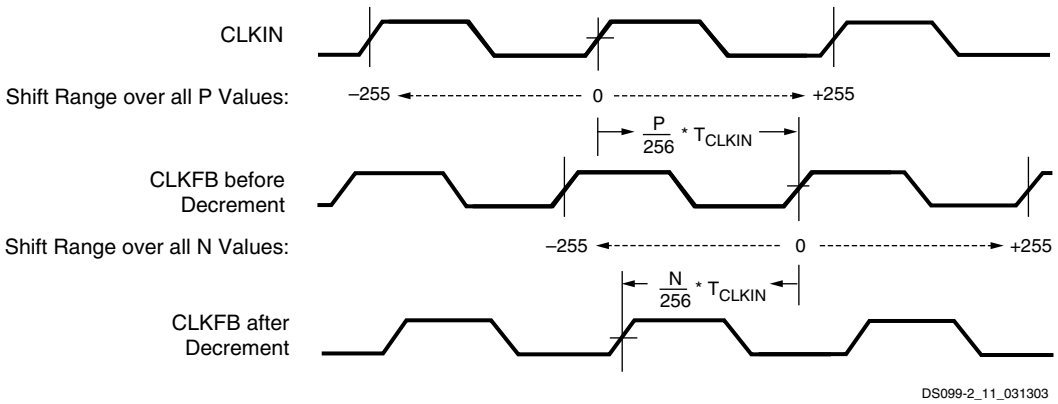
**a. CLKOUT_PHASE_SHIFT = NONE**




**b. CLKOUT_PHASE_SHIFT = FIXED**




**c. CLKOUT_PHASE_SHIFT = VARIABLE**




**Notes:**

1. P represents the integer value ranging from –255 to +255 to which the PHASE_SHIFT attribute is assigned.
2. N is an integer value ranging from –255 to +255 that represents the net phase shift effect from a series of increment and/or decrement operations.
   N = {Total number of increments} – {Total number of decrements}
   A positive value for N indicates a net increment; a negative value indicates a net decrement.

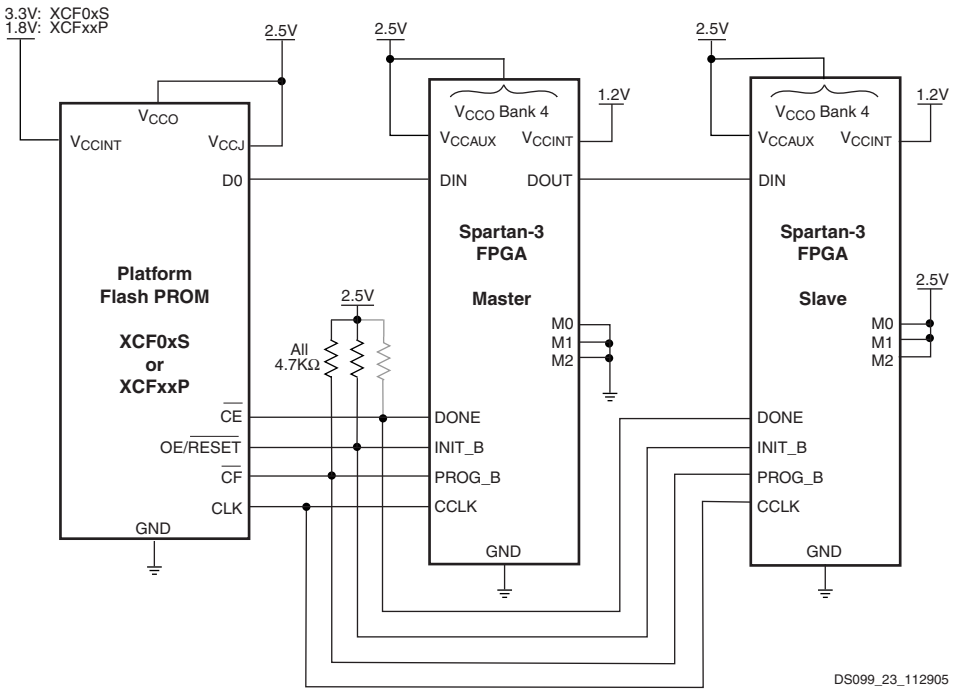
*Figure 23:* **Phase Shifter Waveforms**

## The Status Logic Component

The Status Logic component not only reports on the state of the DCM but also provides a means of resetting the DCM to an initial known state. The signals associated with the Status Logic component are described in Table 22.

As a rule, the Reset (RST) input is asserted only upon configuring the device or changing the CLKIN frequency. A DCM reset does not affect attribute values (e.g., CLKFX_MULTIPLY and CLKFX_DIVIDE). If not used, RST must be tied to GND.

The eight bits of the STATUS bus are defined in Table 23.




**Notes:**

1. There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.
2. For information on how to program the FPGA using 3.3V signals and power, see 3.3V-Tolerant Configuration Interface.

*Figure 26:* **Connection Diagram for Master and Slave Serial Configuration**

Slave Serial mode is selected by applying <111> to the mode pins (M0, M1, and M2). A pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

### Master Serial Mode

In Master Serial mode, the FPGA drives CCLK pin, which behaves as a bidirectional I/O pin. The FPGA in the center of Figure 26 is set for Master Serial mode and connects to the serial configuration PROM and to the CCLK inputs of any slave FPGAs in a configuration daisy-chain. The master FPGA drives the configuration clock on the CCLK pin to the Xilinx Serial PROM, which, in response, provides bit-serial data to the FPGA's DIN input. The FPGA accepts this data on each rising CCLK edge. After the master FPGA finishes configuring, it passes data on its DOUT pin to the next FPGA device in a daisy-chain. The DOUT data appears after the falling CCLK clock edge.

The Master Serial mode interface is identical to Slave Serial except that an internal oscillator generates the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK, which always starts at a default frequency of 6 MHz. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

### Slave Parallel Mode (SelectMAP)

The Parallel or SelectMAP modes support the fastest configuration. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data. An external source provides 8-bit-wide data, CCLK, an active-Low Chip Select (CS_B) signal and an active-Low Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the Slave Parallel mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, it is possible to use any of the Multipurpose pins (DIN/D0-D7, DOUT/BUSY, INIT_B, CS_B, and RDWR_B) as User I/Os. To do this, simply set the BitGen option *Persist* to *No* and assign the desired signals to multipurpose configuration pins using the Xilinx development software. Alternatively, it is possible to continue using the configuration port

*Table 45:* **Timing for the IOB Output Path**

| Symbol | Description | Conditions | Device | Speed Grade | | Units |
|---|---|---|---|---|---|---|
| | | | | -5 | -4 | |
| | | | | Max[3] | Max[3] | |
| **Clock-to-Output Times** | | | | | | |
| $T_{IOCKP}$ | When reading from the Output Flip-Flop (OFF), the time from the active transition at the OTCLK input to data appearing at the Output pin | LVCMOS25[2], 12 mA output drive, Fast slew rate | XC3S200<br>XC3S400 | 1.28 | 1.47 | ns |
| | | | XC3S50<br>XC3S1000<br>XC3S1500<br>XC3S2000<br>XC3S4000<br>XC3S5000 | 1.95 | 2.24 | ns |
| **Propagation Times** | | | | | | |
| $T_{IOOP}$ | The time it takes for data to travel from the IOB's O input to the Output pin | LVCMOS25[2], 12 mA output drive, Fast slew rate | XC3S200<br>XC3S400 | 1.28 | 1.46 | ns |
| | | | XC3S50<br>XC3S1000<br>XC3S1500<br>XC3S2000<br>XC3S4000<br>XC3S5000 | 1.94 | 2.23 | ns |
| $T_{IOOLP}$ | The time it takes for data to travel from the O input through the OFF latch to the Output pin | | XC3S200<br>XC3S400 | 1.28 | 1.47 | ns |
| | | | XC3S50<br>XC3S1000<br>XC3S1500<br>XC3S2000<br>XC3S4000<br>XC3S5000 | 1.95 | 2.24 | ns |
| **Set/Reset Times** | | | | | | |
| $T_{IOSRP}$ | Time from asserting the OFF's SR input to setting/resetting data at the Output pin | LVCMOS25[2], 12 mA output drive, Fast slew rate | XC3S200<br>XC3S400 | 2.10 | 2.41 | ns |
| | | | XC3S50<br>XC3S1000<br>XC3S1500<br>XC3S2000<br>XC3S4000<br>XC3S5000 | 2.77 | 3.18 | ns |
| $T_{IOGSRQ}$ | Time from asserting the Global Set Reset (GSR) net to setting/resetting data at the Output pin | | All | 8.07 | 9.28 | ns |

**Notes:**

1. The numbers in this table are tested using the methodology presented in Table 48 and are based on the operating conditions set forth in Table 32 and Table 35.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 47.
3. For minimums, use the values reported by the Xilinx timing analyzer.

*Table 54:* **Synchronous 18 x 18 Multiplier Timing**

| Symbol | Description | P Outputs | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -5 | | -4 | | |
| | | | Min | Max | Min | Max | |
| **Clock-to-Output Times** | | | | | | | |
| $T_{MULTCK}$ | When reading from the Multiplier, the time from the active transition at the C clock input to data appearing at the P outputs | P[0] | – | 1.00 | – | 1.15 | ns |
| | | P[15] | – | 1.15 | – | 1.32 | ns |
| | | P[17] | – | 1.30 | – | 1.50 | ns |
| | | P[19] | – | 1.45 | – | 1.67 | ns |
| | | P[23] | – | 1.76 | – | 2.02 | ns |
| | | P[31] | – | 2.37 | – | 2.72 | ns |
| | | P[35] | – | 2.67 | – | 3.07 | ns |
| **Setup Times** | | | | | | | |
| $T_{MULIDCK}$ | Time from the setup of data at the A and B inputs to the active transition at the C input of the Multiplier | - | 1.84 | – | 2.11 | – | ns |
| **Hold Times** | | | | | | | |
| $T_{MULCKID}$ | Time from the active transition at the Multiplier's C input to the point where data is last held at the A and B inputs | - | 0 | – | 0 | – | ns |

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 32.

*Table 55:* **Asynchronous 18 x 18 Multiplier Timing**

| Symbol | Description | P Outputs | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -5 | -4 | |
| | | | Max | Max | |
| **Propagation Times** | | | | | |
| $T_{MULT}$ | The time it takes for data to travel from the A and B inputs to the P outputs | P[0] | 1.55 | 1.78 | ns |
| | | P[15] | 3.15 | 3.62 | ns |
| | | P[17] | 3.36 | 3.86 | ns |
| | | P[19] | 3.49 | 4.01 | ns |
| | | P[23] | 3.73 | 4.29 | ns |
| | | P[31] | 4.23 | 4.86 | ns |
| | | P[35] | 4.47 | 5.14 | ns |

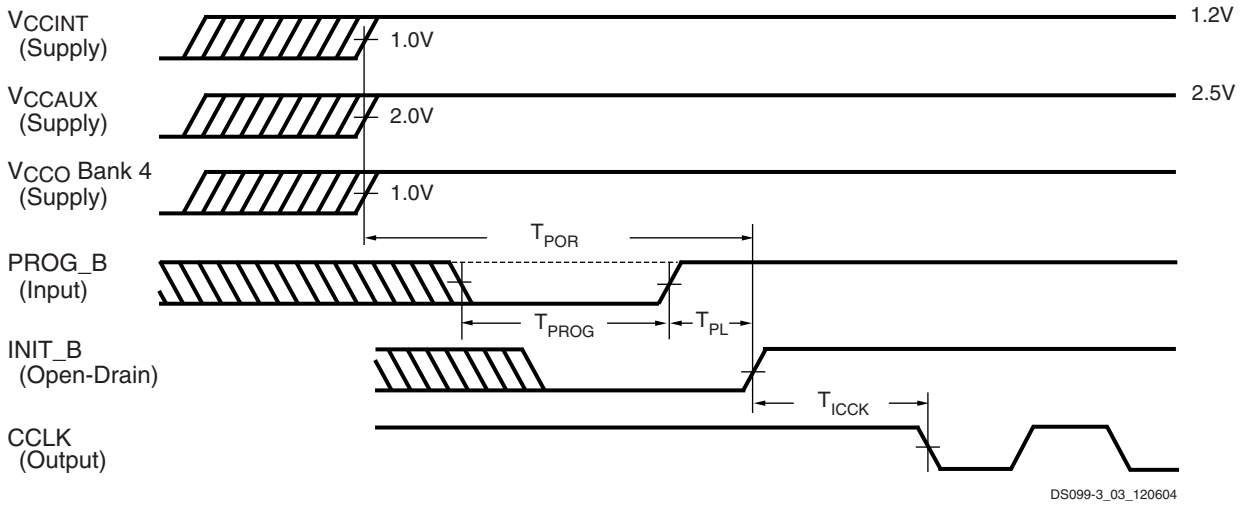
**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 32.

*Table 59:* **Switching Characteristics for the DLL**

| Symbol | Description | Frequency Mode / FCLKIN Range | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | -5 | | -4 | | |
| | | | | Min | Max | Min | Max | |
| **Output Frequency Ranges** | | | | | | | | |
| CLKOUT_FREQ_1X_LF | Frequency for the CLK0, CLK90, CLK180, and CLK270 outputs | Low | All | 18 | 167 | 18 | 167 | MHz |
| CLKOUT_FREQ_1X_HF | Frequency for the CLK0 and CLK180 outputs | High | | 48 | 280 | 48 | 280 | MHz |
| CLKOUT_FREQ_2X_LF(3) | Frequency for the CLK2X and CLK2X180 outputs | Low | | 36 | 334 | 36 | 334 | MHz |
| CLKOUT_FREQ_DV_LF | Frequency for the CLKDV output | Low | | 1.125 | 110 | 1.125 | 110 | MHz |
| CLKOUT_FREQ_DV_HF | | High | | 3 | 185 | 3 | 185 | MHz |
| **Output Clock Jitter**(4) | | | | | | | | |
| CLKOUT_PER_JITT_0 | Period jitter at the CLK0 output | All | All | – | ±100 | – | ±100 | ps |
| CLKOUT_PER_JITT_90 | Period jitter at the CLK90 output | | | – | ±150 | – | ±150 | ps |
| CLKOUT_PER_JITT_180 | Period jitter at the CLK180 output | | | – | ±150 | – | ±150 | ps |
| CLKOUT_PER_JITT_270 | Period jitter at the CLK270 output | | | – | ±150 | – | ±150 | ps |
| CLKOUT_PER_JITT_2X | Period jitter at the CLK2X and CLK2X180 outputs | | | – | ±200 | – | ±200 | ps |
| CLKOUT_PER_JITT_DV1 | Period jitter at the CLKDV output when performing integer division | | | – | ±150 | – | ±150 | ps |
| CLKOUT_PER_JITT_DV2 | Period jitter at the CLKDV output when performing non-integer division | | | – | ±300 | – | ±300 | ps |
| **Duty Cycle** | | | | | | | | |
| CLKOUT_DUTY_CYCLE_DLL(5) | Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs | All | XC3S50 | – | ±150 | – | ±150 | ps |
| | | | XC3S200 | – | ±150 | – | ±150 | ps |
| | | | XC3S400 | – | ±250 | – | ±250 | ps |
| | | | XC3S1000 | – | ±400 | – | ±400 | ps |
| | | | XC3S1500 | – | ±400 | – | ±400 | ps |
| | | | XC3S2000 | – | ±400 | – | ±400 | ps |
| | | | XC3S4000 | – | ±400 | – | ±400 | ps |
| | | | XC3S5000 | – | ±400 | – | ±400 | ps |
| **Phase Alignment** | | | | | | | | |
| CLKIN_CLKFB_PHASE | Phase offset between the CLKIN and CLKFB inputs | All | All | – | ±150 | – | ±150 | ps |
| CLKOUT_PHASE | Phase offset between any two DLL outputs (except CLK2X and CLK0) | | | – | ±140 | – | ±140 | ps |
| | Phase offset between the CLK2X and CLK0 outputs | | | – | ±250 | – | ±250 | ps |

## Configuration and JTAG Timing




**Notes:**

1. The $V_{CCINT}$, $V_{CCAUX}$, and $V_{CCO}$ supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

*Figure 36:* **Waveforms for Power-On and the Beginning of Configuration**

*Table 65:* **Power-On Timing and the Beginning of Configuration**

| Symbol | Description | Device | All Speed Grades | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $T_{POR}$(2) | The time from the application of $V_{CCINT}$, $V_{CCAUX}$, and $V_{CCO}$ Bank 4 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin | XC3S50 | – | 5 | ms |
| | | XC3S200 | – | 5 | ms |
| | | XC3S400 | – | 5 | ms |
| | | XC3S1000 | – | 5 | ms |
| | | XC3S1500 | – | 7 | ms |
| | | XC3S2000 | – | 7 | ms |
| | | XC3S4000 | – | 7 | ms |
| | | XC3S5000 | – | 7 | ms |
| $T_{PROG}$ | The width of the low-going pulse on the PROG_B pin | All | 0.3 | – | µs |
| $T_{PL}$(2) | The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin | XC3S50 | – | 2 | ms |
| | | XC3S200 | – | 2 | ms |
| | | XC3S400 | – | 2 | ms |
| | | XC3S1000 | – | 2 | ms |
| | | XC3S1500 | – | 3 | ms |
| | | XC3S2000 | – | 3 | ms |
| | | XC3S4000 | – | 3 | ms |
| | | XC3S5000 | – | 3 | ms |
| $T_{INIT}$ | Minimum Low pulse width on INIT_B output | All | 250 | – | ns |
| $T_{ICCK}$(3) | The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin | All | 0.25 | 4.0 | µs |

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 32. This means power must be applied to all $V_{CCINT}$, $V_{CCO}$, and $V_{CCAUX}$ lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only for the Master Serial and Master Parallel modes.

### HSWAP_EN: Disable Pull-up Resistors During Configuration

As shown in Table 76, a Low on this asynchronous pin enables pull-up resistors on all user I/Os not actively involved in the configuration process, although only until device configuration completes. A High disables the pull-up resistors during configuration, which is the desired state for some applications.

The dedicated configuration CONFIG pins (CCLK, DONE, PROG_B, HSWAP_EN, M2, M1, M0), the JTAG pins (TDI, TMS, TCK, TDO) and the INIT_B always have active pull-up resistors during configuration, regardless of the value on HSWAP_EN.

After configuration, HSWAP_EN becomes a "don't care" input and any pull-up resistors previously enabled by HSWAP_EN are disabled. If a user I/O in the application requires a pull-up resistor after configuration, place a PULLUP primitive on the associated I/O pin or, for some pins, set the associated bitstream generator option.

*Table 76:* **HSWAP_EN Encoding**

| HSWAP_EN | Function |
|---|---|
| **During Configuration** | |
| 0 | Enable pull-up resistors on all pins not actively involved in the configuration process. Pull-ups are only active until configuration completes. See Table 79. |
| 1 | No pull-up resistors during configuration. |
| **After Configuration, User Mode** | |
| X | This pin has no function except during device configuration. |

**Notes:**

1. X = don't care, either 0 or 1.

The Bitstream generator option HswapenPin determines whether a pull-up resistor to VCCAUX, a pull-down resistor, or no resistor is present on HSWAP_EN after configuration.

## JTAG: Dedicated JTAG Port Pins

*Table 77:* **JTAG Pin Descriptions**

| Pin Name | Direction | Description | Bitstream Generation Option |
|---|---|---|---|
| TCK | Input | **Test Clock:** The TCK clock signal synchronizes all boundary scan operations on its rising edge. | The BitGen option **TckPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present. |
| TDI | Input | **Test Data Input:** TDI is the serial data input for all JTAG instruction and data registers. This input is sampled on the rising edge of TCK. | The BitGen option **TdiPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present. |
| TMS | Input | **Test Mode Select:** The TMS input controls the sequence of states through which the JTAG TAP state machine passes. This input is sampled on the rising edge of TCK. | The BitGen option **TmsPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present. |
| TDO | Output | **Test Data Output:** The TDO pin is the data output for all JTAG instruction and data registers. This output is sampled on the rising edge of TCK. The TDO output is an active totem-pole driver and is not like the open-collector TDO output on Virtex®-II Pro FPGAs. | The BitGen option **TdoPin** determines whether a pull-up resistor, pull-down resistor or no resistor is present. |

These pins are dedicated connections to the four-wire IEEE 1532/IEEE 1149.1 JTAG port, shown in Figure 43 and described in Table 77. The JTAG port is used for boundary-scan testing, device configuration, application debugging, and possibly an additional serial port for the application. These pins are dedicated and are not available as user-I/O pins. Every package has four dedicated JTAG pins and these pins are powered by the +2.5V VCCAUX supply.

For additional information on JTAG configuration, see Boundary-Scan (JTAG) Mode, page 50.

## Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx website at the specified location in Table 83.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx website for each package.

*Table 83:* **Xilinx Package Mechanical Drawings**

| Package | Web Link (URL) |
|---|---|
| VQ100 and VQG100 | http://www.xilinx.com/support/documentation/package_specs/vq100.pdf |
| CP132 and CPG132(1) | http://www.xilinx.com/support/documentation/package_specs/cp132.pdf |
| TQ144 and TQG144 | http://www.xilinx.com/support/documentation/package_specs/tq144.pdf |
| PQ208 and PQG208 | http://www.xilinx.com/support/documentation/package_specs/pq208.pdf |
| FT256 and FTG256 | http://www.xilinx.com/support/documentation/package_specs/ft256.pdf |
| FG320 and FGG320 | http://www.xilinx.com/support/documentation/package_specs/fg320.pdf |
| FG456 and FGG456 | http://www.xilinx.com/support/documentation/package_specs/fg456.pdf |
| FG676 and FGG676 | http://www.xilinx.com/support/documentation/package_specs/fg676.pdf |
| FG900 and FGG900 | http://www.xilinx.com/support/documentation/package_specs/fg900.pdf |
| FG1156 and FGG1156(1) | http://www.xilinx.com/support/documentation/package_specs/fg1156.pdf |

**Notes:**

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

## Power, Ground, and I/O by Package

Each package has three separate voltage supply inputs—VCCINT, VCCAUX, and VCCO—and a common ground return, GND. The numbers of pins dedicated to these functions varies by package, as shown in Table 84.

*Table 84:* **Power and Ground Supply Pins by Package**

| Package | VCCINT | VCCAUX | VCCO | GND |
|---|---|---|---|---|
| VQ100 | 4 | 4 | 8 | 10 |
| CP132(1) | 4 | 4 | 12 | 12 |
| TQ144 | 4 | 4 | 12 | 16 |
| PQ208 | 4 | 8 | 12 | 28 |
| FT256 | 8 | 8 | 24 | 32 |
| FG320 | 12 | 8 | 28 | 40 |
| FG456 | 12 | 8 | 40 | 52 |
| FG676 | 20 | 16 | 64 | 76 |
| FG900 | 32 | 24 | 80 | 120 |
| FG1156(1) | 40 | 32 | 104 | 184 |

**Notes:**

1. The CP132, CPG132, FG1156, and FGG1156 packages are discontinued. See http://www.xilinx.com/support/documentation/spartan-3_customer_notices.htm.

A majority of package pins are user-defined I/O pins. However, the numbers and characteristics of these I/O depends on the device type and the package in which it is available, as shown in Table 85. The table shows the maximum number of single-ended I/O pins available, assuming that all I/O-, DUAL-, DCI-, VREF-, and GCLK-type pins are used as general-purpose I/O. Likewise, the table shows the maximum number of differential pin-pairs available on the package. Finally, the table shows how the total maximum user I/Os are distributed by pin type, including the number of unconnected—i.e., N.C.—pins on the device.

# PQ208: 208-lead Plastic Quad Flat Pack

The 208-lead plastic quad flat package, PQ208, supports three different Spartan-3 devices, including the XC3S50, the XC3S200, and the XC3S400. The footprints for the XC3S200 and XC3S400 are identical, as shown in Table 93 and Figure 47. The XC3S50, however, has fewer I/O pins resulting in 17 unconnected pins on the PQ208 package, labeled as "N.C." In Table 93 and Figure 47, these unconnected pins are indicated with a black diamond symbol (◆).

All the package pins appear in Table 93 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S50 pinout and the pinout for the XC3S200 and XC3S400, then that difference is highlighted in Table 93. If the table entry is shaded grey, then there is an unconnected pin on the XC3S50 that maps to a user-I/O pin on the XC3S200 and XC3S400. If the table entry is shaded tan, then the unconnected pin on the XC3S50 maps to a VREF-type pin on the XC3S200 and XC3S400. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S50 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S50 device to an XC3S200 or XC3S400 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip

## Pinout Table

*Table 93:* **PQ208 Package Pinout**

| Bank | XC3S50 Pin Name | XC3S200, XC3S400 Pin Names | PQ208 Pin Number | Type |
|---|---|---|---|---|
| 0 | IO | IO | P189 | I/O |
| 0 | IO | IO | P197 | I/O |
| 0 | N.C. (◆) | IO/VREF_0 | P200 | VREF |
| 0 | IO/VREF_0 | IO/VREF_0 | P205 | VREF |
| 0 | IO_L01N_0/VRP_0 | IO_L01N_0/VRP_0 | P204 | DCI |
| 0 | IO_L01P_0/VRN_0 | IO_L01P_0/VRN_0 | P203 | DCI |
| 0 | IO_L25N_0 | IO_L25N_0 | P199 | I/O |
| 0 | IO_L25P_0 | IO_L25P_0 | P198 | I/O |
| 0 | IO_L27N_0 | IO_L27N_0 | P196 | I/O |
| 0 | IO_L27P_0 | IO_L27P_0 | P194 | I/O |
| 0 | IO_L30N_0 | IO_L30N_0 | P191 | I/O |
| 0 | IO_L30P_0 | IO_L30P_0 | P190 | I/O |
| 0 | IO_L31N_0 | IO_L31N_0 | P187 | I/O |
| 0 | IO_L31P_0/VREF_0 | IO_L31P_0/VREF_0 | P185 | VREF |
| 0 | IO_L32N_0/GCLK7 | IO_L32N_0/GCLK7 | P184 | GCLK |
| 0 | IO_L32P_0/GCLK6 | IO_L32P_0/GCLK6 | P183 | GCLK |
| 0 | VCCO_0 | VCCO_0 | P188 | VCCO |
| 0 | VCCO_0 | VCCO_0 | P201 | VCCO |
| 1 | IO | IO | P167 | I/O |
| 1 | IO | IO | P175 | I/O |
| 1 | IO | IO | P182 | I/O |
| 1 | IO_L01N_1/VRP_1 | IO_L01N_1/VRP_1 | P162 | DCI |
| 1 | IO_L01P_1/VRN_1 | IO_L01P_1/VRN_1 | P161 | DCI |

## User I/Os by Bank

Table 94 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S50 in the PQ208 package. Similarly, Table 95 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S200 and XC3S400 in the PQ208 package.

*Table 94:* **User I/Os Per Bank for XC3S50 in PQ208 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | DUAL | DCI | VREF | GCLK |
| Top | 0 | 15 | 9 | 0 | 2 | 2 | 2 |
| | 1 | 15 | 9 | 0 | 2 | 2 | 2 |
| Right | 2 | 16 | 13 | 0 | 2 | 2 | 0 |
| | 3 | 16 | 12 | 0 | 2 | 2 | 0 |
| Bottom | 4 | 15 | 3 | 6 | 2 | 2 | 2 |
| | 5 | 15 | 3 | 6 | 2 | 2 | 2 |
| Left | 6 | 16 | 12 | 0 | 2 | 2 | 0 |
| | 7 | 16 | 12 | 0 | 2 | 2 | 0 |

*Table 95:* **User I/Os Per Bank for XC3S200 and XC3S400 in PQ208 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | DUAL | DCI | VREF | GCLK |
| Top | 0 | 16 | 9 | 0 | 2 | 3 | 2 |
| | 1 | 15 | 9 | 0 | 2 | 2 | 2 |
| Right | 2 | 19 | 14 | 0 | 2 | 3 | 0 |
| | 3 | 20 | 15 | 0 | 2 | 3 | 0 |
| Bottom | 4 | 17 | 4 | 6 | 2 | 3 | 2 |
| | 5 | 15 | 3 | 6 | 2 | 2 | 2 |
| Left | 6 | 19 | 14 | 0 | 2 | 3 | 0 |
| | 7 | 20 | 15 | 0 | 2 | 3 | 0 |

*Right Half of Package (Top View)*

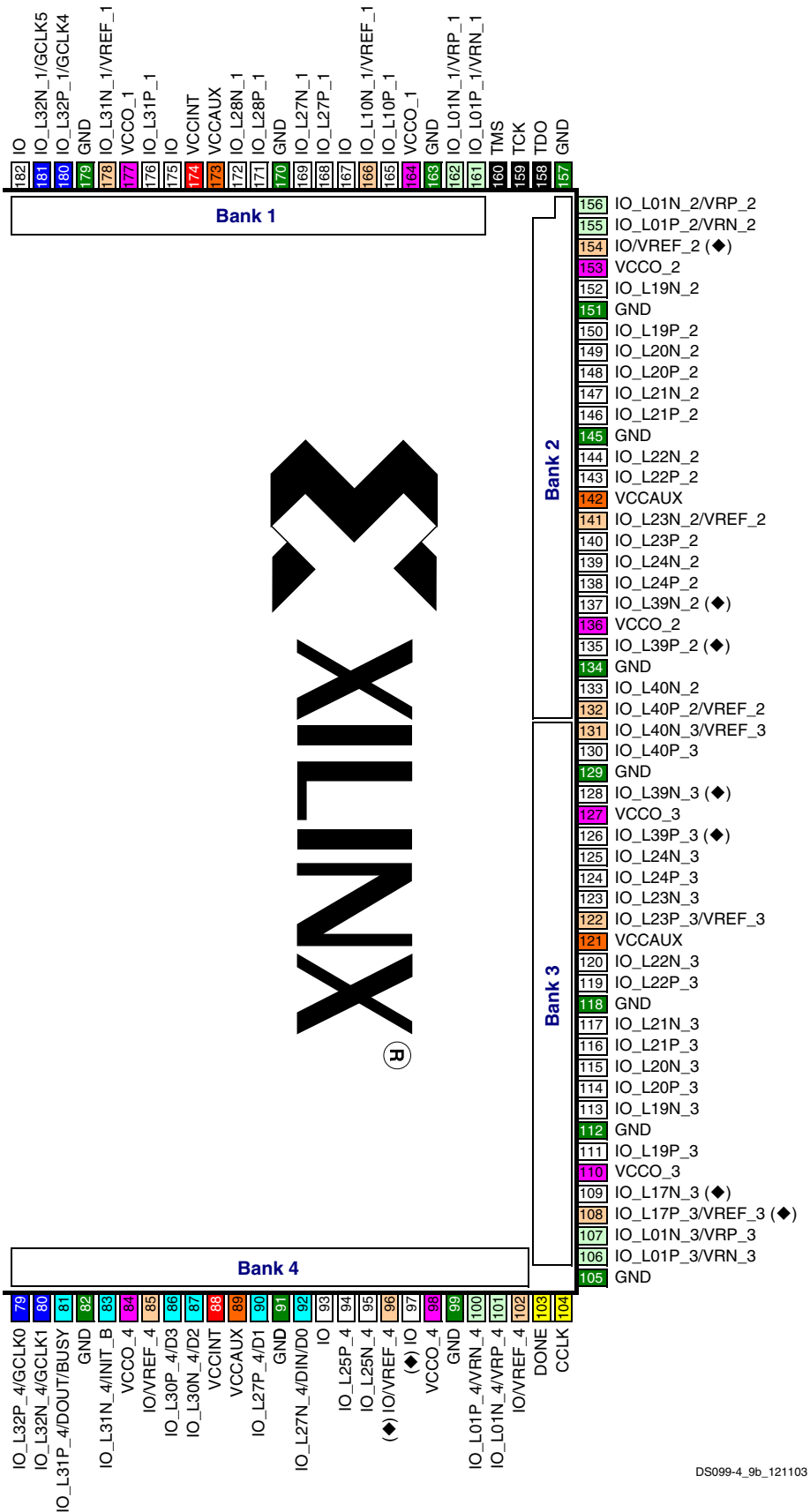



**Figure 48: PQ208 Package Footprint (Top View) Continued**

*Table 98:* **FG320 Package Pinout *(Cont'd)***

| Bank | XC3S400, XC3S1000, XC3S1500 Pin Name | FG320 Pin Number | Type |
|---|---|---|---|
| 2 | IO_L20N_2 | E17 | I/O |
| 2 | IO_L20P_2 | E18 | I/O |
| 2 | IO_L21N_2 | F15 | I/O |
| 2 | IO_L21P_2 | E15 | I/O |
| 2 | IO_L22N_2 | F14 | I/O |
| 2 | IO_L22P_2 | G14 | I/O |
| 2 | IO_L23N_2/VREF_2 | G18 | VREF |
| 2 | IO_L23P_2 | F17 | I/O |
| 2 | IO_L24N_2 | G15 | I/O |
| 2 | IO_L24P_2 | G16 | I/O |
| 2 | IO_L27N_2 | H13 | I/O |
| 2 | IO_L27P_2 | H14 | I/O |
| 2 | IO_L34N_2/VREF_2 | H16 | VREF |
| 2 | IO_L34P_2 | H15 | I/O |
| 2 | IO_L35N_2 | H17 | I/O |
| 2 | IO_L35P_2 | H18 | I/O |
| 2 | IO_L39N_2 | J18 | I/O |
| 2 | IO_L39P_2 | J17 | I/O |
| 2 | IO_L40N_2 | J15 | I/O |
| 2 | IO_L40P_2/VREF_2 | J14 | VREF |
| 2 | VCCO_2 | F16 | VCCO |
| 2 | VCCO_2 | H12 | VCCO |
| 2 | VCCO_2 | J12 | VCCO |
| 3 | IO | K15 | I/O |
| 3 | IO_L01N_3/VRP_3 | T17 | DCI |
| 3 | IO_L01P_3/VRN_3 | T16 | DCI |
| 3 | IO_L16N_3 | T18 | I/O |
| 3 | IO_L16P_3 | U18 | I/O |
| 3 | IO_L17N_3 | P16 | I/O |
| 3 | IO_L17P_3/VREF_3 | R16 | VREF |
| 3 | IO_L19N_3 | R17 | I/O |
| 3 | IO_L19P_3 | R18 | I/O |
| 3 | IO_L20N_3 | P18 | I/O |
| 3 | IO_L20P_3 | P17 | I/O |
| 3 | IO_L21N_3 | P15 | I/O |
| 3 | IO_L21P_3 | N15 | I/O |
| 3 | IO_L22N_3 | M14 | I/O |
| 3 | IO_L22P_3 | N14 | I/O |
| 3 | IO_L23N_3 | M15 | I/O |
| 3 | IO_L23P_3/VREF_3 | M16 | VREF |

*Table 100:* **FG456 Package Pinout *(Cont'd)***

| Bank | 3S400 Pin Name | 3S1000, 3S1500, 3S2000 Pin Name | FG456 Pin Number | Type |
|---|---|---|---|---|
| 5 | IO_L27N_5/VREF_5 | IO_L27N_5/VREF_5 | W9 | VREF |
| 5 | IO_L27P_5 | IO_L27P_5 | V9 | I/O |
| 5 | IO_L28N_5/D6 | IO_L28N_5/D6 | AB9 | DUAL |
| 5 | IO_L28P_5/D7 | IO_L28P_5/D7 | AA9 | DUAL |
| 5 | IO_L29N_5 | IO_L29N_5 | Y10 | I/O |
| 5 | IO_L29P_5/VREF_5 | IO_L29P_5/VREF_5 | W10 | VREF |
| 5 | IO_L30N_5 | IO_L30N_5 | AB10 | I/O |
| 5 | IO_L30P_5 | IO_L30P_5 | AA10 | I/O |
| 5 | IO_L31N_5/D4 | IO_L31N_5/D4 | W11 | DUAL |
| 5 | IO_L31P_5/D5 | IO_L31P_5/D5 | V11 | DUAL |
| 5 | IO_L32N_5/GCLK3 | IO_L32N_5/GCLK3 | AA11 | GCLK |
| 5 | IO_L32P_5/GCLK2 | IO_L32P_5/GCLK2 | Y11 | GCLK |
| 5 | VCCO_5 | VCCO_5 | T9 | VCCO |
| 5 | VCCO_5 | VCCO_5 | T10 | VCCO |
| 5 | VCCO_5 | VCCO_5 | T11 | VCCO |
| 5 | VCCO_5 | VCCO_5 | U8 | VCCO |
| 5 | VCCO_5 | VCCO_5 | Y8 | VCCO |
| 6 | IO | IO | Y1 | I/O |
| 6 | IO_L01N_6/VRP_6 | IO_L01N_6/VRP_6 | Y3 | DCI |
| 6 | IO_L01P_6/VRN_6 | IO_L01P_6/VRN_6 | Y2 | DCI |
| 6 | IO_L16N_6 | IO_L16N_6 | W4 | I/O |
| 6 | IO_L16P_6 | IO_L16P_6 | W3 | I/O |
| 6 | IO_L17N_6 | IO_L17N_6 | W2 | I/O |
| 6 | IO_L17P_6/VREF_6 | IO_L17P_6/VREF_6 | W1 | VREF |
| 6 | IO_L19N_6 | IO_L19N_6 | V5 | I/O |
| 6 | IO_L19P_6 | IO_L19P_6 | U5 | I/O |
| 6 | IO_L20N_6 | IO_L20N_6 | V4 | I/O |
| 6 | IO_L20P_6 | IO_L20P_6 | V3 | I/O |
| 6 | IO_L21N_6 | IO_L21N_6 | V2 | I/O |
| 6 | IO_L21P_6 | IO_L21P_6 | V1 | I/O |
| 6 | IO_L22N_6 | IO_L22N_6 | T6 | I/O |
| 6 | IO_L22P_6 | IO_L22P_6 | T5 | I/O |
| 6 | IO_L23N_6 | IO_L23N_6 | U4 | I/O |
| 6 | IO_L23P_6 | IO_L23P_6 | T4 | I/O |
| 6 | IO_L24N_6/VREF_6 | IO_L24N_6/VREF_6 | U3 | VREF |
| 6 | IO_L24P_6 | IO_L24P_6 | U2 | I/O |
| 6 | N.C. (◆) | IO_L26N_6 | T3 | I/O |
| 6 | N.C. (◆) | IO_L26P_6 | R4 | I/O |
| 6 | IO_L27N_6 | IO_L27N_6 | T2 | I/O |
| 6 | IO_L27P_6 | IO_L27P_6 | T1 | I/O |

# FG676: 676-lead Fine-pitch Ball Grid Array

The 676-lead fine-pitch ball grid array package, FG676, supports five different Spartan-3 devices, including the XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000. All five have nearly identical footprints but are slightly different, primarily due to unconnected pins on the XC3S1000 and XC3S1500. For example, because the XC3S1000 has fewer I/O pins, this device has 98 unconnected pins on the FG676 package, labeled as "N.C." In Table 103 and Figure 53, these unconnected pins are indicated with a black diamond symbol (◆). The XC3S1500, however, has only two unconnected pins, also labeled "N.C." in the pinout table but indicated with a black square symbol (■).

All the package pins appear in Table 103 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

If there is a difference between the XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000 pinouts, then that difference is highlighted in Table 103. If the table entry is shaded grey, then there is an unconnected pin on either the XC3S1000 or XC3S1500 that maps to a user-I/O pin on the XC3S2000, XC3S4000, and XC3S5000. If the table entry is shaded tan, then the unconnected pin on either the XC3S1000 or XC3S1500 maps to a VREF-type pin on the XC3S2000, XC3S4000, and XC3S5000. If the other VREF pins in the bank all connect to a voltage reference to support a special I/O standard, then also connect the N.C. pin on the XC3S1000 or XC3S1500 to the same VREF voltage. This provides maximum flexibility as you could potentially migrate a design from the XC3S1000 through to the XC3S5000 FPGA without changing the printed circuit board.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

## Pinout Table

*Table 103:* **FG676 Package Pinout**

| Bank | XC3S1000 Pin Name | XC3S1500 Pin Name | XC3S2000 Pin Name | XC3S4000 Pin Name | XC3S5000 Pin Name | FG676 Pin Number | Type |
|---|---|---|---|---|---|---|---|
| 0 | IO | IO | IO | IO | IO_L04N_0(3) | A3 | I/O |
| 0 | IO | IO | IO | IO | IO | A5 | I/O |
| 0 | IO | IO | IO | IO | IO | A6 | I/O |
| 0 | IO | IO | IO | IO | IO_L04P_0(3) | C4 | I/O |
| 0 | N.C. (◆) | IO | IO | IO | IO_L13N_0(3) | C8 | I/O |
| 0 | IO | IO | IO | IO | IO | C12 | I/O |
| 0 | IO | IO | IO | IO | IO | E13 | I/O |
| 0 | IO | IO | IO | IO | IO | H11 | I/O |
| 0 | IO | IO | IO | IO | IO | H12 | I/O |
| 0 | IO/VREF_0 | IO/VREF_0 | IO/VREF_0 | IO/VREF_0 | IO/VREF_0 | B3 | VREF |
| 0 | IO/VREF_0 | IO/VREF_0 | IO/VREF_0 | IO/VREF_0 | IO/VREF_0 | F7 | VREF |
| 0 | IO/VREF_0 | IO/VREF_0 | IO/VREF_0 | IO/VREF_0 | IO/VREF_0 | G10 | VREF |
| 0 | IO_L01N_0/VRP_0 | IO_L01N_0/VRP_0 | IO_L01N_0/VRP_0 | IO_L01N_0/VRP_0 | IO_L01N_0/VRP_0 | E5 | DCI |
| 0 | IO_L01P_0/VRN_0 | IO_L01P_0/VRN_0 | IO_L01P_0/VRN_0 | IO_L01P_0/VRN_0 | IO_L01P_0/VRN_0 | D5 | DCI |
| 0 | IO_L05N_0 | IO_L05N_0 | IO_L05N_0 | IO_L05N_0 | IO_L05N_0 | B4 | I/O |
| 0 | IO_L05P_0/VREF_0 | IO_L05P_0/VREF_0 | IO_L05P_0/VREF_0 | IO_L05P_0/VREF_0 | IO_L05P_0/VREF_0 | A4 | VREF |
| 0 | IO_L06N_0 | IO_L06N_0 | IO_L06N_0 | IO_L06N_0 | IO_L06N_0 | C5 | I/O |
| 0 | IO_L06P_0 | IO_L06P_0 | IO_L06P_0 | IO_L06P_0 | IO_L06P_0 | B5 | I/O |
| 0 | IO_L07N_0 | IO_L07N_0 | IO_L07N_0 | IO_L07N_0 | IO_L07N_0 | E6 | I/O |
| 0 | IO_L07P_0 | IO_L07P_0 | IO_L07P_0 | IO_L07P_0 | IO_L07P_0 | D6 | I/O |
| 0 | IO_L08N_0 | IO_L08N_0 | IO_L08N_0 | IO_L08N_0 | IO_L08N_0 | C6 | I/O |
| 0 | IO_L08P_0 | IO_L08P_0 | IO_L08P_0 | IO_L08P_0 | IO_L08P_0 | B6 | I/O |

## Revision History

| Date | Version | Description |
|---|---|---|
| 04/03/03 | 1.0 | Initial Xilinx release. |
| 04/21/03 | 1.1 | Added information on the VQ100 package footprint, including a complete pinout table (Table 87) and footprint diagram (Figure 44). Updated Table 85 with final I/O counts for the VQ100 package. Also added final differential I/O pair counts for the TQ144 package. Added clarifying comments to HSWAP_EN pin description on page 119. Updated the footprint diagram for the FG900 package shown in Figure 55a and Figure 55b. Some thick lines separating I/O banks were incorrect. Made cosmetic changes to Figure 40, Figure 42, and Figure 43. Updated Xilinx hypertext links. Added XC3S200 and XC3S400 to Pin Name column in Table 91. |
| 05/12/03 | 1.1.1 | AM32 pin was missing GND label in FG1156 package diagram (Figure 53). |
| 07/11/03 | 1.1.2 | Corrected misspellings of GCLK in Table 69 and Table 70. Changed CMOS25 to LVCMOS25 in Dual-Purpose Pin I/O Standard During Configuration section. Clarified references to Module 2. For XC3S5000 in FG1156 package, corrected N.C. symbol to a black square in Table 110, key, and package drawing. |
| 07/29/03 | 1.2 | Corrected pin names on FG1156 package. Some package balls incorrectly included LVDS pair names. The affected balls on the FG1156 package include G1, G2, G33, G34, U9, U10, U25, U26, V9, V10, V25, V26, AH1, AH2, AH33, AH34. The number of LVDS pairs is unaffected. Modified affected balls and re-sorted rows in Table 110. Updated affected balls in Figure 53. Also updated ASCII and Excel electronic versions of FG1156 pinout. |
| 08/19/03 | 1.2.1 | Removed 100 MHz ConfigRate option in CCLK: Configuration Clock section and in Table 80. Added note that TDO is a totem-pole output in Table 77. |
| 10/09/03 | 1.2.2 | Some pins had incorrect bank designations and were improperly sorted in Table 93. No pin names or functions changed. Renamed DCI_IN to DCI and added black diamond to N.C. pins in Table 93. In Figure 47, removed some extraneous text from pin 106 and corrected spelling of pins 45, 48, and 81. |
| 12/17/03 | 1.3 | Added FG320 pin tables and pinout diagram (FG320: 320-lead Fine-pitch Ball Grid Array). Made cosmetic changes to the TQ144 footprint (Figure 46), the PQ208 footprint (Figure 47), the FG676 footprint (Figure 53), and the FG900 footprint (Figure 55). Clarified wording in Precautions When Using the JTAG Port in 3.3V Environments section. |
| 02/27/04 | 1.4 | Clarified wording in Using JTAG Port After Configuration section. In Table 81, reduced package height for FG320 and increased maximum I/O values for the FG676, FG900, and FG1156 packages. |
| 07/13/04 | 1.5 | Added information on lead-free (Pb-free) package options to the Package Overview section plus Table 81 and Table 83. Clarified the VRN_# reference resistor requirements for I/O standards that use single termination as described in the DCI Termination Types section and in Figure 42b. Graduated from Advance Product Specification to Product Specification. |
| 08/24/04 | 1.5.1 | Removed XC3S2000 references from FG1156: 1156-lead Fine-pitch Ball Grid Array. |
| 01/17/05 | 1.6 | Added XC3S50 in CP132 package option. Added XC3S2000 in FG456 package option. Added XC3S4000 in FG676 package option. Added Selecting the Right Package Option section. Modified or added Table 81, Table 83, Table 84, Table 85, Table 89, Table 90, Table 100, Table 102, Table 103, Table 106, Figure 45, and Figure 53. |
| 08/19/05 | 1.7 | Removed term “weak” from the description of pull-up and pull-down resistors. Added IDCODE Register values. Added signal integrity precautions to CCLK: Configuration Clock and indicated that CCLK should be treated as an I/O during Master mode in Table 79. |
| 04/03/06 | 2.0 | Added Package Thermal Characteristics. Updated Figure 41 to make it a more obvious example. Added detail about which pins have dedicated pull-up resistors during configuration, regardless of the HSWAP_EN value to Table 70 and to Pin Behavior During Configuration. Updated Precautions When Using the JTAG Port in 3.3V Environments. |
| 04/26/06 | 2.1 | Corrected swapped data row in Table 86. The Theta-JA with zero airflow column was swapped with the Theta-JC column. Made additional notations on CONFIG and JTAG pins that have pull-up resistors during configuration, regardless of the HSWAP_EN input. |
| 05/25/07 | 2.2 | Added link on page 128 to Material Declaration Data Sheets. Corrected units typo in Table 74. Added Note 1 to Table 103 about VREF for XC3S1500 in FG676. |