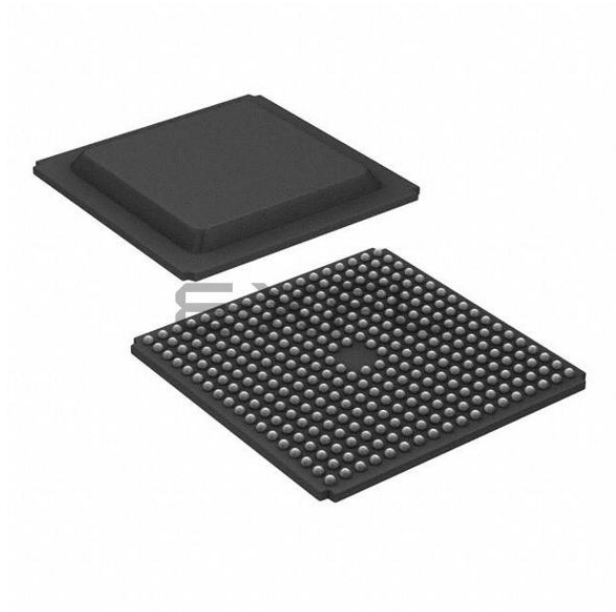


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	294912
Number of I/O	221
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s400-4fgg320c

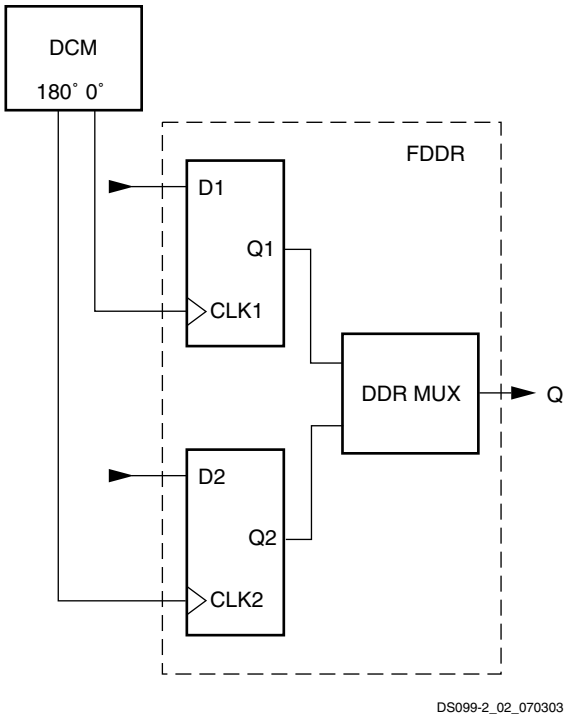


Figure 8: **Clocking the DDR Register**

Aside from high bandwidth data transfers, DDR can also be used to reproduce, or “mirror”, a clock signal on the output. This approach is used to transmit clock and data signals together. A similar approach is used to reproduce a clock signal at multiple outputs. The advantage for both approaches is that skew across the outputs will be minimal.

Some adjacent I/O blocks (IOBs) share common routing connecting the ICLK1, ICLK2, OTCLK1, and OTCLK2 clock inputs of both IOBs. These IOB pairs are identified by their differential pair names IO_LxxN_# and IO_LxxP_#, where "xx" is an I/O pair number and ‘#’ is an I/O bank number. Two adjacent IOBs containing DDR registers must share common clock inputs, otherwise one or more of the clock signals will be unroutable.

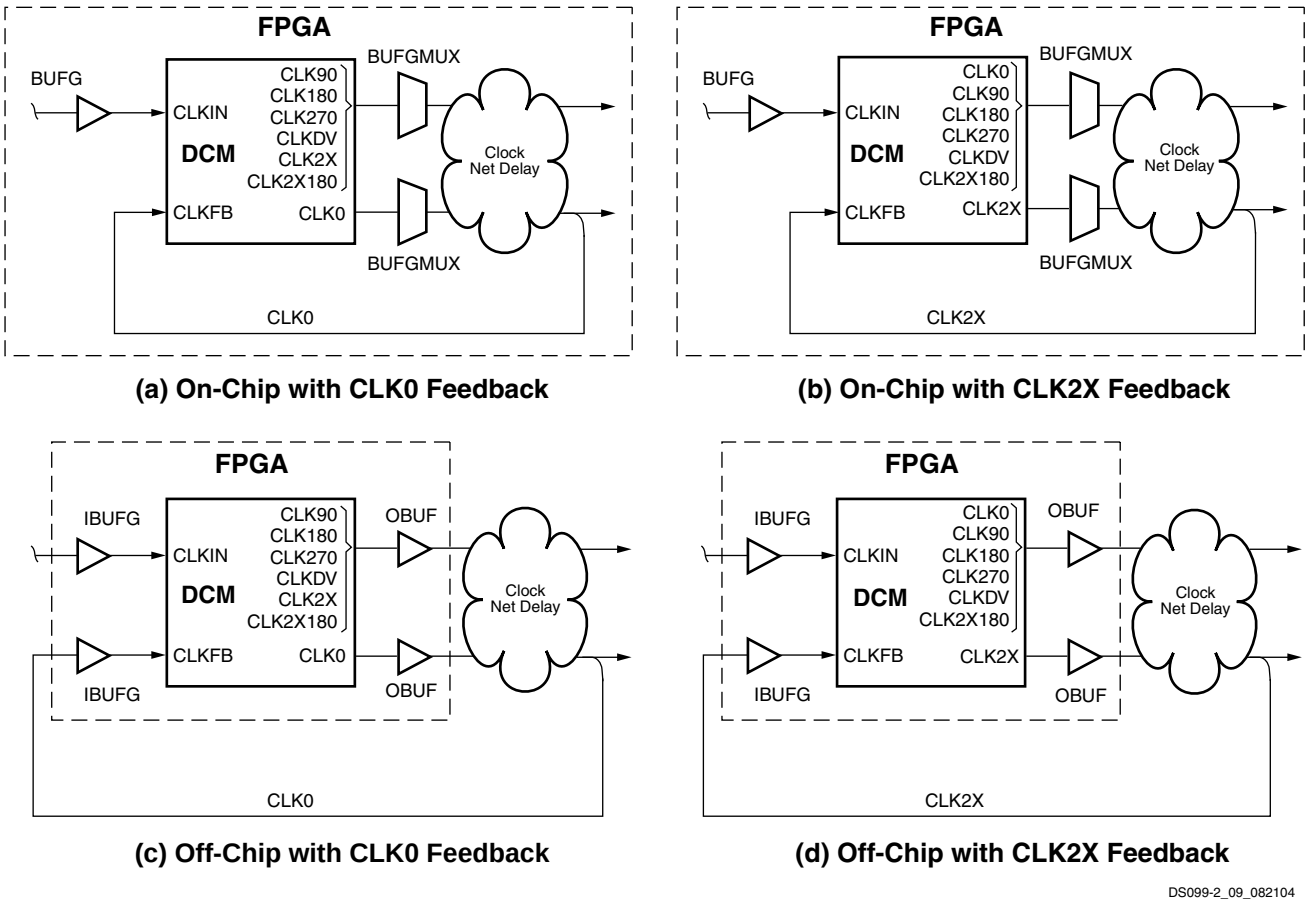
Pull-Up and Pull-Down Resistors

The optional pull-up and pull-down resistors are intended to establish High and Low levels, respectively, at unused I/Os. The pull-up resistor optionally connects each IOB pad to V_{CCO}. A pull-down resistor optionally connects each pad to GND. These resistors are placed in a design using the PULLUP and PULLDOWN symbols in a schematic, respectively. They can also be instantiated as components, set as constraints or passed as attributes in HDL code. These resistors can also be selected for all unused I/O using the Bitstream Generator (BitGen) option UnusedPin. A Low logic level on HSWAP_EN activates the pull-up resistors on all I/Os during configuration (see The I/Os During Power-On, Configuration, and User Mode, page 21).

The Spartan-3 FPGAs I/O pull-up and pull-down resistors are significantly stronger than the "weak" pull-up/pull-down resistors used in previous Xilinx FPGA families. See Table 33, page 61 for equivalent resistor strengths.

Keeper Circuit

Each I/O has an optional keeper circuit that retains the last logic level on a line after all drivers have been turned off. This is useful to keep bus lines from floating when all connected drivers are in a high-impedance state. This function is placed in a design using the KEEPER symbol. Pull-up and pull-down resistors override the keeper circuit.



(a) On-Chip with CLK0 Feedback

(b) On-Chip with CLK2X Feedback

(c) Off-Chip with CLK0 Feedback

(d) Off-Chip with CLK2X Feedback

DS099-2_09_082104

Notes:

1. In the Low Frequency mode, all seven DLL outputs are available. In the High Frequency mode, only the CLK0, CLK180, and CLKDV outputs are available.

Figure 21: **Input Clock, Output Clock, and Feedback Connections for the DLL**

In the on-chip synchronization case (the [a] and [b] sections of Figure 21), it is possible to connect any of the DLL's seven output clock signals through general routing resources to the FPGA's internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. As shown in the [a] section of Figure 21, the feedback loop is created by routing CLK0 (or CLK2X, in the [b] section) to a global clock net, which in turn drives the CLKFB input.

In the off-chip synchronization case (the [c] and [d] sections of Figure 21), CLK0 (or CLK2X) plus any of the DLL's other output clock signals exit the FPGA using output buffers (OBUF) to drive an external clock network plus registers on the board. As shown in the [c] section of Figure 21, the feedback loop is formed by feeding CLK0 (or CLK2X, in the [d] section) back into the FPGA using an IBUFG, which directly accesses the global clock network, or an IBUF. Then, the global clock net is connected directly to the CLKFB input.

DLL Frequency Modes

The DLL supports two distinct operating modes, High Frequency and Low Frequency, with each specified over a different clock frequency range. The DLL_FREQUENCY_MODE attribute chooses between the two modes. When the attribute is set to LOW, the Low Frequency mode permits all seven DLL clock outputs to operate over a low-to-moderate frequency range. When the attribute is set to HIGH, the High Frequency mode allows the CLK0, CLK180 and CLKDV outputs to operate at the highest possible frequencies. The remaining DLL clock outputs are not available for use in High Frequency mode.

Accommodating High Input Frequencies

If the frequency of the CLKIN signal is high such that it exceeds the maximum permitted, divide it down to an acceptable value using the CLKIN_DIVIDE_BY_2 attribute. When this attribute is set to TRUE, the CLKIN frequency is divided by a factor of two just as it enters the DCM.

Initial Spartan-3 FPGA mask revisions have a limit on how fast the V_{CCO} supply can ramp. The minimum allowed V_{CCO} ramp rate appears as T_{CCO} in Table 30, page 60. The minimum rate is affected by the package inductance. Consequently, the ball grid array and chip-scale packages (CP132, FT256, FG456, FG676, and FG900) allow a faster ramp rate than the quad-flat packages (VQ100, TQ144, and PQ208).

Configuration Data Retention, Brown-Out

The FPGA's configuration data is stored in robust CMOS configuration latches. The data in these latches is retained even when the voltages drop to the minimum levels necessary to preserve RAM contents. This is specified in Table 31, page 60.

If, after configuration, the V_{CCAUX} or V_{CCINT} supply drops below its data retention voltage, clear the current device configuration using one of the following methods:

- Force the V_{CCAUX} or V_{CCINT} supply voltage below the minimum Power On Reset (POR) voltage threshold Table 29, page 59).
- Assert PROG_B Low.

The POR circuit does not monitor the VCCO_4 supply after configuration. Consequently, dropping the VCCO_4 voltage does not reset the device by triggering a Power-On Reset (POR) event.

No Internal Charge Pumps or Free-Running Oscillators

Some system applications are sensitive to sources of analog noise. Spartan-3 FPGA circuitry is fully static and does not employ internal charge pumps.

The CCLK configuration clock is active during the FPGA configuration process. After configuration completes, the CCLK oscillator is automatically disabled unless the Bitstream Generator (BitGen) option ***Persist=Yes***. See Module 4: Table 80, page 125.

Spartan-3 FPGAs optionally support a featured called Digitally Controlled Impedance (DCI). When used in an application, the DCI logic uses an internal oscillator. The DCI logic is only enabled if the FPGA application specifies an I/O standard that requires DCI (LVDCI_33, LVDCI_25, etc.). If DCI is not used, the associated internal oscillator is also disabled.

In summary, unless an application uses the ***Persist=Yes*** option or specifies a DCI I/O standard, an FPGA with no external switching remains fully static.

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
HSLVDCI_25			0.27	0.31	ns
HSLVDCI_33			0.28	0.32	ns
HSTL_I			0.60	0.69	ns
HSTL_I_DCI			0.59	0.68	ns
HSTL_III			0.19	0.22	ns
HSTL_III_DCI			0.20	0.23	ns
HSTL_I_18			0.18	0.21	ns
HSTL_I_DCI_18			0.17	0.19	ns
HSTL_II_18			–0.02	–0.01	ns
HSTL_II_DCI_18			0.75	0.86	ns
HSTL_III_18			0.28	0.32	ns
HSTL_III_DCI_18			0.28	0.32	ns
LVCMOS12	Slow	2 mA	7.60	8.73	ns
		4 mA	7.42	8.53	ns
		6 mA	6.67	7.67	ns
	Fast	2 mA	3.16	3.63	ns
		4 mA	2.70	3.10	ns
		6 mA	2.41	2.77	ns
LVCMOS15	Slow	2 mA	4.55	5.23	ns
		4 mA	3.76	4.32	ns
		6 mA	3.57	4.11	ns
		8 mA	3.55	4.09	ns
		12 mA	3.00	3.45	ns
	Fast	2 mA	3.11	3.57	ns
		4 mA	1.71	1.96	ns
		6 mA	1.44	1.66	ns
		8 mA	1.26	1.44	ns
		12 mA	1.11	1.27	ns
LVDCI_15			1.51	1.74	ns
LVDCI_DV2_15			1.32	1.52	ns

Table 47: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS33	Slow	2 mA	6.38	7.34	ns
		4 mA	4.83	5.55	ns
		6 mA	4.01	4.61	ns
		8 mA	3.92	4.51	ns
		12 mA	2.91	3.35	ns
		16 mA	2.81	3.23	ns
		24 mA	2.49	2.86	ns
	Fast	2 mA	3.86	4.44	ns
		4 mA	1.87	2.15	ns
		6 mA	0.62	0.71	ns
		8 mA	0.61	0.70	ns
		12 mA	0.16	0.19	ns
		16 mA	0.14	0.16	ns
		24 mA	0.06	0.07	ns
LVDCI_33			0.28	0.32	ns
LVDCI_DV2_33			0.26	0.30	ns
LVTTL	Slow	2 mA	7.27	8.36	ns
		4 mA	4.94	5.69	ns
		6 mA	3.98	4.58	ns
		8 mA	3.98	4.58	ns
		12 mA	2.97	3.42	ns
		16 mA	2.84	3.26	ns
		24 mA	2.65	3.04	ns
	Fast	2 mA	4.32	4.97	ns
		4 mA	1.87	2.15	ns
		6 mA	1.27	1.47	ns
		8 mA	1.19	1.37	ns
		12 mA	0.42	0.48	ns
		16 mA	0.27	0.32	ns
		24 mA	0.16	0.18	ns

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair**

Signal Standard (IOSTANDARD)			Package				
			VQ100	TQ144	PQ208	CP132	FT256, FG320, FG456, FG676, FG900, FG1156
Single-Ended Standards							
GTL			0	0	0	1	14
GTL_DCI			0	0	0	1	14
GTLP			0	0	0	1	19
GTLP_DCI			0	0	0	1	19
HSLVDCI_15			6	6	6	6	14
HSLVDCI_18			7	7	7	7	10
HSLVDCI_25			7	7	7	7	11
HSLVDCI_33			10	10	10	10	10
HSTL_I			11	11	11	11	17
HSTL_I_DCI			11	11	11	11	17
HSTL_III			7	7	7	7	7
HSTL_III_DCI			7	7	7	7	7
HSTL_I_18			13	13	13	13	17
HSTL_I_DCI_18			13	13	13	13	17
HSTL_II_18			9	9	9	9	9
HSTL_II_DCI_18			9	9	9	9	9
HSTL_III_18			8	8	8	8	8
HSTL_III_DCI_18			8	8	8	8	8
LVCMOS12	Slow	2	17	17	17	17	55
		4	13	13	13	13	32
		6	10	10	10	10	18
	Fast	2	12	12	12	12	31
		4	11	11	11	11	13
		6	9	9	9	9	9
LVCMOS15	Slow	2	16	12	12	19	55
		4	8	7	7	9	31
		6	7	7	7	9	18
		8	6	6	6	6	15
		12	5	5	5	5	10
	Fast	2	10	10	10	13	25
		4	6	7	7	7	16
		6	7	7	7	7	13
		8	6	6	6	6	11
		12	6	6	6	6	7

Table 69: **Types of Pins on Spartan-3 FPGAs *(Cont'd)***

Pin Type/ Color Code	Description	Pin Name
VREF	Dual-purpose pin that is either a user-I/O pin or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IO/VREF_# IO_Lxxy_#/VREF_#
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. All must be connected to +2.5V.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V.	VCCINT
VCCO	Dedicated I/O bank, output buffer power supply pin. Along with other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards.	VCCO_# **CP132 and TQ144 Packages Only:** VCCO_LEFT, VCCO_TOP, VCCO_RIGHT, VCCO_BOTTOM
GCLK	Dual-purpose pin that is either a user-I/O pin or an input to a specific global buffer input. Every package has eight dedicated GCLK pins.	IO_Lxxy_#/GCLK0, IO_Lxxy_#/GCLK1, IO_Lxxy_#/GCLK2, IO_Lxxy_#/GCLK3, IO_Lxxy_#/GCLK4, IO_Lxxy_#/GCLK5, IO_Lxxy_#/GCLK6, IO_Lxxy_#/GCLK7
N.C.	This package pin is not connected in this specific device/package combination but may be connected in larger devices in the same package.	N.C.

Notes:

1. # = I/O bank number, an integer between 0 and 7.

I/Os with Lxxy_# are part of a differential output pair. 'L' indicates differential output capability. The "xx" field is a two-digit integer, unique to each bank that identifies a differential pin-pair. The 'y' field is either 'P' for the true signal or 'N' for the inverted signal in the differential pair. The '#' field is the I/O bank number.

Pin Definitions

Table 70 provides a brief description of each pin listed in the Spartan-3 FPGA pinout tables and package footprint diagrams. Pins are categorized by their pin type, as listed in Table 69. See Detailed, Functional Pin Descriptions for more information.

Table 70: **Spartan-3 FPGA Pin Definitions**

Pin Name	Direction	Description
I/O: General-purpose I/O pins		
I/O	User-defined as input, output, bidirectional, three-state output, open-drain output, open-source output	**User I/O:** Unrestricted single-ended user-I/O pin. Supports all I/O standards except the differential standards.
I/O_Lxxy_#	User-defined as input, output, bidirectional, three-state output, open-drain output, open-source output	**User I/O, Half of Differential Pair:** Unrestricted single-ended user-I/O pin or half of a differential pair. Supports all I/O standards including the differential standards.
DUAL: Dual-purpose configuration pins		
IO_Lxxy_#/DIN/D0, IO_Lxxy_#/D1, IO_Lxxy_#/D2, IO_Lxxy_#/D3, IO_Lxxy_#/D4, IO_Lxxy_#/D5, IO_Lxxy_#/D6, IO_Lxxy_#/D7	Input during configuration Possible bidirectional I/O after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Configuration Data Port:** In Parallel (SelectMAP) modes, D0-D7 are byte-wide configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained via the Persist bitstream option. In Serial modes, DIN (D0) serves as the single configuration data input. This pin becomes a user I/O after configuration unless retained by the Persist bitstream option.
IO_Lxxy_#/CS_B	Input during Parallel mode configuration Possible input after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Chip Select for Parallel Mode Configuration:** In Parallel (SelectMAP) modes, this is the active-Low Chip Select signal. This pin becomes a user I/O after configuration unless the SelectMAP port is retained via the Persist bitstream option.
IO_Lxxy_#/RDWR_B	Input during Parallel mode configuration Possible input after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Read/Write Control for Parallel Mode Configuration:** In Parallel (SelectMAP) modes, this is the active-Low Write Enable, active-High Read Enable signal. This pin becomes a user I/O after configuration unless the SelectMAP port is retained via the Persist bitstream option.
IO_Lxxy_#/ BUSY/DOUT	Output during configuration Possible output after configuration if SelectMap port is retained Otherwise, user I/O after configuration	**Configuration Data Rate Control for Parallel Mode, Serial Data Output for Serial Mode:** In Parallel (SelectMAP) modes, BUSY throttles the rate at which configuration data is loaded. This pin becomes a user I/O after configuration unless the SelectMAP port is retained via the Persist bitstream option. In Serial modes, DOUT provides preamble and configuration data to downstream devices in a multi-FPGA daisy-chain. This pin becomes a user I/O after configuration.
IO_Lxxy_#/INIT_B	Bidirectional (open-drain) during configuration User I/O after configuration	**Initializing Configuration Memory/Detected Configuration Error:** When Low, this pin indicates that configuration memory is being cleared. When held Low, this pin delays the start of configuration. After this pin is released or configuration memory is cleared, the pin goes High. During configuration, a Low on this output indicates that a configuration data error occurred. This pin always has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM during configuration, regardless of the HSWAP_EN pin. This pin becomes a user I/O after configuration.
DCI: Digitally Controlled Impedance reference resistor input pins		
IO_Lxxy_#/VRN_# or IO/VRN_#	Input when using DCI Otherwise, same as I/O	**DCI Reference Resistor for NMOS I/O Transistor (per bank):** If using DCI, a 1% precision impedance-matching resistor is connected between this pin and the VCCO supply for this bank. Otherwise, this pin is a user I/O.
IO_Lxxy_#/VRP_# or IO/VRP_#	Input when using DCI Otherwise, same as I/O	**DCI Reference Resistor for PMOS I/O Transistor (per bank):** If using DCI, a 1% precision impedance-matching resistor is connected between this pin and the ground supply. Otherwise, this pin is a user I/O.

Table 91: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
2	IO_L23N_2/VREF_2	P98	VREF
2	IO_L23P_2	P97	I/O
2	IO_L24N_2	P96	I/O
2	IO_L24P_2	P95	I/O
2	IO_L40N_2	P93	I/O
2	IO_L40P_2/VREF_2	P92	VREF
3	IO	P76	I/O
3	IO_L01N_3/VRP_3	P74	DCI
3	IO_L01P_3/VRN_3	P73	DCI
3	IO_L20N_3	P78	I/O
3	IO_L20P_3	P77	I/O
3	IO_L21N_3	P80	I/O
3	IO_L21P_3	P79	I/O
3	IO_L22N_3	P83	I/O
3	IO_L22P_3	P82	I/O
3	IO_L23N_3	P85	I/O
3	IO_L23P_3/VREF_3	P84	VREF
3	IO_L24N_3	P87	I/O
3	IO_L24P_3	P86	I/O
3	IO_L40N_3/VREF_3	P90	VREF
3	IO_L40P_3	P89	I/O
4	IO/VREF_4	P70	VREF
4	IO_L01N_4/VRP_4	P69	DCI
4	IO_L01P_4/VRN_4	P68	DCI
4	IO_L27N_4/DIN/D0	P65	DUAL
4	IO_L27P_4/D1	P63	DUAL
4	IO_L30N_4/D2	P60	DUAL
4	IO_L30P_4/D3	P59	DUAL
4	IO_L31N_4/INIT_B	P58	DUAL
4	IO_L31P_4/DOUT/BUSY	P57	DUAL
4	IO_L32N_4/GCLK1	P56	GCLK
4	IO_L32P_4/GCLK0	P55	GCLK
5	IO/VREF_5	P44	VREF
5	IO_L01N_5/RDWR_B	P41	DUAL
5	IO_L01P_5/CS_B	P40	DUAL
5	IO_L28N_5/D6	P47	DUAL
5	IO_L28P_5/D7	P46	DUAL
5	IO_L31N_5/D4	P51	DUAL
5	IO_L31P_5/D5	P50	DUAL
5	IO_L32N_5/GCLK3	P53	GCLK

Table 91: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
6,7	VCCO_LEFT	P34	VCCO
6,7	VCCO_LEFT	P3	VCCO
N/A	GND	P136	GND
N/A	GND	P139	GND
N/A	GND	P114	GND
N/A	GND	P117	GND
N/A	GND	P94	GND
N/A	GND	P101	GND
N/A	GND	P81	GND
N/A	GND	P88	GND
N/A	GND	P64	GND
N/A	GND	P67	GND
N/A	GND	P42	GND
N/A	GND	P45	GND
N/A	GND	P22	GND
N/A	GND	P29	GND
N/A	GND	P9	GND
N/A	GND	P16	GND
N/A	VCCAUX	P134	VCCAUX
N/A	VCCAUX	P120	VCCAUX
N/A	VCCAUX	P62	VCCAUX
N/A	VCCAUX	P48	VCCAUX
N/A	VCCINT	P133	VCCINT
N/A	VCCINT	P121	VCCINT
N/A	VCCINT	P61	VCCINT
N/A	VCCINT	P49	VCCINT
VCCAUX	CCLK	P72	CONFIG
VCCAUX	DONE	P71	CONFIG
VCCAUX	HSWAP_EN	P142	CONFIG
VCCAUX	M0	P38	CONFIG
VCCAUX	M1	P37	CONFIG
VCCAUX	M2	P39	CONFIG
VCCAUX	PROG_B	P143	CONFIG
VCCAUX	TCK	P110	JTAG
VCCAUX	TDI	P144	JTAG
VCCAUX	TDO	P109	JTAG
VCCAUX	TMS	P111	JTAG

TQ144 Footprint

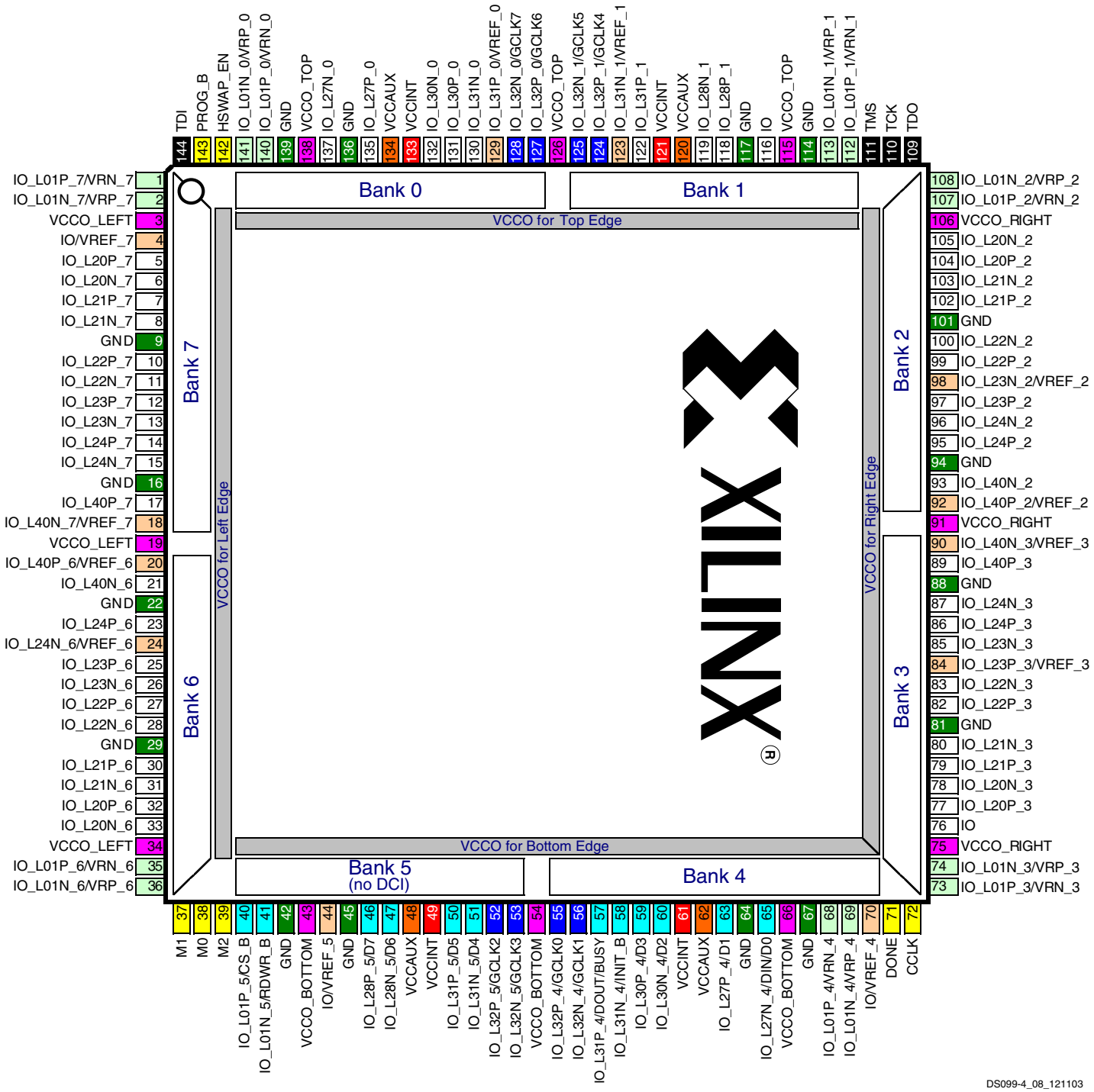


Figure 46: **TQ144 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

51 **I/O:** Unrestricted, general-purpose user I/O	12 **DUAL:** Configuration pin, then possible user I/O	12 **VREF:** User I/O or input voltage reference for bank
14 **DCI:** User I/O or reference resistor input for bank	8 **GCLK:** User I/O or global clock buffer input	12 **VCCO:** Output voltage supply for bank
7 **CONFIG:** Dedicated configuration pins	4 **JTAG:** Dedicated JTAG port pins	4 **VCCINT:** Internal core voltage supply (+1.2V)
0 **N.C.:** No unconnected pins in this package	16 **GND:** Ground	4 **VCCAUX:** Auxiliary voltage supply (+2.5V)

PQ208 Footprint

Left Half of Package (Top View)

XC3S50
(124 max. user I/O)

72 **I/O:** Unrestricted, general-purpose user I/O

16 **VREF:** User I/O or input voltage reference for bank

17 **N.C.:** Unconnected pins for XC3S50 (◆)

XC3S200, XC3S400
(141 max user I/O)

83 **I/O:** Unrestricted, general-purpose user I/O

22 **VREF:** User I/O or input voltage reference for bank

0 **N.C.:** No unconnected pins in this package

All devices

12 **DUAL:** Configuration pin, then possible user I/O

8 **GCLK:** User I/O or global clock buffer input

16 **DCI:** User I/O or reference resistor input for bank

7 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

4 **VCCINT:** Internal core voltage supply (+1.2V)

12 **VCCO:** Output voltage supply for bank

8 **VCCAUX:** Auxiliary voltage supply (+2.5V)

28 **GND:** Ground

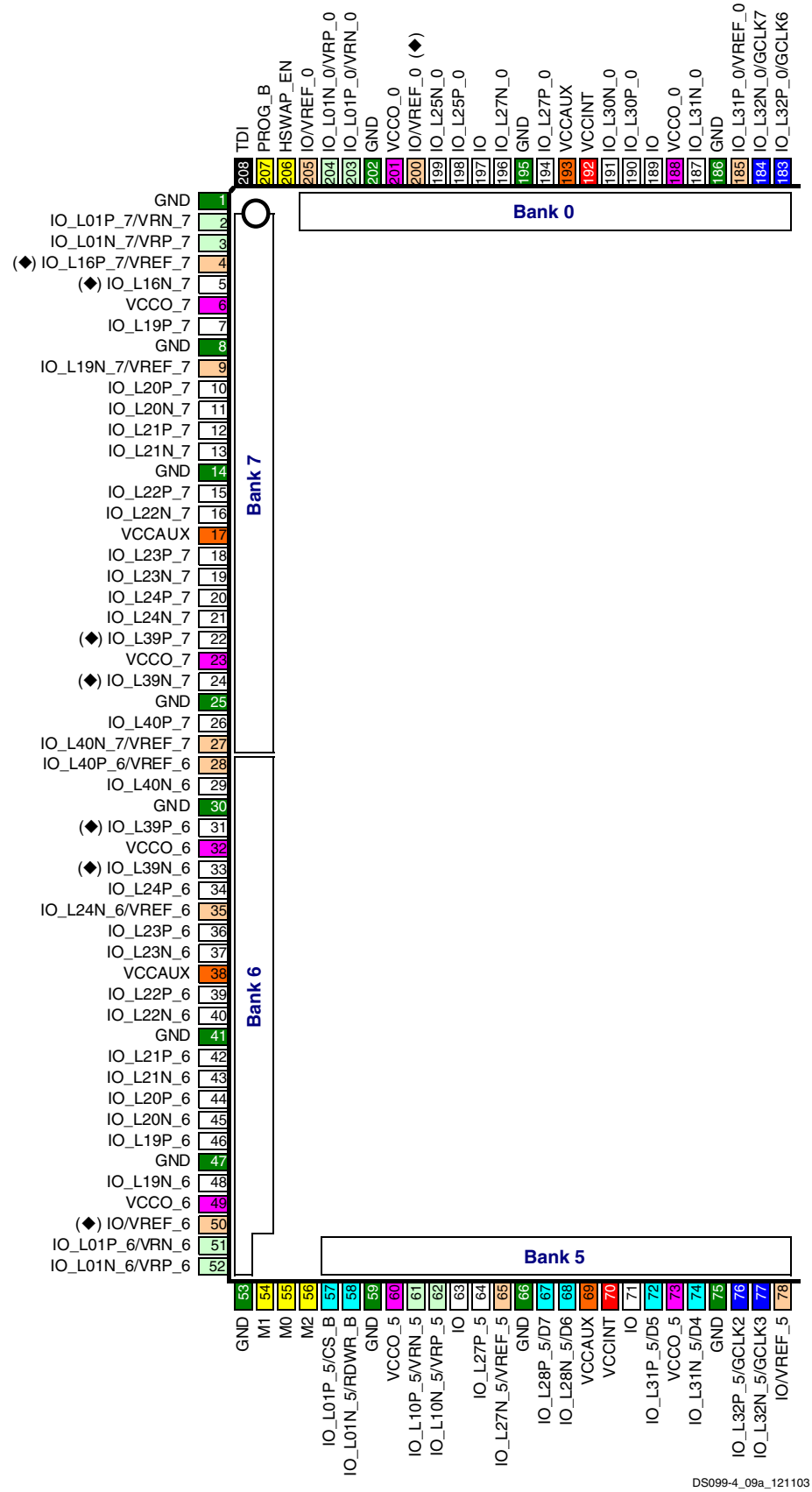


Figure 47: **PQ208 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

User I/Os by Bank

Table 97 indicates how the available user-I/O pins are distributed between the eight I/O banks on the FT256 package.

Table 97: **User I/Os Per Bank in FT256 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	20	13	0	2	3	2
	1	20	13	0	2	3	2
Right	2	23	18	0	2	3	0
	3	23	18	0	2	3	0
Bottom	4	21	8	6	2	3	2
	5	20	7	6	2	3	2
Left	6	23	18	0	2	3	0
	7	23	18	0	2	3	0

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO_L10N_0	IO_L10N_0	J9	I/O
0	IO_L10P_0	IO_L10P_0	H9	I/O
0	IO_L11N_0	IO_L11N_0	G10	I/O
0	IO_L11P_0	IO_L11P_0	F10	I/O
0	IO_L12N_0	IO_L12N_0	C10	I/O
0	IO_L12P_0	IO_L12P_0	B10	I/O
0	IO_L13N_0	IO_L13N_0	J10	I/O
0	IO_L13P_0	IO_L13P_0	K11	I/O
0	IO_L14N_0	IO_L14N_0	H11	I/O
0	IO_L14P_0	IO_L14P_0	G11	I/O
0	IO_L15N_0	IO_L15N_0	F11	I/O
0	IO_L15P_0	IO_L15P_0	E11	I/O
0	IO_L16N_0	IO_L16N_0	D11	I/O
0	IO_L16P_0	IO_L16P_0	C11	I/O
0	IO_L17N_0	IO_L17N_0	B11	I/O
0	IO_L17P_0	IO_L17P_0	A11	I/O
0	IO_L18N_0	IO_L18N_0	K12	I/O
0	IO_L18P_0	IO_L18P_0	J12	I/O
0	IO_L19N_0	IO_L19N_0	H12	I/O
0	IO_L19P_0	IO_L19P_0	G12	I/O
0	IO_L20N_0	IO_L20N_0	F12	I/O
0	IO_L20P_0	IO_L20P_0	E12	I/O
0	IO_L21N_0	IO_L21N_0	D12	I/O
0	IO_L21P_0	IO_L21P_0	C12	I/O
0	IO_L22N_0	IO_L22N_0	B12	I/O
0	IO_L22P_0	IO_L22P_0	A12	I/O
0	IO_L23N_0	IO_L23N_0	J13	I/O
0	IO_L23P_0	IO_L23P_0	H13	I/O
0	IO_L24N_0	IO_L24N_0	F13	I/O
0	IO_L24P_0	IO_L24P_0	E13	I/O
0	IO_L25N_0	IO_L25N_0	B13	I/O
0	IO_L25P_0	IO_L25P_0	A13	I/O
0	IO_L26N_0	IO_L26N_0	K14	I/O
0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	J14	VREF
0	IO_L27N_0	IO_L27N_0	G14	I/O
0	IO_L27P_0	IO_L27P_0	F14	I/O
0	IO_L28N_0	IO_L28N_0	C14	I/O
0	IO_L28P_0	IO_L28P_0	B14	I/O
0	IO_L29N_0	IO_L29N_0	J15	I/O
0	IO_L29P_0	IO_L29P_0	H15	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
1	IO_L25P_1	IO_L25P_1	D19	I/O
1	IO_L26N_1	IO_L26N_1	A19	I/O
1	IO_L26P_1	IO_L26P_1	B19	I/O
1	IO_L27N_1	IO_L27N_1	F17	I/O
1	IO_L27P_1	IO_L27P_1	G17	I/O
1	IO_L28N_1	IO_L28N_1	B17	I/O
1	IO_L28P_1	IO_L28P_1	C17	I/O
1	IO_L29N_1	IO_L29N_1	J16	I/O
1	IO_L29P_1	IO_L29P_1	K16	I/O
1	IO_L30N_1	IO_L30N_1	G16	I/O
1	IO_L30P_1	IO_L30P_1	H16	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D16	VREF
1	IO_L31P_1	IO_L31P_1	E16	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B16	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C16	GCLK
1	N.C. (◆)	IO_L37N_1	H18	I/O
1	N.C. (◆)	IO_L37P_1	J18	I/O
1	N.C. (◆)	IO_L38N_1	D18	I/O
1	N.C. (◆)	IO_L38P_1	E18	I/O
1	N.C. (◆)	IO_L39N_1	A18	I/O
1	N.C. (◆)	IO_L39P_1	B18	I/O
1	N.C. (◆)	IO_L40N_1	K17	I/O
1	N.C. (◆)	IO_L40P_1	K18	I/O
1	VCCO_1	VCCO_1	L17	VCCO
1	VCCO_1	VCCO_1	C18	VCCO
1	VCCO_1	VCCO_1	G18	VCCO
1	VCCO_1	VCCO_1	L18	VCCO
1	VCCO_1	VCCO_1	L19	VCCO
1	VCCO_1	VCCO_1	J20	VCCO
1	VCCO_1	VCCO_1	C22	VCCO
1	VCCO_1	VCCO_1	G22	VCCO
1	VCCO_1	VCCO_1	E24	VCCO
1	VCCO_1	VCCO_1	C26	VCCO
2	IO	IO	J25	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C29	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C30	DCI
2	IO_L02N_2	IO_L02N_2	D27	I/O
2	IO_L02P_2	IO_L02P_2	D28	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	D29	VREF
2	IO_L03P_2	IO_L03P_2	D30	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	IO_L04N_2	IO_L04N_2	E29	I/O
2	IO_L04P_2	IO_L04P_2	E30	I/O
2	IO_L05N_2	IO_L05N_2	F28	I/O
2	IO_L05P_2	IO_L05P_2	F29	I/O
2	IO_L06N_2	IO_L06N_2	G27	I/O
2	IO_L06P_2	IO_L06P_2	G28	I/O
2	IO_L07N_2	IO_L07N_2	G29	I/O
2	IO_L07P_2	IO_L07P_2	G30	I/O
2	IO_L08N_2	IO_L08N_2	G25	I/O
2	IO_L08P_2	IO_L08P_2	H24	I/O
2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	H25	VREF
2	IO_L09P_2	IO_L09P_2	H26	I/O
2	IO_L10N_2	IO_L10N_2	H27	I/O
2	IO_L10P_2	IO_L10P_2	H28	I/O
2	IO_L12N_2	IO_L12N_2	H29	I/O
2	IO_L12P_2	IO_L12P_2	H30	I/O
2	IO_L13N_2	IO_L13N_2	J26	I/O
2	IO_L13P_2/VREF_2	IO_L13P_2/VREF_2	J27	VREF
2	IO_L14N_2	IO_L14N_2	J29	I/O
2	IO_L14P_2	IO_L14P_2	J30	I/O
2	IO_L15N_2	IO_L15N_2	J23	I/O
2	IO_L15P_2	IO_L15P_2	K22	I/O
2	IO_L16N_2	IO_L16N_2	K24	I/O
2	IO_L16P_2	IO_L16P_2	K25	I/O
2	IO_L19N_2	IO_L19N_2	L25	I/O
2	IO_L19P_2	IO_L19P_2	L26	I/O
2	IO_L20N_2	IO_L20N_2	L27	I/O
2	IO_L20P_2	IO_L20P_2	L28	I/O
2	IO_L21N_2	IO_L21N_2	L29	I/O
2	IO_L21P_2	IO_L21P_2	L30	I/O
2	IO_L22N_2	IO_L22N_2	M22	I/O
2	IO_L22P_2	IO_L22P_2	M23	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	M24	VREF
2	IO_L23P_2	IO_L23P_2	M25	I/O
2	IO_L24N_2	IO_L24N_2	M27	I/O
2	IO_L24P_2	IO_L24P_2	M28	I/O
2	IO_L26N_2	IO_L26N_2	M21	I/O
2	IO_L26P_2	IO_L26P_2	N21	I/O
2	IO_L27N_2	IO_L27N_2	N22	I/O
2	IO_L27P_2	IO_L27P_2	N23	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	GND	GND	K30	GND
N/A	GND	GND	P30	GND
N/A	GND	GND	U30	GND
N/A	GND	GND	AA30	GND
N/A	GND	GND	AE30	GND
N/A	GND	GND	AJ30	GND
N/A	GND	GND	AK30	GND
N/A	GND	GND	AK2	GND
N/A	VCCAUX	VCCAUX	F4	VCCAUX
N/A	VCCAUX	VCCAUX	K4	VCCAUX
N/A	VCCAUX	VCCAUX	P4	VCCAUX
N/A	VCCAUX	VCCAUX	U4	VCCAUX
N/A	VCCAUX	VCCAUX	AA4	VCCAUX
N/A	VCCAUX	VCCAUX	AE4	VCCAUX
N/A	VCCAUX	VCCAUX	D6	VCCAUX
N/A	VCCAUX	VCCAUX	AG6	VCCAUX
N/A	VCCAUX	VCCAUX	D10	VCCAUX
N/A	VCCAUX	VCCAUX	AG10	VCCAUX
N/A	VCCAUX	VCCAUX	D14	VCCAUX
N/A	VCCAUX	VCCAUX	AG14	VCCAUX
N/A	VCCAUX	VCCAUX	D17	VCCAUX
N/A	VCCAUX	VCCAUX	AG17	VCCAUX
N/A	VCCAUX	VCCAUX	D21	VCCAUX
N/A	VCCAUX	VCCAUX	AG21	VCCAUX
N/A	VCCAUX	VCCAUX	D25	VCCAUX
N/A	VCCAUX	VCCAUX	AG25	VCCAUX
N/A	VCCAUX	VCCAUX	F27	VCCAUX
N/A	VCCAUX	VCCAUX	K27	VCCAUX
N/A	VCCAUX	VCCAUX	P27	VCCAUX
N/A	VCCAUX	VCCAUX	U27	VCCAUX
N/A	VCCAUX	VCCAUX	AA27	VCCAUX
N/A	VCCAUX	VCCAUX	AE27	VCCAUX
N/A	VCCINT	VCCINT	L11	VCCINT
N/A	VCCINT	VCCINT	R11	VCCINT
N/A	VCCINT	VCCINT	T11	VCCINT
N/A	VCCINT	VCCINT	Y11	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	N12	VCCINT
N/A	VCCINT	VCCINT	P12	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	C2	DCI
7	IO_L02N_7	IO_L02N_7	D1	I/O
7	IO_L02P_7	IO_L02P_7	D2	I/O
7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	E2	VREF
7	IO_L03P_7	IO_L03P_7	E3	I/O
7	IO_L04N_7	IO_L04N_7	F3	I/O
7	IO_L04P_7	IO_L04P_7	F4	I/O
7	IO_L05N_7	IO_L05N_7	F1	I/O
7	IO_L05P_7	IO_L05P_7	F2	I/O
7	IO_L06N_7	IO_L06N_7	G5	I/O
7	IO_L06P_7	IO_L06P_7	G6	I/O
7	IO_L07N_7	IO_L07N_7	H5	I/O
7	IO_L07P_7	IO_L07P_7	H6	I/O
7	IO_L08N_7	IO_L08N_7	H1	I/O
7	IO_L08P_7	IO_L08P_7	H2	I/O
7	IO_L09N_7	IO_L09N_7	J6	I/O
7	IO_L09P_7	IO_L09P_7	J7	I/O
7	IO_L10N_7	IO_L10N_7	J4	I/O
7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	H4	VREF
7	IO_L11N_7	IO_L11N_7	J2	I/O
7	IO_L11P_7	IO_L11P_7	J3	I/O
7	IO_L12N_7	IO_L12N_7	K9	I/O
7	IO_L12P_7	IO_L12P_7	J8	I/O
7	IO_L13N_7	IO_L13N_7	K7	I/O
7	IO_L13P_7	IO_L13P_7	K8	I/O
7	IO_L14N_7	IO_L14N_7	K5	I/O
7	IO_L14P_7	IO_L14P_7	K6	I/O
7	IO_L15N_7	IO_L15N_7	K3	I/O
7	IO_L15P_7	IO_L15P_7	K4	I/O
7	IO_L16N_7	IO_L16N_7	K1	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	K2	VREF
7	IO_L17N_7	IO_L17N_7	L9	I/O
7	IO_L17P_7	IO_L17P_7	L10	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	L1	VREF
7	IO_L19P_7	IO_L19P_7	L2	I/O
7	IO_L20N_7	IO_L20N_7	M10	I/O
7	IO_L20P_7	IO_L20P_7	M11	I/O
7	IO_L21N_7	IO_L21N_7	M7	I/O
7	IO_L21P_7	IO_L21P_7	M8	I/O
7	IO_L22N_7	IO_L22N_7	M5	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
7	IO_L22P_7	IO_L22P_7	M6	I/O
7	IO_L23N_7	IO_L23N_7	M3	I/O
7	IO_L23P_7	IO_L23P_7	M4	I/O
7	IO_L24N_7	IO_L24N_7	N10	I/O
7	IO_L24P_7	IO_L24P_7	M9	I/O
7	IO_L25N_7	IO_L25N_7	N3	I/O
7	IO_L25P_7	IO_L25P_7	N4	I/O
7	IO_L26N_7	IO_L26N_7	P11	I/O
7	IO_L26P_7	IO_L26P_7	N11	I/O
7	IO_L27N_7	IO_L27N_7	P7	I/O
7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	P8	VREF
7	IO_L28N_7	IO_L28N_7	P5	I/O
7	IO_L28P_7	IO_L28P_7	P6	I/O
7	IO_L29N_7	IO_L29N_7	P3	I/O
7	IO_L29P_7	IO_L29P_7	P4	I/O
7	IO_L30N_7	IO_L30N_7	R6	I/O
7	IO_L30P_7	IO_L30P_7	R7	I/O
7	IO_L31N_7	IO_L31N_7	R3	I/O
7	IO_L31P_7	IO_L31P_7	R4	I/O
7	IO_L32N_7	IO_L32N_7	R1	I/O
7	IO_L32P_7	IO_L32P_7	R2	I/O
7	IO_L33N_7	IO_L33N_7	T10	I/O
7	IO_L33P_7	IO_L33P_7	R9	I/O
7	IO_L34N_7	IO_L34N_7	T6	I/O
7	IO_L34P_7	IO_L34P_7	T7	I/O
7	IO_L35N_7	IO_L35N_7	T2	I/O
7	IO_L35P_7	IO_L35P_7	T3	I/O
7	IO_L37N_7	IO_L37N_7	U7	I/O
7	IO_L37P_7/VREF_7	IO_L37P_7/VREF_7	U8	VREF
7	IO_L38N_7	IO_L38N_7	U5	I/O
7	IO_L38P_7	IO_L38P_7	U6	I/O
7	IO_L39N_7	IO_L39N_7	U3	I/O
7	IO_L39P_7	IO_L39P_7	U4	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	U1	VREF
7	IO_L40P_7	IO_L40P_7	U2	I/O
7	N.C. (◆)	IO_L41N_7	G3	I/O
7	N.C. (◆)	IO_L41P_7	G4	I/O
7	N.C. (◆)	IO_L44N_7	L6	I/O
7	N.C. (◆)	IO_L44P_7	L7	I/O
7	IO_L45N_7	IO_L45N_7	M1	I/O

Revision History

Date	Version	Description
04/03/03	1.0	Initial Xilinx release.
04/21/03	1.1	Added information on the VQ100 package footprint, including a complete pinout table (Table 87) and footprint diagram (Figure 44). Updated Table 85 with final I/O counts for the VQ100 package. Also added final differential I/O pair counts for the TQ144 package. Added clarifying comments to HSWAP_EN pin description on page 119. Updated the footprint diagram for the FG900 package shown in Figure 55a and Figure 55b. Some thick lines separating I/O banks were incorrect. Made cosmetic changes to Figure 40, Figure 42, and Figure 43. Updated Xilinx hypertext links. Added XC3S200 and XC3S400 to Pin Name column in Table 91.
05/12/03	1.1.1	AM32 pin was missing GND label in FG1156 package diagram (Figure 53).
07/11/03	1.1.2	Corrected misspellings of GCLK in Table 69 and Table 70. Changed CMOS25 to LVCMOS25 in Dual-Purpose Pin I/O Standard During Configuration section. Clarified references to Module 2. For XC3S5000 in FG1156 package, corrected N.C. symbol to a black square in Table 110, key, and package drawing.
07/29/03	1.2	Corrected pin names on FG1156 package. Some package balls incorrectly included LVDS pair names. The affected balls on the FG1156 package include G1, G2, G33, G34, U9, U10, U25, U26, V9, V10, V25, V26, AH1, AH2, AH33, AH34. The number of LVDS pairs is unaffected. Modified affected balls and re-sorted rows in Table 110. Updated affected balls in Figure 53. Also updated ASCII and Excel electronic versions of FG1156 pinout.
08/19/03	1.2.1	Removed 100 MHz ConfigRate option in CCLK: Configuration Clock section and in Table 80. Added note that TDO is a totem-pole output in Table 77.
10/09/03	1.2.2	Some pins had incorrect bank designations and were improperly sorted in Table 93. No pin names or functions changed. Renamed DCI_IN to DCI and added black diamond to N.C. pins in Table 93. In Figure 47, removed some extraneous text from pin 106 and corrected spelling of pins 45, 48, and 81.
12/17/03	1.3	Added FG320 pin tables and pinout diagram (FG320: 320-lead Fine-pitch Ball Grid Array). Made cosmetic changes to the TQ144 footprint (Figure 46), the PQ208 footprint (Figure 47), the FG676 footprint (Figure 53), and the FG900 footprint (Figure 55). Clarified wording in Precautions When Using the JTAG Port in 3.3V Environments section.
02/27/04	1.4	Clarified wording in Using JTAG Port After Configuration section. In Table 81, reduced package height for FG320 and increased maximum I/O values for the FG676, FG900, and FG1156 packages.
07/13/04	1.5	Added information on lead-free (Pb-free) package options to the Package Overview section plus Table 81 and Table 83. Clarified the VRN_# reference resistor requirements for I/O standards that use single termination as described in the DCI Termination Types section and in Figure 42b. Graduated from Advance Product Specification to Product Specification.
08/24/04	1.5.1	Removed XC3S2000 references from FG1156: 1156-lead Fine-pitch Ball Grid Array.
01/17/05	1.6	Added XC3S50 in CP132 package option. Added XC3S2000 in FG456 package option. Added XC3S4000 in FG676 package option. Added Selecting the Right Package Option section. Modified or added Table 81, Table 83, Table 84, Table 85, Table 89, Table 90, Table 100, Table 102, Table 103, Table 106, Figure 45, and Figure 53.
08/19/05	1.7	Removed term “weak” from the description of pull-up and pull-down resistors. Added IDCODE Register values. Added signal integrity precautions to CCLK: Configuration Clock and indicated that CCLK should be treated as an I/O during Master mode in Table 79.
04/03/06	2.0	Added Package Thermal Characteristics. Updated Figure 41 to make it a more obvious example. Added detail about which pins have dedicated pull-up resistors during configuration, regardless of the HSWAP_EN value to Table 70 and to Pin Behavior During Configuration. Updated Precautions When Using the JTAG Port in 3.3V Environments.
04/26/06	2.1	Corrected swapped data row in Table 86. The Theta-JA with zero airflow column was swapped with the Theta-JC column. Made additional notations on CONFIG and JTAG pins that have pull-up resistors during configuration, regardless of the HSWAP_EN input.
05/25/07	2.2	Added link on page 128 to Material Declaration Data Sheets. Corrected units typo in Table 74. Added Note 1 to Table 103 about VREF for XC3S1500 in FG676.