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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	294912
Number of I/O	264
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s400-4fgg456i

IOBs

For additional information, refer to the chapter entitled “Using I/O Resources” in [UG331: Spartan-3 Generation FPGA User Guide](#).

IOB Overview

The Input/Output Block (IOB) provides a programmable, bidirectional interface between an I/O pin and the FPGA's internal logic.

A simplified diagram of the IOB's internal structure appears in [Figure 7](#). There are three main signal paths within the IOB: the output path, input path, and 3-state path. Each path has its own pair of storage elements that can act as either registers or latches. For more information, see the [Storage Element Functions](#) section. The three main signal paths are as follows:

- The input path carries data from the pad, which is bonded to a package pin, through an optional programmable delay element directly to the I line. There are alternate routes through a pair of storage elements to the IQ1 and IQ2 lines. The IOB outputs I, IQ1, and IQ2 all lead to the FPGA's internal logic. The delay element can be set to ensure a hold time of zero.
- The output path, starting with the O1 and O2 lines, carries data from the FPGA's internal logic through a multiplexer and then a three-state driver to the IOB pad. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.
- The 3-state path determines when the output driver is high impedance. The T1 and T2 lines carry data from the FPGA's internal logic through a multiplexer to the output driver. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements. When the T1 or T2 lines are asserted High, the output driver is high-impedance (floating, hi-Z). The output driver is active-Low enabled.
- All signal paths entering the IOB, including those associated with the storage elements, have an inverter option. Any inverter placed on these paths is automatically absorbed into the IOB.

Storage Element Functions

There are three pairs of storage elements in each IOB, one pair for each of the three paths. It is possible to configure each of these storage elements as an edge-triggered D-type flip-flop (FD) or a level-sensitive latch (LD).

The storage-element-pair on either the Output path or the Three-State path can be used together with a special multiplexer to produce Double-Data-Rate (DDR) transmission. This is accomplished by taking data synchronized to the clock signal's rising edge and converting them to bits synchronized on both the rising and the falling edge. The combination of two registers and a multiplexer is referred to as a Double-Data-Rate D-type flip-flop (FDDR). See [Double-Data-Rate Transmission, page 12](#) for more information.

The signal paths associated with the storage element are described in [Table 5](#).

Table 5: Storage Element Signal Description

Storage Element Signal	Description	Function
D	Data input	Data at this input is stored on the active edge of CK enabled by CE. For latch operation when the input is enabled, data passes directly to the output Q.
Q	Data output	The data on this output reflects the state of the storage element. For operation as a latch in transparent mode, Q will mirror the data at D.
CK	Clock input	A signal's active edge on this input with CE asserted, loads data into the storage element.
CE	Clock Enable input	When asserted, this input enables CK. If not connected, CE defaults to the asserted state.
SR	Set/Reset	Forces storage element into the state specified by the SRHIGH/SRLOW attributes. The SYNC/ASYNC attribute setting determines if the SR input is synchronized to the clock or not.
REV	Reverse	Used together with SR. Forces storage element into the state opposite from what SR does.

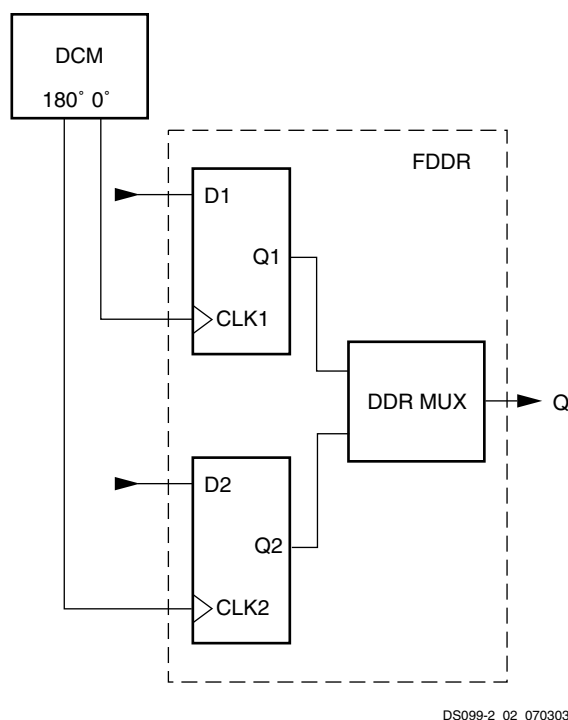


Figure 8: Clocking the DDR Register

Aside from high bandwidth data transfers, DDR can also be used to reproduce, or “mirror”, a clock signal on the output. This approach is used to transmit clock and data signals together. A similar approach is used to reproduce a clock signal at multiple outputs. The advantage for both approaches is that skew across the outputs will be minimal.

Some adjacent I/O blocks (IOBs) share common routing connecting the ICLK1, ICLK2, OTCLK1, and OTCLK2 clock inputs of both IOBs. These IOB pairs are identified by their differential pair names IO_LxxN_# and IO_LxxP_#, where “xx” is an I/O pair number and “#” is an I/O bank number. Two adjacent IOBs containing DDR registers must share common clock inputs, otherwise one or more of the clock signals will be unroutable.

Pull-Up and Pull-Down Resistors

The optional pull-up and pull-down resistors are intended to establish High and Low levels, respectively, at unused I/Os. The pull-up resistor optionally connects each IOB pad to V_{CCO} . A pull-down resistor optionally connects each pad to GND. These resistors are placed in a design using the PULLUP and PULLDOWN symbols in a schematic, respectively. They can also be instantiated as components, set as constraints or passed as attributes in HDL code. These resistors can also be selected for all unused I/O using the Bitstream Generator (BitGen) option UnusedPin. A Low logic level on HSWAP_EN activates the pull-up resistors on all I/Os during configuration (see [The I/Os During Power-On, Configuration, and User Mode, page 21](#)).

The Spartan-3 FPGAs I/O pull-up and pull-down resistors are significantly stronger than the “weak” pull-up/pull-down resistors used in previous Xilinx FPGA families. See [Table 33, page 61](#) for equivalent resistor strengths.

Keeper Circuit

Each I/O has an optional keeper circuit that retains the last logic level on a line after all drivers have been turned off. This is useful to keep bus lines from floating when all connected drivers are in a high-impedance state. This function is placed in a design using the KEEPER symbol. Pull-up and pull-down resistors override the keeper circuit.

Configuration

Spartan-3 devices are configured by loading application specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are "Dedicated" to one function only, while others, indicated by the term "Dual-Purpose", can be re-used as general-purpose User I/Os once configuration is complete.

Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M0, M1, and M2 are Dedicated pins. The mode pin settings are shown in [Table 26](#).

Table 26: Spartan-3 FPGAs Configuration Mode Pin Settings

Configuration Mode ⁽¹⁾	M0	M1	M2	Synchronizing Clock	Data Width	Serial DOUT ⁽²⁾
Master Serial	0	0	0	CCLK Output	1	Yes
Slave Serial	1	1	1	CCLK Input	1	Yes
Master Parallel	1	1	0	CCLK Output	8	No
Slave Parallel	0	1	1	CCLK Input	8	No
JTAG	1	0	1	TCK Input	1	No

Notes:

1. The voltage levels on the M0, M1, and M2 pins select the configuration mode.
2. The daisy chain is possible only in the Serial modes when DOUT is used.

The HSWAP_EN input pin defines whether the I/O pins that are not actively used during configuration have pull-up resistors during configuration. By default, HSWAP_EN is tied High (via an internal pull-up resistor if left floating) which shuts off the pull-up resistors on the user I/O pins during configuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration. The Dedicated configuration pins (CCLK, DONE, PROG_B, M2, M1, M0, HSWAP_EN) and the JTAG pins (TDI, TMS, TCK, and TDO) always have a pull-up resistor to VCCAUX during configuration, regardless of the value on the HSWAP_EN pin. Similarly, the dual-purpose INIT_B pin has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM, depending on the package style.

Depending on the chosen configuration mode, the FPGA either generates a CCLK output, or CCLK is an input accepting an externally generated clock.

A persist option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected then the configuration pins with the exception of CCLK, PROG_B, and DONE can be used as user I/O in normal operation. The persist option does not apply to the boundary-scan related pins. The persist feature is valuable in applications that readback configuration data after entering the User mode.

[Table 27](#) lists the total number of bits required to configure each FPGA as well as the PROMs suitable for storing those bits. See [DS123: Platform Flash In-System Programmable Configuration PROMs](#) data sheet for more information.

Table 27: Spartan-3 FPGA Configuration Data

Device	File Sizes	Xilinx Platform Flash PROM	
		Serial Configuration	Parallel Configuration
XC3S50	439,264	XCF01S	XCF08P
XC3S200	1,047,616	XCF01S	XCF08P
XC3S400	1,699,136	XCF02S	XCF08P
XC3S1000	3,223,488	XCF04S	XCF08P
XC3S1500	5,214,784	XCF08P	XCF08P
XC3S2000	7,673,024	XCF08P	XCF08P
XC3S4000	11,316,864	XCF16P	XCF16P
XC3S5000	13,271,936	XCF16P	XCF16P

The maximum bitstream length that Spartan-3 FPGAs support in serial daisy-chains is 4,294,967,264 bits (4 Gbits), roughly equivalent to a daisy-chain with 323 XC3S5000 FPGAs. This is a limit only for serial daisy-chains where configuration data is passed via the FPGA's DOUT pin. There is no such limit for JTAG chains.

The Standard Configuration Interface

Configuration signals belong to one of two different categories: Dedicated or Dual-Purpose. Which category determines which of the FPGA's power rails supplies the signal's driver and, thus, helps describe the electrical characteristics at the pin.

The Dedicated configuration pins include PROG_B, HSWAP_EN, TDI, TMS, TCK, TDO, CCLK, DONE, and M0-M2. These pins are powered by the V_{CCAUX} supply.

The Dual-Purpose configuration pins comprise INIT_B, DOUT, BUSY, RDWR_B, CS_B, and DIN/D0-D7. Each of these pins, according to its bank placement, uses the V_{CCO} lines for either Bank 4 (V_{CCO_4} on most packages, V_{CCO_BOTTOM} on TQ144 and CP132 packages) or Bank 5 (V_{CCO_5}). All the signals used in the serial configuration modes rely on V_{CCO_4} power. Signals used in the parallel configuration modes and Readback require from V_{CCO_5} as well as from V_{CCO_4} .

Both the Dedicated signals described above and the Dual-Purpose signals constitute the configuration interface. The Dedicated pins, powered by the 2.5V V_{CCAUX} supply, always use the LVCMOS25 I/O standard. The Dual-Purpose signals, however, are powered by the V_{CCO_4} supply and also by the V_{CCO_5} supply in the Parallel configuration modes. The simplest configuration interface uses 2.5V for V_{CCO_4} and V_{CCO_5} , if required. However, V_{CCO_4} and, if needed, V_{CCO_5} can be voltages other than 2.5V but then the configuration interface will have two voltage levels: 2.5V for V_{CCAUX} and a separate V_{CCO} supply. The Dual-Purpose signals default to the LVCMOS input and output levels for the associated V_{CCO} voltage supply.

3.3V-Tolerant Configuration Interface

A 3.3V-tolerant configuration interface simply requires adding a few external resistors as described in detail in [XAPP453: The 3.3V Configuration of Spartan-3 FPGAs](#).

The 3.3V-tolerance is implemented as follows (a similar approach can be used for other supply voltage levels):

Apply 3.3V to V_{CCO_4} and, in some configuration modes, to V_{CCO_5} to power the Dual-Purpose configuration pins. This scales the output voltages and input thresholds associated with these pins so that they become 3.3V-compatible.

Apply 2.5V to V_{CCAUX} to power the Dedicated configuration pins. For 3.3V-tolerance, the Dedicated inputs require series resistors to limit the incoming current to 10 mA or less. The Dedicated outputs have reduced noise margin when the FPGA drives a High logic level into another device's 3.3V receiver. Choose a power regulator or supply that can tolerate reverse current on the V_{CCAUX} lines.

Configuration Modes

Spartan-3 FPGAs support the following five configuration modes:

- Slave Serial mode
- Master Serial mode
- Slave Parallel (SelectMAP) mode
- Master Parallel (SelectMAP) mode
- Boundary-Scan (JTAG) mode (IEEE 1532/IEEE 1149.1)

Slave Serial Mode

In Slave Serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other serial source of configuration data. The FPGA on the far right of [Figure 26](#) is set for the Slave Serial mode. The CCLK pin on the FPGA is an input in this mode. The serial bitstream must be set up at the DIN input pin a short time before each rising edge of the externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the DOUT pin. The data on the DOUT pin changes on the falling edge of CCLK.

Additional Configuration Details

Additional details about the Spartan-3 FPGA configuration architecture and command set are available in [UG332: Spartan-3 Generation Configuration User Guide](#) and in application note [XAPP452: Spartan-3 Advanced Configuration Architecture](#).

Powering Spartan-3 FPGAs

Voltage Regulators

Various power supply manufacturers offer complete power solutions for Xilinx FPGAs, including some with integrated multi-rail regulators specifically designed for Spartan-3 FPGAs. The [Xilinx Power Corner](#) web page provides links to vendor solution guides as well as Xilinx power estimation and analysis tools.

Power Distribution System (PDS) Design and Bypass/Decoupling Capacitors

Good power distribution system (PDS) design is important for all FPGA designs, especially for high-performance applications. Proper design results in better overall performance, lower clock and DCM jitter, and a generally more robust system. Before designing the printed circuit board (PCB) for the FPGA design, review application note [XAPP623: Power Distribution System \(PDS\) Design: Using Bypass/Decoupling Capacitors](#).

Power-On Behavior

Spartan-3 FPGAs have a built-in Power-On Reset (POR) circuit that monitors the three power rails required to successfully configure the FPGA. At power-up, the POR circuit holds the FPGA in a reset state until the V_{CCINT} , V_{CCAUX} , and V_{CCO} Bank 4 supplies reach their respective input threshold levels (see [Table 29, page 59](#)). After all three supplies reach their respective threshold, the POR reset is released and the FPGA begins its configuration process.

Because the three supply inputs must be valid to release the POR reset and can be supplied in any order, there are no specific voltage sequencing requirements. However, applying the FPGA's V_{CCAUX} supply before the V_{CCINT} supply uses the least I_{CCINT} current.

Once all three supplies are valid, the minimum current required to power-on the FPGA is equal to the worst-case quiescent current, as specified in [Table 34, page 62](#). Spartan-3 FPGAs do not require Power-On Surge (POS) current to successfully configure.

Surplus I_{CCINT} if V_{CCINT} Applied before V_{CCAUX}

If the V_{CCINT} supply is applied before the V_{CCAUX} supply, the FPGA may draw a surplus I_{CCINT} current in addition to the I_{CCINT} quiescent current levels specified in [Table 34](#). The momentary additional I_{CCINT} surplus current might be a few hundred milliamperes under nominal conditions, significantly less than the instantaneous current consumed by the bypass capacitors at power-on. However, the surplus current immediately disappears when the V_{CCAUX} supply is applied, and, in response, the FPGA's I_{CCINT} quiescent current demand drops to the levels specified in [Table 34](#). The FPGA does not use nor does it require the surplus current to successfully power-on and configure. If applying V_{CCINT} before V_{CCAUX} , ensure that the regulator does not have a foldback feature that could inadvertently shut down in the presence of the surplus current.

Maximum Allowed V_{CCINT} Ramp Rate on Early Devices, if V_{CCINT} Supply is Last in Sequence

All devices with a mask revision code 'E' or later do not have a V_{CCINT} ramp rate requirement. See [Mask and Fab Revisions, page 58](#).

Early Spartan-3 FPGAs were produced at a 200 mm wafer production facility and are identified by a fabrication/process code of "FQ" on the device top marking, as shown in [Package Marking, page 5](#). These "FQ" devices have a maximum V_{CCINT} ramp rate requirement if and only if V_{CCINT} is the last supply to ramp, after the V_{CCAUX} and V_{CCO} Bank 4 supplies. This maximum ramp rate appears as T_{CCINT} in [Table 30, page 60](#).

Minimum Allowed V_{CCO} Ramp Rate on Early Devices

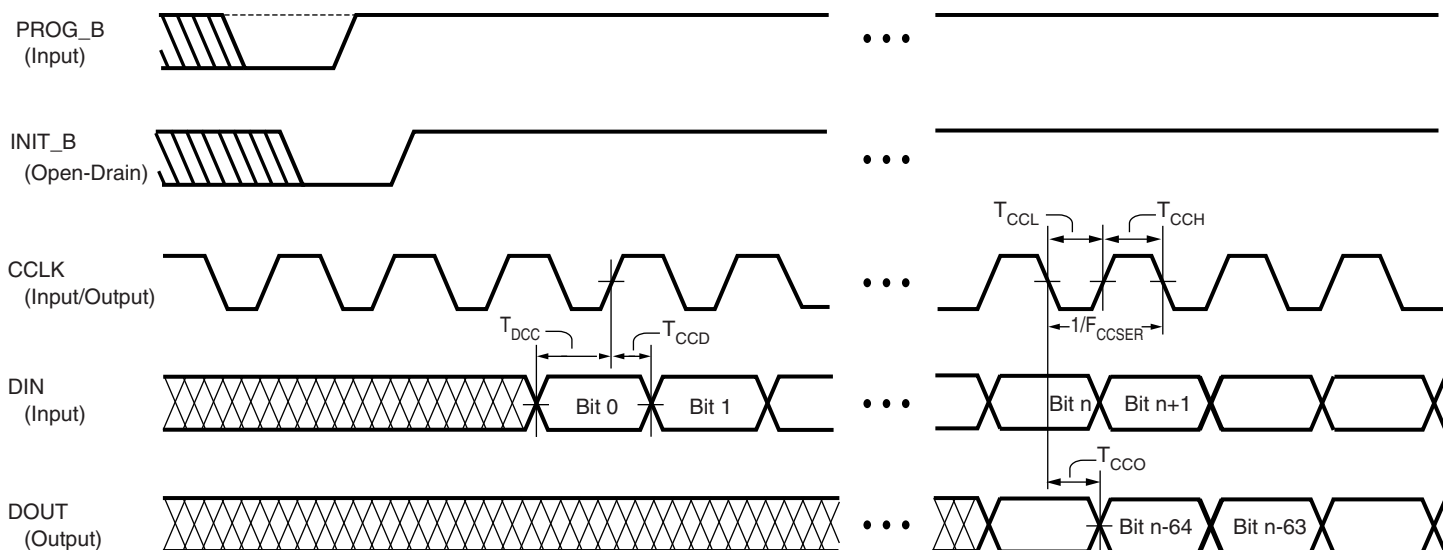
Devices shipped since 2006 essentially have no V_{CCO} ramp rate limits, shown in [Table 30, page 60](#). Similarly, all devices with a mask revision code 'E' or later do not have a V_{CCO} ramp rate limit. See [Mask and Fab Revisions, page 58](#).

Table 61: Switching Characteristics for the DFS

Symbol	Description	Frequency Mode	Device	Speed Grade				Units	
				-5		-4			
				Min	Max	Min	Max		
Output Frequency Ranges									
CLKOUT_FREQ_FX_LF	Frequency for the CLKFX and CLKFX180 outputs	Low	All	18	210	18	210	MHz	
CLKOUT_FREQ_FX_HF		High	All	210	326 ⁽²⁾	210	307 ⁽²⁾	MHz	
Output Clock Jitter									
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs	All	All	Note 3	Note 3	Note 3	Note 3	ps	
Duty Cycle ⁽⁴⁾									
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs	All	XC3S50	–	±100	–	±100	ps	
			XC3S200	–	±100	–	±100	ps	
			XC3S400	–	±250	–	±250	ps	
			XC3S1000	–	±400	–	±400	ps	
			XC3S1500	–	±400	–	±400	ps	
			XC3S2000	–	±400	–	±400	ps	
			XC3S4000	–	±400	–	±400	ps	
			XC3S5000	–	±400	–	±400	ps	
Phase Alignment									
CLKOUT_PHASE	Phase offset between the DFS output and the CLK0 output	All	All	–	±300	–	±300	ps	
Lock Time									
LOCK_DLL_FX	When using the DFS in conjunction with the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.	All	All	–	10.0	–	10.0	ms	
LOCK_FX	When using the DFS without the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. By asserting the LOCKED signal, the DFS indicates valid CLKFX and CLKFX180 signals.	All	All	–	10.0	–	10.0	ms	

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 32](#) and [Table 60](#).
2. Mask revisions prior to the E mask revision have a CLKOUT_FREQ_FX_HF max of 280 MHz. See [Mask and Fab Revisions, page 58](#).
3. Use the DCM Clocking Wizard in the ISE software for a Spartan-3 device specific number. Jitter number assumes 150 ps of input clock jitter.
4. The CLKFX and CLKFX180 outputs always approximate 50% duty cycles.
5. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) is in use.



DS099-3_04_071604

Figure 37: Waveforms for Master and Slave Serial Configuration

Table 66: Timing for the Master and Slave Serial Configuration Modes

Symbol	Description	Slave/ Master	All Speed Grades		Units	
			Min	Max		
Clock-to-Output Times						
T _{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin	Both	1.5	12.0	ns	
Setup Times						
T _{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin	Both	10.0	—	ns	
Hold Times						
T _{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin	Both	0	—	ns	
Clock Timing						
T _{CCH}	CCLK input pin High pulse width		Slave	5.0	∞	ns
T _{CCL}	CCLK input pin Low pulse width			5.0	∞	ns
F _{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression		0	66 ⁽²⁾	MHz
		With bitstream compression		0	20	MHz
		During STARTUP phase		0	50	MHz
ΔF _{CCSER}	Variation from the CCLK output frequency set using the ConfigRate BitGen option		Master	–50%	+50%	—

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

VREF: User I/O or Input Buffer Reference Voltage for Special Interface Standards

These pins are individual user-I/O pins unless collectively they supply an input reference voltage, VREF_#, for any SSTL, HSTL, GTL, or GTLP I/Os implemented in the associated I/O bank. The '#' character in the pin name represents an integer, 0 through 7, that indicates the associated I/O bank.

The VREF function becomes active for this pin whenever a signal standard requiring a reference voltage is used in the associated bank. If used as a user I/O, then each pin behaves as an independent I/O described in the I/O type section. If used for a reference voltage within a bank, then *all* VREF pins within the bank must be connected to the same reference voltage.

Spartan-3 devices are designed and characterized to support certain I/O standards when VREF is connected to +1.25V, +1.10V, +1.00V, +0.90V, +0.80V, and +0.75V. During configuration, the VREF pins behave exactly like user-I/O pins.

If designing for footprint compatibility across the range of devices in a specific package, and if the VREF_# pins within a bank connect to an input reference voltage, then also connect any N.C. (not connected) pins on the smaller devices in that package to the input reference voltage. More details are provided later for each package type.

N.C. Type: Unconnected Package Pins

Pins marked as "N.C." are unconnected for the specific device/package combination. For other devices in this same package, this pin may be used as an I/O or VREF connection. In both the pinout tables and the footprint diagrams, unconnected pins are noted with either a black diamond symbol (◆) or a black square symbol (■).

If designing for footprint compatibility across multiple device densities, check the pin types of the other Spartan-3 devices available in the same footprint. If the N.C. pin matches to VREF pins in other devices, and the VREF pins are used in the associated I/O bank, then connect the N.C. to the VREF voltage source.

VCCO Type: Output Voltage Supply for I/O Bank

Each I/O bank has its own set of voltage supply pins that determines the output voltage for the output buffers in the I/O bank. Furthermore, for some I/O standards such as LVCMOS, LVCMOS25, LVTTTL, etc., VCCO sets the input threshold voltage on the associated input buffers.

Spartan-3 devices are designed and characterized to support various I/O standards for VCCO values of +1.2V, +1.5V, +1.8V, +2.5V, and +3.3V.

Most VCCO pins are labeled as VCCO_# where the '#' symbol represents the associated I/O bank number, an integer ranging from 0 to 7. In the 144-pin TQFP package (TQ144) however, the VCCO pins along an edge of the device are combined into a single VCCO input. For example, the VCCO inputs for Bank 0 and Bank 1 along the top edge of the package are combined and relabeled VCCO_TOP. The bottom, left, and right edges are similarly combined.

In Serial configuration mode, VCCO_4 must be at a level compatible with the attached configuration memory or data source. In Parallel configuration mode, both VCCO_4 and VCCO_5 must be at the same compatible voltage level.

All VCCO inputs to a bank must be connected together and to the voltage supply. Furthermore, there must be sufficient supply decoupling to guarantee problem-free operation, as described in [XAPP623: Power Distribution System \(PDS\) Design: Using Bypass/Decoupling Capacitors](#).

VCCINT Type: Voltage Supply for Internal Core Logic

Internal core logic circuits such as the configurable logic blocks (CLBs) and programmable interconnect operate from the VCCINT voltage supply inputs. VCCINT must be +1.2V.

All VCCINT inputs must be connected together and to the +1.2V voltage supply. Furthermore, there must be sufficient supply decoupling to guarantee problem-free operation, as described in [XAPP623](#).

VCCAUX Type: Voltage Supply for Auxiliary Logic

The VCCAUX pins supply power to various auxiliary circuits, such as to the Digital Clock Managers (DCMs), the JTAG pins, and to the dedicated configuration pins (CONFIG type). VCCAUX must be +2.5V.

Table 91: TQ144 Package Pinout (Cont'd)

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
5	IO_L32P_5/GCLK2	P52	GCLK
6	IO_L01N_6/VRP_6	P36	DCI
6	IO_L01P_6/VRN_6	P35	DCI
6	IO_L20N_6	P33	I/O
6	IO_L20P_6	P32	I/O
6	IO_L21N_6	P31	I/O
6	IO_L21P_6	P30	I/O
6	IO_L22N_6	P28	I/O
6	IO_L22P_6	P27	I/O
6	IO_L23N_6	P26	I/O
6	IO_L23P_6	P25	I/O
6	IO_L24N_6/VREF_6	P24	VREF
6	IO_L24P_6	P23	I/O
6	IO_L40N_6	P21	I/O
6	IO_L40P_6/VREF_6	P20	VREF
7	IO/VREF_7	P4	VREF
7	IO_L01N_7/VRP_7	P2	DCI
7	IO_L01P_7/VRN_7	P1	DCI
7	IO_L20N_7	P6	I/O
7	IO_L20P_7	P5	I/O
7	IO_L21N_7	P8	I/O
7	IO_L21P_7	P7	I/O
7	IO_L22N_7	P11	I/O
7	IO_L22P_7	P10	I/O
7	IO_L23N_7	P13	I/O
7	IO_L23P_7	P12	I/O
7	IO_L24N_7	P15	I/O
7	IO_L24P_7	P14	I/O
7	IO_L40N_7/VREF_7	P18	VREF
7	IO_L40P_7	P17	I/O
0,1	VCCO_TOP	P126	VCCO
0,1	VCCO_TOP	P138	VCCO
0,1	VCCO_TOP	P115	VCCO
2,3	VCCO_RIGHT	P106	VCCO
2,3	VCCO_RIGHT	P75	VCCO
2,3	VCCO_RIGHT	P91	VCCO
4,5	VCCO_BOTTOM	P54	VCCO
4,5	VCCO_BOTTOM	P43	VCCO
4,5	VCCO_BOTTOM	P66	VCCO
6,7	VCCO_LEFT	P19	VCCO

PQ208 Footprint

Left Half of Package (Top View)

XC3S50

(124 max. user I/O)

72 I/O: Unrestricted,
general-purpose user I/O

16 VREF: User I/O or input
voltage reference for bank

17 N.C.: Unconnected pins for
XC3S50 (◆)

XC3S200, XC3S400

(141 max user I/O)

83 I/O: Unrestricted,
general-purpose user I/O

22 VREF: User I/O or input
voltage reference for bank

0 N.C.: No unconnected pins
in this package

All devices

12 DUAL: Configuration pin,
then possible user I/O

8 GCLK: User I/O or global
clock buffer input

16 DCI: User I/O or reference
resistor input for bank

7 CONFIG: Dedicated
configuration pins

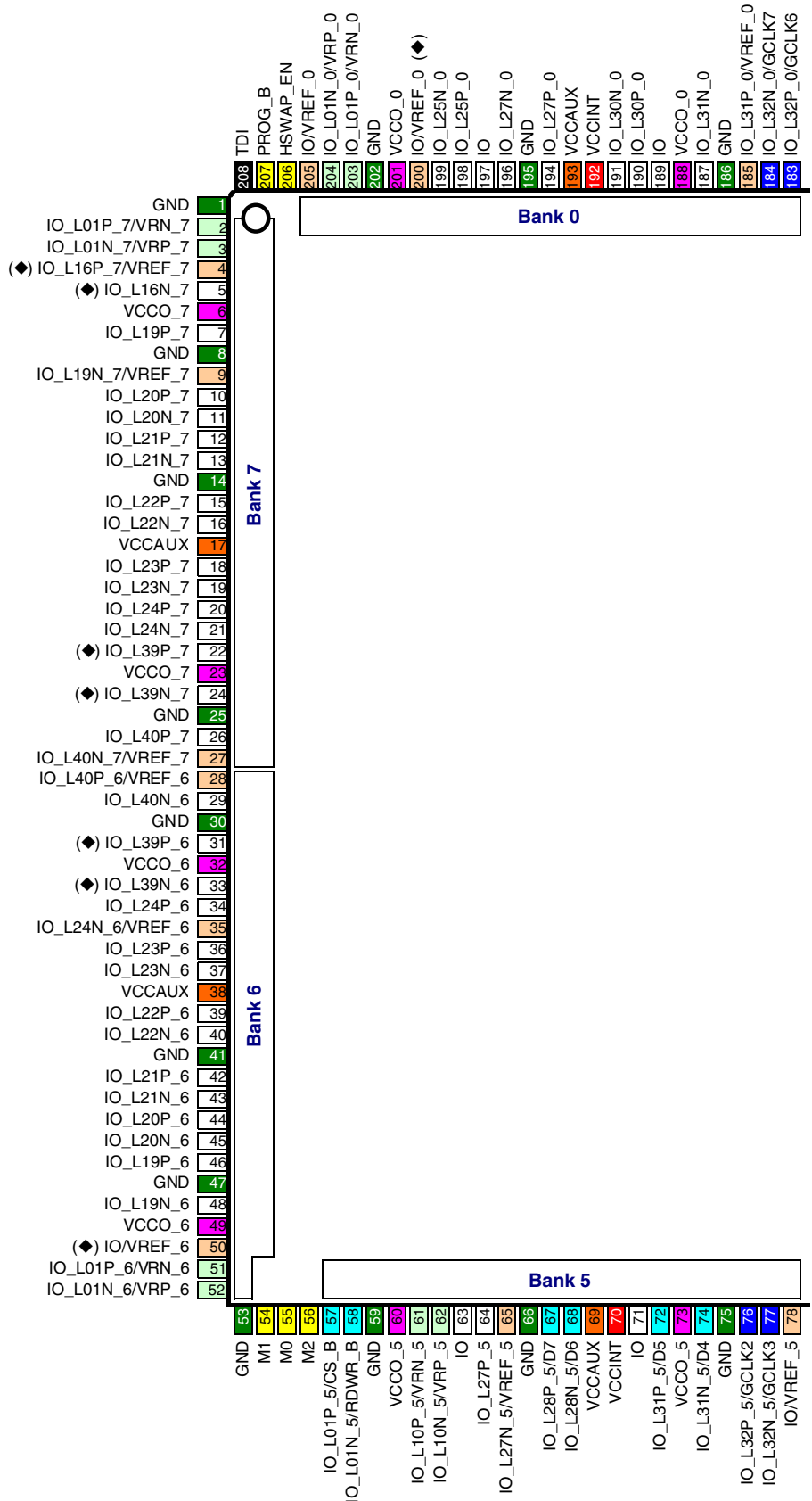
4 JTAG: Dedicated JTAG
port pins

4 VCCINT: Internal core
voltage supply (+1.2V)

12 VCCO: Output voltage
supply for bank

8 VCCAUX: Auxiliary voltage
supply (+2.5V)

28 GND: Ground



DS099-4_09a_121103

Figure 47: PQ208 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.

FG320: 320-lead Fine-pitch Ball Grid Array

The 320-lead fine-pitch ball grid array package, FG320, supports three different Spartan-3 devices, including the XC3S400, the XC3S1000, and the XC3S1500. The footprint for all three devices is identical, as shown in [Table 98](#) and [Figure 50](#).

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

All the package pins appear in [Table 98](#) and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_sheets/s3_pin.zip.

Pinout Table

Table 98: FG320 Package Pinout

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
0	IO	D9	I/O
0	IO	E7	I/O
0	IO/VREF_0	B3	VREF
0	IO/VREF_0	D6	VREF
0	IO_L01N_0/VRP_0	A2	DCI
0	IO_L01P_0/VRN_0	A3	DCI
0	IO_L09N_0	B4	I/O
0	IO_L09P_0	C4	I/O
0	IO_L10N_0	C5	I/O
0	IO_L10P_0	D5	I/O
0	IO_L15N_0	A4	I/O
0	IO_L15P_0	A5	I/O
0	IO_L25N_0	B5	I/O
0	IO_L25P_0	B6	I/O
0	IO_L27N_0	C7	I/O
0	IO_L27P_0	D7	I/O
0	IO_L28N_0	C8	I/O
0	IO_L28P_0	D8	I/O
0	IO_L29N_0	E8	I/O
0	IO_L29P_0	F8	I/O
0	IO_L30N_0	A7	I/O
0	IO_L30P_0	A8	I/O
0	IO_L31N_0	B9	I/O
0	IO_L31P_0/VREF_0	A9	VREF
0	IO_L32N_0/GCLK7	E9	GCLK
0	IO_L32P_0/GCLK6	F9	GCLK
0	VCCO_0	B8	VCCO
0	VCCO_0	C6	VCCO
0	VCCO_0	G8	VCCO

Table 98: FG320 Package Pinout (Cont'd)

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
4	IO_L31P_4/ DOUT/BUSY	V10	DUAL
4	IO_L32N_4/GCLK1	N10	GCLK
4	IO_L32P_4/GCLK0	P10	GCLK
4	VCCO_4	M10	VCCO
4	VCCO_4	M11	VCCO
4	VCCO_4	T13	VCCO
4	VCCO_4	U11	VCCO
5	IO	N8	I/O
5	IO	P8	I/O
5	IO	U6	I/O
5	IO/VREF_5	R9	VREF
5	IO_L01N_5/RDWR_B	V3	DUAL
5	IO_L01P_5/CS_B	V2	DUAL
5	IO_L06N_5	T5	I/O
5	IO_L06P_5	T4	I/O
5	IO_L10N_5/VRP_5	V4	DCI
5	IO_L10P_5/VRN_5	U4	DCI
5	IO_L15N_5	R6	I/O
5	IO_L15P_5	R5	I/O
5	IO_L16N_5	V5	I/O
5	IO_L16P_5	U5	I/O
5	IO_L27N_5/VREF_5	P6	VREF
5	IO_L27P_5	P7	I/O
5	IO_L28N_5/D6	R7	DUAL
5	IO_L28P_5/D7	T7	DUAL
5	IO_L29N_5	V8	I/O
5	IO_L29P_5/VREF_5	V7	VREF
5	IO_L30N_5	R8	I/O
5	IO_L30P_5	T8	I/O
5	IO_L31N_5/D4	U9	DUAL
5	IO_L31P_5/D5	V9	DUAL
5	IO_L32N_5/GCLK3	N9	GCLK
5	IO_L32P_5/GCLK2	P9	GCLK
5	VCCO_5	M8	VCCO
5	VCCO_5	M9	VCCO
5	VCCO_5	T6	VCCO
5	VCCO_5	U8	VCCO
6	IO	K6	I/O
6	IO_L01N_6/VRP_6	T3	DCI

Table 98: FG320 Package Pinout (Cont'd)

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
6	IO_L01P_6/VRN_6	T2	DCI
6	IO_L16N_6	U1	I/O
6	IO_L16P_6	T1	I/O
6	IO_L17N_6	R2	I/O
6	IO_L17P_6/VREF_6	R1	VREF
6	IO_L19N_6	R3	I/O
6	IO_L19P_6	P3	I/O
6	IO_L20N_6	P2	I/O
6	IO_L20P_6	P1	I/O
6	IO_L21N_6	N4	I/O
6	IO_L21P_6	P4	I/O
6	IO_L22N_6	N5	I/O
6	IO_L22P_6	M5	I/O
6	IO_L23N_6	M3	I/O
6	IO_L23P_6	M4	I/O
6	IO_L24N_6/VREF_6	N2	VREF
6	IO_L24P_6	M1	I/O
6	IO_L27N_6	L6	I/O
6	IO_L27P_6	L5	I/O
6	IO_L34N_6/VREF_6	L3	VREF
6	IO_L34P_6	L4	I/O
6	IO_L35N_6	L2	I/O
6	IO_L35P_6	L1	I/O
6	IO_L39N_6	K5	I/O
6	IO_L39P_6	K4	I/O
6	IO_L40N_6	K1	I/O
6	IO_L40P_6/VREF_6	K2	VREF
6	VCCO_6	K7	VCCO
6	VCCO_6	L7	VCCO
6	VCCO_6	N3	VCCO
7	IO	J6	I/O
7	IO_L01N_7/VRP_7	C3	DCI
7	IO_L01P_7/VRN_7	C2	DCI
7	IO_L16N_7	C1	I/O
7	IO_L16P_7/VREF_7	B1	VREF
7	IO_L17N_7	D1	I/O
7	IO_L17P_7	D2	I/O
7	IO_L19N_7/VREF_7	E3	VREF
7	IO_L19P_7	D3	I/O
7	IO_L20N_7	E2	I/O

Table 103: FG676 Package Pinout (Cont'd)

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AB5	DUAL
5	IO_L04N_5	IO_L04N_5	IO_L04N_5	IO_L04N_5	IO_L04N_5	AE4	I/O
5	IO_L04P_5	IO_L04P_5	IO_L04P_5	IO_L04P_5	IO_L04P_5	AD4	I/O
5	IO_L05N_5	IO_L05N_5	IO_L05N_5	IO_L05N_5	IO_L05N_5	AB6	I/O
5	IO_L05P_5	IO_L05P_5	IO_L05P_5	IO_L05P_5	IO_L05P_5	AA6	I/O
5	IO_L06N_5	IO_L06N_5	IO_L06N_5	IO_L06N_5	IO_L06N_5	AE5	I/O
5	IO_L06P_5	IO_L06P_5	IO_L06P_5	IO_L06P_5	IO_L06P_5	AD5	I/O
5	IO_L07N_5	IO_L07N_5	IO_L07N_5	IO_L07N_5	IO_L07N_5	AD6	I/O
5	IO_L07P_5	IO_L07P_5	IO_L07P_5	IO_L07P_5	IO_L07P_5	AC6	I/O
5	IO_L08N_5	IO_L08N_5	IO_L08N_5	IO_L08N_5	IO_L08N_5	AF6	I/O
5	IO_L08P_5	IO_L08P_5	IO_L08P_5	IO_L08P_5	IO_L08P_5	AE6	I/O
5	IO_L09N_5	IO_L09N_5	IO_L09N_5	IO_L09N_5	IO_L09N_5	AC7	I/O
5	IO_L09P_5	IO_L09P_5	IO_L09P_5	IO_L09P_5	IO_L09P_5	AB7	I/O
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	AF7	DCI
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	AE7	DCI
5	N.C. (◆)	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	AB8	VREF
5	N.C. (◆)	IO_L11P_5	IO_L11P_5	IO_L11P_5	IO_L11P_5	AA8	I/O
5	N.C. (◆)	IO_L12N_5	IO_L12N_5	IO_L12N_5	IO_L12N_5	AD8	I/O
5	N.C. (◆)	IO_L12P_5	IO_L12P_5	IO_L12P_5	IO_L12P_5	AC8	I/O
5	IO_L15N_5	IO_L15N_5	IO_L15N_5	IO_L15N_5	IO_L15N_5	AF8	I/O
5	IO_L15P_5	IO_L15P_5	IO_L15P_5	IO_L15P_5	IO_L15P_5	AE8	I/O
5	IO_L16N_5	IO_L16N_5	IO_L16N_5	IO_L16N_5	IO_L16N_5	AA9	I/O
5	IO_L16P_5	IO_L16P_5	IO_L16P_5	IO_L16P_5	IO_L16P_5	Y9	I/O
5	N.C. (◆)	IO_L18N_5	IO_L18N_5	IO_L18N_5	IO_L18N_5	AE9	I/O
5	N.C. (◆)	IO_L18P_5	IO_L18P_5	IO_L18P_5	IO_L18P_5	AD9	I/O
5	IO_L19N_5	IO_L19N_5	IO_L19N_5	IO_L19N_5	IO_L19N_5	AA10	I/O
5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	Y10	VREF
5	IO_L22N_5	IO_L22N_5	IO_L22N_5	IO_L22N_5	IO_L22N_5	AC10	I/O
5	IO_L22P_5	IO_L22P_5	IO_L22P_5	IO_L22P_5	IO_L22P_5	AB10	I/O
5	N.C. (◆)	IO_L23N_5	IO_L23N_5	IO_L23N_5	IO_L23N_5	AF10	I/O
5	N.C. (◆)	IO_L23P_5	IO_L23P_5	IO_L23P_5	IO_L23P_5	AE10	I/O
5	IO_L24N_5	IO_L24N_5	IO_L24N_5	IO_L24N_5	IO_L24N_5	Y11	I/O
5	IO_L24P_5	IO_L24P_5	IO_L24P_5	IO_L24P_5	IO_L24P_5	W11	I/O
5	IO_L25N_5	IO_L25N_5	IO_L25N_5	IO_L25N_5	IO_L25N_5	AB11	I/O
5	IO_L25P_5	IO_L25P_5	IO_L25P_5	IO_L25P_5	IO_L25P_5	AA11	I/O
5	N.C. (◆)	IO_L26N_5	IO_L26N_5	IO_L26N_5	IO_L26N_5	AF11	I/O
5	N.C. (◆)	IO_L26P_5	IO_L26P_5	IO_L26P_5	IO_L26P_5	AE11	I/O
5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	IO_L27N_5/VREF_5	Y12	VREF
5	IO_L27P_5	IO_L27P_5	IO_L27P_5	IO_L27P_5	IO_L27P_5	W12	I/O
5	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	IO_L28N_5/D6	AB12	DUAL
5	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	IO_L28P_5/D7	AA12	DUAL
5	IO_L29N_5	IO_L29N_5	IO_L29N_5	IO_L29N_5	IO_L29N_5	AF12	I/O

Table 103: FG676 Package Pinout (Cont'd)

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	IO_L01P_7/VRN_7	F6	DCI
7	IO_L02N_7	IO_L02N_7	IO_L02N_7	IO_L02N_7	IO_L02N_7	E3	I/O
7	IO_L02P_7	IO_L02P_7	IO_L02P_7	IO_L02P_7	IO_L02P_7	E4	I/O
7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	IO_L03N_7/VREF_7	D1	VREF
7	IO_L03P_7	IO_L03P_7	IO_L03P_7	IO_L03P_7	IO_L03P_7	D2	I/O
7	N.C. (◆)	IO_L05N_7	IO_L05N_7	IO_L05N_7	IO_L05N_7	G6	I/O
7	N.C. (◆)	IO_L05P_7	IO_L05P_7	IO_L05P_7	IO_L05P_7	G7	I/O
7	N.C. (◆)	IO_L06N_7	IO_L06N_7	IO_L06N_7	IO_L06N_7	E1	I/O
7	N.C. (◆)	IO_L06P_7	IO_L06P_7	IO_L06P_7	IO_L06P_7	E2	I/O
7	N.C. (◆)	IO_L07N_7	IO_L07N_7	IO_L07N_7	IO_L07N_7	F3	I/O
7	N.C. (◆)	IO_L07P_7	IO_L07P_7	IO_L07P_7	IO_L07P_7	F4	I/O
7	N.C. (◆)	IO_L08N_7	IO_L08N_7	IO_L08N_7	IO_L08N_7	G4	I/O
7	N.C. (◆)	IO_L08P_7	IO_L08P_7	IO_L08P_7	IO_L08P_7	G5	I/O
7	N.C. (◆)	IO_L09N_7	IO_L09N_7	IO_L09N_7	IO_L09N_7	F1	I/O
7	N.C. (◆)	IO_L09P_7	IO_L09P_7	IO_L09P_7	IO_L09P_7	F2	I/O
7	N.C. (◆)	IO_L10N_7	IO_L10N_7	IO_L10N_7	IO_L10N_7	H6	I/O
7	N.C. (◆)	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	IO_L10P_7/VREF_7	H7	VREF
7	IO_L14N_7	IO_L14N_7	IO_L14N_7	IO_L14N_7	IO_L14N_7	G1	I/O
7	IO_L14P_7	IO_L14P_7	IO_L14P_7	IO_L14P_7	IO_L14P_7	G2	I/O
7	IO_L16N_7	IO_L16N_7	IO_L16N_7	IO_L16N_7	IO_L16N_7	J6	I/O
7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	IO_L16P_7/VREF_7	H5	VREF
7	IO_L17N_7	IO_L17N_7	IO_L17N_7	IO_L17N_7	IO_L17N_7	H3	I/O
7	IO_L17P_7	IO_L17P_7	IO_L17P_7	IO_L17P_7	IO_L17P_7	H4	I/O
7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	IO_L19N_7/VREF_7	H1	VREF
7	IO_L19P_7	IO_L19P_7	IO_L19P_7	IO_L19P_7	IO_L19P_7	H2	I/O
7	IO_L20N_7	IO_L20N_7	IO_L20N_7	IO_L20N_7	IO_L20N_7	K7	I/O
7	IO_L20P_7	IO_L20P_7	IO_L20P_7	IO_L20P_7	IO_L20P_7	J7	I/O
7	IO_L21N_7	IO_L21N_7	IO_L21N_7	IO_L21N_7	IO_L21N_7	J4	I/O
7	IO_L21P_7	IO_L21P_7	IO_L21P_7	IO_L21P_7	IO_L21P_7	J5	I/O
7	IO_L22N_7	IO_L22N_7	IO_L22N_7	IO_L22N_7	IO_L22N_7	J2	I/O
7	IO_L22P_7	IO_L22P_7	IO_L22P_7	IO_L22P_7	IO_L22P_7	J3	I/O
7	IO_L23N_7	IO_L23N_7	IO_L23N_7	IO_L23N_7	IO_L23N_7	K5	I/O
7	IO_L23P_7	IO_L23P_7	IO_L23P_7	IO_L23P_7	IO_L23P_7	K6	I/O
7	IO_L24N_7	IO_L24N_7	IO_L24N_7	IO_L24N_7	IO_L24N_7	K3	I/O
7	IO_L24P_7	IO_L24P_7	IO_L24P_7	IO_L24P_7	IO_L24P_7	K4	I/O
7	IO_L26N_7	IO_L26N_7	IO_L26N_7	IO_L26N_7	IO_L26N_7	K1	I/O
7	IO_L26P_7	IO_L26P_7	IO_L26P_7	IO_L26P_7	IO_L26P_7	K2	I/O
7	IO_L27N_7	IO_L27N_7	IO_L27N_7	IO_L27N_7	IO_L27N_7	L7	I/O
7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	L8	VREF
7	IO_L28N_7	IO_L28N_7	IO_L28N_7	IO_L28N_7	IO_L28N_7	L5	I/O
7	IO_L28P_7	IO_L28P_7	IO_L28P_7	IO_L28P_7	IO_L28P_7	L6	I/O
7	IO_L29N_7	IO_L29N_7	IO_L29N_7	IO_L29N_7	IO_L29N_7	L1	I/O

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	IO_L28N_2	IO_L28N_2	M26	I/O
2	IO_L28P_2	IO_L28P_2	N25	I/O
2	IO_L29N_2	IO_L29N_2	N26	I/O
2	IO_L29P_2	IO_L29P_2	N27	I/O
2	IO_L31N_2	IO_L31N_2	N29	I/O
2	IO_L31P_2	IO_L31P_2	N30	I/O
2	IO_L32N_2	IO_L32N_2	P21	I/O
2	IO_L32P_2	IO_L32P_2	P22	I/O
2	IO_L33N_2	IO_L33N_2	P24	I/O
2	IO_L33P_2	IO_L33P_2	P25	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	P28	VREF
2	IO_L34P_2	IO_L34P_2	P29	I/O
2	IO_L35N_2	IO_L35N_2	R21	I/O
2	IO_L35P_2	IO_L35P_2	R22	I/O
2	IO_L37N_2	IO_L37N_2	R23	I/O
2	IO_L37P_2	IO_L37P_2	R24	I/O
2	IO_L38N_2	IO_L38N_2	R25	I/O
2	IO_L38P_2	IO_L38P_2	R26	I/O
2	IO_L39N_2	IO_L39N_2	R27	I/O
2	IO_L39P_2	IO_L39P_2	R28	I/O
2	IO_L40N_2	IO_L40N_2	R29	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	R30	VREF
2	N.C. (◆)	IO_L41N_2	E27	I/O
2	N.C. (◆)	IO_L41P_2	F26	I/O
2	N.C. (◆)	IO_L45N_2	K28	I/O
2	N.C. (◆)	IO_L45P_2	K29	I/O
2	N.C. (◆)	IO_L46N_2	K21	I/O
2	N.C. (◆)	IO_L46P_2	L21	I/O
2	N.C. (◆)	IO_L47N_2	L23	I/O
2	N.C. (◆)	IO_L47P_2	L24	I/O
2	N.C. (◆)	IO_L50N_2	M29	I/O
2	N.C. (◆)	IO_L50P_2	M30	I/O
2	VCCO_2	VCCO_2	M20	VCCO
2	VCCO_2	VCCO_2	N20	VCCO
2	VCCO_2	VCCO_2	P20	VCCO
2	VCCO_2	VCCO_2	L22	VCCO
2	VCCO_2	VCCO_2	J24	VCCO
2	VCCO_2	VCCO_2	N24	VCCO
2	VCCO_2	VCCO_2	G26	VCCO
2	VCCO_2	VCCO_2	E28	VCCO

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L03P_3	IO_L03P_3	AK32	I/O
3	IO_L04N_3	IO_L04N_3	AJ32	I/O
3	IO_L04P_3	IO_L04P_3	AJ31	I/O
3	IO_L05N_3	IO_L05N_3	AJ34	I/O
3	IO_L05P_3	IO_L05P_3	AJ33	I/O
3	IO_L06N_3	IO_L06N_3	AH30	I/O
3	IO_L06P_3	IO_L06P_3	AH29	I/O
3	IO_L07N_3	IO_L07N_3	AG30	I/O
3	IO_L07P_3	IO_L07P_3	AG29	I/O
3	IO_L08N_3	IO_L08N_3	AG34	I/O
3	IO_L08P_3	IO_L08P_3	AG33	I/O
3	IO_L09N_3	IO_L09N_3	AF29	I/O
3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	AF28	VREF
3	IO_L10N_3	IO_L10N_3	AF31	I/O
3	IO_L10P_3	IO_L10P_3	AG31	I/O
3	IO_L11N_3	IO_L11N_3	AF33	I/O
3	IO_L11P_3	IO_L11P_3	AF32	I/O
3	IO_L12N_3	IO_L12N_3	AE26	I/O
3	IO_L12P_3	IO_L12P_3	AF27	I/O
3	IO_L13N_3/VREF_3	IO_L13N_3/VREF_3	AE28	VREF
3	IO_L13P_3	IO_L13P_3	AE27	I/O
3	IO_L14N_3	IO_L14N_3	AE30	I/O
3	IO_L14P_3	IO_L14P_3	AE29	I/O
3	IO_L15N_3	IO_L15N_3	AE32	I/O
3	IO_L15P_3	IO_L15P_3	AE31	I/O
3	IO_L16N_3	IO_L16N_3	AE34	I/O
3	IO_L16P_3	IO_L16P_3	AE33	I/O
3	IO_L17N_3	IO_L17N_3	AD26	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	AD25	VREF
3	IO_L19N_3	IO_L19N_3	AD34	I/O
3	IO_L19P_3	IO_L19P_3	AD33	I/O
3	IO_L20N_3	IO_L20N_3	AC25	I/O
3	IO_L20P_3	IO_L20P_3	AC24	I/O
3	IO_L21N_3	IO_L21N_3	AC28	I/O
3	IO_L21P_3	IO_L21P_3	AC27	I/O
3	IO_L22N_3	IO_L22N_3	AC30	I/O
3	IO_L22P_3	IO_L22P_3	AC29	I/O
3	IO_L23N_3	IO_L23N_3	AC32	I/O
3	IO_L23P_3/VREF_3	IO_L23P_3/VREF_3	AC31	VREF
3	IO_L24N_3	IO_L24N_3	AB25	I/O

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L24P_3	IO_L24P_3	AC26	I/O
3	IO_L26N_3	IO_L26N_3	AA28	I/O
3	IO_L26P_3	IO_L26P_3	AA27	I/O
3	IO_L27N_3	IO_L27N_3	AA30	I/O
3	IO_L27P_3	IO_L27P_3	AA29	I/O
3	IO_L28N_3	IO_L28N_3	AA32	I/O
3	IO_L28P_3	IO_L28P_3	AA31	I/O
3	IO_L29N_3	IO_L29N_3	AA34	I/O
3	IO_L29P_3	IO_L29P_3	AA33	I/O
3	IO_L30N_3	IO_L30N_3	Y29	I/O
3	IO_L30P_3	IO_L30P_3	Y28	I/O
3	IO_L31N_3	IO_L31N_3	Y32	I/O
3	IO_L31P_3	IO_L31P_3	Y31	I/O
3	IO_L32N_3	IO_L32N_3	Y34	I/O
3	IO_L32P_3	IO_L32P_3	Y33	I/O
3	IO_L33N_3	IO_L33N_3	W25	I/O
3	IO_L33P_3	IO_L33P_3	Y26	I/O
3	IO_L34N_3	IO_L34N_3	W29	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	W28	VREF
3	IO_L35N_3	IO_L35N_3	W33	I/O
3	IO_L35P_3	IO_L35P_3	W32	I/O
3	IO_L37N_3	IO_L37N_3	V28	I/O
3	IO_L37P_3	IO_L37P_3	V27	I/O
3	IO_L38N_3	IO_L38N_3	V30	I/O
3	IO_L38P_3	IO_L38P_3	V29	I/O
3	IO_L39N_3	IO_L39N_3	V32	I/O
3	IO_L39P_3	IO_L39P_3	V31	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	V34	VREF
3	IO_L40P_3	IO_L40P_3	V33	I/O
3	N.C. (◆)	IO_L41N_3	AH32	I/O
3	N.C. (◆)	IO_L41P_3	AH31	I/O
3	N.C. (◆)	IO_L44N_3	AD29	I/O
3	N.C. (◆)	IO_L44P_3	AD28	I/O
3	IO_L45N_3	IO_L45N_3	AC34	I/O
3	IO_L45P_3	IO_L45P_3	AC33	I/O
3	IO_L46N_3	IO_L46N_3	AB28	I/O
3	IO_L46P_3	IO_L46P_3	AB27	I/O
3	IO_L47N_3	IO_L47N_3	AB32	I/O
3	IO_L47P_3	IO_L47P_3	AB31	I/O
3	IO_L48N_3	IO_L48N_3	AA24	I/O

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
7	IO_L45P_7	IO_L45P_7	M2	I/O
7	IO_L46N_7	IO_L46N_7	N7	I/O
7	IO_L46P_7	IO_L46P_7	N8	I/O
7	N.C. (◆)	IO_L47N_7	P9	I/O
7	N.C. (◆)	IO_L47P_7	P10	I/O
7	IO_L49N_7	IO_L49N_7	P1	I/O
7	IO_L49P_7	IO_L49P_7	P2	I/O
7	IO_L50N_7	IO_L50N_7	R10	I/O
7	IO_L50P_7	IO_L50P_7	R11	I/O
7	N.C. (◆)	IO_L51N_7	U11	I/O
7	N.C. (◆)	IO_L51P_7	T11	I/O
7	VCCO_7	VCCO_7	D3	VCCO
7	VCCO_7	VCCO_7	H3	VCCO
7	VCCO_7	VCCO_7	H7	VCCO
7	VCCO_7	VCCO_7	L4	VCCO
7	VCCO_7	VCCO_7	L8	VCCO
7	VCCO_7	VCCO_7	N12	VCCO
7	VCCO_7	VCCO_7	N2	VCCO
7	VCCO_7	VCCO_7	N6	VCCO
7	VCCO_7	VCCO_7	P12	VCCO
7	VCCO_7	VCCO_7	R12	VCCO
7	VCCO_7	VCCO_7	R8	VCCO
7	VCCO_7	VCCO_7	T12	VCCO
7	VCCO_7	VCCO_7	T4	VCCO
N/A	GND	GND	A1	GND
N/A	GND	GND	A13	GND
N/A	GND	GND	A16	GND
N/A	GND	GND	A19	GND
N/A	GND	GND	A2	GND
N/A	GND	GND	A22	GND
N/A	GND	GND	A26	GND
N/A	GND	GND	A30	GND
N/A	GND	GND	A33	GND
N/A	GND	GND	A34	GND
N/A	GND	GND	A5	GND
N/A	GND	GND	A9	GND
N/A	GND	GND	AA14	GND
N/A	GND	GND	AA15	GND
N/A	GND	GND	AA16	GND
N/A	GND	GND	AA17	GND

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
GND	GND	GND	GND	GND	VCCINT	I/O L51N_3 ◆	I/O	I/O	I/O L37P_3	I/O L37N_3	I/O L38P_3	I/O L38N_3	I/O L39P_3	I/O L39N_3	I/O L40P_3	I/O L40N_3 VREF_3	V
GND	GND	GND	GND	VCCINT	VCCO_3	I/O L51P_3 ◆	I/O L33N_3	GND	VCCAUX	I/O L34P_3 VREF_3	I/O L34N_3	GND	VCCO_3	I/O L35P_3	I/O L35N_3	GND	W
GND	GND	GND	GND	VCCINT	VCCO_3	I/O L50P_3	I/O L50N_3	I/O L33P_3	VCCO_3	I/O L30P_3	I/O L30N_3	VCCAUX	I/O L31P_3	I/O L31N_3	I/O L32P_3	I/O L32N_3	Y
GND	GND	GND	GND	VCCINT	VCCO_3	I/O L48N_3 ◆	I/O L49P_3 ◆	I/O L49N_3 ◆	I/O L26P_3	I/O L26N_3	I/O L27P_3	I/O L27N_3	I/O L28P_3	I/O L28N_3	I/O L29P_3	I/O L29N_3	A A
GND	VCCINT	VCCINT	VCCINT	VCCINT	VCCO_3	I/O L48P_3	I/O L24N_3	GND	I/O L46P_3	I/O L46N_3	VCCO_3	GND	I/O L47P_3	I/O L47N_3	VCCO_3	GND	A B
VCCINT	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCINT	I/O L20P_3	I/O L20N_3	I/O L24P_3	I/O L21P_3	I/O L21N_3	I/O L22P_3	I/O L22N_3	I/O L23P_3 VREF_3	I/O L23N_3	I/O L45P_3	I/O L45N_3	A C
I/O	I/O	I/O	I/O L18N_4	I/O	I/O L11N_4	DONE	I/O L17P_3 VREF_3	I/O L17N_3	VCCO_3	I/O L44P_3 ◆	I/O L44N_3 ◆	VCCAUX	VCCO_3	GND	I/O L19P_3	I/O L19N_3	A D
I/O	I/O	I/O L23N_4	I/O L18P_4	I/O	I/O L11P_4	I/O ◆	GND	I/O L12N_3	I/O L13P_3	I/O L13N_3 VREF_3	I/O L14P_3	I/O L14N_3	I/O L15P_3	I/O L15N_3	I/O L16P_3	I/O L16N_3	A E
I/O L29N_4	GND	I/O L23P_4	I/O VREF_4	GND	I/O L12N_4	I/O	I/O L07N_4 ◆	I/O	I/O L12P_3	I/O L09P_3 VREF_3	I/O L09N_3	GND	I/O L10N_3	I/O L11P_3	I/O L11N_3	GND	A F
I/O L29P_4	VCCAUX	VCCO_4	I/O L19N_4	I/O L16N_4	I/O L12P_4	VCCO_4	I/O L07P_4	I/O	I/O	VCCO_3	I/O L07P_3	I/O L07N_3	I/O L10P_3	VCCO_3	I/O L08P_3	I/O L08N_3	A G
I/O L30N_4 D2	I/O L27N_4 DIN D0	I/O L24N_4	I/O L19P_4	I/O L16P_4	I/O VREF_4	I/O L39N_4 ◆	I/O L08N_4	I/O L05N_4	VCCO_4	GND	I/O L06P_3	I/O L06N_3	I/O L41P_3 ◆	I/O L41N_3 ◆	I/O	I/O	A H
I/O L30P_4 D3	I/O L27P_4 D1	I/O L24P_4	I/O L20N_4	VCCO_4	I/O L13N_4	I/O L39P_4 ◆	I/O L08P_4	I/O L05P_4	I/O	I/O L35N_4	I/O	VCCAUX	I/O L04P_3	I/O L04N_3	I/O L05P_3	I/O L05N_3	A J
I/O VREF_4	GND	VCCAUX	I/O L20P_4	GND	I/O L13P_4	VCCAUX	I/O	GND	I/O L38N_4	I/O L35P_4	VCCAUX	GND	N.C. ◆ ■	I/O L03P_3	I/O L03N_3	GND	A K
I/O L31N_4 INIT_B	VCCO_4	I/O L25N_4	I/O L21N_4	I/O L17N_4	I/O L14N_4	VCCO_4	I/O L09N_4	I/O L06N_4 VREF_4	I/O L38P_4	I/O L36N_4 ◆	I/O L33N_4	I/O VREF_4	CCLK	VCCO_3	I/O L02P_3	I/O L02N_3 VREF_3	A L
I/O L31P_4 DOUT BUSY	I/O L28N_4	I/O L25P_4	I/O L21P_4	I/O L17P_4	I/O L14P_4	GND	I/O L09P_4	I/O L06P_4	VCCO_4	I/O L36P_4 ◆	I/O L33P_4	I/O L03N_4	VCCO_4	GND	I/O L01P_3 VRN_3	I/O L01N_3 VRP_3	A M
I/O L32N_4 GCLK1	I/O L28P_4	I/O L26N_4	I/O L22N_4 VREF_4	VCCO_4	I/O L15N_4	I/O L40N_4 ◆	I/O L10N_4	I/O	I/O L04N_4	I/O L37N_4 ◆	I/O L34N_4	I/O L03P_4	I/O L02N_4	I/O L01N_4 VRP_4	GND	GND	A N
I/O L32P_4 GCLK0	GND	I/O L26P_4 VREF_4	I/O L22P_4	GND	I/O L15P_4	I/O L40P_4 ◆	I/O L10P_4	GND	I/O L04P_4	I/O L37P_4 ◆	I/O L34P_4	GND	I/O L02P_4	I/O L01P_4 VRN_4	GND	GND	A P

Bank 3

Bank 4

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Bottom Right Corner
of FG1156 Package
(Top View)

Figure 60: FG1156 Package Footprint (Top View) Continued