AMD Xilinx - XC3S400-4FT256I Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	294912
Number of I/O	173
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s400-4ft256i

Table 9: **Differential I/O Standards**

Signal Standard (IOSTANDARD)	V_{CCO} (Volts)		V_{REF} for Inputs (Volts)
	For Outputs	For Inputs	
LDT_25 (ULVDS_25)	2.5	–	–
LVDS_25	2.5	–	–
BLVDS_25	2.5	–	–
LVDSEXT_25	2.5	–	–
LVPECL_25	2.5	–	–
RSDS_25	2.5	–	–
DIFF_HSTL_II_18	1.8	–	–
DIFF_SSTL2_II	2.5	–	–

Notes:

1. See Table 10 for a listing of the differential DCI standards.

The need to supply V_{REF} and V_{CCO} imposes constraints on which standards can be used in the same bank. See The Organization of IOBs into Banks section for additional guidelines concerning the use of the V_{CCO} and V_{REF} lines.

Digitally Controlled Impedance (DCI)

When the round-trip delay of an output signal—i.e., from output to input and back again—exceeds rise and fall times, it is common practice to add termination resistors to the line carrying the signal. These resistors effectively match the impedance of a device's I/O to the characteristic impedance of the transmission line, thereby preventing reflections that adversely affect signal integrity. However, with the high I/O counts supported by modern devices, adding resistors requires significantly more components and board area. Furthermore, for some packages—e.g., ball grid arrays—it may not always be possible to place resistors close to pins.

DCI answers these concerns by providing two kinds of on-chip terminations: Parallel terminations make use of an integrated resistor network. Series terminations result from controlling the impedance of output drivers. DCI actively adjusts both parallel and series terminations to accurately match the characteristic impedance of the transmission line. This adjustment process compensates for differences in I/O impedance that can result from normal variation in the ambient temperature, the supply voltage and the manufacturing process. When the output driver turns off, the series termination, by definition, approaches a very high impedance; in contrast, parallel termination resistors remain at the targeted values.

DCI is available only for certain I/O standards, as listed in Table 10. DCI is selected by applying the appropriate I/O standard extensions to symbols or components. There are five basic ways to configure terminations, as shown in Table 11. The DCI I/O standard determines which of these terminations is put into effect.

HSTL_I_DCI-, HSTL_III_DCI-, and SSTL2_I_DCI-type outputs do not require the VRN and VRP reference resistors. Likewise, LVDCI-type inputs do not require the VRN and VRP reference resistors. In a bank without any DCI I/O or a bank containing non-DCI I/O and purely HSTL_I_DCI- or HSTL_III_DCI-type outputs, or SSTL2_I_DCI-type outputs or LVDCI-type inputs, the associated VRN and VRP pins can be used as general-purpose I/O pins.

The HSLVDCI (High-Speed LVDCI) standard is intended for bidirectional use. The driver is identical to LVDCI, while the input is identical to HSTL. By using a V_{REF}-referenced input, HSLVDCI allows greater input sensitivity at the receiver than when using a single-ended LVCMOS-type receiver.

Table 48: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
HSTL_III_DCI_18							
LVCMOS12		-	0	1.2	1M	0	0.6
LVCMOS15		-	0	1.5	1M	0	0.75
LVDCI_15							
LVDCI_DV2_15							
HSLVDCI_15							
LVCMOS18		-	0	1.8	1M	0	0.9
LVDCI_18							
LVDCI_DV2_18							
HSLVDCI_18							
LVCMOS25		-	0	2.5	1M	0	1.25
LVDCI_25							
LVDCI_DV2_25							
HSLVDCI_25							
LVCMOS33		-	0	3.3	1M	0	1.65
LVDCI_33							
LVDCI_DV2_33							
HSLVDCI_33							
LVTTL		-	0	3.3	1M	0	1.4
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_I_DCI							
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_I_DCI							
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL2_II_DCI					50	1.25	
Differential							
LDT_25 (ULVDS_25)		-	V_{ICM} – 0.125	V_{ICM} + 0.125	60	0.6	V_{ICM}
LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_25_DCI					N/A	N/A	
BLVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
LVDSEXT_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDSEXT_25_DCI					N/A	N/A	
LVPECL_25		-	V_{ICM} – 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25		-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
DIFF_HSTL_II_18		-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.8	V_{ICM}
DIFF_HSTL_II_18_DCI							

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)	Package				
	VQ100	TQ144	PQ208	CP132	FT256, FG320, FG456, FG676, FG900, FG1156
PCI33_3	9	9	9	9	9
SSTL18_I	13	13	13	13	17
SSTL18_I_DCI	13	13	13	13	17
SSTL18_II	8	8	8	8	9
SSTL2_I	10	10	10	10	13
SSTL2_I_DCI	10	10	10	10	13
SSTL2_II	6	6	6	6	9
SSTL2_II_DCI	6	6	6	6	9
Differential Standards (Number of I/O Pairs or Channels)					
LDT_25 (ULVDS_25)	5	5	5	5	5
LVDS_25	7	5	5	12	20
BLVDS_25	2	1	1		4
LVDSEXT_25	5	5	5	5	5
LVPECL_25	2	1	1		4
RSDS_25	7	5	5	12	20
DIFF_HSTL_II_18	4	4	4	4	4
DIFF_HSTL_II_18_DCI	4	4	4	4	4
DIFF_SSTL2_II	3	3	3	3	4
DIFF_SSTL2_II_DCI	3	3	3	3	4

Notes:

1. The numbers in this table are recommendations that assume the FPGA is soldered on a printed circuit board using sound practices. This table assumes the following parasitic factors: combined PCB trace and land inductance per V_{CCO} and GND pin of 1.0 nH, receiver capacitive load of 15 pF. Test limits are the V_{IL}/V_{IH} voltage limits for the respective I/O standard.
2. Regarding the SSO numbers for all DCI standards, the R_{REF} resistors connected to the VRN and VRP pins of the FPGA are 50W..
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: *Managing Ground Bounce in Large FPGAs* for information on how to perform weighted average SSO calculations.
4. Results are based on actual silicon testing using an FPGA soldered on a typical printed-circuit board.

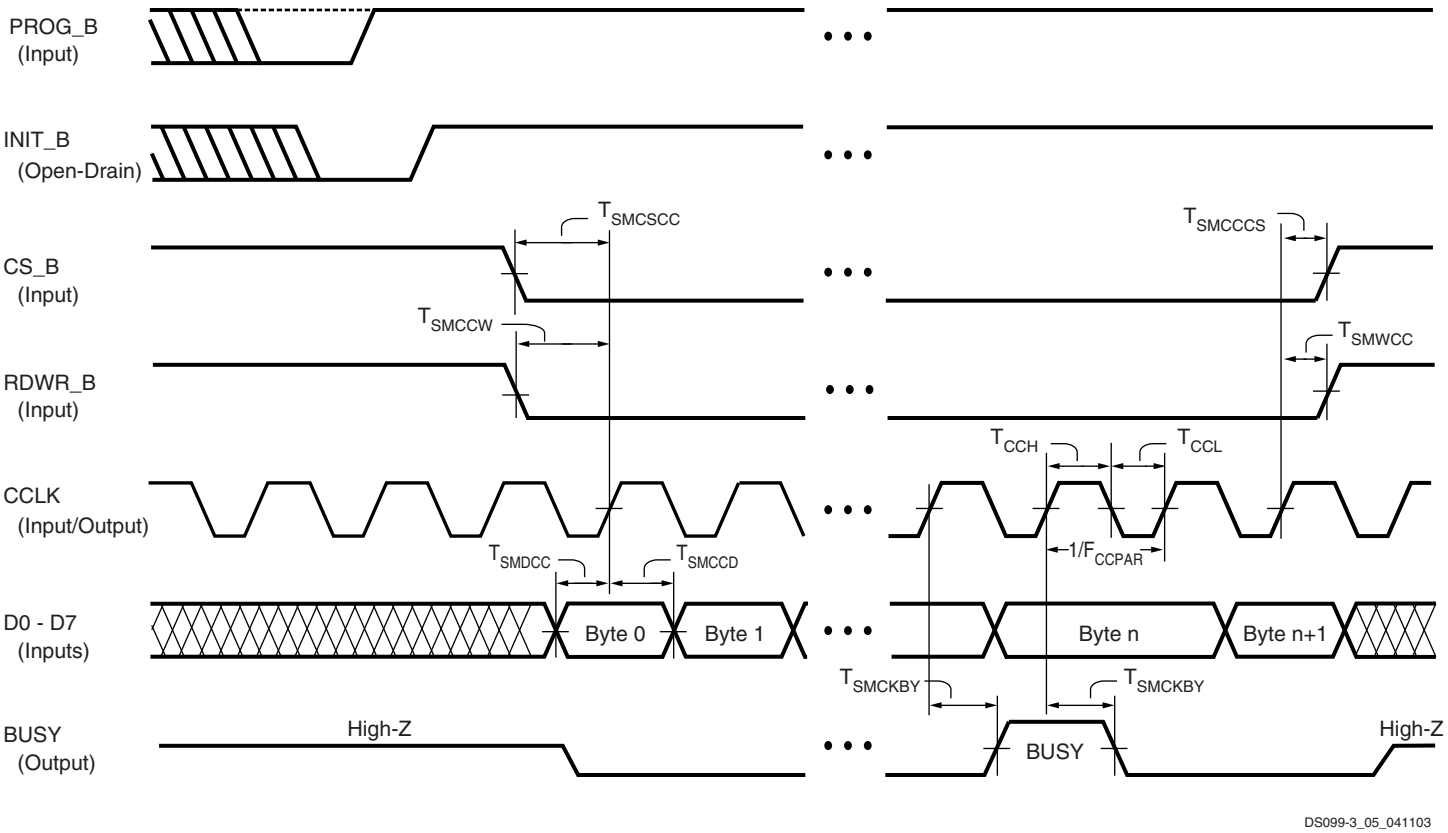

Figure 38: **Waveforms for Master and Slave Parallel Configuration**

Table 67: **Timing for the Master and Slave Parallel Configuration Modes**

Symbol	Description	Slave/ Master	All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin	Slave	–	12.0	ns
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	Both	10.0	–	ns
T_{SMCSCC}	The time from the setup of a logic level at the CS_B pin to the rising transition at the CCLK pin		10.0	–	ns
T_{SMCCW}(3)	The time from the setup of a logic level at the RDWR_B pin to the rising transition at the CCLK pin		10.0	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins	Both	0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CS_B pin		0	–	ns
T_{SMWCC}(3)	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns

Table 70: **Spartan-3 FPGA Pin Definitions *(Cont'd)***

Pin Name	Direction	Description
GCLK: Global clock buffer inputs		
IO_Lxxy_#/GCLK0, IO_Lxxy_#/GCLK1, IO_Lxxy_#/GCLK2, IO_Lxxy_#/GCLK3, IO_Lxxy_#/GCLK4, IO_Lxxy_#/GCLK5, IO_Lxxy_#/GCLK6, IO_Lxxy_#/GCLK7	Input if connected to global clock buffers Otherwise, same as I/O	**Global Buffer Input:** Direct input to a low-skew global clock buffer. If not connected to a global clock buffer, this pin is a user I/O.
VREF: I/O bank input reference voltage pins		
IO_Lxxy_#/VREF_# or IO/VREF_#	Voltage supply input when VREF pins are used within a bank. Otherwise, same as I/O	**Input Buffer Reference Voltage for Special I/O Standards (per bank):** If required to support special I/O standards, all the VREF pins within a bank connect to a input threshold voltage source. If not used as input reference voltage pins, these pins are available as individual user-I/O pins.
CONFIG: Dedicated configuration pins (pull-up resistor to VCCAUX always active during configuration, regardless of HSWAP_EN pin)		
CCLK	Input in Slave configuration modes Output in Master configuration modes	**Configuration Clock:** The configuration clock signal synchronizes configuration data. This pin has an internal pull-up resistor to VCCAUX during configuration.
PROG_B	Input	**Program/Configure Device:** Active Low asynchronous reset to configuration logic. Asserting PROG_B Low for an extended period delays the configuration process. This pin has an internal pull-up resistor to VCCAUX during configuration.
DONE	Bidirectional with open-drain or totem-pole Output	**Configuration Done, Delay Start-up Sequence:** A Low-to-High output transition on this bidirectional pin signals the end of the configuration process. The FPGA produces a Low-to-High transition on this pin to indicate that the configuration process is complete. The DriveDone bitstream generation option defines whether this pin functions as a totem-pole output that actively drives High or as an open-drain output. An open-drain output requires a pull-up resistor to produce a High logic level. The open-drain option permits the DONE lines of multiple FPGAs to be tied together, so that the common node transitions High only after all of the FPGAs have completed configuration. Externally holding the open-drain output Low delays the start-up sequence, which marks the transition to user mode.
M0, M1, M2	Input	**Configuration Mode Selection:** These inputs select the configuration mode. The logic levels applied to the mode pins are sampled on the rising edge of INIT_B. See Table 75. These pins have an internal pull-up resistor to VCCAUX during configuration, making Slave Serial the default configuration mode.
HSWAP_EN	Input	**Disable Pull-up Resistors During Configuration:** A Low on this pin enables pull-up resistors on all pins that are not actively involved in the configuration process. A High value disables all pull-ups, allowing the non-configuration pins to float.
JTAG: JTAG interface pins (pull-up resistor to VCCAUX always active during configuration, regardless of HSWAP_EN pin)		
TCK	Input	**JTAG Test Clock:** The TCK clock signal synchronizes all JTAG port operations. This pin has an internal pull-up resistor to VCCAUX during configuration.

Table 91: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
2	IO_L23N_2/VREF_2	P98	VREF
2	IO_L23P_2	P97	I/O
2	IO_L24N_2	P96	I/O
2	IO_L24P_2	P95	I/O
2	IO_L40N_2	P93	I/O
2	IO_L40P_2/VREF_2	P92	VREF
3	IO	P76	I/O
3	IO_L01N_3/VRP_3	P74	DCI
3	IO_L01P_3/VRN_3	P73	DCI
3	IO_L20N_3	P78	I/O
3	IO_L20P_3	P77	I/O
3	IO_L21N_3	P80	I/O
3	IO_L21P_3	P79	I/O
3	IO_L22N_3	P83	I/O
3	IO_L22P_3	P82	I/O
3	IO_L23N_3	P85	I/O
3	IO_L23P_3/VREF_3	P84	VREF
3	IO_L24N_3	P87	I/O
3	IO_L24P_3	P86	I/O
3	IO_L40N_3/VREF_3	P90	VREF
3	IO_L40P_3	P89	I/O
4	IO/VREF_4	P70	VREF
4	IO_L01N_4/VRP_4	P69	DCI
4	IO_L01P_4/VRN_4	P68	DCI
4	IO_L27N_4/DIN/D0	P65	DUAL
4	IO_L27P_4/D1	P63	DUAL
4	IO_L30N_4/D2	P60	DUAL
4	IO_L30P_4/D3	P59	DUAL
4	IO_L31N_4/INIT_B	P58	DUAL
4	IO_L31P_4/DOUT/BUSY	P57	DUAL
4	IO_L32N_4/GCLK1	P56	GCLK
4	IO_L32P_4/GCLK0	P55	GCLK
5	IO/VREF_5	P44	VREF
5	IO_L01N_5/RDWR_B	P41	DUAL
5	IO_L01P_5/CS_B	P40	DUAL
5	IO_L28N_5/D6	P47	DUAL
5	IO_L28P_5/D7	P46	DUAL
5	IO_L31N_5/D4	P51	DUAL
5	IO_L31P_5/D5	P50	DUAL
5	IO_L32N_5/GCLK3	P53	GCLK

User I/Os by Bank

Table 94 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S50 in the PQ208 package. Similarly, Table 95 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S200 and XC3S400 in the PQ208 package.

Table 94: **User I/Os Per Bank for XC3S50 in PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	15	9	0	2	2	2
	1	15	9	0	2	2	2
Right	2	16	13	0	2	2	0
	3	16	12	0	2	2	0
Bottom	4	15	3	6	2	2	2
	5	15	3	6	2	2	2
Left	6	16	12	0	2	2	0
	7	16	12	0	2	2	0

Table 95: **User I/Os Per Bank for XC3S200 and XC3S400 in PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	16	9	0	2	3	2
	1	15	9	0	2	2	2
Right	2	19	14	0	2	3	0
	3	20	15	0	2	3	0
Bottom	4	17	4	6	2	3	2
	5	15	3	6	2	2	2
Left	6	19	14	0	2	3	0
	7	20	15	0	2	3	0

Table 100: **FG456 Package Pinout *(Cont'd)***

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
0	N.C. (◆)	IO_L22N_0	E8	I/O
0	N.C. (◆)	IO_L22P_0	D8	I/O
0	IO_L24N_0	IO_L24N_0	B8	I/O
0	IO_L24P_0	IO_L24P_0	A8	I/O
0	IO_L25N_0	IO_L25N_0	F9	I/O
0	IO_L25P_0	IO_L25P_0	E9	I/O
0	IO_L27N_0	IO_L27N_0	B9	I/O
0	IO_L27P_0	IO_L27P_0	A9	I/O
0	IO_L28N_0	IO_L28N_0	F10	I/O
0	IO_L28P_0	IO_L28P_0	E10	I/O
0	IO_L29N_0	IO_L29N_0	C10	I/O
0	IO_L29P_0	IO_L29P_0	B10	I/O
0	IO_L30N_0	IO_L30N_0	F11	I/O
0	IO_L30P_0	IO_L30P_0	E11	I/O
0	IO_L31N_0	IO_L31N_0	D11	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C11	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B11	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A11	GCLK
0	VCCO_0	VCCO_0	C8	VCCO
0	VCCO_0	VCCO_0	F8	VCCO
0	VCCO_0	VCCO_0	G9	VCCO
0	VCCO_0	VCCO_0	G10	VCCO
0	VCCO_0	VCCO_0	G11	VCCO
1	IO	IO	A12	I/O
1	IO	IO	E16	I/O
1	IO	IO	F12	I/O
1	IO	IO	F13	I/O
1	IO	IO	F16	I/O
1	IO	IO	F17	I/O
1	IO/VREF_1	IO/VREF_1	E13	VREF
1	N.C. (◆)	IO/VREF_1	F14	VREF
1	IO_L01N_1/VRP_1	IO_L01N_1/VRP_1	C19	DCI
1	IO_L01P_1/VRN_1	IO_L01P_1/VRN_1	B20	DCI
1	IO_L06N_1/VREF_1	IO_L06N_1/VREF_1	A19	VREF
1	IO_L06P_1	IO_L06P_1	B19	I/O
1	IO_L09N_1	IO_L09N_1	C18	I/O
1	IO_L09P_1	IO_L09P_1	D18	I/O
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	A18	VREF
1	IO_L10P_1	IO_L10P_1	B18	I/O
1	IO_L15N_1	IO_L15N_1	D17	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	M25	VREF
2	IO_L34P_2	IO_L34P_2	IO_L34P_2	IO_L34P_2	IO_L34P_2	M26	I/O
2	IO_L35N_2	IO_L35N_2	IO_L35N_2	IO_L35N_2	IO_L35N_2	N19	I/O
2	IO_L35P_2	IO_L35P_2	IO_L35P_2	IO_L35P_2	IO_L35P_2	N20	I/O
2	IO_L38N_2	IO_L38N_2	IO_L38N_2	IO_L38N_2	IO_L38N_2	N21	I/O
2	IO_L38P_2	IO_L38P_2	IO_L38P_2	IO_L38P_2	IO_L38P_2	N22	I/O
2	IO_L39N_2	IO_L39N_2	IO_L39N_2	IO_L39N_2	IO_L39N_2	N23	I/O
2	IO_L39P_2	IO_L39P_2	IO_L39P_2	IO_L39P_2	IO_L39P_2	N24	I/O
2	IO_L40N_2	IO_L40N_2	IO_L40N_2	IO_L40N_2	IO_L40N_2	N25	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	N26	VREF
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	G24	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	J19	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	K19	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	L18	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	L24	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	M18	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	N17	VCCO
2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	VCCO_2	N18	VCCO
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	AA22	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	AA21	DCI
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	AB24	VREF
3	IO_L02P_3	IO_L02P_3	IO_L02P_3	IO_L02P_3	IO_L02P_3	AB23	I/O
3	IO_L03N_3	IO_L03N_3	IO_L03N_3	IO_L03N_3	IO_L03N_3	AC26	I/O
3	IO_L03P_3	IO_L03P_3	IO_L03P_3	IO_L03P_3	IO_L03P_3	AC25	I/O
3	N.C. (◆)	IO_L05N_3	IO_L05N_3	IO_L05N_3	IO_L05N_3	Y21	I/O
3	N.C. (◆)	IO_L05P_3	IO_L05P_3	IO_L05P_3	IO_L05P_3	Y20	I/O
3	N.C. (◆)	IO_L06N_3	IO_L06N_3	IO_L06N_3	IO_L06N_3	AB26	I/O
3	N.C. (◆)	IO_L06P_3	IO_L06P_3	IO_L06P_3	IO_L06P_3	AB25	I/O
3	N.C. (◆)	IO_L07N_3	IO_L07N_3	IO_L07N_3	IO_L07N_3	AA24	I/O
3	N.C. (◆)	IO_L07P_3	IO_L07P_3	IO_L07P_3	IO_L07P_3	AA23	I/O
3	N.C. (◆)	IO_L08N_3	IO_L08N_3	IO_L08N_3	IO_L08N_3	Y23	I/O
3	N.C. (◆)	IO_L08P_3	IO_L08P_3	IO_L08P_3	IO_L08P_3	Y22	I/O
3	N.C. (◆)	IO_L09N_3	IO_L09N_3	IO_L09N_3	IO_L09N_3	AA26	I/O
3	N.C. (◆)	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	AA25	VREF
3	N.C. (◆)	IO_L10N_3	IO_L10N_3	IO_L10N_3	IO_L10N_3	W21	I/O
3	N.C. (◆)	IO_L10P_3	IO_L10P_3	IO_L10P_3	IO_L10P_3	W20	I/O
3	IO_L14N_3	IO_L14N_3	IO_L14N_3	IO_L14N_3	IO_L14N_3	Y26	I/O
3	IO_L14P_3	IO_L14P_3	IO_L14P_3	IO_L14P_3	IO_L14P_3	Y25	I/O
3	IO_L16N_3	IO_L16N_3	IO_L16N_3	IO_L16N_3	IO_L16N_3	V21	I/O
3	IO_L16P_3	IO_L16P_3	IO_L16P_3	IO_L16P_3	IO_L16P_3	W22	I/O
3	IO_L17N_3	IO_L17N_3	IO_L17N_3	IO_L17N_3	IO_L17N_3	W24	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	W23	VREF

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	VCCO_3	Y24	VCCO
4	IO	IO	IO	IO	IO	AA20	I/O
4	IO	IO	IO	IO	IO	AD15	I/O
4	N.C. (◆)	IO	IO	IO	IO	AD19	I/O
4	IO	IO	IO	IO	IO	AD23	I/O
4	IO	IO	IO	IO	IO	AF21	I/O
4	IO	IO	IO	IO	IO	AF22	I/O
4	IO	IO	IO	IO	IO	W15	I/O
4	IO	IO	IO	IO	IO	W16	I/O
4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	AB14	VREF
4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	AD25	VREF
4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	IO/VREF_4	Y17	VREF
4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	IO_L01N_4/VRP_4	AB22	DCI
4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	IO_L01P_4/VRN_4	AC22	DCI
4	IO_L04N_4	IO_L04N_4	IO_L04N_4	IO_L04N_4	IO_L04N_4	AE24	I/O
4	IO_L04P_4	IO_L04P_4	IO_L04P_4	IO_L04P_4	IO_L04P_4	AF24	I/O
4	IO_L05N_4	IO_L05N_4	IO_L05N_4	IO_L05N_4	IO_L05N_4	AE23	I/O
4	IO_L05P_4	IO_L05P_4	IO_L05P_4	IO_L05P_4	IO_L05P_4	AF23	I/O
4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	IO_L06N_4/VREF_4	AD22	VREF
4	IO_L06P_4	IO_L06P_4	IO_L06P_4	IO_L06P_4	IO_L06P_4	AE22	I/O
4	IO_L07N_4	IO_L07N_4	IO_L07N_4	IO_L07N_4	IO_L07N_4	AB21	I/O
4	IO_L07P_4	IO_L07P_4	IO_L07P_4	IO_L07P_4	IO_L07P_4	AC21	I/O
4	IO_L08N_4	IO_L08N_4	IO_L08N_4	IO_L08N_4	IO_L08N_4	AD21	I/O
4	IO_L08P_4	IO_L08P_4	IO_L08P_4	IO_L08P_4	IO_L08P_4	AE21	I/O
4	IO_L09N_4	IO_L09N_4	IO_L09N_4	IO_L09N_4	IO_L09N_4	AB20	I/O
4	IO_L09P_4	IO_L09P_4	IO_L09P_4	IO_L09P_4	IO_L09P_4	AC20	I/O
4	IO_L10N_4	IO_L10N_4	IO_L10N_4	IO_L10N_4	IO_L10N_4	AE20	I/O
4	IO_L10P_4	IO_L10P_4	IO_L10P_4	IO_L10P_4	IO_L10P_4	AF20	I/O
4	N.C. (◆)	IO_L11N_4	IO_L11N_4	IO_L11N_4	IO_L11N_4	Y19	I/O
4	N.C. (◆)	IO_L11P_4	IO_L11P_4	IO_L11P_4	IO_L11P_4	AA19	I/O
4	N.C. (◆)	IO_L12N_4	IO_L12N_4	IO_L12N_4	IO_L12N_4	AB19	I/O
4	N.C. (◆)	IO_L12P_4	IO_L12P_4	IO_L12P_4	IO_L12P_4	AC19	I/O
4	IO_L15N_4	IO_L15N_4	IO_L15N_4	IO_L15N_4	IO_L15N_4	AE19	I/O
4	IO_L15P_4	IO_L15P_4	IO_L15P_4	IO_L15P_4	IO_L15P_4	AF19	I/O
4	IO_L16N_4	IO_L16N_4	IO_L16N_4	IO_L16N_4	IO_L16N_4	Y18	I/O
4	IO_L16P_4	IO_L16P_4	IO_L16P_4	IO_L16P_4	IO_L16P_4	AA18	I/O
4	N.C. (◆)	IO_L17N_4	IO_L17N_4	IO_L17N_4	IO_L17N_4	AB18	I/O
4	N.C. (◆)	IO_L17P_4	IO_L17P_4	IO_L17P_4	IO_L17P_4	AC18	I/O
4	N.C. (◆)	IO_L18N_4	IO_L18N_4	IO_L18N_4	IO_L18N_4	AD18	I/O
4	N.C. (◆)	IO_L18P_4	IO_L18P_4	IO_L18P_4	IO_L18P_4	AE18	I/O
4	IO_L19N_4	IO_L19N_4	IO_L19N_4	IO_L19N_4	IO_L19N_4	AC17	I/O
4	IO_L19P_4	IO_L19P_4	IO_L19P_4	IO_L19P_4	IO_L19P_4	AA17	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	U17	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	U18	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V9	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V10	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V17	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	V18	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	W8	VCCINT
N/A	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	W19	VCCINT
VCC AUX	CCLK	CCLK	CCLK	CCLK	CCLK	AD26	CONFIG
VCC AUX	DONE	DONE	DONE	DONE	DONE	AC24	CONFIG
VCC AUX	HSWAP_EN	HSWAP_EN	HSWAP_EN	HSWAP_EN	HSWAP_EN	C2	CONFIG
VCC AUX	M0	M0	M0	M0	M0	AE3	CONFIG
VCC AUX	M1	M1	M1	M1	M1	AC3	CONFIG
VCC AUX	M2	M2	M2	M2	M2	AF3	CONFIG
VCC AUX	PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	D3	CONFIG
VCC AUX	TCK	TCK	TCK	TCK	TCK	B24	JTAG
VCC AUX	TDI	TDI	TDI	TDI	TDI	C1	JTAG
VCC AUX	TDO	TDO	TDO	TDO	TDO	D24	JTAG
VCC AUX	TMS	TMS	TMS	TMS	TMS	A24	JTAG

Notes:
1. XC3S1500 balls D25 and F25 are not VREF pins although they are designated as such. If a design uses an IOSTANDARD requiring VREF in bank 2 then apply the workaround in Answer Record 20519.
2. XC3S4000 is pin compatible with XC3S2000 but uses alternate differential pair labeling on six package balls (H20, H21, H22, H23, H24, J21).
3. XC3S5000 is pin compatible with XC3S4000 but uses alternate differential pair functionality on fifteen package balls (A3, A8, B8, B18, C4, C8, C18, D8, D18, E8, E18, H23, H24, AB9, and AC9).

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	VCCO_2	VCCO_2	J28	VCCO
2	VCCO_2	VCCO_2	N28	VCCO
3	IO	IO	AB25	I/O
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	AH30	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	AH29	DCI
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	AG28	VREF
3	IO_L02P_3	IO_L02P_3	AG27	I/O
3	IO_L03N_3	IO_L03N_3	AG30	I/O
3	IO_L03P_3	IO_L03P_3	AG29	I/O
3	IO_L04N_3	IO_L04N_3	AF30	I/O
3	IO_L04P_3	IO_L04P_3	AF29	I/O
3	IO_L05N_3	IO_L05N_3	AE26	I/O
3	IO_L05P_3	IO_L05P_3	AF27	I/O
3	IO_L06N_3	IO_L06N_3	AE29	I/O
3	IO_L06P_3	IO_L06P_3	AE28	I/O
3	IO_L07N_3	IO_L07N_3	AD28	I/O
3	IO_L07P_3	IO_L07P_3	AD27	I/O
3	IO_L08N_3	IO_L08N_3	AD30	I/O
3	IO_L08P_3	IO_L08P_3	AD29	I/O
3	IO_L09N_3	IO_L09N_3	AC24	I/O
3	IO_L09P_3/VREF_3	IO_L09P_3/VREF_3	AD25	VREF
3	IO_L10N_3	IO_L10N_3	AC26	I/O
3	IO_L10P_3	IO_L10P_3	AC25	I/O
3	IO_L11N_3	IO_L11N_3	AC28	I/O
3	IO_L11P_3	IO_L11P_3	AC27	I/O
3	IO_L13N_3/VREF_3	IO_L13N_3/VREF_3	AC30	VREF
3	IO_L13P_3	IO_L13P_3	AC29	I/O
3	IO_L14N_3	IO_L14N_3	AB27	I/O
3	IO_L14P_3	IO_L14P_3	AB26	I/O
3	IO_L15N_3	IO_L15N_3	AB30	I/O
3	IO_L15P_3	IO_L15P_3	AB29	I/O
3	IO_L16N_3	IO_L16N_3	AA22	I/O
3	IO_L16P_3	IO_L16P_3	AB23	I/O
3	IO_L17N_3	IO_L17N_3	AA25	I/O
3	IO_L17P_3/VREF_3	IO_L17P_3/VREF_3	AA24	VREF
3	IO_L19N_3	IO_L19N_3	AA29	I/O
3	IO_L19P_3	IO_L19P_3	AA28	I/O
3	IO_L20N_3	IO_L20N_3	Y21	I/O
3	IO_L20P_3	IO_L20P_3	AA21	I/O
3	IO_L21N_3	IO_L21N_3	Y24	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
4	IO_L31P_4/DOUT/BUSY	IO_L31P_4/DOUT/BUSY	AH16	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	AJ16	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	AK16	GCLK
4	N.C. (◆)	IO_L33N_4	AH25	I/O
4	N.C. (◆)	IO_L33P_4	AJ25	I/O
4	N.C. (◆)	IO_L34N_4	AE25	I/O
4	N.C. (◆)	IO_L34P_4	AE24	I/O
4	N.C. (◆)	IO_L35N_4	AG24	I/O
4	N.C. (◆)	IO_L35P_4	AH24	I/O
4	N.C. (◆)	IO_L38N_4	AJ24	I/O
4	N.C. (◆)	IO_L38P_4	AK24	I/O
4	VCCO_4	VCCO_4	Y17	VCCO
4	VCCO_4	VCCO_4	Y18	VCCO
4	VCCO_4	VCCO_4	AD18	VCCO
4	VCCO_4	VCCO_4	AH18	VCCO
4	VCCO_4	VCCO_4	Y19	VCCO
4	VCCO_4	VCCO_4	AB20	VCCO
4	VCCO_4	VCCO_4	AD22	VCCO
4	VCCO_4	VCCO_4	AH22	VCCO
4	VCCO_4	VCCO_4	AF24	VCCO
4	VCCO_4	VCCO_4	AH26	VCCO
5	IO	IO	AE6	I/O
5	IO	IO	AB10	I/O
5	IO	IO	AA11	I/O
5	IO	IO	AA15	I/O
5	IO	IO	AE15	I/O
5	IO/VREF_5	IO/VREF_5	AH4	VREF
5	IO/VREF_5	IO/VREF_5	AK15	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	AK4	DUAL
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AJ4	DUAL
5	IO_L02N_5	IO_L02N_5	AK5	I/O
5	IO_L02P_5	IO_L02P_5	AJ5	I/O
5	IO_L03N_5	IO_L03N_5	AF6	I/O
5	IO_L03P_5	IO_L03P_5	AG5	I/O
5	IO_L04N_5	IO_L04N_5	AJ6	I/O
5	IO_L04P_5	IO_L04P_5	AH6	I/O
5	IO_L05N_5	IO_L05N_5	AE7	I/O
5	IO_L05P_5	IO_L05P_5	AD7	I/O
5	IO_L06N_5	IO_L06N_5	AH7	I/O
5	IO_L06P_5	IO_L06P_5	AG7	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
7	IO_L23N_7	IO_L23N_7	L3	I/O
7	IO_L23P_7	IO_L23P_7	L4	I/O
7	IO_L24N_7	IO_L24N_7	L1	I/O
7	IO_L24P_7	IO_L24P_7	L2	I/O
7	N.C. (◆)	IO_L25N_7	M6	I/O
7	N.C. (◆)	IO_L25P_7	M7	I/O
7	IO_L26N_7	IO_L26N_7	M3	I/O
7	IO_L26P_7	IO_L26P_7	M4	I/O
7	IO_L27N_7	IO_L27N_7	M1	I/O
7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	M2	VREF
7	IO_L28N_7	IO_L28N_7	N10	I/O
7	IO_L28P_7	IO_L28P_7	M10	I/O
7	IO_L29N_7	IO_L29N_7	N8	I/O
7	IO_L29P_7	IO_L29P_7	N9	I/O
7	IO_L31N_7	IO_L31N_7	N1	I/O
7	IO_L31P_7	IO_L31P_7	N2	I/O
7	IO_L32N_7	IO_L32N_7	P9	I/O
7	IO_L32P_7	IO_L32P_7	P10	I/O
7	IO_L33N_7	IO_L33N_7	P6	I/O
7	IO_L33P_7	IO_L33P_7	P7	I/O
7	IO_L34N_7	IO_L34N_7	P2	I/O
7	IO_L34P_7	IO_L34P_7	P3	I/O
7	IO_L35N_7	IO_L35N_7	R9	I/O
7	IO_L35P_7	IO_L35P_7	R10	I/O
7	IO_L37N_7	IO_L37N_7	R7	I/O
7	IO_L37P_7/VREF_7	IO_L37P_7/VREF_7	R8	VREF
7	IO_L38N_7	IO_L38N_7	R5	I/O
7	IO_L38P_7	IO_L38P_7	R6	I/O
7	IO_L39N_7	IO_L39N_7	R3	I/O
7	IO_L39P_7	IO_L39P_7	R4	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	R1	VREF
7	IO_L40P_7	IO_L40P_7	R2	I/O
7	N.C. (◆)	IO_L46N_7	M8	I/O
7	N.C. (◆)	IO_L46P_7	M9	I/O
7	N.C. (◆)	IO_L49N_7	N6	I/O
7	N.C. (◆)	IO_L49P_7	M5	I/O
7	N.C. (◆)	IO_L50N_7	N4	I/O
7	N.C. (◆)	IO_L50P_7	N5	I/O
7	VCCO_7	VCCO_7	E3	VCCO
7	VCCO_7	VCCO_7	J3	VCCO

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
0	IO_L23P_0	IO_L23P_0	J15	I/O
0	IO_L24N_0	IO_L24N_0	G15	I/O
0	IO_L24P_0	IO_L24P_0	F15	I/O
0	IO_L25N_0	IO_L25N_0	D15	I/O
0	IO_L25P_0	IO_L25P_0	C15	I/O
0	IO_L26N_0	IO_L26N_0	B15	I/O
0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	A15	VREF
0	IO_L27N_0	IO_L27N_0	G16	I/O
0	IO_L27P_0	IO_L27P_0	F16	I/O
0	IO_L28N_0	IO_L28N_0	C16	I/O
0	IO_L28P_0	IO_L28P_0	B16	I/O
0	IO_L29N_0	IO_L29N_0	J17	I/O
0	IO_L29P_0	IO_L29P_0	H17	I/O
0	IO_L30N_0	IO_L30N_0	G17	I/O
0	IO_L30P_0	IO_L30P_0	F17	I/O
0	IO_L31N_0	IO_L31N_0	D17	I/O
0	IO_L31P_0/VREF_0	IO_L31P_0/VREF_0	C17	VREF
0	IO_L32N_0/GCLK7	IO_L32N_0/GCLK7	B17	GCLK
0	IO_L32P_0/GCLK6	IO_L32P_0/GCLK6	A17	GCLK
0	N.C. (◆)	IO_L33N_0	D7	I/O
0	N.C. (◆)	IO_L33P_0	C7	I/O
0	N.C. (◆)	IO_L34N_0	B7	I/O
0	N.C. (◆)	IO_L34P_0	A7	I/O
0	IO_L35N_0	IO_L35N_0	E8	I/O
0	IO_L35P_0	IO_L35P_0	D8	I/O
0	IO_L36N_0	IO_L36N_0	B8	I/O
0	IO_L36P_0	IO_L36P_0	A8	I/O
0	IO_L37N_0	IO_L37N_0	D10	I/O
0	IO_L37P_0	IO_L37P_0	C10	I/O
0	IO_L38N_0	IO_L38N_0	B10	I/O
0	IO_L38P_0	IO_L38P_0	A10	I/O
0	N.C. (◆)	IO_L39N_0	G11	I/O
0	N.C. (◆)	IO_L39P_0	F11	I/O
0	N.C. (◆)	IO_L40N_0	B11	I/O
0	N.C. (◆)	IO_L40P_0	A11	I/O
0	VCCO_0	VCCO_0	B13	VCCO
0	VCCO_0	VCCO_0	C4	VCCO
0	VCCO_0	VCCO_0	C8	VCCO
0	VCCO_0	VCCO_0	D11	VCCO
0	VCCO_0	VCCO_0	D16	VCCO

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
1	VCCO_1	VCCO_1	M22	VCCO
2	IO	IO	G33	I/O
2	IO	IO	G34	I/O
2	IO	IO	U25	I/O
2	IO	IO	U26	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C33	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C34	DCI
2	IO_L02N_2	IO_L02N_2	D33	I/O
2	IO_L02P_2	IO_L02P_2	D34	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	E32	VREF
2	IO_L03P_2	IO_L03P_2	E33	I/O
2	IO_L04N_2	IO_L04N_2	F31	I/O
2	IO_L04P_2	IO_L04P_2	F32	I/O
2	IO_L05N_2	IO_L05N_2	G29	I/O
2	IO_L05P_2	IO_L05P_2	G30	I/O
2	IO_L06N_2	IO_L06N_2	H29	I/O
2	IO_L06P_2	IO_L06P_2	H30	I/O
2	IO_L07N_2	IO_L07N_2	H33	I/O
2	IO_L07P_2	IO_L07P_2	H34	I/O
2	IO_L08N_2	IO_L08N_2	J28	I/O
2	IO_L08P_2	IO_L08P_2	J29	I/O
2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	H31	VREF
2	IO_L09P_2	IO_L09P_2	J31	I/O
2	IO_L10N_2	IO_L10N_2	J32	I/O
2	IO_L10P_2	IO_L10P_2	J33	I/O
2	IO_L11N_2	IO_L11N_2	J27	I/O
2	IO_L11P_2	IO_L11P_2	K26	I/O
2	IO_L12N_2	IO_L12N_2	K27	I/O
2	IO_L12P_2	IO_L12P_2	K28	I/O
2	IO_L13N_2	IO_L13N_2	K29	I/O
2	IO_L13P_2/VREF_2	IO_L13P_2/VREF_2	K30	VREF
2	IO_L14N_2	IO_L14N_2	K31	I/O
2	IO_L14P_2	IO_L14P_2	K32	I/O
2	IO_L15N_2	IO_L15N_2	K33	I/O
2	IO_L15P_2	IO_L15P_2	K34	I/O
2	IO_L16N_2	IO_L16N_2	L25	I/O
2	IO_L16P_2	IO_L16P_2	L26	I/O
2	N.C. (◆)	IO_L17N_2	L28	I/O
2	N.C. (◆)	IO_L17P_2/ VREF_2	L29	VREF

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L24P_3	IO_L24P_3	AC26	I/O
3	IO_L26N_3	IO_L26N_3	AA28	I/O
3	IO_L26P_3	IO_L26P_3	AA27	I/O
3	IO_L27N_3	IO_L27N_3	AA30	I/O
3	IO_L27P_3	IO_L27P_3	AA29	I/O
3	IO_L28N_3	IO_L28N_3	AA32	I/O
3	IO_L28P_3	IO_L28P_3	AA31	I/O
3	IO_L29N_3	IO_L29N_3	AA34	I/O
3	IO_L29P_3	IO_L29P_3	AA33	I/O
3	IO_L30N_3	IO_L30N_3	Y29	I/O
3	IO_L30P_3	IO_L30P_3	Y28	I/O
3	IO_L31N_3	IO_L31N_3	Y32	I/O
3	IO_L31P_3	IO_L31P_3	Y31	I/O
3	IO_L32N_3	IO_L32N_3	Y34	I/O
3	IO_L32P_3	IO_L32P_3	Y33	I/O
3	IO_L33N_3	IO_L33N_3	W25	I/O
3	IO_L33P_3	IO_L33P_3	Y26	I/O
3	IO_L34N_3	IO_L34N_3	W29	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	W28	VREF
3	IO_L35N_3	IO_L35N_3	W33	I/O
3	IO_L35P_3	IO_L35P_3	W32	I/O
3	IO_L37N_3	IO_L37N_3	V28	I/O
3	IO_L37P_3	IO_L37P_3	V27	I/O
3	IO_L38N_3	IO_L38N_3	V30	I/O
3	IO_L38P_3	IO_L38P_3	V29	I/O
3	IO_L39N_3	IO_L39N_3	V32	I/O
3	IO_L39P_3	IO_L39P_3	V31	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	V34	VREF
3	IO_L40P_3	IO_L40P_3	V33	I/O
3	N.C. (◆)	IO_L41N_3	AH32	I/O
3	N.C. (◆)	IO_L41P_3	AH31	I/O
3	N.C. (◆)	IO_L44N_3	AD29	I/O
3	N.C. (◆)	IO_L44P_3	AD28	I/O
3	IO_L45N_3	IO_L45N_3	AC34	I/O
3	IO_L45P_3	IO_L45P_3	AC33	I/O
3	IO_L46N_3	IO_L46N_3	AB28	I/O
3	IO_L46P_3	IO_L46P_3	AB27	I/O
3	IO_L47N_3	IO_L47N_3	AB32	I/O
3	IO_L47P_3	IO_L47P_3	AB31	I/O
3	IO_L48N_3	IO_L48N_3	AA24	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
7	IO_L45P_7	IO_L45P_7	M2	I/O
7	IO_L46N_7	IO_L46N_7	N7	I/O
7	IO_L46P_7	IO_L46P_7	N8	I/O
7	N.C. (◆)	IO_L47N_7	P9	I/O
7	N.C. (◆)	IO_L47P_7	P10	I/O
7	IO_L49N_7	IO_L49N_7	P1	I/O
7	IO_L49P_7	IO_L49P_7	P2	I/O
7	IO_L50N_7	IO_L50N_7	R10	I/O
7	IO_L50P_7	IO_L50P_7	R11	I/O
7	N.C. (◆)	IO_L51N_7	U11	I/O
7	N.C. (◆)	IO_L51P_7	T11	I/O
7	VCCO_7	VCCO_7	D3	VCCO
7	VCCO_7	VCCO_7	H3	VCCO
7	VCCO_7	VCCO_7	H7	VCCO
7	VCCO_7	VCCO_7	L4	VCCO
7	VCCO_7	VCCO_7	L8	VCCO
7	VCCO_7	VCCO_7	N12	VCCO
7	VCCO_7	VCCO_7	N2	VCCO
7	VCCO_7	VCCO_7	N6	VCCO
7	VCCO_7	VCCO_7	P12	VCCO
7	VCCO_7	VCCO_7	R12	VCCO
7	VCCO_7	VCCO_7	R8	VCCO
7	VCCO_7	VCCO_7	T12	VCCO
7	VCCO_7	VCCO_7	T4	VCCO
N/A	GND	GND	A1	GND
N/A	GND	GND	A13	GND
N/A	GND	GND	A16	GND
N/A	GND	GND	A19	GND
N/A	GND	GND	A2	GND
N/A	GND	GND	A22	GND
N/A	GND	GND	A26	GND
N/A	GND	GND	A30	GND
N/A	GND	GND	A33	GND
N/A	GND	GND	A34	GND
N/A	GND	GND	A5	GND
N/A	GND	GND	A9	GND
N/A	GND	GND	AA14	GND
N/A	GND	GND	AA15	GND
N/A	GND	GND	AA16	GND
N/A	GND	GND	AA17	GND

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	VCCAUX	VCCAUX	Y5	VCCAUX
N/A	VCCINT	VCCINT	AA13	VCCINT
N/A	VCCINT	VCCINT	AA22	VCCINT
N/A	VCCINT	VCCINT	AB13	VCCINT
N/A	VCCINT	VCCINT	AB14	VCCINT
N/A	VCCINT	VCCINT	AB15	VCCINT
N/A	VCCINT	VCCINT	AB16	VCCINT
N/A	VCCINT	VCCINT	AB19	VCCINT
N/A	VCCINT	VCCINT	AB20	VCCINT
N/A	VCCINT	VCCINT	AB21	VCCINT
N/A	VCCINT	VCCINT	AB22	VCCINT
N/A	VCCINT	VCCINT	AC12	VCCINT
N/A	VCCINT	VCCINT	AC17	VCCINT
N/A	VCCINT	VCCINT	AC18	VCCINT
N/A	VCCINT	VCCINT	AC23	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	M23	VCCINT
N/A	VCCINT	VCCINT	N13	VCCINT
N/A	VCCINT	VCCINT	N14	VCCINT
N/A	VCCINT	VCCINT	N15	VCCINT
N/A	VCCINT	VCCINT	N16	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	N20	VCCINT
N/A	VCCINT	VCCINT	N21	VCCINT
N/A	VCCINT	VCCINT	N22	VCCINT
N/A	VCCINT	VCCINT	P13	VCCINT
N/A	VCCINT	VCCINT	P22	VCCINT
N/A	VCCINT	VCCINT	R13	VCCINT
N/A	VCCINT	VCCINT	R22	VCCINT
N/A	VCCINT	VCCINT	T13	VCCINT
N/A	VCCINT	VCCINT	T22	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT
N/A	VCCINT	VCCINT	U23	VCCINT
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	V23	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	W22	VCCINT
N/A	VCCINT	VCCINT	Y13	VCCINT

Revision History

Date	Version	Description
04/03/03	1.0	Initial Xilinx release.
04/21/03	1.1	Added information on the VQ100 package footprint, including a complete pinout table (Table 87) and footprint diagram (Figure 44). Updated Table 85 with final I/O counts for the VQ100 package. Also added final differential I/O pair counts for the TQ144 package. Added clarifying comments to HSWAP_EN pin description on page 119. Updated the footprint diagram for the FG900 package shown in Figure 55a and Figure 55b. Some thick lines separating I/O banks were incorrect. Made cosmetic changes to Figure 40, Figure 42, and Figure 43. Updated Xilinx hypertext links. Added XC3S200 and XC3S400 to Pin Name column in Table 91.
05/12/03	1.1.1	AM32 pin was missing GND label in FG1156 package diagram (Figure 53).
07/11/03	1.1.2	Corrected misspellings of GCLK in Table 69 and Table 70. Changed CMOS25 to LVCMOS25 in Dual-Purpose Pin I/O Standard During Configuration section. Clarified references to Module 2. For XC3S5000 in FG1156 package, corrected N.C. symbol to a black square in Table 110, key, and package drawing.
07/29/03	1.2	Corrected pin names on FG1156 package. Some package balls incorrectly included LVDS pair names. The affected balls on the FG1156 package include G1, G2, G33, G34, U9, U10, U25, U26, V9, V10, V25, V26, AH1, AH2, AH33, AH34. The number of LVDS pairs is unaffected. Modified affected balls and re-sorted rows in Table 110. Updated affected balls in Figure 53. Also updated ASCII and Excel electronic versions of FG1156 pinout.
08/19/03	1.2.1	Removed 100 MHz ConfigRate option in CCLK: Configuration Clock section and in Table 80. Added note that TDO is a totem-pole output in Table 77.
10/09/03	1.2.2	Some pins had incorrect bank designations and were improperly sorted in Table 93. No pin names or functions changed. Renamed DCI_IN to DCI and added black diamond to N.C. pins in Table 93. In Figure 47, removed some extraneous text from pin 106 and corrected spelling of pins 45, 48, and 81.
12/17/03	1.3	Added FG320 pin tables and pinout diagram (FG320: 320-lead Fine-pitch Ball Grid Array). Made cosmetic changes to the TQ144 footprint (Figure 46), the PQ208 footprint (Figure 47), the FG676 footprint (Figure 53), and the FG900 footprint (Figure 55). Clarified wording in Precautions When Using the JTAG Port in 3.3V Environments section.
02/27/04	1.4	Clarified wording in Using JTAG Port After Configuration section. In Table 81, reduced package height for FG320 and increased maximum I/O values for the FG676, FG900, and FG1156 packages.
07/13/04	1.5	Added information on lead-free (Pb-free) package options to the Package Overview section plus Table 81 and Table 83. Clarified the VRN_# reference resistor requirements for I/O standards that use single termination as described in the DCI Termination Types section and in Figure 42b. Graduated from Advance Product Specification to Product Specification.
08/24/04	1.5.1	Removed XC3S2000 references from FG1156: 1156-lead Fine-pitch Ball Grid Array.
01/17/05	1.6	Added XC3S50 in CP132 package option. Added XC3S2000 in FG456 package option. Added XC3S4000 in FG676 package option. Added Selecting the Right Package Option section. Modified or added Table 81, Table 83, Table 84, Table 85, Table 89, Table 90, Table 100, Table 102, Table 103, Table 106, Figure 45, and Figure 53.
08/19/05	1.7	Removed term “weak” from the description of pull-up and pull-down resistors. Added IDCODE Register values. Added signal integrity precautions to CCLK: Configuration Clock and indicated that CCLK should be treated as an I/O during Master mode in Table 79.
04/03/06	2.0	Added Package Thermal Characteristics. Updated Figure 41 to make it a more obvious example. Added detail about which pins have dedicated pull-up resistors during configuration, regardless of the HSWAP_EN value to Table 70 and to Pin Behavior During Configuration. Updated Precautions When Using the JTAG Port in 3.3V Environments.
04/26/06	2.1	Corrected swapped data row in Table 86. The Theta-JA with zero airflow column was swapped with the Theta-JC column. Made additional notations on CONFIG and JTAG pins that have pull-up resistors during configuration, regardless of the HSWAP_EN input.
05/25/07	2.2	Added link on page 128 to Material Declaration Data Sheets. Corrected units typo in Table 74. Added Note 1 to Table 103 about VREF for XC3S1500 in FG676.