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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	294912
Number of I/O	141
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s400-4pqg208c



Spartan-3 FPGA Family: Introduction and Ordering Information

DS099 (v3.0) October 29, 2012

Product Specification

Introduction

The Spartan®-3 family of Field-Programmable Gate Arrays is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The eight-member family offers densities ranging from 50,000 to 5,000,000 system gates, as shown in [Table 1](#).

The Spartan-3 family builds on the success of the earlier Spartan-IIE family by increasing the amount of logic resources, the capacity of internal RAM, the total number of I/Os, and the overall level of performance as well as by improving clock management functions. Numerous enhancements derive from the Virtex®-II platform technology. These Spartan-3 FPGA enhancements, combined with advanced process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3 FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection and digital television equipment.

The Spartan-3 family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

Table 1: Summary of Spartan-3 FPGA Attributes

Device	System Gates	Equivalent Logic Cells ⁽¹⁾	CLB Array (One CLB = Four Slices)			Distributed RAM Bits (K=1024)	Block RAM Bits (K=1024)	Dedicated Multipliers	DCMs	Max. User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs						
XC3S50 ⁽²⁾	50K	1,728	16	12	192	12K	72K	4	2	124	56
XC3S200 ⁽²⁾	200K	4,320	24	20	480	30K	216K	12	4	173	76
XC3S400 ⁽²⁾	400K	8,064	32	28	896	56K	288K	16	4	264	116
XC3S1000 ⁽²⁾	1M	17,280	48	40	1,920	120K	432K	24	4	391	175
XC3S1500	1.5M	29,952	64	52	3,328	208K	576K	32	4	487	221
XC3S2000	2M	46,080	80	64	5,120	320K	720K	40	4	565	270
XC3S4000	4M	62,208	96	72	6,912	432K	1,728K	96	4	633	300
XC3S5000	5M	74,880	104	80	8,320	520K	1,872K	104	4	633	300

Notes:

- Logic Cell = 4-input Look-Up Table (LUT) plus a 'D' flip-flop. "Equivalent Logic Cells" equals "Total CLBs" x 8 Logic Cells/CLB x 1.125 effectiveness.
- These devices are available in Xilinx Automotive versions as described in [DS314: Spartan-3 Automotive XA FPGA Family](#).

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Features

- Low-cost, high-performance logic solution for high-volume, consumer-oriented applications
 - Densities up to 74,880 logic cells
- SelectIO™ interface signaling
 - Up to 633 I/O pins
 - 622+ Mb/s data transfer rate per I/O
 - 18 single-ended signal standards
 - 8 differential I/O standards including LVDS, RSDS
 - Termination by Digitally Controlled Impedance
 - Signal swing ranging from 1.14V to 3.465V
 - Double Data Rate (DDR) support
 - [DDR, DDR2 SDRAM support](#) up to 333 Mb/s
- Logic resources
 - Abundant logic cells with shift register capability
 - Wide, fast multiplexers
 - Fast look-ahead carry logic
 - Dedicated 18 x 18 multipliers
 - JTAG logic compatible with IEEE 1149.1/1532
- SelectRAM™ hierarchical memory
 - Up to 1,872 Kbits of total block RAM
 - Up to 520 Kbits of total distributed RAM
- Digital Clock Manager (up to four DCMs)
 - Clock skew elimination
 - Frequency synthesis
 - High resolution phase shifting
- Eight global clock lines and abundant routing
- Fully supported by [Xilinx ISE®](#) and [WebPACK™](#) software development systems
- [MicroBlaze™](#) and [PicoBlaze™](#) processor, [PCI®](#), [PCI Express® PIPE Endpoint](#), and other [IP cores](#)
- Pb-free packaging options
- Automotive [Spartan-3 XA Family](#) variant

Table 10: DCI I/O Standards

Category of Signal Standard	Signal Standard (IOSTANDARD)	V _{CCO} (V)		V _{REF} for Inputs (V)	Termination Type	
		For Outputs	For Inputs		At Output	At Input
Single-Ended						
Gunning Transceiver Logic	GTL_DCI	1.2	1.2	0.8	Single	Single
	GTLP_DCI	1.5	1.5	1.0		
High-Speed Transceiver Logic	HSTL_I_DCI	1.5	1.5	0.75	None	Split
	HSTL_III_DCI	1.5	1.5	0.9	None	Single
	HSTL_I_DCI_18	1.8	1.8	0.9	None	Split
	HSTL_II_DCI_18 DIFF_HSTL_II_18_DCI	1.8	1.8	0.9	Split	
	HSTL_III_DCI_18	1.8	1.8	1.1	None	Single
Low-Voltage CMOS	LVDCI_15	1.5	1.5	—	Controlled impedance driver	None
	LVDCI_18	1.8	1.8	—		
	LVDCI_25	2.5	2.5	—		
	LVDCI_33 ⁽²⁾	3.3	3.3	—		
	LVDCI_DV2_15	1.5	1.5	—	Controlled driver with half-impedance	
	LVDCI_DV2_18	1.8	1.8	—		
	LVDCI_DV2_25	2.5	2.5	—		
	LVDCI_DV2_33	3.3	3.3	—		
Hybrid HSTL Input and LVCMOS Output	HSLVDCI_15	1.5	1.5	0.75	Controlled impedance driver	None
	HSLVDCI_18	1.8	1.8	0.9		
	HSLVDCI_25	2.5	2.5	1.25		
	HSLVDCI_33	3.3	3.3	1.65		
Stub Series Terminated Logic ⁽³⁾	SSTL18_I_DCI	1.8	1.8	0.9	25Ω driver	Split
	SSTL2_I_DCI	2.5	2.5	1.25	25Ω driver	
	SSTL2_II_DCI DIFF_SSTL2_II_DCI	2.5	2.5	1.25	Split with 25Ω driver	
Differential						
Low-Voltage Differential Signaling	LVDS_25_DCI	N/A	2.5	—	None	Split on each line of pair
	LVDS_25_DCI	N/A	2.5	—		

Notes:

- DCI signal standards are not supported in Bank 5 of any Spartan-3 FPGA packaged in a VQ100, CP132, or TQ144 package.
- Equivalent to LVTTTL DCI.
- The SSTL18_II signal standard does not have a DCI equivalent.

The DCI feature operates independently for each of the device's eight banks. Each bank has an 'N' reference pin (VRN) and a 'P' reference pin, (VRP), to calibrate driver and termination resistance. Only when using a DCI standard on a given bank do these two pins function as VRN and VRP. When not using a DCI standard, the two pins function as user I/Os. As shown in Figure 9, add an external reference resistor to pull the VRN pin up to V_{CCO} and another reference resistor to pull the VRP pin down to GND. Also see Figure 42, page 116. Both resistors have the same value—commonly 50Ω —with one-percent tolerance, which is either the characteristic impedance of the line or twice that, depending on the DCI standard in use. Standards having a symbol name that contains the letters "DV2" use a reference resistor value that is twice the line impedance. DCI adjusts the output driver impedance to match the reference resistors' value or half that, according to the standard. DCI always adjusts the on-chip termination resistors to directly match the reference resistors' value.

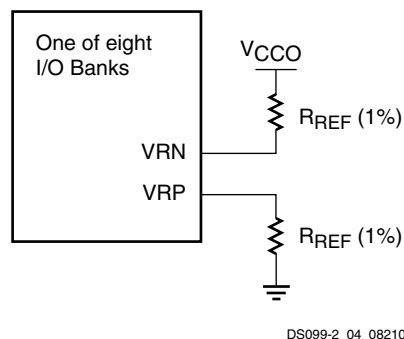


Figure 9: Connection of Reference Resistors (R_{REF})

The rules guiding the use of DCI standards on banks are as follows:

- No more than one DCI I/O standard with a Single Termination is allowed per bank.
- No more than one DCI I/O standard with a Split Termination is allowed per bank.
- Single Termination, Split Termination, Controlled- Impedance Driver, and Controlled-Impedance Driver with Half Impedance can co-exist in the same bank.

See also [The Organization of IOBs into Banks](#), immediately below, and [DCI: User I/O or Digitally Controlled Impedance Resistor Reference Input](#), page 115.

The Organization of IOBs into Banks

IOBs are allocated among eight banks, so that each side of the device has two banks, as shown in Figure 10. For all packages, each bank has independent V_{REF} lines. For example, V_{REF} Bank 3 lines are separate from the V_{REF} lines going to all other banks.

For the Very Thin Quad Flat Pack (VQ), Plastic Quad Flat Pack (PQ), Fine Pitch Thin Ball Grid Array (FT), and Fine Pitch Ball Grid Array (FG) packages, each bank has dedicated V_{CCO} lines. For example, the V_{CCO} Bank 7 lines are separate from the V_{CCO} lines going to all other banks. Thus, Spartan-3 devices in these packages support eight independent V_{CCO} supplies.

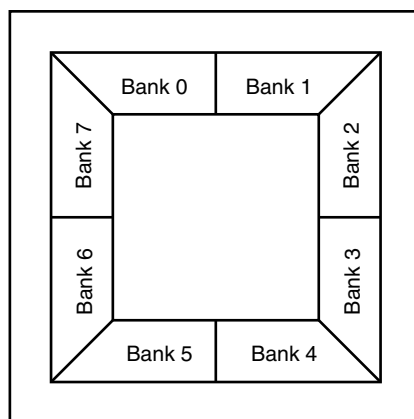


Figure 10: Spartan-3 FPGA I/O Banks (Top View)

The output frequency (f_{CLKFX}) can be expressed as a function of the incoming clock frequency (f_{CLKIN}) as follows:

$$f_{CLKFX} = f_{CLKIN}(\text{CLKFX_MULTIPLY}/\text{CLKFX_DIVIDE}) \quad \text{Equation 3}$$

Regarding the two attributes, it is possible to assign any combination of integer values, provided that two conditions are met:

- The two values fall within their corresponding ranges, as specified in [Table 18](#).
- The f_{CLKFX} frequency calculated from the above expression accords with the DCM's operating frequency specifications.

For example, if $\text{CLKFX_MULTIPLY} = 5$ and $\text{CLKFX_DIVIDE} = 3$, then the frequency of the output clock signal would be 5/3 that of the input clock signal.

DFS Frequency Modes

The DFS supports two operating modes, High Frequency and Low Frequency, with each specified over a different clock frequency range. The $\text{DFS_FREQUENCY_MODE}$ attribute chooses between the two modes. When the attribute is set to LOW, the Low Frequency mode permits the two DFS outputs to operate over a low-to-moderate frequency range. When the attribute is set to HIGH, the High Frequency mode allows both these outputs to operate at the highest possible frequencies.

DFS With or Without the DLL

The DFS component can be used with or without the DLL component:

Without the DLL, the DFS component multiplies or divides the CLKIN signal frequency according to the respective CLKFX_MULTIPLY and CLKFX_DIVIDE values, generating a clock with the new target frequency on the CLKFX and CLKFX180 outputs. Though classified as belonging to the DLL component, the CLKIN input is shared with the DFS component. This case does not employ feedback loop; therefore, it cannot correct for clock distribution delay.

With the DLL, the DFS operates as described in the preceding case, only with the additional benefit of eliminating the clock distribution delay. In this case, a feedback loop from the CLK0 output to the CLKFB input must be present.

The DLL and DFS components work together to achieve this phase correction as follows: Given values for the CLKFX_MULTIPLY and CLKFX_DIVIDE attributes, the DLL selects the delay element for which the output clock edge coincides with the input clock edge whenever mathematically possible. For example, when $\text{CLKFX_MULTIPLY} = 5$ and $\text{CLKFX_DIVIDE} = 3$, the input and output clock edges will coincide every three input periods, which is equivalent in time to five output periods.

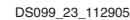
Smaller CLKFX_MULTIPLY and CLKFX_DIVIDE values achieve faster lock times. With no factors common to the two attributes, alignment will occur once with every number of cycles equal to the CLKFX_DIVIDE value. Therefore, it is recommended that the user reduce these values by factoring wherever possible. For example, given $\text{CLKFX_MULTIPLY} = 9$ and $\text{CLKFX_DIVIDE} = 6$, removing a factor of three yields $\text{CLKFX_MULTIPLY} = 3$ and $\text{CLKFX_DIVIDE} = 2$. While both value-pairs will result in the multiplication of clock frequency by 3/2, the latter value-pair will enable the DLL to lock more quickly.

Table 18: DFS Attributes

Attribute	Description	Values
$\text{DFS_FREQUENCY_MODE}$	Chooses between High Frequency and Low Frequency modes	Low, High
CLKFX_MULTIPLY	Frequency multiplier constant	Integer from 2 to 32
CLKFX_DIVIDE	Frequency divisor constant	Integer from 1 to 32

Table 19: DFS Signals

Signal	Direction	Description
CLKFX	Output	Multiplies the CLKIN frequency by the attribute-value ratio ($\text{CLKFX_MULTIPLY}/\text{CLKFX_DIVIDE}$) to generate a clock signal with a new target frequency.
CLKFX180	Output	Generates a clock signal with same frequency as CLKFX, only shifted 180° out-of-phase.



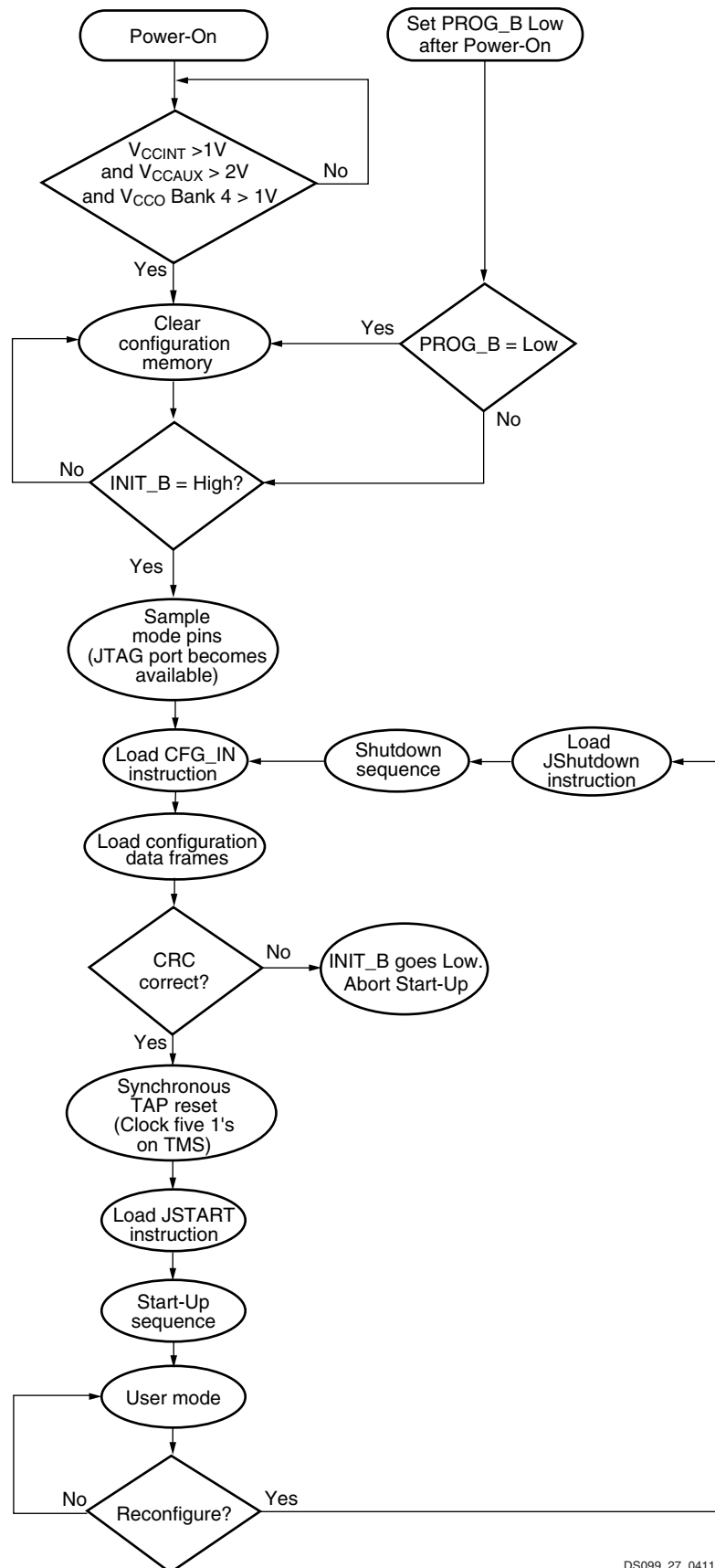
1. There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3K Ω to 4.7K Ω is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330 Ω) in order to ensure a rise time within one clock cycle.
2. For information on how to program the FPGA using 3.3V signals and power, see [3.3V-Tolerant Configuration Interface](#).

Slave Serial mode is selected by applying <111> to the mode pins (M0, M1, and M2). A pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

In Master Serial mode, the FPGA drives CCLK pin, which behaves as a bidirectional I/O pin. The FPGA in the center of [Figure 26](#) is set for Master Serial mode and connects to the serial configuration PROM and to the CCLK inputs of any slave FPGAs in a configuration daisy-chain. The master FPGA drives the configuration clock on the CCLK pin to the Xilinx Serial PROM, which, in response, provides bit-serial data to the FPGA's DIN input. The FPGA accepts this data on each rising CCLK edge. After the master FPGA finishes configuring, it passes data on its DOUT pin to the next FPGA device in a daisy-chain. The DOUT data appears after the falling CCLK clock edge.

Slave Parallel Mode (SelectMAP)

After configuration, it is possible to use any of the Multipurpose pins (DIN/D0-D7, DOUT/BUSY, INIT_B, CS_B, and RDWR_B) as User I/Os. To do this, simply set the BitGen option *Persist* to *No* and assign the desired signals to multipurpose configuration pins using the Xilinx development software. Alternatively, it is possible to continue using the configuration port



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Figure 30: Boundary-Scan Configuration Flow Diagram

Configuration is automatically initiated after power-on unless it is delayed by the user. INIT_B is an open-drain line that the FPGA holds Low during the clearing of the configuration memory. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High. At this point, the configuration data is written to the FPGA. The FPGA pulses the Global Set/Reset (GSR) signal at the end of configuration, resetting all flip-flops. The completion of the entire process is signaled by the DONE pin going High.

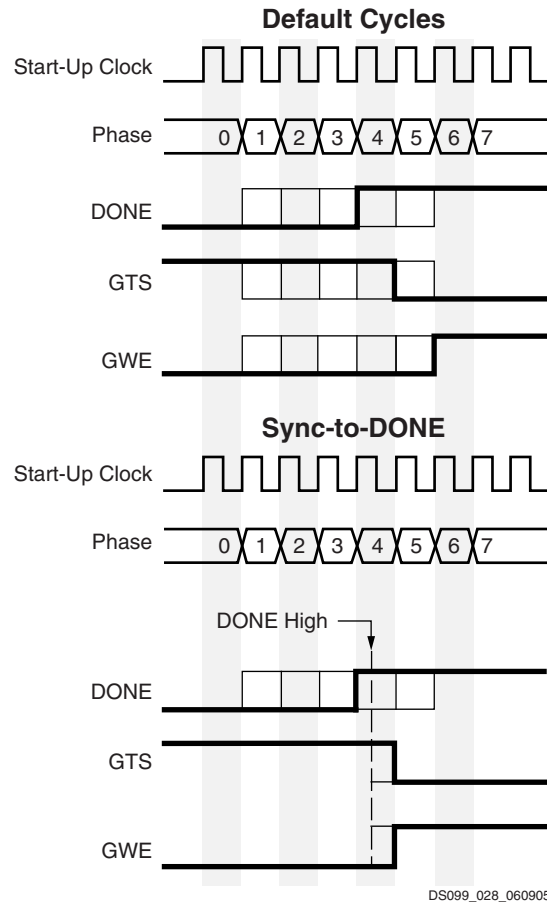


Figure 31: Default Start-Up Sequence

The default start-up sequence, shown in Figure 31, serves as a transition to the User mode. The default start-up sequence is that one CCLK cycle after DONE goes High, the Global Three-State signal (GTS) is released. This permits device outputs to which signals have been assigned to become active. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage elements to begin changing state in response to the design logic and the user clock.

The relative timing of configuration events can be changed via the BitGen options in the Xilinx development software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start synchronously. The sequence can also be paused at any stage, until lock has been achieved on any DCM.

Readback

Using Slave Parallel mode, configuration data from the FPGA can be read back. Readback is supported only in the Slave Parallel and Boundary-Scan modes.

Along with the configuration data, it is possible to read back the contents of all registers, distributed RAM, and block RAM resources. This capability is used for real-time debugging.

Table 56: Block RAM Timing

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T _{BCKO}	When reading from the Block RAM, the time from the active transition at the CLK input to data appearing at the DOUT output	–	2.09	–	2.40	ns
Setup Times						
T _{BDCK}	Time from the setup of data at the DIN inputs to the active transition at the CLK input of the Block RAM	0.43	–	0.49	–	ns
Hold Times						
T _{BCKD}	Time from the active transition at the Block RAM's CLK input to the point where data is last held at the DIN inputs	0	–	0	–	ns
Clock Timing						
T _{BPWH}	Block RAM CLK signal High pulse width	1.19	∞	1.37	∞	ns
T _{BPWL}	Block RAM CLK signal Low pulse width	1.19	∞	1.37	∞	ns

Notes:

- The numbers in this table are based on the operating conditions set forth in [Table 32](#).
- For minimums, use the values reported by the Xilinx timing analyzer.

Clock Distribution Switching Characteristics
Table 57: Clock Distribution Switching Characteristics

Description	Symbol	Maximum		Units
		Speed Grade		
		-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I-input to O-output delay	T _{GIO}	0.36	0.41	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0- and I1-inputs. Same as BUFGCE enable CE-input	T _{GSI}	0.53	0.60	ns

Notes:

- For minimums, use the values reported by the Xilinx timing analyzer.

The 1% precision impedance-matching resistor attached to the VRN_# pin controls the pull-down impedance of NMOS transistor in the input or output buffer. Consequently, the VRN_# pin must connect to VCCO. The 'N' character in "VRN" indicates that this pin controls the I/O buffer's NMOS transistor impedance. The VRN_# pin is only used for split termination.

Each VRN or VRP reference input requires its own resistor. A single resistor cannot be shared between VRN or VRP pins associated with different banks.

During configuration, these pins behave exactly like user-I/O pins. The associated DCI behavior is not active or valid until after configuration completes.

Also see [Digitally Controlled Impedance \(DCI\), page 16](#).

DCI Termination Types

If the I/O in an I/O bank do not use the DCI feature, then no external resistors are required and both the VRP_# and VRN_# pins are available for user I/O, as shown in section [a] of [Figure 42](#).

If the I/O standards within the associated I/O bank require single termination—such as GTL_DCI, GTLP_DCI, or HSTL_III_DCI—then only the VRP_# signal connects to a 1% precision impedance-matching resistor, as shown in section [b] of [Figure 42](#). A resistor is not required for the VRN_# pin.

Finally, if the I/O standards with the associated I/O bank require split termination—such as HSTL_I_DCI, SSTL2_I_DCI, SSTL2_II_DCI, or LVDS_25_DCI and LVDSEXT_25_DCI receivers—then both the VRP_# and VRN_# pins connect to separate 1% precision impedance-matching resistors, as shown in section [c] of [Figure 42](#). Neither pin is available for user I/O.

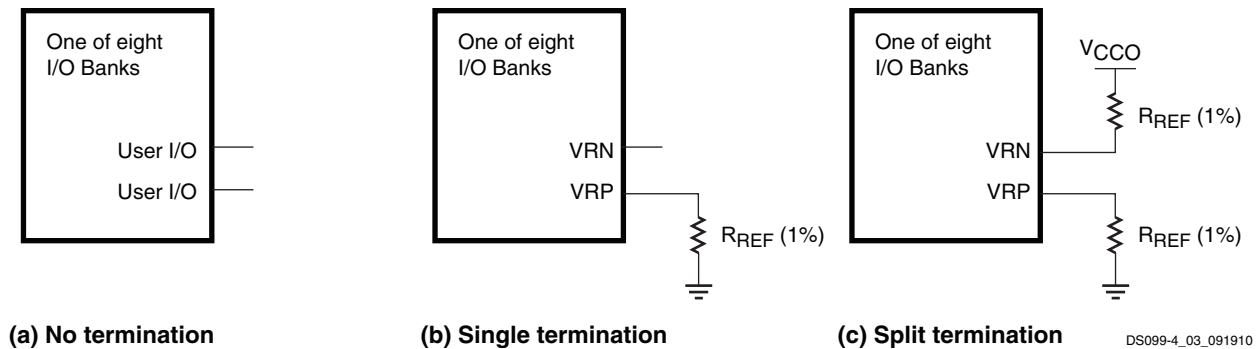


Figure 42: DCI Termination Types

GCLK: Global Clock Buffer Inputs or General-Purpose I/O Pins

These pins are user-I/O pins unless they specifically connect to one of the eight low-skew global clock buffers on the device, specified using the IBUFG primitive.

There are eight GCLK pins per device and two each appear in the top-edge banks, Bank 0 and 1, and the bottom-edge banks, Banks 4 and 5. See [Figure 40](#) for a picture of bank labeling.

During configuration, these pins behave exactly like user-I/O pins.

Also see [Global Clock Network, page 42](#).

CONFIG: Dedicated Configuration Pins

The dedicated configuration pins control the configuration process and are not available as user-I/O pins. Every package has seven dedicated configuration pins. All CONFIG-type pins are powered by the +2.5V VCCAUX supply.

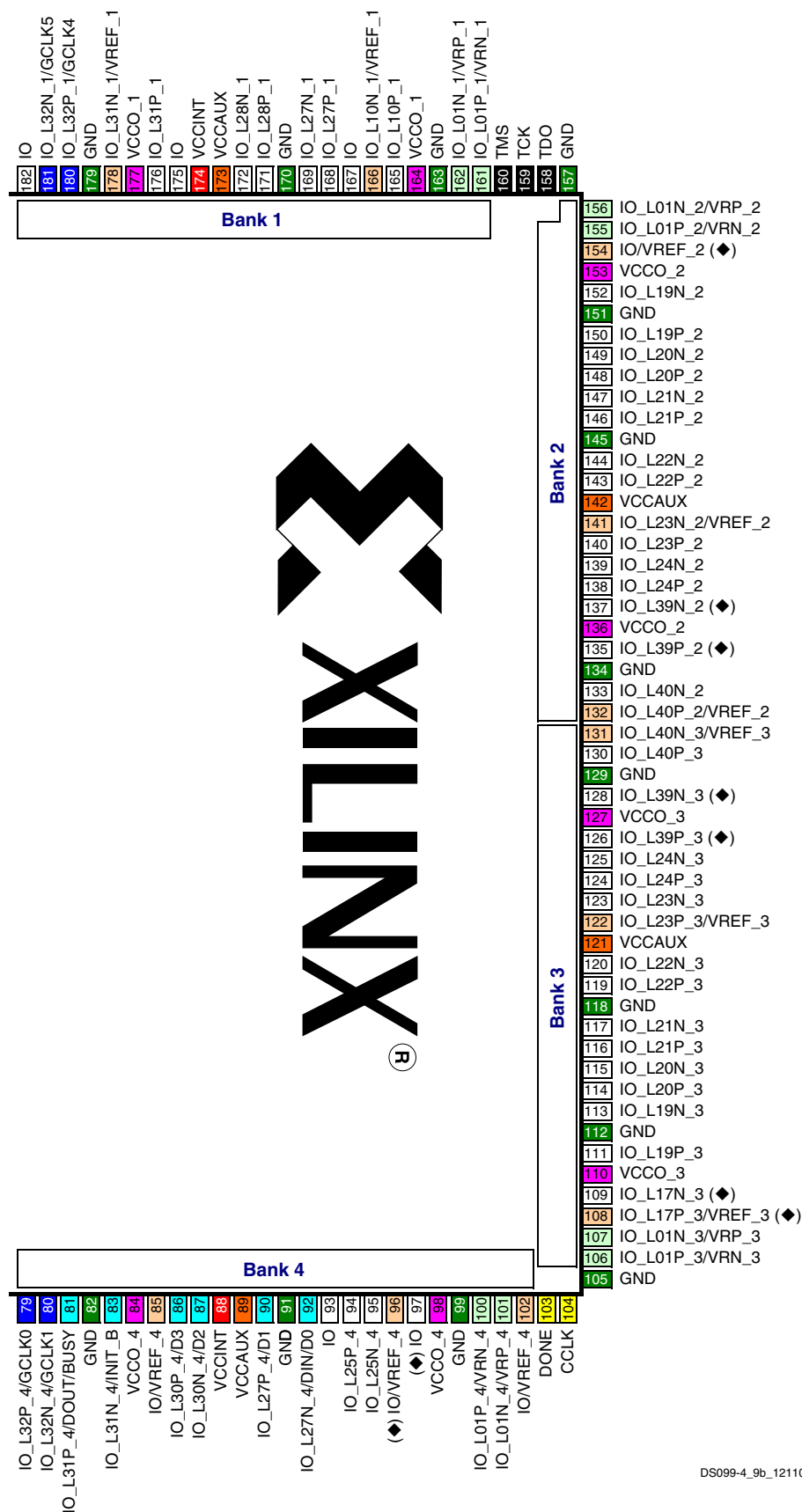
Also see [Configuration, page 46](#).

Table 89: CP132 Package Pinout (Cont'd)

Bank	XC3S50 Pin Name	CP132 Ball	Type
6	IO_L22N_6	K1	I/O
6	IO_L22P_6	J3	I/O
6	IO_L23N_6	J2	I/O
6	IO_L23P_6	J1	I/O
6	IO_L24N_6/VREF_6	H3	VREF
6	IO_L24P_6	H2	I/O
6	IO_L40N_6	H1	I/O
6	IO_L40P_6/VREF_6	G3	VREF
7	IO_L01N_7/VRP_7	B2	DCI
7	IO_L01P_7/VRN_7	B1	DCI
7	IO_L21N_7	C1	I/O
7	IO_L21P_7	D3	I/O
7	IO_L22N_7	D1	I/O
7	IO_L22P_7	D2	I/O
7	IO_L23N_7	E2	I/O
7	IO_L23P_7	E3	I/O
7	IO_L24N_7	F3	I/O
7	IO_L24P_7	E1	I/O
7	IO_L40N_7/VREF_7	G1	VREF
7	IO_L40P_7	F2	I/O
0,1	VCCO_TOP	B12	VCCO
0,1	VCCO_TOP	A4	VCCO
0,1	VCCO_TOP	B8	VCCO
2,3	VCCO_RIGHT	D13	VCCO
2,3	VCCO_RIGHT	H13	VCCO
2,3	VCCO_RIGHT	M12	VCCO
4,5	VCCO_BOTTOM	N7	VCCO
4,5	VCCO_BOTTOM	P11	VCCO
4,5	VCCO_BOTTOM	N3	VCCO
6,7	VCCO_LEFT	G2	VCCO
6,7	VCCO_LEFT	L2	VCCO
6,7	VCCO_LEFT	C3	VCCO
N/A	GND	B4	GND
N/A	GND	B9	GND
N/A	GND	C2	GND
N/A	GND	C12	GND
N/A	GND	D14	GND
N/A	GND	F1	GND
N/A	GND	J14	GND
N/A	GND	L1	GND

Table 91: TQ144 Package Pinout (Cont'd)

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
2	IO_L23N_2/VREF_2	P98	VREF
2	IO_L23P_2	P97	I/O
2	IO_L24N_2	P96	I/O
2	IO_L24P_2	P95	I/O
2	IO_L40N_2	P93	I/O
2	IO_L40P_2/VREF_2	P92	VREF
3	IO	P76	I/O
3	IO_L01N_3/VRP_3	P74	DCI
3	IO_L01P_3/VRN_3	P73	DCI
3	IO_L20N_3	P78	I/O
3	IO_L20P_3	P77	I/O
3	IO_L21N_3	P80	I/O
3	IO_L21P_3	P79	I/O
3	IO_L22N_3	P83	I/O
3	IO_L22P_3	P82	I/O
3	IO_L23N_3	P85	I/O
3	IO_L23P_3/VREF_3	P84	VREF
3	IO_L24N_3	P87	I/O
3	IO_L24P_3	P86	I/O
3	IO_L40N_3/VREF_3	P90	VREF
3	IO_L40P_3	P89	I/O
4	IO/VREF_4	P70	VREF
4	IO_L01N_4/VRP_4	P69	DCI
4	IO_L01P_4/VRN_4	P68	DCI
4	IO_L27N_4/DIN/D0	P65	DUAL
4	IO_L27P_4/D1	P63	DUAL
4	IO_L30N_4/D2	P60	DUAL
4	IO_L30P_4/D3	P59	DUAL
4	IO_L31N_4/INIT_B	P58	DUAL
4	IO_L31P_4/DOOUT/BUSY	P57	DUAL
4	IO_L32N_4/GCLK1	P56	GCLK
4	IO_L32P_4/GCLK0	P55	GCLK
5	IO/VREF_5	P44	VREF
5	IO_L01N_5/RDWR_B	P41	DUAL
5	IO_L01P_5/CS_B	P40	DUAL
5	IO_L28N_5/D6	P47	DUAL
5	IO_L28P_5/D7	P46	DUAL
5	IO_L31N_5/D4	P51	DUAL
5	IO_L31P_5/D5	P50	DUAL
5	IO_L32N_5/GCLK3	P53	GCLK



Right Half of Package
(Top View)

Figure 48: PQ208 Package Footprint (Top View) Continued

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Table 96: FT256 Package Pinout (Cont'd)

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
2	VCCO_2	G11	VCCO
2	VCCO_2	H11	VCCO
2	VCCO_2	H12	VCCO
3	IO	K15	I/O
3	IO_L01N_3/VRP_3	P16	DCI
3	IO_L01P_3/VRN_3	R16	DCI
3	IO_L16N_3	P15	I/O
3	IO_L16P_3	P14	I/O
3	IO_L17N_3	N16	I/O
3	IO_L17P_3/VREF_3	N15	VREF
3	IO_L19N_3	M14	I/O
3	IO_L19P_3	N14	I/O
3	IO_L20N_3	M16	I/O
3	IO_L20P_3	M15	I/O
3	IO_L21N_3	L13	I/O
3	IO_L21P_3	M13	I/O
3	IO_L22N_3	L15	I/O
3	IO_L22P_3	L14	I/O
3	IO_L23N_3	K12	I/O
3	IO_L23P_3/VREF_3	L12	VREF
3	IO_L24N_3	K14	I/O
3	IO_L24P_3	K13	I/O
3	IO_L39N_3	J14	I/O
3	IO_L39P_3	J13	I/O
3	IO_L40N_3/VREF_3	J16	VREF
3	IO_L40P_3	K16	I/O
3	VCCO_3	J11	VCCO
3	VCCO_3	J12	VCCO
3	VCCO_3	K11	VCCO
4	IO	T12	I/O
4	IO	T14	I/O
4	IO/VREF_4	N12	VREF
4	IO/VREF_4	P13	VREF
4	IO/VREF_4	T10	VREF
4	IO_L01N_4/VRP_4	R13	DCI
4	IO_L01P_4/VRN_4	T13	DCI
4	IO_L25N_4	P12	I/O
4	IO_L25P_4	R12	I/O
4	IO_L27N_4/DIN/D0	M11	DUAL
4	IO_L27P_4/D1	N11	DUAL

Table 96: FT256 Package Pinout (Cont'd)

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
7	IO_L24P_7	G4	I/O
7	IO_L39N_7	H3	I/O
7	IO_L39P_7	H4	I/O
7	IO_L40N_7/VREF_7	H1	VREF
7	IO_L40P_7	G1	I/O
7	VCCO_7	G6	VCCO
7	VCCO_7	H5	VCCO
7	VCCO_7	H6	VCCO
N/A	GND	A1	GND
N/A	GND	A16	GND
N/A	GND	B2	GND
N/A	GND	B9	GND
N/A	GND	B15	GND
N/A	GND	F6	GND
N/A	GND	F11	GND
N/A	GND	G7	GND
N/A	GND	G8	GND
N/A	GND	G9	GND
N/A	GND	G10	GND
N/A	GND	H2	GND
N/A	GND	H7	GND
N/A	GND	H8	GND
N/A	GND	H9	GND
N/A	GND	H10	GND
N/A	GND	J7	GND
N/A	GND	J8	GND
N/A	GND	J9	GND
N/A	GND	J10	GND
N/A	GND	J15	GND
N/A	GND	K7	GND
N/A	GND	K8	GND
N/A	GND	K9	GND
N/A	GND	K10	GND
N/A	GND	L6	GND
N/A	GND	L11	GND
N/A	GND	R2	GND
N/A	GND	R8	GND
N/A	GND	R15	GND
N/A	GND	T1	GND

Table 98: FG320 Package Pinout (Cont'd)

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
3	IO_L24N_3	M18	I/O
3	IO_L24P_3	N17	I/O
3	IO_L27N_3	L14	I/O
3	IO_L27P_3	L13	I/O
3	IO_L34N_3	L15	I/O
3	IO_L34P_3/VREF_3	L16	VREF
3	IO_L35N_3	L18	I/O
3	IO_L35P_3	L17	I/O
3	IO_L39N_3	K13	I/O
3	IO_L39P_3	K14	I/O
3	IO_L40N_3/VREF_3	K17	VREF
3	IO_L40P_3	K18	I/O
3	VCCO_3	K12	VCCO
3	VCCO_3	L12	VCCO
3	VCCO_3	N16	VCCO
4	IO	P12	I/O
4	IO	V14	I/O
4	IO/VREF_4	R10	VREF
4	IO/VREF_4	U13	VREF
4	IO/VREF_4	V17	VREF
4	IO_L01N_4/VRP_4	U16	DCI
4	IO_L01P_4/VRN_4	V16	DCI
4	IO_L06N_4/VREF_4	P14	VREF
4	IO_L06P_4	R14	I/O
4	IO_L09N_4	U15	I/O
4	IO_L09P_4	V15	I/O
4	IO_L10N_4	T14	I/O
4	IO_L10P_4	U14	I/O
4	IO_L25N_4	R13	I/O
4	IO_L25P_4	P13	I/O
4	IO_L27N_4/DIN/D0	T12	DUAL
4	IO_L27P_4/D1	R12	DUAL
4	IO_L28N_4	V12	I/O
4	IO_L28P_4	V11	I/O
4	IO_L29N_4	R11	I/O
4	IO_L29P_4	T11	I/O
4	IO_L30N_4/D2	N11	DUAL
4	IO_L30P_4/D3	P11	DUAL
4	IO_L31N_4/INIT_B	U10	DUAL

Table 103: FG676 Package Pinout (Cont'd)

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
6	IO_L20N_6	IO_L20N_6	IO_L20N_6	IO_L20N_6	IO_L20N_6	V7	I/O
6	IO_L20P_6	IO_L20P_6	IO_L20P_6	IO_L20P_6	IO_L20P_6	U7	I/O
6	IO_L21N_6	IO_L21N_6	IO_L21N_6	IO_L21N_6	IO_L21N_6	V5	I/O
6	IO_L21P_6	IO_L21P_6	IO_L21P_6	IO_L21P_6	IO_L21P_6	V4	I/O
6	IO_L22N_6	IO_L22N_6	IO_L22N_6	IO_L22N_6	IO_L22N_6	V3	I/O
6	IO_L22P_6	IO_L22P_6	IO_L22P_6	IO_L22P_6	IO_L22P_6	V2	I/O
6	IO_L23N_6	IO_L23N_6	IO_L23N_6	IO_L23N_6	IO_L23N_6	U6	I/O
6	IO_L23P_6	IO_L23P_6	IO_L23P_6	IO_L23P_6	IO_L23P_6	U5	I/O
6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	IO_L24N_6/VREF_6	U4	VREF
6	IO_L24P_6	IO_L24P_6	IO_L24P_6	IO_L24P_6	IO_L24P_6	U3	I/O
6	IO_L26N_6	IO_L26N_6	IO_L26N_6	IO_L26N_6	IO_L26N_6	U2	I/O
6	IO_L26P_6	IO_L26P_6	IO_L26P_6	IO_L26P_6	IO_L26P_6	U1	I/O
6	IO_L27N_6	IO_L27N_6	IO_L27N_6	IO_L27N_6	IO_L27N_6	T8	I/O
6	IO_L27P_6	IO_L27P_6	IO_L27P_6	IO_L27P_6	IO_L27P_6	T7	I/O
6	IO_L28N_6	IO_L28N_6	IO_L28N_6	IO_L28N_6	IO_L28N_6	T6	I/O
6	IO_L28P_6	IO_L28P_6	IO_L28P_6	IO_L28P_6	IO_L28P_6	T5	I/O
6	IO_L29N_6	IO_L29N_6	IO_L29N_6	IO_L29N_6	IO_L29N_6	T2	I/O
6	IO_L29P_6	IO_L29P_6	IO_L29P_6	IO_L29P_6	IO_L29P_6	T1	I/O
6	IO_L31N_6	IO_L31N_6	IO_L31N_6	IO_L31N_6	IO_L31N_6	R8	I/O
6	IO_L31P_6	IO_L31P_6	IO_L31P_6	IO_L31P_6	IO_L31P_6	R7	I/O
6	IO_L32N_6	IO_L32N_6	IO_L32N_6	IO_L32N_6	IO_L32N_6	R6	I/O
6	IO_L32P_6	IO_L32P_6	IO_L32P_6	IO_L32P_6	IO_L32P_6	R5	I/O
6	IO_L33N_6	IO_L33N_6	IO_L33N_6	IO_L33N_6	IO_L33N_6	T4	I/O
6	IO_L33P_6	IO_L33P_6	IO_L33P_6	IO_L33P_6	IO_L33P_6	R3	I/O
6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	IO_L34N_6/VREF_6	R2	VREF
6	IO_L34P_6	IO_L34P_6	IO_L34P_6	IO_L34P_6	IO_L34P_6	R1	I/O
6	IO_L35N_6	IO_L35N_6	IO_L35N_6	IO_L35N_6	IO_L35N_6	P8	I/O
6	IO_L35P_6	IO_L35P_6	IO_L35P_6	IO_L35P_6	IO_L35P_6	P7	I/O
6	IO_L38N_6	IO_L38N_6	IO_L38N_6	IO_L38N_6	IO_L38N_6	P6	I/O
6	IO_L38P_6	IO_L38P_6	IO_L38P_6	IO_L38P_6	IO_L38P_6	P5	I/O
6	IO_L39N_6	IO_L39N_6	IO_L39N_6	IO_L39N_6	IO_L39N_6	P4	I/O
6	IO_L39P_6	IO_L39P_6	IO_L39P_6	IO_L39P_6	IO_L39P_6	P3	I/O
6	IO_L40N_6	IO_L40N_6	IO_L40N_6	IO_L40N_6	IO_L40N_6	P2	I/O
6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	IO_L40P_6/VREF_6	P1	VREF
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	P9	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	P10	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	R9	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	T3	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	T9	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	U8	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	V8	VCCO
6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	VCCO_6	Y3	VCCO
7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	IO_L01N_7/VRP_7	F5	DCI

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
0	IO_L10N_0	IO_L10N_0	J9	I/O
0	IO_L10P_0	IO_L10P_0	H9	I/O
0	IO_L11N_0	IO_L11N_0	G10	I/O
0	IO_L11P_0	IO_L11P_0	F10	I/O
0	IO_L12N_0	IO_L12N_0	C10	I/O
0	IO_L12P_0	IO_L12P_0	B10	I/O
0	IO_L13N_0	IO_L13N_0	J10	I/O
0	IO_L13P_0	IO_L13P_0	K11	I/O
0	IO_L14N_0	IO_L14N_0	H11	I/O
0	IO_L14P_0	IO_L14P_0	G11	I/O
0	IO_L15N_0	IO_L15N_0	F11	I/O
0	IO_L15P_0	IO_L15P_0	E11	I/O
0	IO_L16N_0	IO_L16N_0	D11	I/O
0	IO_L16P_0	IO_L16P_0	C11	I/O
0	IO_L17N_0	IO_L17N_0	B11	I/O
0	IO_L17P_0	IO_L17P_0	A11	I/O
0	IO_L18N_0	IO_L18N_0	K12	I/O
0	IO_L18P_0	IO_L18P_0	J12	I/O
0	IO_L19N_0	IO_L19N_0	H12	I/O
0	IO_L19P_0	IO_L19P_0	G12	I/O
0	IO_L20N_0	IO_L20N_0	F12	I/O
0	IO_L20P_0	IO_L20P_0	E12	I/O
0	IO_L21N_0	IO_L21N_0	D12	I/O
0	IO_L21P_0	IO_L21P_0	C12	I/O
0	IO_L22N_0	IO_L22N_0	B12	I/O
0	IO_L22P_0	IO_L22P_0	A12	I/O
0	IO_L23N_0	IO_L23N_0	J13	I/O
0	IO_L23P_0	IO_L23P_0	H13	I/O
0	IO_L24N_0	IO_L24N_0	F13	I/O
0	IO_L24P_0	IO_L24P_0	E13	I/O
0	IO_L25N_0	IO_L25N_0	B13	I/O
0	IO_L25P_0	IO_L25P_0	A13	I/O
0	IO_L26N_0	IO_L26N_0	K14	I/O
0	IO_L26P_0/VREF_0	IO_L26P_0/VREF_0	J14	VREF
0	IO_L27N_0	IO_L27N_0	G14	I/O
0	IO_L27P_0	IO_L27P_0	F14	I/O
0	IO_L28N_0	IO_L28N_0	C14	I/O
0	IO_L28P_0	IO_L28P_0	B14	I/O
0	IO_L29N_0	IO_L29N_0	J15	I/O
0	IO_L29P_0	IO_L29P_0	H15	I/O

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	IO_L28N_2	IO_L28N_2	M26	I/O
2	IO_L28P_2	IO_L28P_2	N25	I/O
2	IO_L29N_2	IO_L29N_2	N26	I/O
2	IO_L29P_2	IO_L29P_2	N27	I/O
2	IO_L31N_2	IO_L31N_2	N29	I/O
2	IO_L31P_2	IO_L31P_2	N30	I/O
2	IO_L32N_2	IO_L32N_2	P21	I/O
2	IO_L32P_2	IO_L32P_2	P22	I/O
2	IO_L33N_2	IO_L33N_2	P24	I/O
2	IO_L33P_2	IO_L33P_2	P25	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	P28	VREF
2	IO_L34P_2	IO_L34P_2	P29	I/O
2	IO_L35N_2	IO_L35N_2	R21	I/O
2	IO_L35P_2	IO_L35P_2	R22	I/O
2	IO_L37N_2	IO_L37N_2	R23	I/O
2	IO_L37P_2	IO_L37P_2	R24	I/O
2	IO_L38N_2	IO_L38N_2	R25	I/O
2	IO_L38P_2	IO_L38P_2	R26	I/O
2	IO_L39N_2	IO_L39N_2	R27	I/O
2	IO_L39P_2	IO_L39P_2	R28	I/O
2	IO_L40N_2	IO_L40N_2	R29	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	R30	VREF
2	N.C. (◆)	IO_L41N_2	E27	I/O
2	N.C. (◆)	IO_L41P_2	F26	I/O
2	N.C. (◆)	IO_L45N_2	K28	I/O
2	N.C. (◆)	IO_L45P_2	K29	I/O
2	N.C. (◆)	IO_L46N_2	K21	I/O
2	N.C. (◆)	IO_L46P_2	L21	I/O
2	N.C. (◆)	IO_L47N_2	L23	I/O
2	N.C. (◆)	IO_L47P_2	L24	I/O
2	N.C. (◆)	IO_L50N_2	M29	I/O
2	N.C. (◆)	IO_L50P_2	M30	I/O
2	VCCO_2	VCCO_2	M20	VCCO
2	VCCO_2	VCCO_2	N20	VCCO
2	VCCO_2	VCCO_2	P20	VCCO
2	VCCO_2	VCCO_2	L22	VCCO
2	VCCO_2	VCCO_2	J24	VCCO
2	VCCO_2	VCCO_2	N24	VCCO
2	VCCO_2	VCCO_2	G26	VCCO
2	VCCO_2	VCCO_2	E28	VCCO

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
7	IO_L23N_7	IO_L23N_7	L3	I/O
7	IO_L23P_7	IO_L23P_7	L4	I/O
7	IO_L24N_7	IO_L24N_7	L1	I/O
7	IO_L24P_7	IO_L24P_7	L2	I/O
7	N.C. (◆)	IO_L25N_7	M6	I/O
7	N.C. (◆)	IO_L25P_7	M7	I/O
7	IO_L26N_7	IO_L26N_7	M3	I/O
7	IO_L26P_7	IO_L26P_7	M4	I/O
7	IO_L27N_7	IO_L27N_7	M1	I/O
7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	M2	VREF
7	IO_L28N_7	IO_L28N_7	N10	I/O
7	IO_L28P_7	IO_L28P_7	M10	I/O
7	IO_L29N_7	IO_L29N_7	N8	I/O
7	IO_L29P_7	IO_L29P_7	N9	I/O
7	IO_L31N_7	IO_L31N_7	N1	I/O
7	IO_L31P_7	IO_L31P_7	N2	I/O
7	IO_L32N_7	IO_L32N_7	P9	I/O
7	IO_L32P_7	IO_L32P_7	P10	I/O
7	IO_L33N_7	IO_L33N_7	P6	I/O
7	IO_L33P_7	IO_L33P_7	P7	I/O
7	IO_L34N_7	IO_L34N_7	P2	I/O
7	IO_L34P_7	IO_L34P_7	P3	I/O
7	IO_L35N_7	IO_L35N_7	R9	I/O
7	IO_L35P_7	IO_L35P_7	R10	I/O
7	IO_L37N_7	IO_L37N_7	R7	I/O
7	IO_L37P_7/VREF_7	IO_L37P_7/VREF_7	R8	VREF
7	IO_L38N_7	IO_L38N_7	R5	I/O
7	IO_L38P_7	IO_L38P_7	R6	I/O
7	IO_L39N_7	IO_L39N_7	R3	I/O
7	IO_L39P_7	IO_L39P_7	R4	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	R1	VREF
7	IO_L40P_7	IO_L40P_7	R2	I/O
7	N.C. (◆)	IO_L46N_7	M8	I/O
7	N.C. (◆)	IO_L46P_7	M9	I/O
7	N.C. (◆)	IO_L49N_7	N6	I/O
7	N.C. (◆)	IO_L49P_7	M5	I/O
7	N.C. (◆)	IO_L50N_7	N4	I/O
7	N.C. (◆)	IO_L50P_7	N5	I/O
7	VCCO_7	VCCO_7	E3	VCCO
7	VCCO_7	VCCO_7	J3	VCCO

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	W12	VCCINT
N/A	VCCINT	VCCINT	M13	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	M14	VCCINT
N/A	VCCINT	VCCINT	W14	VCCINT
N/A	VCCINT	VCCINT	L15	VCCINT
N/A	VCCINT	VCCINT	Y15	VCCINT
N/A	VCCINT	VCCINT	L16	VCCINT
N/A	VCCINT	VCCINT	Y16	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	W17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	W18	VCCINT
N/A	VCCINT	VCCINT	M19	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	P19	VCCINT
N/A	VCCINT	VCCINT	U19	VCCINT
N/A	VCCINT	VCCINT	V19	VCCINT
N/A	VCCINT	VCCINT	W19	VCCINT
N/A	VCCINT	VCCINT	L20	VCCINT
N/A	VCCINT	VCCINT	R20	VCCINT
N/A	VCCINT	VCCINT	T20	VCCINT
N/A	VCCINT	VCCINT	Y20	VCCINT
VCCAUX	CCLK	CCLK	AH28	CONFIG
VCCAUX	DONE	DONE	AJ28	CONFIG
VCCAUX	HSWAP_EN	HSWAP_EN	A3	CONFIG
VCCAUX	M0	M0	AJ3	CONFIG
VCCAUX	M1	M1	AH3	CONFIG
VCCAUX	M2	M2	AK3	CONFIG
VCCAUX	PROG_B	PROG_B	B3	CONFIG
VCCAUX	TCK	TCK	B28	JTAG
VCCAUX	TDI	TDI	C3	JTAG
VCCAUX	TDO	TDO	C28	JTAG
VCCAUX	TMS	TMS	A28	JTAG