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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	294912
Number of I/O	141
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s400-4pqg208i

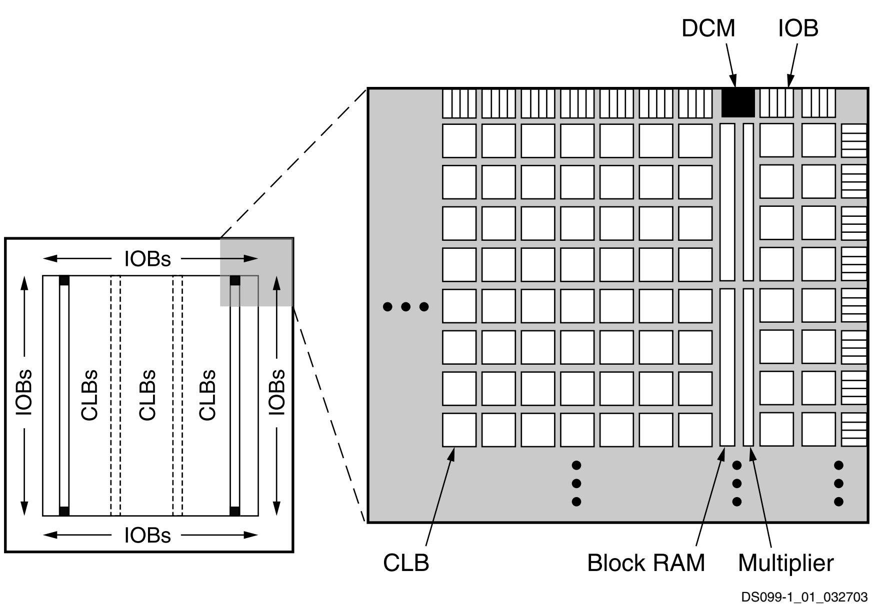
Architectural Overview

The Spartan-3 family architecture consists of five fundamental programmable functional elements:

- Configurable Logic Blocks (CLBs) contain RAM-based Look-Up Tables (LUTs) to implement logic and storage elements that can be used as flip-flops or latches. CLBs can be programmed to perform a wide variety of logical functions as well as to store data.
- Input/Output Blocks (IOBs) control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Twenty-six different signal standards, including eight high-performance differential standards, are available as shown in Table 2. Double Data-Rate (DDR) registers are included. The Digitally Controlled Impedance (DCI) feature provides automatic on-chip terminations, simplifying board designs.
- Block RAM provides data storage in the form of 18-Kbit dual-port blocks.
- Multiplier blocks accept two 18-bit binary numbers as inputs and calculate the product.
- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. The XC3S50 has a single column of block RAM embedded in the array. Those devices ranging from the XC3S200 to the XC3S2000 have two columns of block RAM. The XC3S4000 and XC3S5000 devices have four RAM columns. Each column is made up of several 18-Kbit RAM blocks; each block is associated with a dedicated multiplier. The DCMs are positioned at the ends of the outer block RAM columns.

The Spartan-3 family features a rich network of traces and switches that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The two additional block RAM columns of the XC3S4000 and XC3S5000 devices are shown with dashed lines. The XC3S50 has only the block RAM column on the far left.

Figure 1: **Spartan-3 Family Architecture**

Configuration

Spartan-3 FPGAs are programmed by loading configuration data into robust reprogrammable static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. Before powering on the FPGA, configuration data is stored externally in a PROM or some other nonvolatile medium either on or off the board. After applying

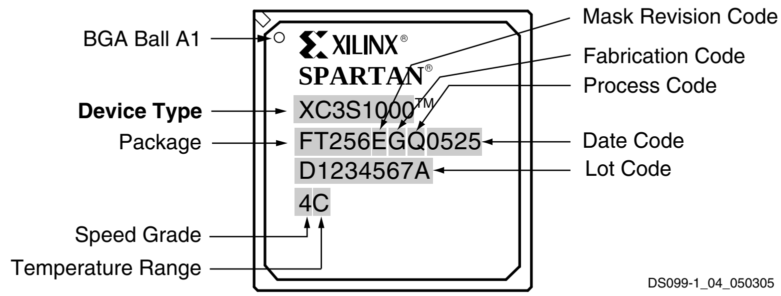


Figure 3: **Spartan-3 FPGA BGA Package Marking Example for Part Number XC3S1000-4FT256C**

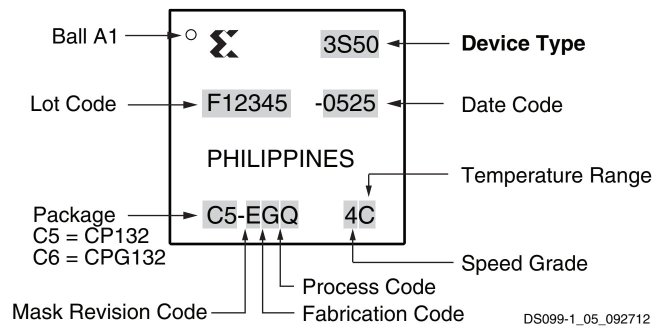


Figure 4: **Spartan-3 FPGA CP132 and CPG132 Package Marking Example for XC3S50-4CP132C**

Ordering Information

Spartan-3 FPGAs are available in both standard (Figure 5) and Pb-free (Figure 6) packaging options for all device/package combinations. The Pb-free packages include a special 'G' character in the ordering code.

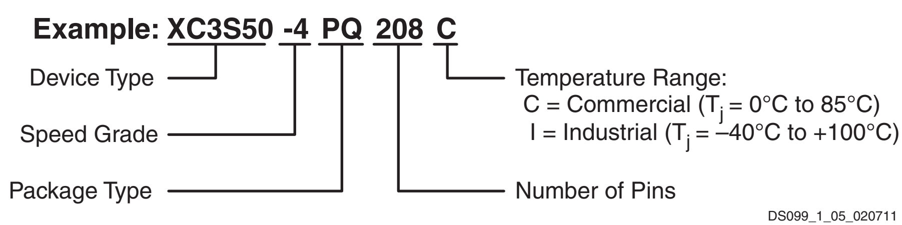


Figure 5: **Standard Packaging**

For additional information on Pb-free packaging, see XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

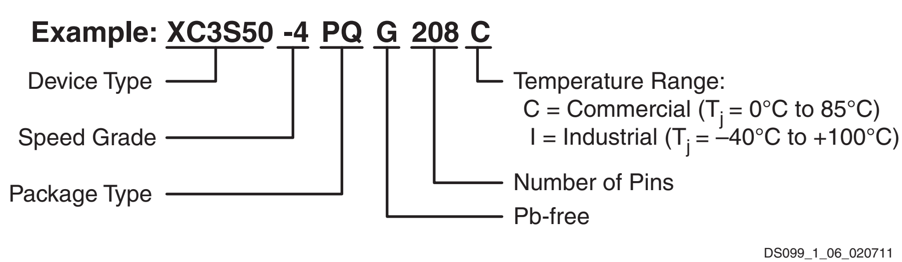


Figure 6: **Pb-Free Packaging**

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Table 10: **DCI I/O Standards**

Category of Signal Standard	Signal Standard (IOSTANDARD)	V_{CCO} (V)		V_{REF} for Inputs (V)	Termination Type	
		For Outputs	For Inputs		At Output	At Input
Single-Ended						
Gunning Transceiver Logic	GTL_DCI	1.2	1.2	0.8	Single	Single
	GTLP_DCI	1.5	1.5	1.0		
High-Speed Transceiver Logic	HSTL_I_DCI	1.5	1.5	0.75	None	Split
	HSTL_III_DCI	1.5	1.5	0.9	None	Single
	HSTL_I_DCI_18	1.8	1.8	0.9	None	Split
	HSTL_II_DCI_18 DIFF_HSTL_II_18_DCI	1.8	1.8	0.9	Split	
	HSTL_III_DCI_18	1.8	1.8	1.1	None	Single
Low-Voltage CMOS	LVDCI_15	1.5	1.5	–	Controlled impedance driver	None
	LVDCI_18	1.8	1.8	–		
	LVDCI_25	2.5	2.5	–		
	LVDCI_33[(2)]	3.3	3.3	–		
	LVDCI_DV2_15	1.5	1.5	–	Controlled driver with half-impedance	
	LVDCI_DV2_18	1.8	1.8	–		
	LVDCI_DV2_25	2.5	2.5	–		
	LVDCI_DV2_33	3.3	3.3	–		
Hybrid HSTL Input and LVCMOS Output	HSLVDCI_15	1.5	1.5	0.75	Controlled impedance driver	None
	HSLVDCI_18	1.8	1.8	0.9		
	HSLVDCI_25	2.5	2.5	1.25		
	HSLVDCI_33	3.3	3.3	1.65		
Stub Series Terminated Logic[(3)]	SSTL18_I_DCI	1.8	1.8	0.9	25Ω driver	Split
	SSTL2_I_DCI	2.5	2.5	1.25	25Ω driver	
	SSTL2_II_DCI DIFF_SSTL2_II_DCI	2.5	2.5	1.25	Split with 25Ω driver	
Differential						
Low-Voltage Differential Signaling	LVDS_25_DCI	N/A	2.5	–	None	Split on each line of pair
	LVDSEXT_25_DCI	N/A	2.5	–		

Notes:

1. DCI signal standards are not supported in Bank 5 of any Spartan-3 FPGA packaged in a VQ100, CP132, or TQ144 package.
2. Equivalent to LVTTL DCI.
3. The SSTL18_II signal standard does not have a DCI equivalent.

Supply Voltages for the IOBs

Three different supplies power the IOBs:

- The V_{CCO} supplies, one for each of the FPGA's I/O banks, power the output drivers, except when using the GTL and GTLP signal standards. The voltage on the V_{CCO} pins determines the voltage swing of the output signal.
- V_{CCINT} is the main power supply for the FPGA's internal logic.
- The V_{CCAUX} is an auxiliary source of power, primarily to optimize the performance of various FPGA functions such as I/O switching.

The I/Os During Power-On, Configuration, and User Mode

With no power applied to the FPGA, all I/Os are in a high-impedance state. The V_{CCINT} (1.2V), V_{CCAUX} (2.5V), and V_{CCO} supplies may be applied in any order. Before power-on can finish, V_{CCINT}, V_{CCO} Bank 4, and V_{CCAUX} must have reached their respective minimum recommended operating levels (see Table 29, page 59). At this time, all I/O drivers also will be in a high-impedance state. V_{CCO} Bank 4, V_{CCINT}, and V_{CCAUX} serve as inputs to the internal Power-On Reset circuit (POR).

A Low level applied to the HSWAP_EN input enables pull-up resistors on User I/Os from power-on throughout configuration. A High level on HSWAP_EN disables the pull-up resistors, allowing the I/Os to float. If the HSWAP_EN pin is floating, then an internal pull-up resistor pulls HSWAP_EN High. As soon as power is applied, the FPGA begins initializing its configuration memory. At the same time, the FPGA internally asserts the Global Set-Reset (GSR), which asynchronously resets all IOB storage elements to a Low state.

Upon the completion of initialization, INIT_B goes High, sampling the M0, M1, and M2 inputs to determine the configuration mode. At this point, the configuration data is loaded into the FPGA. The I/O drivers remain in a high-impedance state (with or without pull-up resistors, as determined by the HSWAP_EN input) throughout configuration.

The Global Three State (GTS) net is released during Start-Up, marking the end of configuration and the beginning of design operation in the User mode. At this point, those I/Os to which signals have been assigned go active while all unused I/Os remain in a high-impedance state. The release of the GSR net, also part of Start-up, leaves the IOB registers in a Low state by default, unless the loaded design reverses the polarity of their respective RS inputs.

In User mode, all internal pull-up resistors on the I/Os are disabled and HSWAP_EN becomes a "don't care" input. If it is desirable to have pull-up or pull-down resistors on I/Os carrying signals, the appropriate symbol—e.g., PULLUP, PULLDOWN—must be placed at the appropriate pads in the design. The Bitstream Generator (Bitgen) option UnusedPin available in the Xilinx development software determines whether unused I/Os collectively have pull-up resistors, pull-down resistors, or no resistors in User mode.

CLB Overview

For more details on the CLBs, refer to the chapter entitled "Using Configurable Logic Blocks" in UG331.

The Configurable Logic Blocks (CLBs) constitute the main logic resource for implementing synchronous as well as combinatorial circuits. Each CLB comprises four interconnected slices, as shown in Figure 11. These slices are grouped in pairs. Each pair is organized as a column with an independent carry chain.

The nomenclature that the FPGA Editor—part of the Xilinx development software—uses to designate slices is as follows: The letter 'X' followed by a number identifies columns of slices. The 'X' number counts up in sequence from the left side of the die to the right. The letter 'Y' followed by a number identifies the position of each slice in a pair as well as indicating the CLB row. The 'Y' number counts slices starting from the bottom of the die according to the sequence: 0, 1, 0, 1 (the first CLB row); 2, 3, 2, 3 (the second CLB row); etc. Figure 11 shows the CLB located in the lower left-hand corner of the die. Slices X0Y0 and X0Y1 make up the column-pair on the left where as slices X1Y0 and X1Y1 make up the column-pair on the right. For each CLB, the term "left-hand" (or SLICEM) indicates the pair of slices labeled with an even 'X' number, such as X0, and the term "right-hand" (or SLICEL) designates the pair of slices with an odd 'X' number, e.g., X1.

Table 34: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical[1]	Commercial Maximum[1]	Industrial Maximum[1]	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50	5	24	31	mA
		XC3S200	10	54	80	mA
		XC3S400	15	110	157	mA
		XC3S1000	35	160	262	mA
		XC3S1500	45	260	332	mA
		XC3S2000	60	360	470	mA
		XC3S4000	100	450	810	mA
		XC3S5000	120	600	870	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50	1.5	2.0	2.5	mA
		XC3S200	1.5	3.0	3.5	mA
		XC3S400	1.5	3.0	3.5	mA
		XC3S1000	2.0	4.0	5.0	mA
		XC3S1500	2.5	4.0	5.0	mA
		XC3S2000	3.0	5.0	6.0	mA
		XC3S4000	3.5	5.0	6.0	mA
		XC3S5000	3.5	5.0	6.0	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50	7	20	22	mA
		XC3S200	10	30	33	mA
		XC3S400	15	40	44	mA
		XC3S1000	20	50	55	mA
		XC3S1500	35	75	85	mA
		XC3S2000	45	90	100	mA
		XC3S4000	55	110	125	mA
		XC3S5000	70	130	145	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using devices with typical processing at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). Maximum values are the production test limits measured for each device at the maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.465V, and V_{CCAUX} = 2.625V. The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements, the use of DCI standards, etc.), measured quiescent current levels may be different than the values in the table. Use the XPower Estimator or XPower Analyzer for more accurate estimates. See Note 2.
2. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3 XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer, part of the Xilinx ISE development software, uses the FPGA netlist as input to provide more accurate maximum and typical estimates.
3. The maximum numbers in this table also indicate the minimum current each power rail requires in order for the FPGA to power-on successfully, once all three rails are supplied. If V_{CCINT} is applied before V_{CCAUX}, there may be temporary additional I_{CCINT} current until V_{CCAUX} is applied. See Surplus I_{CCINT} if V_{CCINT} Applied before V_{CCAUX}, page 54

Table 36: **DC Characteristics of User I/Os Using Single-Ended Standards**

Signal Standard (IOSTANDARD) and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
GTL		32	–	0.4	–
GTL_DCI		Note 3	Note 3		
GTLP		36	–	0.6	–
GTLP_DCI		Note 3	Note 3		
HSLVDCI_15		Note 3	Note 3	0.4	V_{CCO} – 0.4
HSLVDCI_18					
HSLVDCI_25					
HSLVDCI_33					
HSTL_I		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI		Note 3	Note 3		
HSTL_III		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI		Note 3	Note 3		
HSTL_I_18		8	–8	0.4	V_{CCO} – 0.4
HSTL_I_DCI_18		Note 3	Note 3		
HSTL_II_18		16	–16	0.4	V_{CCO} – 0.4
HSTL_II_DCI_18		Note 3	Note 3		
HSTL_III_18		24	–8	0.4	V_{CCO} – 0.4
HSTL_III_DCI_18		Note 3	Note 3		
LVCMOS12(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
LVCMOS15(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
LVDCI_15, LVDCI_DV2_15		Note 3	Note 3		
LVCMOS18(4)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
LVDCI_18, LVDCI_DV2_18		Note 3	Note 3		
LVCMOS25(4,5)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_25, LVDCI_DV2_25		Note 3	Note 3		

Table 48: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
HSTL_III_DCI_18							
LVCMOS12		-	0	1.2	1M	0	0.6
LVCMOS15		-	0	1.5	1M	0	0.75
LVDCI_15							
LVDCI_DV2_15							
HSLVDCI_15							
LVCMOS18		-	0	1.8	1M	0	0.9
LVDCI_18							
LVDCI_DV2_18							
HSLVDCI_18							
LVCMOS25		-	0	2.5	1M	0	1.25
LVDCI_25							
LVDCI_DV2_25							
HSLVDCI_25							
LVCMOS33		-	0	3.3	1M	0	1.65
LVDCI_33							
LVDCI_DV2_33							
HSLVDCI_33							
LVTTL		-	0	3.3	1M	0	1.4
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_I_DCI							
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_I_DCI							
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL2_II_DCI					50	1.25	
Differential							
LDT_25 (ULVDS_25)		-	V_{ICM} – 0.125	V_{ICM} + 0.125	60	0.6	V_{ICM}
LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_25_DCI					N/A	N/A	
BLVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
LVDSEXT_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDSEXT_25_DCI					N/A	N/A	
LVPECL_25		-	V_{ICM} – 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25		-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
DIFF_HSTL_II_18		-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.8	V_{ICM}
DIFF_HSTL_II_18_DCI							

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package				
			VQ100	TQ144	PQ208	CP132	FT256, FG320, FG456, FG676, FG900, FG1156
LVCMOS33	Slow	2	34	24	24	52	76
		4	17	14	14	26	46
		6	17	11	11	26	27
		8	10	10	10	13	20
		12	9	9	9	13	13
		16	8	8	8	8	10
		24	8	8	8	8	9
	Fast	2	20	20	20	26	44
		4	15	15	15	15	26
		6	11	11	11	13	16
		8	10	10	10	10	12
		12	8	8	8	8	10
		16	8	8	8	8	8
		24	7	7	7	7	7
LVDCI_33			10	10	10	10	10
LVDCI_DV2_33			10	10	10	10	10
HSLVDCI_33			10	10	10	10	10
LVTTL	Slow	2	34	25	25	52	60
		4	17	16	16	26	41
		6	17	15	15	26	29
		8	12	12	12	13	22
		12	10	10	10	13	13
		16	10	10	10	10	11
		24	8	8	8	8	9
	Fast	2	20	20	20	26	34
		4	13	13	13	13	20
		6	11	11	11	13	15
		8	10	10	10	10	12
		12	9	9	9	9	10
		16	8	8	8	8	9
		24	7	7	7	7	7

Table 50: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)	Package				
	VQ100	TQ144	PQ208	CP132	FT256, FG320, FG456, FG676, FG900, FG1156
PCI33_3	9	9	9	9	9
SSTL18_I	13	13	13	13	17
SSTL18_I_DCI	13	13	13	13	17
SSTL18_II	8	8	8	8	9
SSTL2_I	10	10	10	10	13
SSTL2_I_DCI	10	10	10	10	13
SSTL2_II	6	6	6	6	9
SSTL2_II_DCI	6	6	6	6	9
Differential Standards (Number of I/O Pairs or Channels)					
LDT_25 (ULVDS_25)	5	5	5	5	5
LVDS_25	7	5	5	12	20
BLVDS_25	2	1	1		4
LVDSEXT_25	5	5	5	5	5
LVPECL_25	2	1	1		4
RSDS_25	7	5	5	12	20
DIFF_HSTL_II_18	4	4	4	4	4
DIFF_HSTL_II_18_DCI	4	4	4	4	4
DIFF_SSTL2_II	3	3	3	3	4
DIFF_SSTL2_II_DCI	3	3	3	3	4

Notes:

1. The numbers in this table are recommendations that assume the FPGA is soldered on a printed circuit board using sound practices. This table assumes the following parasitic factors: combined PCB trace and land inductance per V_{CCO} and GND pin of 1.0 nH, receiver capacitive load of 15 pF. Test limits are the V_{IL}/V_{IH} voltage limits for the respective I/O standard.
2. Regarding the SSO numbers for all DCI standards, the R_{REF} resistors connected to the VRN and VRP pins of the FPGA are 50W..
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: *Managing Ground Bounce in Large FPGAs* for information on how to perform weighted average SSO calculations.
4. Results are based on actual silicon testing using an FPGA soldered on a typical printed-circuit board.

Phase Shifter (PS)

Phase shifter operation is only supported if the DLL is in low-frequency mode, see Table 58. Fixed phase shift requires ISE software version 10.1.03 (or later).

Table 62: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Frequency Mode/ F_{CLKIN} Range		Speed Grade -5 Min	Speed Grade -5 Max	Speed Grade -4 Min	Speed Grade -4 Max	Units
Operating Frequency Ranges								
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	Low		1	167	1	167	MHz
Input Pulse Requirements								
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	Low	$F_{CLKIN} \leq$ 100 MHz	40%	60%	40%	60%	-
			F_{CLKIN} > 100 MHz	45%	55%	45%	55%	-

Table 63: **Switching Characteristics for the PS in Variable or Fixed Phase Shift Mode**

Symbol	Description	Frequency Mode/ F_{CLKIN} Range	Speed Grade -5 Min	Speed Grade -5 Max	Speed Grade -4 Min	Speed Grade -4 Max	Units
Phase Shifting Range							
FINE_SHIFT_RANGE	Phase shift range	Low	–	10.0	–	10.0	ns
Lock Time							
LOCK_DLL_PS	When using the PS in conjunction with the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.	18 MHz $\leq F_{CLKIN} \leq$ 30 MHz	–	3.28	–	3.28	ms
		30 MHz < $F_{CLKIN} \leq$ 40 MHz	–	2.56	–	2.56	ms
		40 MHz < $F_{CLKIN} \leq$ 50 MHz	–	1.60	–	1.60	ms
		50 MHz < $F_{CLKIN} \leq$ 60 MHz	–	1.00	–	1.00	ms
		60 MHz < $F_{CLKIN} \leq$ 165 MHz	–	0.88	–	0.88	ms
LOCK_DLL_PS_FX	When using the PS in conjunction with the DLL and DFS: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.	Low	–	10.40	–	10.40	ms

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32 and Table 62.
2. The PS specifications in this table apply when the PS attribute CLKOUT_PHASE_SHIFT= VARIABLE or FIXED.

CCLK: Configuration Clock

The configuration clock signal on this pin synchronizes the reading or writing of configuration data. The CCLK pin is an input-only pin for the Slave Serial and Slave Parallel configuration modes. In the Master Serial and Master Parallel configuration modes, the FPGA drives the CCLK pin and CCLK should be treated as a full bidirectional I/O pin for signal integrity analysis.

Although the CCLK frequency is relatively low, Spartan-3 FPGA output edge rates are fast. Any potential signal integrity problems on the CCLK board trace can cause FPGA configuration to fail. Therefore, pay careful attention to the CCLK signal integrity on the printed circuit board. Signal integrity simulation with IBIS is recommended. For all configuration modes except JTAG, consider the signal integrity at every CCLK trace destination, including the FPGA's CCLK pin. For more details on CCLK design considerations, see Chapter 2 of UG332, *Spartan-3 Generation Configuration User Guide*.

During configuration, the CCLK pin has a pull-up resistor to VCCAUX, regardless of the HSWAP_EN pin. After configuration, the CCLK pin is pulled High to VCCAUX by default as defined by the ***CclkPin*** bitstream selection, although this behavior is programmable. Any clocks applied to CCLK after configuration are ignored unless the bitstream option ***Persist*** is set to ***Yes***, which retains the configuration interface. ***Persist*** is set to ***No*** by default. However, if ***Persist*** is set to ***Yes***, then all clock edges are potentially active events, depending on the other configuration control signals.

The bitstream generator option ***ConfigRate*** determines the frequency of the internally-generated CCLK oscillator required for the Master configuration modes. The actual frequency is approximate due to the characteristics of the silicon oscillator and varies by up to 50% over the temperature and voltage range. By default, CCLK operates at approximately 6 MHz. Via the ***ConfigRate*** option, the oscillator frequency is set at approximately 3, 6, 12, 25, or 50 MHz. At power-on, CCLK always starts operation at its lowest frequency. The device does not start operating at the higher frequency until the ConfigRate control bits are loaded during the configuration process.

PROG_B: Program/Configure Device

This asynchronous pin initiates the configuration or re-configuration processes. A Low-going pulse resets the configuration logic, initializing the configuration memory. This initialization process cannot finish until PROG_B returns High. Asserting PROG_B Low for an extended period delays the configuration process. At power-up, there is always a pull-up resistor to VCCAUX on this pin, regardless of the HSWAP_EN input. After configuration, the bitstream generator option ***ProgPin*** determines whether or not the pull-up resistor is present. By default, the ***ProgPin*** option retains the pull-up resistor.

After configuration, hold the PROG_B input High. Any Low-going pulse on PROG_B lasting 300 ns or longer restarts the configuration process.

Table 73: **PROG_B Operation**

PROG_B Input	Response
Power-up	Automatically initiates configuration process.
Low-going pulse	Initiate (re-)configuration process and continue to completion.
Extended Low	Initiate (re-)configuration process and stall process at step where configuration memory is cleared. Process is stalled until PROG_B returns High.
1	If the configuration process is started, continue to completion. If configuration process is complete, stay in User mode.

DONE: Configuration Done, Delay Start-Up Sequence

The FPGA produces a Low-to-High transition on this pin indicating that the configuration process is complete. The bitstream generator option ***DriveDone*** determines whether this pin functions as a totem-pole output that can drive High or as an open-drain output. If configured as an open-drain output—which is the default behavior—then a pull-up resistor is required to produce a High logic level. There is a bitstream option that provides an internal pull-up resistor, otherwise an external pull-up resistor is required.

The open-drain option permits the DONE lines of multiple FPGAs to be tied together, so that the common node transitions High only after all of the FPGAs have completed configuration. Externally holding the open-drain DONE pin Low delays the start-up sequence, which marks the transition to user mode.

TQ144: 144-lead Thin Quad Flat Package

The XC3S50, the XC3S200, and the XC3S400 are available in the 144-lead thin quad flat package, TQ144. All devices share a common footprint for this package as shown in Table 91 and Figure 46.

The TQ144 package only has four separate VCCO inputs, unlike the BGA packages, which have eight separate VCCO inputs. The TQ144 package has a separate VCCO input for the top, bottom, left, and right. However, there are still eight separate I/O banks, as shown in Table 91 and Figure 46. Banks 0 and 1 share the VCCO_TOP input, Banks 2 and 3 share the VCCO_RIGHT input, Banks 4 and 5 share the VCCO_BOTTOM input, and Banks 6 and 7 share the VCCO_LEFT input.

All the package pins appear in Table 91 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 91: **TQ144 Package Pinout**

Bank	XC3S50, XC3S200, XC3S400 Pin Name	TQ144 Pin Number	Type
0	IO_L01N_0/VRP_0	P141	DCI
0	IO_L01P_0/VRN_0	P140	DCI
0	IO_L27N_0	P137	I/O
0	IO_L27P_0	P135	I/O
0	IO_L30N_0	P132	I/O
0	IO_L30P_0	P131	I/O
0	IO_L31N_0	P130	I/O
0	IO_L31P_0/VREF_0	P129	VREF
0	IO_L32N_0/GCLK7	P128	GCLK
0	IO_L32P_0/GCLK6	P127	GCLK
1	IO	P116	I/O
1	IO_L01N_1/VRP_1	P113	DCI
1	IO_L01P_1/VRN_1	P112	DCI
1	IO_L28N_1	P119	I/O
1	IO_L28P_1	P118	I/O
1	IO_L31N_1/VREF_1	P123	VREF
1	IO_L31P_1	P122	I/O
1	IO_L32N_1/GCLK5	P125	GCLK
1	IO_L32P_1/GCLK4	P124	GCLK
2	IO_L01N_2/VRP_2	P108	DCI
2	IO_L01P_2/VRN_2	P107	DCI
2	IO_L20N_2	P105	I/O
2	IO_L20P_2	P104	I/O
2	IO_L21N_2	P103	I/O
2	IO_L21P_2	P102	I/O
2	IO_L22N_2	P100	I/O
2	IO_L22P_2	P99	I/O

Table 93: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S50 Pin Name	XC3S200, XC3S400 Pin Names	PQ208 Pin Number	Type
N/A	GND	GND	P14	GND
N/A	GND	GND	P25	GND
N/A	VCCAUX	VCCAUX	P193	VCCAUX
N/A	VCCAUX	VCCAUX	P173	VCCAUX
N/A	VCCAUX	VCCAUX	P142	VCCAUX
N/A	VCCAUX	VCCAUX	P121	VCCAUX
N/A	VCCAUX	VCCAUX	P89	VCCAUX
N/A	VCCAUX	VCCAUX	P69	VCCAUX
N/A	VCCAUX	VCCAUX	P38	VCCAUX
N/A	VCCAUX	VCCAUX	P17	VCCAUX
N/A	VCCINT	VCCINT	P192	VCCINT
N/A	VCCINT	VCCINT	P174	VCCINT
N/A	VCCINT	VCCINT	P88	VCCINT
N/A	VCCINT	VCCINT	P70	VCCINT
VCCAUX	CCLK	CCLK	P104	CONFIG
VCCAUX	DONE	DONE	P103	CONFIG
VCCAUX	HSWAP_EN	HSWAP_EN	P206	CONFIG
VCCAUX	M0	M0	P55	CONFIG
VCCAUX	M1	M1	P54	CONFIG
VCCAUX	M2	M2	P56	CONFIG
VCCAUX	PROG_B	PROG_B	P207	CONFIG
VCCAUX	TCK	TCK	P159	JTAG
VCCAUX	TDI	TDI	P208	JTAG
VCCAUX	TDO	TDO	P158	JTAG
VCCAUX	TMS	TMS	P160	JTAG

User I/Os by Bank

Table 94 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S50 in the PQ208 package. Similarly, Table 95 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S200 and XC3S400 in the PQ208 package.

Table 94: **User I/Os Per Bank for XC3S50 in PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	15	9	0	2	2	2
	1	15	9	0	2	2	2
Right	2	16	13	0	2	2	0
	3	16	12	0	2	2	0
Bottom	4	15	3	6	2	2	2
	5	15	3	6	2	2	2
Left	6	16	12	0	2	2	0
	7	16	12	0	2	2	0

Table 95: **User I/Os Per Bank for XC3S200 and XC3S400 in PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	16	9	0	2	3	2
	1	15	9	0	2	2	2
Right	2	19	14	0	2	3	0
	3	20	15	0	2	3	0
Bottom	4	17	4	6	2	3	2
	5	15	3	6	2	2	2
Left	6	19	14	0	2	3	0
	7	20	15	0	2	3	0

FG320: 320-lead Fine-pitch Ball Grid Array

The 320-lead fine-pitch ball grid array package, FG320, supports three different Spartan-3 devices, including the XC3S400, the XC3S1000, and the XC3S1500. The footprint for all three devices is identical, as shown in Table 98 and Figure 50.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

All the package pins appear in Table 98 and are sorted by bank number, then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at http://www.xilinx.com/support/documentation/data_ sheets/s3_pin.zip.

Pinout Table

Table 98: **FG320 Package Pinout**

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
0	IO	D9	I/O
0	IO	E7	I/O
0	IO/VREF_0	B3	VREF
0	IO/VREF_0	D6	VREF
0	IO_L01N_0/VRP_0	A2	DCI
0	IO_L01P_0/VRN_0	A3	DCI
0	IO_L09N_0	B4	I/O
0	IO_L09P_0	C4	I/O
0	IO_L10N_0	C5	I/O
0	IO_L10P_0	D5	I/O
0	IO_L15N_0	A4	I/O
0	IO_L15P_0	A5	I/O
0	IO_L25N_0	B5	I/O
0	IO_L25P_0	B6	I/O
0	IO_L27N_0	C7	I/O
0	IO_L27P_0	D7	I/O
0	IO_L28N_0	C8	I/O
0	IO_L28P_0	D8	I/O
0	IO_L29N_0	E8	I/O
0	IO_L29P_0	F8	I/O
0	IO_L30N_0	A7	I/O
0	IO_L30P_0	A8	I/O
0	IO_L31N_0	B9	I/O
0	IO_L31P_0/VREF_0	A9	VREF
0	IO_L32N_0/GCLK7	E9	GCLK
0	IO_L32P_0/GCLK6	F9	GCLK
0	VCCO_0	B8	VCCO
0	VCCO_0	C6	VCCO
0	VCCO_0	G8	VCCO

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
1	IO_L25P_1	IO_L25P_1	D19	I/O
1	IO_L26N_1	IO_L26N_1	A19	I/O
1	IO_L26P_1	IO_L26P_1	B19	I/O
1	IO_L27N_1	IO_L27N_1	F17	I/O
1	IO_L27P_1	IO_L27P_1	G17	I/O
1	IO_L28N_1	IO_L28N_1	B17	I/O
1	IO_L28P_1	IO_L28P_1	C17	I/O
1	IO_L29N_1	IO_L29N_1	J16	I/O
1	IO_L29P_1	IO_L29P_1	K16	I/O
1	IO_L30N_1	IO_L30N_1	G16	I/O
1	IO_L30P_1	IO_L30P_1	H16	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D16	VREF
1	IO_L31P_1	IO_L31P_1	E16	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B16	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C16	GCLK
1	N.C. (◆)	IO_L37N_1	H18	I/O
1	N.C. (◆)	IO_L37P_1	J18	I/O
1	N.C. (◆)	IO_L38N_1	D18	I/O
1	N.C. (◆)	IO_L38P_1	E18	I/O
1	N.C. (◆)	IO_L39N_1	A18	I/O
1	N.C. (◆)	IO_L39P_1	B18	I/O
1	N.C. (◆)	IO_L40N_1	K17	I/O
1	N.C. (◆)	IO_L40P_1	K18	I/O
1	VCCO_1	VCCO_1	L17	VCCO
1	VCCO_1	VCCO_1	C18	VCCO
1	VCCO_1	VCCO_1	G18	VCCO
1	VCCO_1	VCCO_1	L18	VCCO
1	VCCO_1	VCCO_1	L19	VCCO
1	VCCO_1	VCCO_1	J20	VCCO
1	VCCO_1	VCCO_1	C22	VCCO
1	VCCO_1	VCCO_1	G22	VCCO
1	VCCO_1	VCCO_1	E24	VCCO
1	VCCO_1	VCCO_1	C26	VCCO
2	IO	IO	J25	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C29	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C30	DCI
2	IO_L02N_2	IO_L02N_2	D27	I/O
2	IO_L02P_2	IO_L02P_2	D28	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	D29	VREF
2	IO_L03P_2	IO_L03P_2	D30	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
7	IO_L23N_7	IO_L23N_7	L3	I/O
7	IO_L23P_7	IO_L23P_7	L4	I/O
7	IO_L24N_7	IO_L24N_7	L1	I/O
7	IO_L24P_7	IO_L24P_7	L2	I/O
7	N.C. (◆)	IO_L25N_7	M6	I/O
7	N.C. (◆)	IO_L25P_7	M7	I/O
7	IO_L26N_7	IO_L26N_7	M3	I/O
7	IO_L26P_7	IO_L26P_7	M4	I/O
7	IO_L27N_7	IO_L27N_7	M1	I/O
7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	M2	VREF
7	IO_L28N_7	IO_L28N_7	N10	I/O
7	IO_L28P_7	IO_L28P_7	M10	I/O
7	IO_L29N_7	IO_L29N_7	N8	I/O
7	IO_L29P_7	IO_L29P_7	N9	I/O
7	IO_L31N_7	IO_L31N_7	N1	I/O
7	IO_L31P_7	IO_L31P_7	N2	I/O
7	IO_L32N_7	IO_L32N_7	P9	I/O
7	IO_L32P_7	IO_L32P_7	P10	I/O
7	IO_L33N_7	IO_L33N_7	P6	I/O
7	IO_L33P_7	IO_L33P_7	P7	I/O
7	IO_L34N_7	IO_L34N_7	P2	I/O
7	IO_L34P_7	IO_L34P_7	P3	I/O
7	IO_L35N_7	IO_L35N_7	R9	I/O
7	IO_L35P_7	IO_L35P_7	R10	I/O
7	IO_L37N_7	IO_L37N_7	R7	I/O
7	IO_L37P_7/VREF_7	IO_L37P_7/VREF_7	R8	VREF
7	IO_L38N_7	IO_L38N_7	R5	I/O
7	IO_L38P_7	IO_L38P_7	R6	I/O
7	IO_L39N_7	IO_L39N_7	R3	I/O
7	IO_L39P_7	IO_L39P_7	R4	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	R1	VREF
7	IO_L40P_7	IO_L40P_7	R2	I/O
7	N.C. (◆)	IO_L46N_7	M8	I/O
7	N.C. (◆)	IO_L46P_7	M9	I/O
7	N.C. (◆)	IO_L49N_7	N6	I/O
7	N.C. (◆)	IO_L49P_7	M5	I/O
7	N.C. (◆)	IO_L50N_7	N4	I/O
7	N.C. (◆)	IO_L50P_7	N5	I/O
7	VCCO_7	VCCO_7	E3	VCCO
7	VCCO_7	VCCO_7	J3	VCCO

Right Half of FG900 Package (Top View)

Bank 1 (top), Bank 2 (right, rows C–R), Bank 3 (right, rows T–AH), Bank 4 (bottom)

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
A	I/O	GND	I/O L39N_1 ◆	I/O L26N_1	I/O L21N_1	GND	I/O L15N_1	I/O L11N_1	I/O L07N_1	GND	I/O L03N_1	I/O L01N_1 VRP_1	TMS	GND	GND
B	I/O L32N_1 GCLK5	I/O L28N_1	I/O L39P_1 ◆	I/O L26P_1	I/O L21P_1	I/O L17N_1 VREF_1	I/O L15P_1	I/O L11P_1	I/O L07P_1	I/O L04N_1	I/O L03P_1	I/O L01P_1 VRN_1	TCK	GND	GND
C	I/O L32P_1 GCLK4	I/O L28P_1	VCCO_1	I/O L25N_1	I/O L20N_1	I/O L17P_1	VCCO_1	I/O L10N_1 VREF_1	I/O L06N_1 VREF_1	I/O L04P_1	VCCO_1	I/O L02P_1	TDO	I/O L01N_2 VRP_2	I/O L01P_2 VRN_2
D	I/O L31N_1 VREF_1	VCCAUX	I/O L38N_1 ◆	I/O L25P_1	I/O L20P_1	VCCAUX	I/O L14N_1	I/O L10P_1	I/O L06P_1	VCCAUX	I/O L02N_1	I/O L02N_2	I/O L02P_2	I/O L03N_2 VREF_2	I/O L03P_2
E	I/O L31P_1	GND	I/O L38P_1 ◆	I/O L24N_1	I/O L19N_1	GND	I/O L14P_1	I/O L13P_1	VCCO_1	I/O	GND	I/O L41N_2 ◆	VCCO_2	I/O L04N_2	I/O L04P_2
F	I/O	I/O L27N_1	I/O	I/O L24P_1	I/O L19P_1	I/O L16N_1	I/O L13N_1	I/O L09N_1	I/O L05N_1	I/O L05P_1	I/O L41P_2 ◆	VCCAUX	I/O L05N_2	I/O L05P_2	GND
G	I/O L30N_1	I/O L27P_1	VCCO_1	I/O L23N_1	I/O L18N_1	I/O L16P_1	VCCO_1	I/O L09P_1	I/O L08P_1	I/O L08N_2	VCCO_2	I/O L06N_2	I/O L06P_2	I/O L07N_2	I/O L07P_2
H	I/O L30P_1	GND	I/O L37N_1 ◆	I/O L23P_1	I/O L18P_1	GND	I/O L12N_1	I/O L08N_1	I/O L08P_2	I/O L09N_2 VREF_2	I/O L09P_2	I/O L10N_2	I/O L10P_2	I/O L12N_2	I/O L12P_2
J	I/O L29N_1	IO VREF_1	I/O L37P_1 ◆	I/O L22N_1	VCCO_1	I/O	I/O L12P_1	I/O L15N_2	VCCO_2	I/O	I/O L13N_2	I/O L13P_2 VREF_2	VCCO_2	I/O L14N_2	I/O L14P_2
K	I/O L29P_1	I/O L40N_1 ◆	I/O L40P_1 ◆	I/O L22P_1	I/O	I/O L46N_2 ◆	I/O L15P_2	GND	I/O L16N_2	I/O L16P_2	GND	VCCAUX	I/O L45N_2 ◆	I/O L45P_2 ◆	GND
L	VCCINT	VCCO_1	VCCO_1	VCCO_1	VCCINT	I/O L46P_2 ◆	VCCO_2	I/O L47N_2 ◆	I/O L47P_2 ◆	I/O L19N_2	I/O L19P_2	I/O L20N_2	I/O L20P_2	I/O L21N_2	I/O L21P_2
M	GND	VCCINT	VCCINT	VCCINT	VCCO_2	I/O L26N_2	I/O L22N_2	I/O L22P_2	I/O L23N_2 VREF_2	I/O L23P_2	I/O L28N_2	I/O L24N_2	I/O L24P_2	I/O L50N_2 ◆	I/O L50P_2 ◆
N	GND	GND	GND	VCCINT	VCCO_2	I/O L26P_2	I/O L27N_2	I/O L27P_2	VCCO_2	I/O L28P_2	I/O L29N_2	I/O L29P_2	VCCO_2	I/O L31N_2	I/O L31P_2
P	GND	GND	GND	VCCINT	VCCO_2	I/O L32N_2	I/O L32P_2	GND	I/O L33N_2	I/O L33P_2	GND	VCCAUX	I/O L34N_2 VREF_2	I/O L34P_2	GND
R	GND	GND	GND	GND	VCCINT	I/O L35N_2	I/O L35P_2	I/O L37N_2	I/O L37P_2	I/O L38N_2	I/O L38P_2	I/O L39N_2	I/O L39P_2	I/O L40N_2	I/O L40P_2 VREF_2
T	GND	GND	GND	GND	VCCINT	I/O L35P_3	I/O L35N_3	I/O L37P_3	I/O L37N_3	I/O L38P_3	I/O L38N_3	I/O L39P_3	I/O L39N_3	I/O L40P_3	I/O L40N_3 VREF_3
U	GND	GND	GND	VCCINT	VCCO_3	I/O L32P_3	I/O L32N_3	GND	I/O L33P_3	I/O L33N_3	GND	VCCAUX	I/O L34P_3 VREF_3	I/O L34N_3	GND
V	GND	GND	GND	VCCINT	VCCO_3	I/O L27N_3	I/O L28P_3	I/O L28N_3	VCCO_3	I/O L29N_3	I/O L50P_3 ◆	I/O L50N_3 ◆	VCCO_3	I/O L31P_3	I/O L31N_3
W	GND	VCCINT	VCCINT	VCCINT	VCCO_3	I/O L27P_3	I/O L46P_3 ◆	I/O L46N_3 ◆	I/O L47P_3 ◆	I/O L47N_3 ◆	I/O L29P_3	I/O L48P_3 ◆	I/O L48N_3 ◆	I/O L26P_3	I/O L26N_3
Y	VCCINT	VCCO_4	VCCO_4	VCCO_4	VCCINT	I/O L20N_3	VCCO_3	I/O L21P_3	I/O L21N_3	I/O L22P_3	I/O L22N_3	I/O L23P_3 VREF_3	I/O L23N_3	I/O L24P_3	I/O L24N_3
AA	I/O	I/O L26N_4	I/O	I/O L18N_4	I/O L13P_4	I/O L20P_3	I/O L16N_3	GND	I/O L17P_3 VREF_3	I/O L17N_3	GND	VCCAUX	I/O L19P_3	I/O L19N_3	GND
AB	I/O L29N_4	I/O L26P_4 VREF_4	I/O L23N_4	I/O L18P_4	VCCO_4	I/O L13N_4	I/O L08N_4	I/O L16P_3	VCCO_3	I/O	I/O L14P_3	I/O L14N_3	VCCO_3	I/O L15P_3	I/O L15N_3
AC	I/O L29P_4	GND	I/O L23P_4	I/O L19N_4	I/O L14N_4	GND	I/O L08P_4	I/O L04P_4	I/O L09N_3	I/O L10P_3	I/O L10N_3	I/O L11P_3	I/O L11N_3	I/O L13P_3	I/O L13N_3 VREF_3
AD	I/O L30N_4 D2	I/O L27N_4 DIN D0	VCCO_4	I/O L19P_4	I/O L14P_4	I/O L11N_4	VCCO_4	I/O	I/O L04N_4	I/O L09P_3 VREF_3	VCCO_3	I/O L07P_3	I/O L07N_3	I/O L08P_3	I/O L08N_3
AE	I/O L30P_4 D3	I/O L27P_4 D1	I/O L24N_4	I/O L20N_4	I/O L15N_4	I/O L11P_4	I/O	I/O L05N_4	I/O L34P_4 ◆	I/O L34N_4 ◆	I/O L05N_3	VCCAUX	I/O L06P_3	I/O L06N_3	GND
AF	I/O VREF_4	GND	I/O L24P_4	I/O L20P_4	I/O L15P_4	GND	I/O L09N_4	I/O L05P_4	VCCO_4	I/O L03P_4	GND	I/O L05P_3	VCCO_3	I/O L04P_3	I/O L04N_3
AG	I/O L31N_4 INIT_B	VCCAUX	I/O	I/O L21N_4	I/O L16N_4	VCCAUX	I/O L09P_4	I/O L06N_4 VREF_4	I/O L35N_4 ◆	VCCAUX	I/O L03N_4	I/O L02P_3	I/O L02N_3 VREF_3	I/O L03P_3	I/O L03N_3
AH	I/O L31P_4 DOUT BUSY	I/O L28N_4	VCCO_4	I/O L21P_4	I/O L16P_4	I/O L12N_4	VCCO_4	I/O L06P_4	I/O L35P_4 ◆	I/O L33N_4 ◆	VCCO_4	I/O	CCLK	I/O L01P_3 VRN_3	I/O L01N_3 VRP_3
AJ	I/O L32N_4 GCLK1	I/O L28P_4	I/O L25N_4	I/O L22N_4 VREF_4	I/O L17N_4	I/O L12P_4	I/O L10N_4	I/O L07N_4	I/O L38N_4 ◆	I/O L33P_4 ◆	I/O L02N_4	I/O L01N_4 VRP_4	DONE	GND	GND
AK	I/O L32P_4 GCLK0	GND	I/O L25P_4	I/O L22P_4	I/O L17P_4	GND	I/O L10P_4	I/O L07P_4	I/O L38P_4 ◆	GND	I/O L02P_4	I/O L01P_4 VRN_4	IO VREF_4	GND	GND

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Figure 56: FG900 Package Footprint (Top View) Continued

Table 110: **FG1156 Package Pinout** ***(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
4	VCCO_4	VCCO_4	AC19	VCCO
4	VCCO_4	VCCO_4	AC20	VCCO
4	VCCO_4	VCCO_4	AC21	VCCO
4	VCCO_4	VCCO_4	AC22	VCCO
4	VCCO_4	VCCO_4	AG20	VCCO
4	VCCO_4	VCCO_4	AG24	VCCO
4	VCCO_4	VCCO_4	AH27	VCCO
4	VCCO_4	VCCO_4	AJ22	VCCO
4	VCCO_4	VCCO_4	AL19	VCCO
4	VCCO_4	VCCO_4	AL24	VCCO
4	VCCO_4	VCCO_4	AM27	VCCO
4	VCCO_4	VCCO_4	AM31	VCCO
4	VCCO_4	VCCO_4	AN22	VCCO
5	IO	IO	AD11	I/O
5	N.C. (◆)	IO	AD12	I/O
5	IO	IO	AD14	I/O
5	IO	IO	AD15	I/O
5	IO	IO	AD16	I/O
5	IO	IO	AD17	I/O
5	IO	IO	AE14	I/O
5	IO	IO	AE16	I/O
5	N.C. (◆)	IO	AF9	I/O
5	IO	IO	AG9	I/O
5	IO	IO	AG12	I/O
5	IO	IO	AJ6	I/O
5	IO	IO	AJ17	I/O
5	IO	IO	AK10	I/O
5	IO	IO	AK14	I/O
5	IO	IO	AM12	I/O
5	IO	IO	AN9	I/O
5	IO/VREF_5	IO/VREF_5	AJ8	VREF
5	IO/VREF_5	IO/VREF_5	AL5	VREF
5	IO/VREF_5	IO/VREF_5	AP17	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	AP3	DUAL
5	IO_L01P_5/CS_B	IO_L01P_5/CS_B	AN3	DUAL
5	IO_L02N_5	IO_L02N_5	AP4	I/O
5	IO_L02P_5	IO_L02P_5	AN4	I/O
5	IO_L03N_5	IO_L03N_5	AN5	I/O
5	IO_L03P_5	IO_L03P_5	AM5	I/O
5	IO_L04N_5	IO_L04N_5	AM6	I/O