AMD Xilinx - XC3S400-4TQ144C Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	294912
Number of I/O	97
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s400-4tq144c

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Spartan-3 FPGA Family: Functional Description

DS099 (v3.0) October 29, 2012

Product Specification

Spartan-3 FPGA Design Documentation

The functionality of the Spartan®-3 FPGA family is described in the following documents. The topics covered in each guide are listed.

- UG331: *Spartan-3 Generation FPGA User Guide*
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Software Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
- UG332: *Spartan-3 Generation Configuration User Guide*
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx Platform Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples

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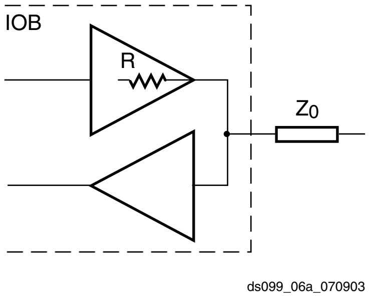
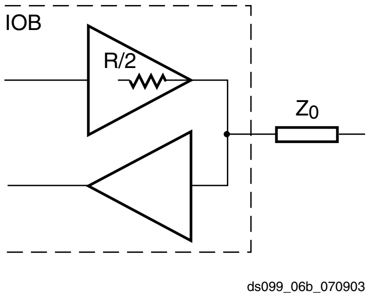
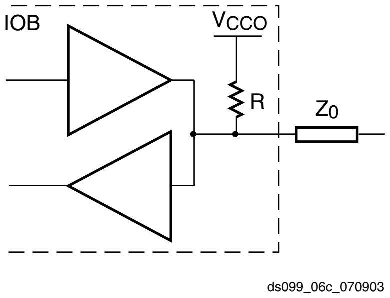
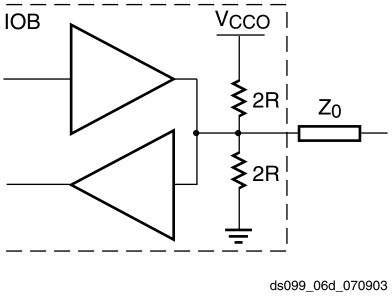
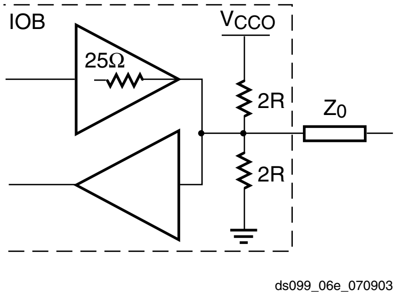
For specific hardware examples, see the Spartan-3 FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- Spartan-3 FPGA Starter Kit Board page
  http://www.xilinx.com/s3starter
- UG130: *Spartan-3 FPGA Starter Kit User Guide*

Table 11: **DCI Terminations**

Termination	Schematic(1)	Signal Standards (IOSTANDARD)
Controlled impedance output driver		LVDCI_15 LVDCI_18 LVDCI_25 LVDCI_33 HSLVDCI_15 HSLVDCI_18 HSLVDCI_25 HSLVDCI_33
Controlled output driver with half impedance		LVDCI_DV2_15 LVDCI_DV2_18 LVDCI_DV2_25 LVDCI_DV2_33
Single resistor		GTL_DCI GTLP_DCI HSTL_III_DCI(2) HSTL_III_DCI_18(2)
Split resistors		HSTL_I_DCI(2) HSTL_I_DCI_18(2) HSTL_II_DCI_18 DIFF_HSTL_II_18_DCI DIFF_SSTL2_II_DCI LVDS_25_DCI LVDSEXT_25_DCI
Split resistors with output driver impedance fixed to 25Ω		SSTL18_I_DCI(3) SSTL2_I_DCI(3) SSTL2_II_DCI

Notes:

1. The value of R is equivalent to the characteristic impedance of the line connected to the I/O. It is also equal to half the value of RREF for the DV2 standards and RREF for all other DCI standards.
2. For DCI using HSTL Classes I and III, terminations only go into effect at inputs (not at outputs).
3. For DCI using SSTL Class I, the split termination only goes into effect at inputs (not at outputs).

Table 13: **Block RAM Port Signals *(Cont'd)***

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Data Output Bus	DOA	DOB	Output	Basic data access occurs whenever WE is inactive. The DO outputs mirror the data stored in the addressed memory location. Data access with WE asserted is also possible if one of the following two attributes is chosen: WRITE_FIRST and READ_FIRST. WRITE_FIRST simultaneously presents the new input data on the DO output port and writes the data to the address RAM location. READ_FIRST presents the previously stored RAM data on the DO output port while writing new data to RAM. A third attribute, NO_CHANGE, latches the DO outputs upon the assertion of WE. It is possible to configure a port's total data path width (w) to be 1, 2, 4, 9, 18, or 36 bits. This selection applies to both the DI and DO paths. See the DI signal description.
Parity Data Output(s)	DOPA	DOPB	Output	Parity inputs represent additional bits included in the data input path to support error detection. The number of parity bits "p" included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 14.
Write Enable	WEA	WEB	Input	When asserted together with EN, this input enables the writing of data to the RAM. In this case, the data access attributes WRITE_FIRST, READ_FIRST or NO_CHANGE determines if and how data is updated on the DO outputs. See the DO signal description. When WE is inactive with EN asserted, read operations are still possible. In this case, a transparent latch passes data from the addressed memory location to the DO outputs.
Clock Enable	ENA	ENB	Input	When asserted, this input enables the CLK signal to synchronize Block RAM functions as follows: the writing of data to the DI inputs (when WE is also asserted), the updating of data at the DO outputs as well as the setting/resetting of the DO output latches. When de-asserted, the above functions are disabled.
Set/Reset	SSRA	SSRB	Input	When asserted, this pin forces the DO output latch to the value that the SRVAL attribute is set to. A Set/Reset operation on one port has no effect on the other ports functioning, nor does it disturb the memory's data contents. It is synchronized to the CLK signal.
Clock	CLKA	CLKB	Input	This input accepts the clock signal to which read and write operations are synchronized. All associated port inputs are required to meet setup times with respect to the clock signal's active edge. The data output bus responds after a clock-to-out delay referenced to the clock signal's active edge.

Port Aspect Ratios

On a given port, it is possible to select a number of different possible widths ($w - p$) for the DI/DO buses as shown in Table 14. These two buses always have the same width. This data bus width selection is independent for each port. If the data bus width of Port A differs from that of Port B, the Block RAM automatically performs a bus-matching function. When data are written to a port with a narrow bus, then read from a port with a wide bus, the latter port will effectively combine "narrow" words to form "wide" words. Similarly, when data are written into a port with a wide bus, then read from a port with a narrow bus, the latter port will divide "wide" words to form "narrow" words. When the data bus width is eight bits or greater, extra parity bits become available. The width of the total data path (w) is the sum of the DI/DO bus width and any parity bits (p).

The width selection made for the DI/DO bus determines the number of address lines according to the relationship expressed below:

$$r = 14 - [\log(w-p)/\log(2)] \qquad \text{Equation 1}$$

In turn, the number of address lines delimits the total number (n) of addressable locations or depth according to the following equation:

$$n = 2^r \qquad \text{Equation 2}$$

Coarse Phase Shift Outputs of the DLL Component

In addition to CLK0 for zero-phase alignment to the CLKIN signal, the DLL also provides the CLK90, CLK180 and CLK270 outputs for 90°, 180° and 270° phase-shifted signals, respectively. These signals are described in Table 16, page 33. Their relative timing in the Low Frequency Mode is shown in Figure 22, page 37. The CLK90, CLK180 and CLK270 outputs are not available when operating in the High Frequency mode. (See the description of the DLL_FREQUENCY_MODE attribute in Table 17, page 33.) For control in finer increments than 90°, see Phase Shifter (PS), page 39.

Basic Frequency Synthesis Outputs of the DLL Component

The DLL component provides basic options for frequency multiplication and division in addition to the more flexible synthesis capability of the DFS component, described in a later section. These operations result in output clock signals with frequencies that are either a fraction (for division) or a multiple (for multiplication) of the incoming clock frequency. The CLK2X output produces an in-phase signal that is twice the frequency of CLKIN. The CLK2X180 output also doubles the frequency, but is 180° out-of-phase with respect to CLKIN. The CLKDIV output generates a clock frequency that is a predetermined fraction of the CLKIN frequency. The CLKDV_DIVIDE attribute determines the factor used to divide the CLKIN frequency. The attribute can be set to various values as described in Table 17. The basic frequency synthesis outputs are described in Table 16. Their relative timing in the Low Frequency Mode is shown in Figure 22.

The CLK2X and CLK2X180 outputs are not available when operating in the High Frequency mode. See the description of the DLL_FREQUENCY_MODE attribute in Table 18.

Duty Cycle Correction of DLL Clock Outputs

The CLK2X(1), CLK2X180, and CLKDV(2) output signals ordinarily exhibit a 50% duty cycle—even if the incoming CLKIN signal has a different duty cycle. A 50% duty cycle means that the High and Low times of each clock cycle are equal. The DUTY_CYCLE_CORRECTION attribute determines whether or not duty cycle correction is applied to the CLK0, CLK90, CLK180 and CLK270 outputs. If DUTY_CYCLE_CORRECTION is set to TRUE, then the duty cycle of these four outputs is corrected to 50%. If DUTY_CYCLE_CORRECTION is set to FALSE, then these outputs exhibit the same duty cycle as the CLKIN signal. Figure 22 compares the characteristics of the DLL's output signals to those of the CLKIN signal.

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1. The CLK2X output generates a 25% duty cycle clock at the same frequency as the CLKIN signal until the DLL has achieved lock.
2. The duty cycle of the CLKDV outputs may differ somewhat from 50% (i.e., the signal will be High for less than 50% of the period) when the CLKDV_DIVIDE attribute is set to a non-integer value *and* the DLL is operating in the High Frequency mode.

The output frequency (f_{CLKFX}) can be expressed as a function of the incoming clock frequency (f_{CLKIN}) as follows:

$$f_{CLKFX} = f_{CLKIN}(CLKFX\_MULTIPLY/CLKFX\_DIVIDE) \qquad \text{Equation 3}$$

Regarding the two attributes, it is possible to assign any combination of integer values, provided that two conditions are met:

- The two values fall within their corresponding ranges, as specified in Table 18.
- The f_{CLKFX} frequency calculated from the above expression accords with the DCM's operating frequency specifications.

For example, if CLKFX_MULTIPLY = 5 and CLKFX_DIVIDE = 3, then the frequency of the output clock signal would be 5/3 that of the input clock signal.

DFS Frequency Modes

The DFS supports two operating modes, High Frequency and Low Frequency, with each specified over a different clock frequency range. The DFS_FREQUENCY_MODE attribute chooses between the two modes. When the attribute is set to LOW, the Low Frequency mode permits the two DFS outputs to operate over a low-to-moderate frequency range. When the attribute is set to HIGH, the High Frequency mode allows both these outputs to operate at the highest possible frequencies.

DFS With or Without the DLL

The DFS component can be used with or without the DLL component:

Without the DLL, the DFS component multiplies or divides the CLKIN signal frequency according to the respective CLKFX_MULTIPLY and CLKFX_DIVIDE values, generating a clock with the new target frequency on the CLKFX and CLKFX180 outputs. Though classified as belonging to the DLL component, the CLKIN input is shared with the DFS component. This case does not employ feedback loop; therefore, it cannot correct for clock distribution delay.

With the DLL, the DFS operates as described in the preceding case, only with the additional benefit of eliminating the clock distribution delay. In this case, a feedback loop from the CLK0 output to the CLKFB input must be present.

The DLL and DFS components work together to achieve this phase correction as follows: Given values for the CLKFX_MULTIPLY and CLKFX_DIVIDE attributes, the DLL selects the delay element for which the output clock edge coincides with the input clock edge whenever mathematically possible. For example, when CLKFX_MULTIPLY = 5 and CLKFX_DIVIDE = 3, the input and output clock edges will coincide every three input periods, which is equivalent in time to five output periods.

Smaller CLKFX_MULTIPLY and CLKFX_DIVIDE values achieve faster lock times. With no factors common to the two attributes, alignment will occur once with every number of cycles equal to the CLKFX_DIVIDE value. Therefore, it is recommended that the user reduce these values by factoring wherever possible. For example, given CLKFX_MULTIPLY = 9 and CLKFX_DIVIDE = 6, removing a factor of three yields CLKFX_MULTIPLY = 3 and CLKFX_DIVIDE = 2. While both value-pairs will result in the multiplication of clock frequency by 3/2, the latter value-pair will enable the DLL to lock more quickly.

Table 18: **DFS Attributes**

Attribute	Description	Values
DFS_FREQUENCY_MODE	Chooses between High Frequency and Low Frequency modes	Low, High
CLKFX_MULTIPLY	Frequency multiplier constant	Integer from 2 to 32
CLKFX_DIVIDE	Frequency divisor constant	Integer from 1 to 32

Table 19: **DFS Signals**

Signal	Direction	Description
CLKFX	Output	Multiplies the CLKIN frequency by the attribute-value ratio (CLKFX_MULTIPLY/CLKFX_DIVIDE) to generate a clock signal with a new target frequency.
CLKFX180	Output	Generates a clock signal with same frequency as CLKFX, only shifted 180° out-of-phase.

Table 52: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	–	1.87	–	2.15	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	0.46	–	0.52	–	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.46	–	0.53	–	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.33	–	0.37	–	ns
Hold Times						
T_{DH}, T_{AH}, T_{WH}	Hold time of the BX, BY data inputs, the F/G address inputs, or the write enable input after the active transition at the CLK input of the distributed RAM	0	–	0	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.85	–	0.97	–	ns

Table 53: **CLB Shift Register Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	–	3.30	–	3.79	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.46	–	0.52	–	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0	–	0	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.85	–	0.97	–	ns

Table 56: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{BCKO}	When reading from the Block RAM, the time from the active transition at the CLK input to data appearing at the DOUT output	–	2.09	–	2.40	ns
Setup Times						
T_{BDCK}	Time from the setup of data at the DIN inputs to the active transition at the CLK input of the Block RAM	0.43	–	0.49	–	ns
Hold Times						
T_{BCKD}	Time from the active transition at the Block RAM's CLK input to the point where data is last held at the DIN inputs	0	–	0	–	ns
Clock Timing						
T_{BPWH}	Block RAM CLK signal High pulse width	1.19	∞	1.37	∞	ns
T_{BPWL}	Block RAM CLK signal Low pulse width	1.19	∞	1.37	∞	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 32.
2. For minimums, use the values reported by the Xilinx timing analyzer.

Clock Distribution Switching Characteristics

Table 57: **Clock Distribution Switching Characteristics**

Description	Symbol	Maximum		Units
		Speed Grade		
		-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I-input to O-output delay	T_{GIO}	0.36	0.41	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0- and I1-inputs. Same as BUFGCE enable CE-input	T_{GSI}	0.53	0.60	ns

Notes:

1. For minimums, use the values reported by the Xilinx timing analyzer.

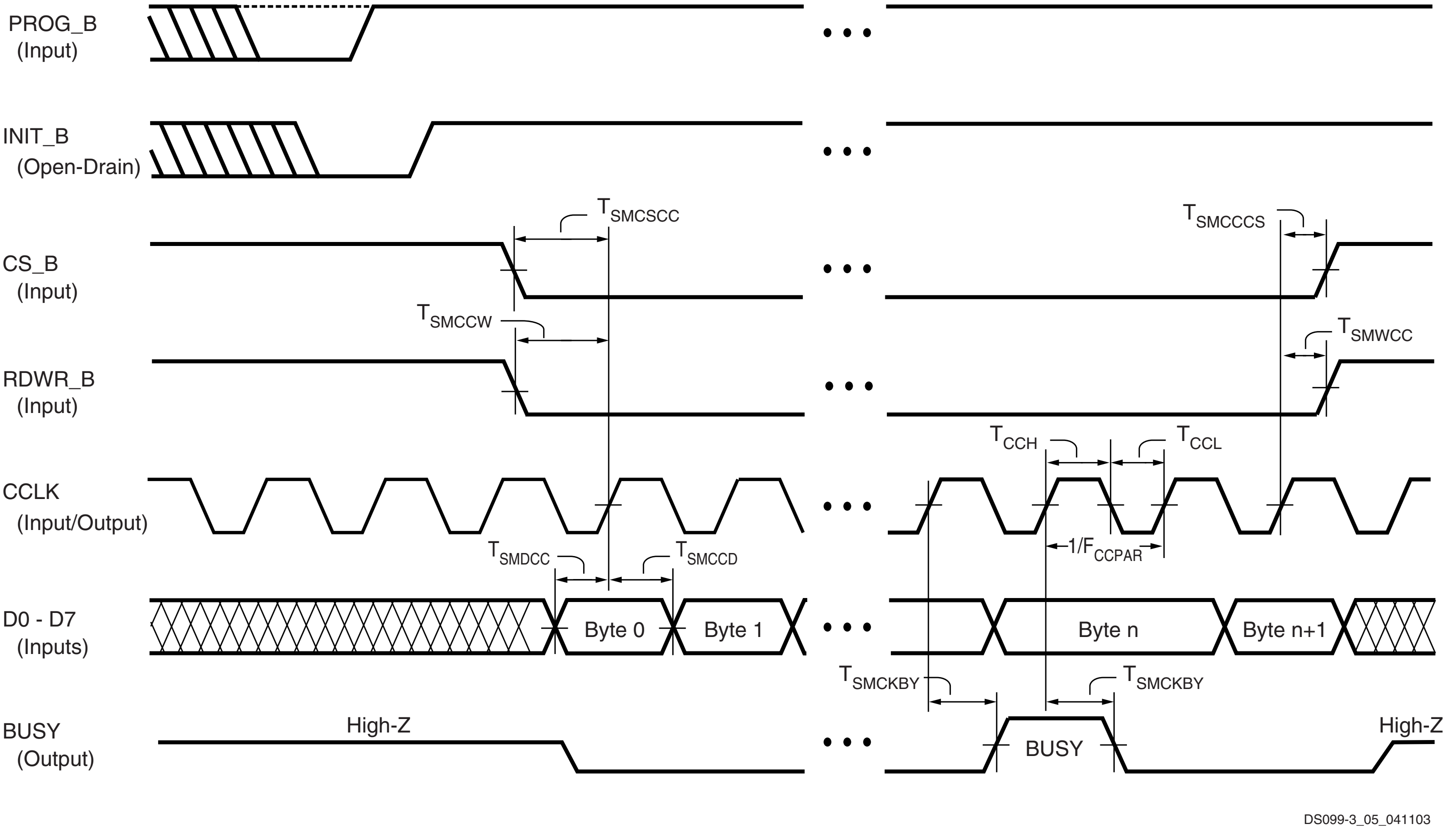


Figure 38: **Waveforms for Master and Slave Parallel Configuration**

Table 67: **Timing for the Master and Slave Parallel Configuration Modes**

Symbol	Description	Slave/ Master	All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin	Slave	–	12.0	ns
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	Both	10.0	–	ns
T_{SMCSCC}	The time from the setup of a logic level at the CS_B pin to the rising transition at the CCLK pin		10.0	–	ns
T_{SMCCW}(3)	The time from the setup of a logic level at the RDWR_B pin to the rising transition at the CCLK pin		10.0	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins	Both	0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CS_B pin		0	–	ns
T_{SMWCC}(3)	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns

VREF: User I/O or Input Buffer Reference Voltage for Special Interface Standards

These pins are individual user-I/O pins unless collectively they supply an input reference voltage, VREF_#, for any SSTL, HSTL, GTL, or GTLP I/Os implemented in the associated I/O bank. The '#' character in the pin name represents an integer, 0 through 7, that indicates the associated I/O bank.

The VREF function becomes active for this pin whenever a signal standard requiring a reference voltage is used in the associated bank. If used as a user I/O, then each pin behaves as an independent I/O described in the I/O type section. If used for a reference voltage within a bank, then *all* VREF pins within the bank must be connected to the same reference voltage.

Spartan-3 devices are designed and characterized to support certain I/O standards when VREF is connected to +1.25V, +1.10V, +1.00V, +0.90V, +0.80V, and +0.75V. During configuration, the VREF pins behave exactly like user-I/O pins.

If designing for footprint compatibility across the range of devices in a specific package, and if the VREF_# pins within a bank connect to an input reference voltage, then also connect any N.C. (not connected) pins on the smaller devices in that package to the input reference voltage. More details are provided later for each package type.

N.C. Type: Unconnected Package Pins

Pins marked as "N.C." are unconnected for the specific device/package combination. For other devices in this same package, this pin may be used as an I/O or VREF connection. In both the pinout tables and the footprint diagrams, unconnected pins are noted with either a black diamond symbol (◆) or a black square symbol (■).

If designing for footprint compatibility across multiple device densities, check the pin types of the other Spartan-3 devices available in the same footprint. If the N.C. pin matches to VREF pins in other devices, and the VREF pins are used in the associated I/O bank, then connect the N.C. to the VREF voltage source.

VCCO Type: Output Voltage Supply for I/O Bank

Each I/O bank has its own set of voltage supply pins that determines the output voltage for the output buffers in the I/O bank. Furthermore, for some I/O standards such as LVCMOS, LVCMOS25, LVTTL, etc., VCCO sets the input threshold voltage on the associated input buffers.

Spartan-3 devices are designed and characterized to support various I/O standards for VCCO values of +1.2V, +1.5V, +1.8V, +2.5V, and +3.3V.

Most VCCO pins are labeled as VCCO_# where the '#' symbol represents the associated I/O bank number, an integer ranging from 0 to 7. In the 144-pin TQFP package (TQ144) however, the VCCO pins along an edge of the device are combined into a single VCCO input. For example, the VCCO inputs for Bank 0 and Bank 1 along the top edge of the package are combined and relabeled VCCO_TOP. The bottom, left, and right edges are similarly combined.

In Serial configuration mode, VCCO_4 must be at a level compatible with the attached configuration memory or data source. In Parallel configuration mode, both VCCO_4 and VCCO_5 must be at the same compatible voltage level.

All VCCO inputs to a bank must be connected together and to the voltage supply. Furthermore, there must be sufficient supply decoupling to guarantee problem-free operation, as described in XAPP623: *Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors*.

VCCINT Type: Voltage Supply for Internal Core Logic

Internal core logic circuits such as the configurable logic blocks (CLBs) and programmable interconnect operate from the VCCINT voltage supply inputs. VCCINT must be +1.2V.

All VCCINT inputs must be connected together and to the +1.2V voltage supply. Furthermore, there must be sufficient supply decoupling to guarantee problem-free operation, as described in XAPP623.

VCCAUX Type: Voltage Supply for Auxiliary Logic

The VCCAUX pins supply power to various auxiliary circuits, such as to the Digital Clock Managers (DCMs), the JTAG pins, and to the dedicated configuration pins (CONFIG type). VCCAUX must be +2.5V.

PQ208 Footprint

Left Half of Package (Top View)

XC3S50
(124 max. user I/O)

72 **I/O:** Unrestricted, general-purpose user I/O

16 **VREF:** User I/O or input voltage reference for bank

17 **N.C.:** Unconnected pins for XC3S50 (◆)

XC3S200, XC3S400
(141 max user I/O)

83 **I/O:** Unrestricted, general-purpose user I/O

22 **VREF:** User I/O or input voltage reference for bank

0 **N.C.:** No unconnected pins in this package

All devices

12 **DUAL:** Configuration pin, then possible user I/O

8 **GCLK:** User I/O or global clock buffer input

16 **DCI:** User I/O or reference resistor input for bank

7 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

4 **VCCINT:** Internal core voltage supply (+1.2V)

12 **VCCO:** Output voltage supply for bank

8 **VCCAUX:** Auxiliary voltage supply (+2.5V)

28 **GND:** Ground

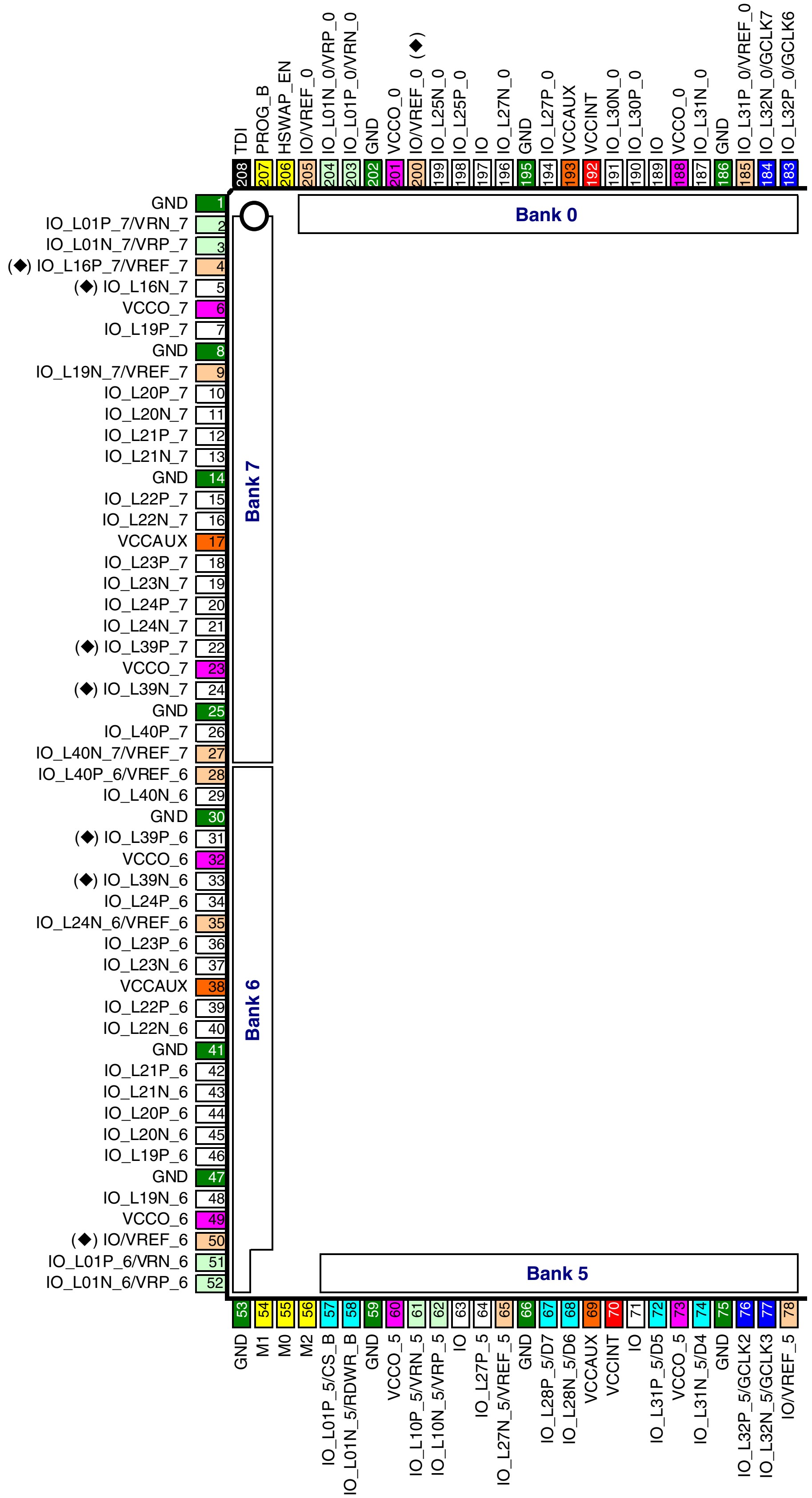


Figure 47: **PQ208 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

Table 96: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S200, XC3S400, XC3S1000 Pin Name	FT256 Pin Number	Type
6	IO_L16P_6	N3	I/O
6	IO_L17N_6	N2	I/O
6	IO_L17P_6/VREF_6	N1	VREF
6	IO_L19N_6	M4	I/O
6	IO_L19P_6	M3	I/O
6	IO_L20N_6	M2	I/O
6	IO_L20P_6	M1	I/O
6	IO_L21N_6	L5	I/O
6	IO_L21P_6	L4	I/O
6	IO_L22N_6	L3	I/O
6	IO_L22P_6	L2	I/O
6	IO_L23N_6	K5	I/O
6	IO_L23P_6	K4	I/O
6	IO_L24N_6/VREF_6	K3	VREF
6	IO_L24P_6	K2	I/O
6	IO_L39N_6	J4	I/O
6	IO_L39P_6	J3	I/O
6	IO_L40N_6	J2	I/O
6	IO_L40P_6/VREF_6	J1	VREF
6	VCCO_6	J5	VCCO
6	VCCO_6	J6	VCCO
6	VCCO_6	K6	VCCO
7	IO	G2	I/O
7	IO_L01N_7/VRP_7	C1	DCI
7	IO_L01P_7/VRN_7	B1	DCI
7	IO_L16N_7	C2	I/O
7	IO_L16P_7/VREF_7	C3	VREF
7	IO_L17N_7	D1	I/O
7	IO_L17P_7	D2	I/O
7	IO_L19N_7/VREF_7	E3	VREF
7	IO_L19P_7	D3	I/O
7	IO_L20N_7	E1	I/O
7	IO_L20P_7	E2	I/O
7	IO_L21N_7	F4	I/O
7	IO_L21P_7	E4	I/O
7	IO_L22N_7	F2	I/O
7	IO_L22P_7	F3	I/O
7	IO_L23N_7	G5	I/O
7	IO_L23P_7	F5	I/O
7	IO_L24N_7	G3	I/O

Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
4	IO_L31P_4/ DOUT/BUSY	V10	DUAL
4	IO_L32N_4/GCLK1	N10	GCLK
4	IO_L32P_4/GCLK0	P10	GCLK
4	VCCO_4	M10	VCCO
4	VCCO_4	M11	VCCO
4	VCCO_4	T13	VCCO
4	VCCO_4	U11	VCCO
5	IO	N8	I/O
5	IO	P8	I/O
5	IO	U6	I/O
5	IO/VREF_5	R9	VREF
5	IO_L01N_5/RDWR_B	V3	DUAL
5	IO_L01P_5/CS_B	V2	DUAL
5	IO_L06N_5	T5	I/O
5	IO_L06P_5	T4	I/O
5	IO_L10N_5/VRP_5	V4	DCI
5	IO_L10P_5/VRN_5	U4	DCI
5	IO_L15N_5	R6	I/O
5	IO_L15P_5	R5	I/O
5	IO_L16N_5	V5	I/O
5	IO_L16P_5	U5	I/O
5	IO_L27N_5/VREF_5	P6	VREF
5	IO_L27P_5	P7	I/O
5	IO_L28N_5/D6	R7	DUAL
5	IO_L28P_5/D7	T7	DUAL
5	IO_L29N_5	V8	I/O
5	IO_L29P_5/VREF_5	V7	VREF
5	IO_L30N_5	R8	I/O
5	IO_L30P_5	T8	I/O
5	IO_L31N_5/D4	U9	DUAL
5	IO_L31P_5/D5	V9	DUAL
5	IO_L32N_5/GCLK3	N9	GCLK
5	IO_L32P_5/GCLK2	P9	GCLK
5	VCCO_5	M8	VCCO
5	VCCO_5	M9	VCCO
5	VCCO_5	T6	VCCO
5	VCCO_5	U8	VCCO
6	IO	K6	I/O
6	IO_L01N_6/VRP_6	T3	DCI

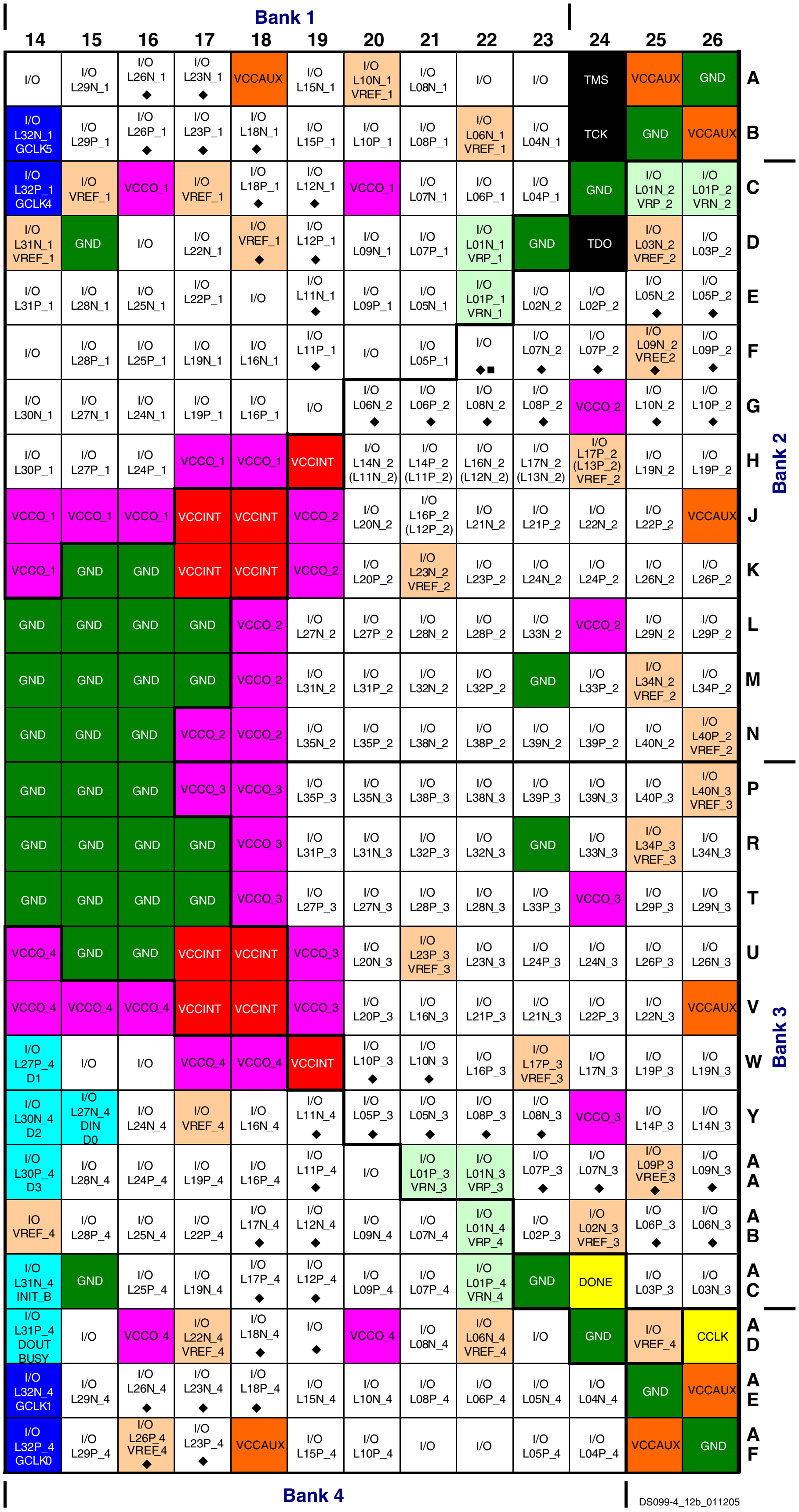
Table 98: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
6	IO_L01P_6/VRN_6	T2	DCI
6	IO_L16N_6	U1	I/O
6	IO_L16P_6	T1	I/O
6	IO_L17N_6	R2	I/O
6	IO_L17P_6/VREF_6	R1	VREF
6	IO_L19N_6	R3	I/O
6	IO_L19P_6	P3	I/O
6	IO_L20N_6	P2	I/O
6	IO_L20P_6	P1	I/O
6	IO_L21N_6	N4	I/O
6	IO_L21P_6	P4	I/O
6	IO_L22N_6	N5	I/O
6	IO_L22P_6	M5	I/O
6	IO_L23N_6	M3	I/O
6	IO_L23P_6	M4	I/O
6	IO_L24N_6/VREF_6	N2	VREF
6	IO_L24P_6	M1	I/O
6	IO_L27N_6	L6	I/O
6	IO_L27P_6	L5	I/O
6	IO_L34N_6/VREF_6	L3	VREF
6	IO_L34P_6	L4	I/O
6	IO_L35N_6	L2	I/O
6	IO_L35P_6	L1	I/O
6	IO_L39N_6	K5	I/O
6	IO_L39P_6	K4	I/O
6	IO_L40N_6	K1	I/O
6	IO_L40P_6/VREF_6	K2	VREF
6	VCCO_6	K7	VCCO
6	VCCO_6	L7	VCCO
6	VCCO_6	N3	VCCO
7	IO	J6	I/O
7	IO_L01N_7/VRP_7	C3	DCI
7	IO_L01P_7/VRN_7	C2	DCI
7	IO_L16N_7	C1	I/O
7	IO_L16P_7/VREF_7	B1	VREF
7	IO_L17N_7	D1	I/O
7	IO_L17P_7	D2	I/O
7	IO_L19N_7/VREF_7	E3	VREF
7	IO_L19P_7	D3	I/O
7	IO_L20N_7	E2	I/O

Table 103: **FG676 Package Pinout *(Cont'd)***

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
1	N.C. (◆)	IO_L18P_1	IO_L18P_1	IO_L18P_1	IO[3]	C18	I/O
1	IO_L19N_1	IO_L19N_1	IO_L19N_1	IO_L19N_1	IO_L19N_1	F17	I/O
1	IO_L19P_1	IO_L19P_1	IO_L19P_1	IO_L19P_1	IO_L19P_1	G17	I/O
1	IO_L22N_1	IO_L22N_1	IO_L22N_1	IO_L22N_1	IO_L22N_1	D17	I/O
1	IO_L22P_1	IO_L22P_1	IO_L22P_1	IO_L22P_1	IO_L22P_1	E17	I/O
1	N.C. (◆)	IO_L23N_1	IO_L23N_1	IO_L23N_1	IO_L23N_1	A17	I/O
1	N.C. (◆)	IO_L23P_1	IO_L23P_1	IO_L23P_1	IO_L23P_1	B17	I/O
1	IO_L24N_1	IO_L24N_1	IO_L24N_1	IO_L24N_1	IO_L24N_1	G16	I/O
1	IO_L24P_1	IO_L24P_1	IO_L24P_1	IO_L24P_1	IO_L24P_1	H16	I/O
1	IO_L25N_1	IO_L25N_1	IO_L25N_1	IO_L25N_1	IO_L25N_1	E16	I/O
1	IO_L25P_1	IO_L25P_1	IO_L25P_1	IO_L25P_1	IO_L25P_1	F16	I/O
1	N.C. (◆)	IO_L26N_1	IO_L26N_1	IO_L26N_1	IO_L26N_1	A16	I/O
1	N.C. (◆)	IO_L26P_1	IO_L26P_1	IO_L26P_1	IO_L26P_1	B16	I/O
1	IO_L27N_1	IO_L27N_1	IO_L27N_1	IO_L27N_1	IO_L27N_1	G15	I/O
1	IO_L27P_1	IO_L27P_1	IO_L27P_1	IO_L27P_1	IO_L27P_1	H15	I/O
1	IO_L28N_1	IO_L28N_1	IO_L28N_1	IO_L28N_1	IO_L28N_1	E15	I/O
1	IO_L28P_1	IO_L28P_1	IO_L28P_1	IO_L28P_1	IO_L28P_1	F15	I/O
1	IO_L29N_1	IO_L29N_1	IO_L29N_1	IO_L29N_1	IO_L29N_1	A15	I/O
1	IO_L29P_1	IO_L29P_1	IO_L29P_1	IO_L29P_1	IO_L29P_1	B15	I/O
1	IO_L30N_1	IO_L30N_1	IO_L30N_1	IO_L30N_1	IO_L30N_1	G14	I/O
1	IO_L30P_1	IO_L30P_1	IO_L30P_1	IO_L30P_1	IO_L30P_1	H14	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D14	VREF
1	IO_L31P_1	IO_L31P_1	IO_L31P_1	IO_L31P_1	IO_L31P_1	E14	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B14	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C14	GCLK
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	C16	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	C20	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	H17	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	H18	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J14	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J15	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	J16	VCCO
1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	VCCO_1	K14	VCCO
2	N.C. (◆)	N.C. (■)	IO	IO	IO	F22	I/O
2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	IO_L01N_2/VRP_2	C25	DCI
2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	IO_L01P_2/VRN_2	C26	DCI
2	IO_L02N_2	IO_L02N_2	IO_L02N_2	IO_L02N_2	IO_L02N_2	E23	I/O
2	IO_L02P_2	IO_L02P_2	IO_L02P_2	IO_L02P_2	IO_L02P_2	E24	I/O
2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2[1]	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	IO_L03N_2/VREF_2	D25	VREF[1]
2	IO_L03P_2	IO_L03P_2	IO_L03P_2	IO_L03P_2	IO_L03P_2	D26	I/O
2	N.C. (◆)	IO_L05N_2	IO_L05N_2	IO_L05N_2	IO_L05N_2	E25	I/O
2	N.C. (◆)	IO_L05P_2	IO_L05P_2	IO_L05P_2	IO_L05P_2	E26	I/O

Right Half of Package (Top View)



14	15	16	17	18	19	20	21	22	23	24	25	26	
I/O	I/O L29N_1	I/O L26N_1 ◆	I/O L23N_1 ◆	VCCAUX	I/O L15N_1	I/O L10N_1 VREF_1	I/O L08N_1	I/O	I/O	TMS	VCCAUX	GND	A
I/O L32N_1 GCLK5	I/O L29P_1	I/O L26P_1 ◆	I/O L23P_1 ◆	I/O L18N_1 ◆	I/O L15P_1	I/O L10P_1	I/O L08P_1	I/O L06N_1 VREF_1	I/O L04N_1	TCK	GND	VCCAUX	B
I/O L32P_1 GCLK4	I/O VREF_1	VCCO_1	I/O VREF_1	I/O L18P_1 ◆	I/O L12N_1 ◆	VCCO_1	I/O L07N_1	I/O L06P_1	I/O L04P_1	GND	I/O L01N_2 VRP_2	I/O L01P_2 VRN_2	C
I/O L31N_1 VREF_1	GND	I/O	I/O L22N_1	I/O VREF_1 ◆	I/O L12P_1 ◆	I/O L09N_1	I/O L07P_1	I/O L01N_1 VRP_1	GND	TDO	I/O L03N_2 VREF_2	I/O L03P_2	D
I/O L31P_1	I/O L28N_1	I/O L25N_1	I/O L22P_1	I/O	I/O L11N_1 ◆	I/O L09P_1	I/O L05N_1	I/O L01P_1 VRN_1	I/O L02N_2	I/O L02P_2	I/O L05N_2 ◆	I/O L05P_2 ◆	E
I/O	I/O L28P_1	I/O L25P_1	I/O L19N_1	I/O L16N_1	I/O L11P_1 ◆	I/O	I/O L05P_1	I/O ◆■	I/O L07N_2 ◆	I/O L07P_2 ◆	I/O L09N_2 VREF_2 ◆	I/O L09P_2 ◆	F
I/O L30N_1	I/O L27N_1	I/O L24N_1	I/O L19P_1	I/O L16P_1	I/O	I/O L06N_2 ◆	I/O L06P_2 ◆	I/O L08N_2 ◆	I/O L08P_2 ◆	VCCO_2	I/O L10N_2 ◆	I/O L10P_2 ◆	G
I/O L30P_1	I/O L27P_1	I/O L24P_1	VCCO_1	VCCO_1	VCCINT	I/O L14N_2 (L11N_2)	I/O L14P_2 (L11P_2)	I/O L16N_2 (L12N_2)	I/O L17N_2 (L13N_2)	I/O L17P_2 (L13P_2) VREF_2	I/O L19N_2	I/O L19P_2	H
VCCO_1	VCCO_1	VCCO_1	VCCINT	VCCINT	VCCO_2	I/O L20N_2	I/O L16P_2 (L12P_2)	I/O L21N_2	I/O L21P_2	I/O L22N_2	I/O L22P_2	VCCAUX	J
VCCO_1	GND	GND	VCCINT	VCCINT	VCCO_2	I/O L20P_2	I/O L23N_2 VREF_2	I/O L23P_2	I/O L24N_2	I/O L24P_2	I/O L26N_2	I/O L26P_2	K
GND	GND	GND	GND	VCCO_2	I/O L27N_2	I/O L27P_2	I/O L28N_2	I/O L28P_2	I/O L33N_2	VCCO_2	I/O L29N_2	I/O L29P_2	L
GND	GND	GND	GND	VCCO_2	I/O L31N_2	I/O L31P_2	I/O L32N_2	I/O L32P_2	GND	I/O L33P_2	I/O L34N_2 VREF_2	I/O L34P_2	M
GND	GND	GND	VCCO_2	VCCO_2	I/O L35N_2	I/O L35P_2	I/O L38N_2	I/O L38P_2	I/O L39N_2	I/O L39P_2	I/O L40N_2	I/O L40P_2 VREF_2	N
GND	GND	GND	VCCO_3	VCCO_3	I/O L35P_3	I/O L35N_3	I/O L38P_3	I/O L38N_3	I/O L39P_3	I/O L39N_3	I/O L40P_3	I/O L40N_3 VREF_3	P
GND	GND	GND	GND	VCCO_3	I/O L31P_3	I/O L31N_3	I/O L32P_3	I/O L32N_3	GND	I/O L33N_3	I/O L34P_3 VREF_3	I/O L34N_3	R
GND	GND	GND	GND	VCCO_3	I/O L27P_3	I/O L27N_3	I/O L28P_3	I/O L28N_3	I/O L33P_3	VCCO_3	I/O L29P_3	I/O L29N_3	T
VCCO_4	GND	GND	VCCINT	VCCINT	VCCO_3	I/O L20N_3	I/O L23P_3 VREF_3	I/O L23N_3	I/O L24P_3	I/O L24N_3	I/O L26P_3	I/O L26N_3	U
VCCO_4	VCCO_4	VCCO_4	VCCINT	VCCINT	VCCO_3	I/O L20P_3	I/O L16N_3	I/O L21P_3	I/O L21N_3	I/O L22P_3	I/O L22N_3	VCCAUX	V
I/O L27P_4 D1	I/O	I/O	VCCO_4	VCCO_4	VCCINT	I/O L10P_3 ◆	I/O L10N_3 ◆	I/O L16P_3	I/O L17P_3 VREF_3	I/O L17N_3	I/O L19P_3	I/O L19N_3	W
I/O L30N_4 D2	I/O L27N_4 DIN D0	I/O L24N_4	I/O VREF_4	I/O L16N_4	I/O L11N_4 ◆	I/O L05P_3 ◆	I/O L05N_3 ◆	I/O L08P_3 ◆	I/O L08N_3 ◆	VCCO_3	I/O L14P_3	I/O L14N_3	Y
I/O L30P_4 D3	I/O L28N_4	I/O L24P_4	I/O L19P_4	I/O L16P_4	I/O L11P_4 ◆	I/O	I/O L01P_3 VRN_3	I/O L01N_3 VRP_3	I/O L07P_3 ◆	I/O L07N_3 ◆	I/O L09P_3 VREF_3 ◆	I/O L09N_3 ◆	AA
IO VREF_4	I/O L28P_4	I/O L25N_4	I/O L22P_4	I/O L17N_4 ◆	I/O L12N_4 ◆	I/O L09N_4	I/O L07N_4	I/O L01N_4 VRP_4	I/O L02P_3	I/O L02N_3 VREF_3	I/O L06P_3 ◆	I/O L06N_3 ◆	AB
I/O L31N_4 INIT_B	GND	I/O L25P_4	I/O L19N_4	I/O L17P_4 ◆	I/O L12P_4 ◆	I/O L09P_4	I/O L07P_4	I/O L01P_4 VRN_4	GND	DONE	I/O L03P_3	I/O L03N_3	AC
I/O L31P_4 DOUT BUSY	I/O	VCCO_4	I/O L22N_4 VREF_4	I/O L18N_4 ◆	I/O ◆	VCCO_4	I/O L08N_4	I/O L06N_4 VREF_4	I/O	GND	I/O VREF_4	CCLK	AD
I/O L32N_4 GCLK1	I/O L29N_4	I/O L26N_4 ◆	I/O L23N_4 ◆	I/O L18P_4 ◆	I/O L15N_4	I/O L10N_4	I/O L08P_4	I/O L06P_4	I/O L05N_4	I/O L04N_4	GND	VCCAUX	AE
I/O L32P_4 GCLK0	I/O L29P_4	I/O L26P_4 VREF_4 ◆	I/O L23P_4 ◆	VCCAUX	I/O L15P_4	I/O L10P_4	I/O	I/O	I/O L05P_4	I/O L04P_4	VCCAUX	GND	AF

Figure 54: FG676 Package Footprint (Top View) Continued

Notes:

1. Differential pair assignments shown in parentheses on balls H20, H21, H22, H23, H24, and J21 are for XC3S4000 only.
2. Differential pair assignments for the XC3S5000 are different on 15 balls (see Table 103 for details.)

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	IO_L04N_2	IO_L04N_2	E29	I/O
2	IO_L04P_2	IO_L04P_2	E30	I/O
2	IO_L05N_2	IO_L05N_2	F28	I/O
2	IO_L05P_2	IO_L05P_2	F29	I/O
2	IO_L06N_2	IO_L06N_2	G27	I/O
2	IO_L06P_2	IO_L06P_2	G28	I/O
2	IO_L07N_2	IO_L07N_2	G29	I/O
2	IO_L07P_2	IO_L07P_2	G30	I/O
2	IO_L08N_2	IO_L08N_2	G25	I/O
2	IO_L08P_2	IO_L08P_2	H24	I/O
2	IO_L09N_2/VREF_2	IO_L09N_2/VREF_2	H25	VREF
2	IO_L09P_2	IO_L09P_2	H26	I/O
2	IO_L10N_2	IO_L10N_2	H27	I/O
2	IO_L10P_2	IO_L10P_2	H28	I/O
2	IO_L12N_2	IO_L12N_2	H29	I/O
2	IO_L12P_2	IO_L12P_2	H30	I/O
2	IO_L13N_2	IO_L13N_2	J26	I/O
2	IO_L13P_2/VREF_2	IO_L13P_2/VREF_2	J27	VREF
2	IO_L14N_2	IO_L14N_2	J29	I/O
2	IO_L14P_2	IO_L14P_2	J30	I/O
2	IO_L15N_2	IO_L15N_2	J23	I/O
2	IO_L15P_2	IO_L15P_2	K22	I/O
2	IO_L16N_2	IO_L16N_2	K24	I/O
2	IO_L16P_2	IO_L16P_2	K25	I/O
2	IO_L19N_2	IO_L19N_2	L25	I/O
2	IO_L19P_2	IO_L19P_2	L26	I/O
2	IO_L20N_2	IO_L20N_2	L27	I/O
2	IO_L20P_2	IO_L20P_2	L28	I/O
2	IO_L21N_2	IO_L21N_2	L29	I/O
2	IO_L21P_2	IO_L21P_2	L30	I/O
2	IO_L22N_2	IO_L22N_2	M22	I/O
2	IO_L22P_2	IO_L22P_2	M23	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	M24	VREF
2	IO_L23P_2	IO_L23P_2	M25	I/O
2	IO_L24N_2	IO_L24N_2	M27	I/O
2	IO_L24P_2	IO_L24P_2	M28	I/O
2	IO_L26N_2	IO_L26N_2	M21	I/O
2	IO_L26P_2	IO_L26P_2	N21	I/O
2	IO_L27N_2	IO_L27N_2	N22	I/O
2	IO_L27P_2	IO_L27P_2	N23	I/O

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
2	IO_L28N_2	IO_L28N_2	M26	I/O
2	IO_L28P_2	IO_L28P_2	N25	I/O
2	IO_L29N_2	IO_L29N_2	N26	I/O
2	IO_L29P_2	IO_L29P_2	N27	I/O
2	IO_L31N_2	IO_L31N_2	N29	I/O
2	IO_L31P_2	IO_L31P_2	N30	I/O
2	IO_L32N_2	IO_L32N_2	P21	I/O
2	IO_L32P_2	IO_L32P_2	P22	I/O
2	IO_L33N_2	IO_L33N_2	P24	I/O
2	IO_L33P_2	IO_L33P_2	P25	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	P28	VREF
2	IO_L34P_2	IO_L34P_2	P29	I/O
2	IO_L35N_2	IO_L35N_2	R21	I/O
2	IO_L35P_2	IO_L35P_2	R22	I/O
2	IO_L37N_2	IO_L37N_2	R23	I/O
2	IO_L37P_2	IO_L37P_2	R24	I/O
2	IO_L38N_2	IO_L38N_2	R25	I/O
2	IO_L38P_2	IO_L38P_2	R26	I/O
2	IO_L39N_2	IO_L39N_2	R27	I/O
2	IO_L39P_2	IO_L39P_2	R28	I/O
2	IO_L40N_2	IO_L40N_2	R29	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	R30	VREF
2	N.C. (◆)	IO_L41N_2	E27	I/O
2	N.C. (◆)	IO_L41P_2	F26	I/O
2	N.C. (◆)	IO_L45N_2	K28	I/O
2	N.C. (◆)	IO_L45P_2	K29	I/O
2	N.C. (◆)	IO_L46N_2	K21	I/O
2	N.C. (◆)	IO_L46P_2	L21	I/O
2	N.C. (◆)	IO_L47N_2	L23	I/O
2	N.C. (◆)	IO_L47P_2	L24	I/O
2	N.C. (◆)	IO_L50N_2	M29	I/O
2	N.C. (◆)	IO_L50P_2	M30	I/O
2	VCCO_2	VCCO_2	M20	VCCO
2	VCCO_2	VCCO_2	N20	VCCO
2	VCCO_2	VCCO_2	P20	VCCO
2	VCCO_2	VCCO_2	L22	VCCO
2	VCCO_2	VCCO_2	J24	VCCO
2	VCCO_2	VCCO_2	N24	VCCO
2	VCCO_2	VCCO_2	G26	VCCO
2	VCCO_2	VCCO_2	E28	VCCO

Table 107: **FG900 Package Pinout *(Cont'd)***

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
5	IO_L07N_5	IO_L07N_5	AK8	I/O
5	IO_L07P_5	IO_L07P_5	AJ8	I/O
5	IO_L08N_5	IO_L08N_5	AC9	I/O
5	IO_L08P_5	IO_L08P_5	AB9	I/O
5	IO_L09N_5	IO_L09N_5	AG9	I/O
5	IO_L09P_5	IO_L09P_5	AF9	I/O
5	IO_L10N_5/VRP_5	IO_L10N_5/VRP_5	AK9	DCI
5	IO_L10P_5/VRN_5	IO_L10P_5/VRN_5	AJ9	DCI
5	IO_L11N_5/VREF_5	IO_L11N_5/VREF_5	AE10	VREF
5	IO_L11P_5	IO_L11P_5	AE9	I/O
5	IO_L12N_5	IO_L12N_5	AJ10	I/O
5	IO_L12P_5	IO_L12P_5	AH10	I/O
5	IO_L13N_5	IO_L13N_5	AD11	I/O
5	IO_L13P_5	IO_L13P_5	AD10	I/O
5	IO_L14N_5	IO_L14N_5	AF11	I/O
5	IO_L14P_5	IO_L14P_5	AE11	I/O
5	IO_L15N_5	IO_L15N_5	AH11	I/O
5	IO_L15P_5	IO_L15P_5	AG11	I/O
5	IO_L16N_5	IO_L16N_5	AK11	I/O
5	IO_L16P_5	IO_L16P_5	AJ11	I/O
5	IO_L17N_5	IO_L17N_5	AB12	I/O
5	IO_L17P_5	IO_L17P_5	AC11	I/O
5	IO_L18N_5	IO_L18N_5	AD12	I/O
5	IO_L18P_5	IO_L18P_5	AC12	I/O
5	IO_L19N_5	IO_L19N_5	AF12	I/O
5	IO_L19P_5/VREF_5	IO_L19P_5/VREF_5	AE12	VREF
5	IO_L20N_5	IO_L20N_5	AH12	I/O
5	IO_L20P_5	IO_L20P_5	AG12	I/O
5	IO_L21N_5	IO_L21N_5	AK12	I/O
5	IO_L21P_5	IO_L21P_5	AJ12	I/O
5	IO_L22N_5	IO_L22N_5	AA13	I/O
5	IO_L22P_5	IO_L22P_5	AA12	I/O
5	IO_L23N_5	IO_L23N_5	AC13	I/O
5	IO_L23P_5	IO_L23P_5	AB13	I/O
5	IO_L24N_5	IO_L24N_5	AG13	I/O
5	IO_L24P_5	IO_L24P_5	AF13	I/O
5	IO_L25N_5	IO_L25N_5	AK13	I/O
5	IO_L25P_5	IO_L25P_5	AJ13	I/O
5	IO_L26N_5	IO_L26N_5	AB14	I/O
5	IO_L26P_5	IO_L26P_5	AA14	I/O

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	GND	GND	J22	GND
N/A	GND	GND	J30	GND
N/A	GND	GND	J34	GND
N/A	GND	GND	J5	GND
N/A	GND	GND	K10	GND
N/A	GND	GND	K25	GND
N/A	GND	GND	L3	GND
N/A	GND	GND	L32	GND
N/A	GND	GND	N1	GND
N/A	GND	GND	N17	GND
N/A	GND	GND	N18	GND
N/A	GND	GND	N26	GND
N/A	GND	GND	N30	GND
N/A	GND	GND	N34	GND
N/A	GND	GND	N5	GND
N/A	GND	GND	N9	GND
N/A	GND	GND	P14	GND
N/A	GND	GND	P15	GND
N/A	GND	GND	P16	GND
N/A	GND	GND	P17	GND
N/A	GND	GND	P18	GND
N/A	GND	GND	P19	GND
N/A	GND	GND	P20	GND
N/A	GND	GND	P21	GND
N/A	GND	GND	R14	GND
N/A	GND	GND	R15	GND
N/A	GND	GND	R16	GND
N/A	GND	GND	R17	GND
N/A	GND	GND	R18	GND
N/A	GND	GND	R19	GND
N/A	GND	GND	R20	GND
N/A	GND	GND	R21	GND
N/A	GND	GND	T1	GND
N/A	GND	GND	T14	GND
N/A	GND	GND	T15	GND
N/A	GND	GND	T16	GND
N/A	GND	GND	T17	GND
N/A	GND	GND	T18	GND
N/A	GND	GND	T19	GND
N/A	GND	GND	T20	GND

Table 110: **FG1156 Package Pinout *(Cont'd)***

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	VCCAUX	VCCAUX	Y5	VCCAUX
N/A	VCCINT	VCCINT	AA13	VCCINT
N/A	VCCINT	VCCINT	AA22	VCCINT
N/A	VCCINT	VCCINT	AB13	VCCINT
N/A	VCCINT	VCCINT	AB14	VCCINT
N/A	VCCINT	VCCINT	AB15	VCCINT
N/A	VCCINT	VCCINT	AB16	VCCINT
N/A	VCCINT	VCCINT	AB19	VCCINT
N/A	VCCINT	VCCINT	AB20	VCCINT
N/A	VCCINT	VCCINT	AB21	VCCINT
N/A	VCCINT	VCCINT	AB22	VCCINT
N/A	VCCINT	VCCINT	AC12	VCCINT
N/A	VCCINT	VCCINT	AC17	VCCINT
N/A	VCCINT	VCCINT	AC18	VCCINT
N/A	VCCINT	VCCINT	AC23	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	M23	VCCINT
N/A	VCCINT	VCCINT	N13	VCCINT
N/A	VCCINT	VCCINT	N14	VCCINT
N/A	VCCINT	VCCINT	N15	VCCINT
N/A	VCCINT	VCCINT	N16	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	N20	VCCINT
N/A	VCCINT	VCCINT	N21	VCCINT
N/A	VCCINT	VCCINT	N22	VCCINT
N/A	VCCINT	VCCINT	P13	VCCINT
N/A	VCCINT	VCCINT	P22	VCCINT
N/A	VCCINT	VCCINT	R13	VCCINT
N/A	VCCINT	VCCINT	R22	VCCINT
N/A	VCCINT	VCCINT	T13	VCCINT
N/A	VCCINT	VCCINT	T22	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT
N/A	VCCINT	VCCINT	U23	VCCINT
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	V23	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	W22	VCCINT
N/A	VCCINT	VCCINT	Y13	VCCINT