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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 896 |
| Number of Logic Elements/Cells | 8064 |
| Total RAM Bits | 294912 |
| Number of I/O | 97 |
| Number of Gates | 400000 |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc3s400-4tq144i |

According to Figure 7, the clock line OTCLK1 connects the CK inputs of the upper registers on the output and three-state paths. Similarly, OTCLK2 connects the CK inputs for the lower registers on the output and three-state paths. The upper and lower registers on the input path have independent clock lines: ICLK1 and ICLK2. The enable line OCE connects the CE inputs of the upper and lower registers on the output path. Similarly, TCE connects the CE inputs for the register pair on the three-state path and ICE does the same for the register pair on the input path. The Set/Reset (SR) line entering the IOB is common to all six registers, as is the Reverse (REV) line.

Each storage element supports numerous options in addition to the control over signal polarity described in the IOB Overview section. These are described in Table 6.

*Table 6:* **Storage Element Options**

| Option Switch | Function | Specificity |
|---|---|---|
| FF/Latch | Chooses between an edge-sensitive flip-flop or a level-sensitive latch | Independent for each storage element. |
| SYNC/ASYNC | Determines whether SR is synchronous or asynchronous | Independent for each storage element. |
| SRHIGH/SRLOW | Determines whether SR acts as a Set, which forces the storage element to a logic “1" (SRHIGH) or a Reset, which forces a logic “0” (SRLOW). | Independent for each storage element, except when using FDDR. In the latter case, the selection for the upper element (OFF1 or TFF2) applies to both elements. |
| INIT1/INIT0 | In the event of a Global Set/Reset, after configuration or upon activation of the GSR net, this switch decides whether to set or reset a storage element. By default, choosing SRLOW also selects INIT0; choosing SRHIGH also selects INIT1. | Independent for each storage element, except when using FDDR. In the latter case, selecting INIT0 for one element applies to both elements (even though INIT1 is selected for the other). |

## Double-Data-Rate Transmission

Double-Data-Rate (DDR) transmission describes the technique of synchronizing signals to both the rising and falling edges of the clock signal. Spartan-3 devices use register-pairs in all three IOB paths to perform DDR operations.

The pair of storage elements on the IOB’s Output path (OFF1 and OFF2), used as registers, combine with a special multiplexer to form a DDR D-type flip-flop (FDDR). This primitive permits DDR transmission where output data bits are synchronized to both the rising and falling edges of a clock. It is possible to access this function by placing either an FDDRRSE or an FDDRCPE component or symbol into the design. DDR operation requires two clock signals (50% duty cycle), one the inverted form of the other. These signals trigger the two registers in alternating fashion, as shown in Figure 8. Commonly, the Digital Clock Manager (DCM) generates the two clock signals by mirroring an incoming signal, then shifting it 180 degrees. This approach ensures minimal skew between the two signals.

The storage-element-pair on the Three-State path (TFF1 and TFF2) can also be combined with a local multiplexer to form an FDDR primitive. This permits synchronizing the output enable to both the rising and falling edges of a clock. This DDR operation is realized in the same way as for the output path.

The storage-element-pair on the input path (IFF1 and IFF2) allows an I/O to receive a DDR signal. An incoming DDR clock signal triggers one register and the inverted clock signal triggers the other register. In this way, the registers take turns capturing bits of the incoming DDR data signal.

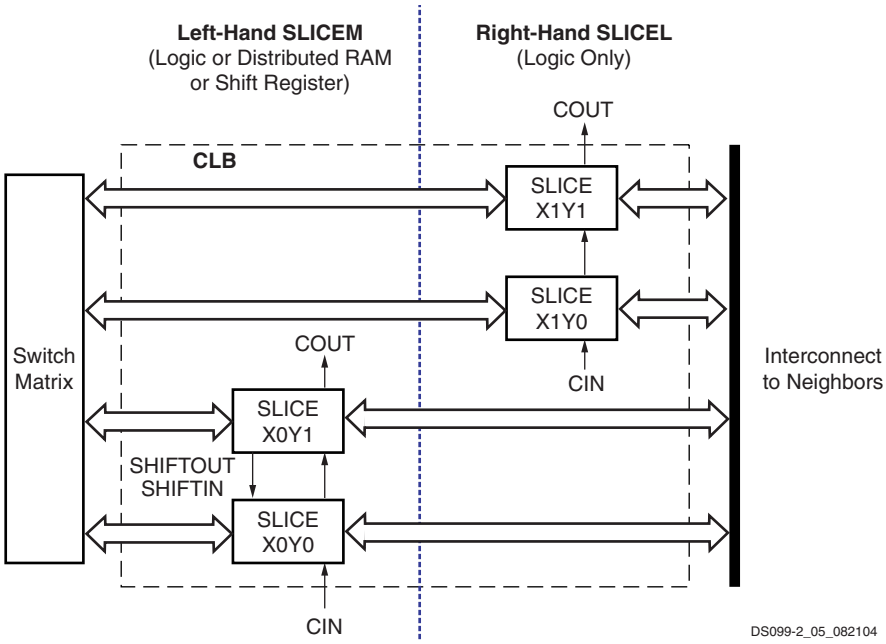


*Figure 11:* **Arrangement of Slices within the CLB**

## Elements Within a Slice

All four slices have the following elements in common: two logic function generators, two storage elements, wide-function multiplexers, carry logic, and arithmetic gates, as shown in Figure 12, page 24. Both the left-hand and right-hand slice pairs use these elements to provide logic, arithmetic, and ROM functions. Besides these, the left-hand pair supports two additional functions: storing data using Distributed RAM and shifting data with 16-bit registers. Figure 12 is a diagram of the left-hand slice; therefore, it represents a superset of the elements and connections to be found in all slices. See Function Generator, page 25 for more information.

The RAM-based function generator—also known as a Look-Up Table or LUT—is the main resource for implementing logic functions. Furthermore, the LUTs in each left-hand slice pair can be configured as Distributed RAM or a 16-bit shift register. For information on the former, refer to the chapter entitled “Using Look-Up Tables as Distributed RAM” in UG331; for information on the latter, refer to the chapter entitled “Using Look-Up Tables as Shift Registers” in UG331. The function generators located in the upper and lower portions of the slice are referred to as the "G" and "F", respectively.

The storage element, which is programmable as either a D-type flip-flop or a level-sensitive latch, provides a means for synchronizing data to a clock signal, among other uses. The storage elements in the upper and lower portions of the slice are called FFY and FFX, respectively.

Wide-function multiplexers effectively combine LUTs in order to permit more complex logic operations. Each slice has two of these multiplexers with F5MUX in the lower portion of the slice and FiMUX in the upper portion. Depending on the slice, FiMUX takes on the name F6MUX, F7MUX, or F8MUX. For more details on the multiplexers, refer to the chapter entitled “Using Dedicated Multiplexers” in UG331.

The carry chain, together with various dedicated arithmetic logic gates, support fast and efficient implementations of math operations. The carry chain enters the slice as CIN and exits as COUT. Five multiplexers control the chain: CYINIT, CY0F, and CYMUXF in the lower portion as well as CY0G and CYMUXG in the upper portion. The dedicated arithmetic logic includes the exclusive-OR gates XORG and XORF (upper and lower portions of the slice, respectively) as well as the AND gates GAND and FAND (upper and lower portions, respectively). For more details on the carry logic, refer to the chapter entitled “Using Carry and Arithmetic Logic” in UG331.

## Main Logic Paths

Central to the operation of each slice are two nearly identical data paths, distinguished using the terms *top* and *bottom*. The description that follows uses names associated with the bottom path. (The top path names appear in parentheses.) The basic path originates at an interconnect-switch matrix outside the CLB. Four lines, F1 through F4 (or G1 through G4 on the

*Table 22:* **Status Logic Signals**

| Signal | Direction | Description |
|---|---|---|
| RST | Input | A High resets the entire DCM to its initial power-on state. Initializes the DLL taps for a delay of zero. Sets the LOCKED output Low. This input is asynchronous. |
| STATUS[7:0] | Output | The bit values on the STATUS bus provide information regarding the state of DLL and PS operation |
| LOCKED | Output | Indicates that the CLKIN and CLKFB signals are in phase by going High. The two signals are out-of-phase when Low. |

*Table 23:* **DCM STATUS Bus**

| Bit | Name | Description |
|---|---|---|
| 0 | Phase Shift Overflow | A value of 1 indicates a phase shift overflow when one of two conditions occurs:<br>Incrementing (or decrementing) TPS beyond 255/256 of a CLKIN cycle.<br>The DLL is producing its maximum possible phase shift (i.e., all delay taps are active).(1) |
| 1 | CLKIN Input Stopped Toggling | A value of 1 indicates that the CLKIN input signal is not toggling. A value of 0 indicates toggling. This bit functions only when the CLKFB input is connected.(2) |
| 2 | CLKFX/CLKFX180 Output Stopped Toggling | A value of 1 indicates that the CLKFX or CLKFX180 output signals are not toggling. A value of 0 indicates toggling. This bit functions only when using the Digital Frequency Synthesizer (DFS). |
| 3:7 | Reserved | – |

**Notes:**

1. The DLL phase shift with all delay taps active is specified as the parameter FINE_SHIFT_RANGE.
2. If only the DFS clock outputs are used, but none of the DLL clock outputs, this bit will not go High when the CLKIN signal stops.

*Table 24:* **Status Attributes**

| Attribute | Description | Values |
|---|---|---|
| STARTUP_WAIT | Delays transition from configuration to user mode until lock condition is achieved. | TRUE, FALSE |

### Stabilizing DCM Clocks Before User Mode

It is possible to delay the completion of device configuration until after the DLL has achieved a lock condition using the STARTUP_WAIT attribute described in Table 24. This option ensures that the FPGA does not enter user mode—i.e., begin functional operation—until all system clocks generated by the DCM are stable. In order to achieve the delay, it is necessary to set the attribute to TRUE as well as set the BitGen option LCK_cycle to one of the six cycles making up the Startup phase of configuration. The selected cycle defines the point at which configuration will halt until the LOCKED output goes High.

## Global Clock Network

Spartan-3 devices have eight Global Clock inputs called GCLK0 - GCLK7. These inputs provide access to a low-capacitance, low-skew network that is well-suited to carrying high-frequency signals. The Spartan-3 FPGAs clock network is shown in Figure 23. GCLK0 through GCLK3 are located in the center of the bottom edge. GCLK4 through GCLK7 are located in the center of the top edge.

Eight Global Clock Multiplexers (also called BUFGMUX elements) are provided that accept signals from Global Clock inputs and route them to the internal clock network as well as DCMs. Four BUFGMUX elements are located in the center of the bottom edge, just above the GCLK0 - GCLK3 inputs. The remaining four BUFGMUX elements are located in the center of the top edge, just below the GCLK4 - GCLK7 inputs.

Pairs of BUFGMUX elements share global inputs, as shown in Figure 24. For example, the GCLK4 and GCLK5 inputs both potentially connect to BUFGMUX4 and BUFGMUX5 located in the upper right center. A differential clock input uses a pair of GCLK inputs to connect to a single BUFGMUX element.

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*Table 33:* **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**

| Symbol | Description | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $I_L$ (2)(4) | Leakage current at User I/O, Dual-Purpose, and Dedicated pins | Driver is Hi-Z, $V_{IN}$ = 0V or $V_{CCO}$ max, sample-tested | $V_{CCO} \geq 3.0V$ | – | - | ±25 | µA |
| | | | $V_{CCO} < 3.0V$ | – | - | ±10 | µA |
| $I_{RPU}$ (3) | Current through pull-up resistor at User I/O, Dual-Purpose, and Dedicated pins | $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V | | –0.84 | - | –2.35 | mA |
| | | $V_{IN}$ = 0V, $V_{CCO}$ = 3.0V | | –0.69 | - | –1.99 | mA |
| | | $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V | | –0.47 | - | –1.41 | mA |
| | | $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | | –0.21 | - | –0.69 | mA |
| | | $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | | –0.13 | - | –0.43 | mA |
| | | $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | | –0.06 | - | –0.22 | mA |
| $R_{PU}$ (3) | Equivalent resistance of pull-up resistor at User I/O, Dual-Purpose, and Dedicated pins, derived from $I_{RPU}$ | $V_{CCO}$ = 3.0V to 3.465V | | 1.27 | - | 4.11 | kΩ |
| | | $V_{CCO}$ = 2.3V to 2.7V | | 1.15 | - | 3.25 | kΩ |
| | | $V_{CCO}$ = 1.7V to 1.9V | | 2.45 | - | 9.10 | kΩ |
| | | $V_{CCO}$ = 1.4V to 1.6V | | 3.25 | - | 12.10 | kΩ |
| | | $V_{CCO}$ = 1.14 to 1.26V | | 5.15 | - | 21.00 | kΩ |
| $I_{RPD}$ (3) | Current through pull-down resistor at User I/O, Dual-Purpose, and Dedicated pins | $V_{IN} = V_{CCO}$ | | 0.37 | - | 1.67 | mA |
| $R_{PD}$ (3) | Equivalent resistance of pull-down resistor at User I/O, Dual-Purpose, and Dedicated pins, driven from $I_{RPD}$ | $V_{IN} = V_{CCO}$ = 3.0V to 3.465V | | 1.75 | - | 9.35 | kΩ |
| | | $V_{IN} = V_{CCO}$ = 2.3V to 2.7V | | 1.35 | - | 7.30 | kΩ |
| | | $V_{IN} = V_{CCO}$ = 1.7V to 1.9V | | 1.00 | - | 5.15 | kΩ |
| | | $V_{IN} = V_{CCO}$ = 1.4V to 1.6V | | 0.85 | - | 4.35 | kΩ |
| | | $V_{IN} = V_{CCO}$ = 1.14 to 1.26V | | 0.68 | - | 3.465 | kΩ |
| $R_{DCI}$ | Value of external reference resistor to support DCI I/O standards | | | 20 | - | 100 | Ω |
| $I_{REF}$ | $V_{REF}$ current per pin | $V_{CCO} \geq 3.0V$ | | – | - | ±25 | µA |
| | | $V_{CCO} < 3.0V$ | | – | - | ±10 | µA |
| $C_{IN}$ | Input capacitance | | | 3 | - | 10 | pF |

**Notes:**

1. The numbers in this table are based on the conditions set forth in Table 32.
2. The $I_L$ specification applies to every I/O pin throughout power-on as long as the voltage on that pin stays between the absolute $V_{IN}$ minimum and maximum values (Table 28). For hot-swap applications, at the time of card connection, be sure to keep all I/O voltages within this range before applying $V_{CCO}$ power. Consider applying $V_{CCO}$ power before connecting the signal lines, to avoid turning on the ESD protection diodes, shown in Module 2: Figure 7, page 11. When the FPGA is completely unpowered, the I/O pins are high impedance, but there is a path through the upper and lower ESD protection diodes.
3. This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPU}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$. Spartan-3 family values for both resistances are stronger than they have been for previous FPGA families.
4. For single-ended signals that are placed on a differential-capable I/O, $V_{IN}$ of –0.2V to –0.3V is supported but can cause increased leakage between the two pins. See the *Parasitic Leakage* section in UG331, *Spartan-3 Generation FPGA User Guide*.

*Table 35:* **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

| Signal Standard (IOSTANDARD) | $V_{CCO}$ | | | $V_{REF}$ | | | $V_{IL}$ | $V_{IH}$ |
|---|---|---|---|---|---|---|---|---|
| | Min (V) | Nom (V) | Max (V) | Min (V) | Nom (V) | Max (V) | Max (V) | Min (V) |
| GTL[3] | – | – | – | 0.74 | 0.8 | 0.86 | $V_{REF}$ – 0.05 | $V_{REF}$ + 0.05 |
| GTL_DCI | – | 1.2 | – | 0.74 | 0.8 | 0.86 | $V_{REF}$ – 0.05 | $V_{REF}$ + 0.05 |
| GTLP[3] | – | – | – | 0.88 | 1 | 1.12 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 |
| GTLP_DCI | – | 1.5 | – | 0.88 | 1 | 1.12 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 |
| HSLVDCI_15 | 1.4 | 1.5 | 1.6 | – | 0.75 | – | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 |
| HSLVDCI_18 | 1.7 | 1.8 | 1.9 | – | 0.9 | – | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 |
| HSLVDCI_25 | 2.3 | 2.5 | 2.7 | – | 1.25 | – | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 |
| HSLVDCI_33 | 3.0 | 3.3 | 3.465 | – | 1.65 | – | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 |
| HSTL_I, HSTL_I_DCI | 1.4 | 1.5 | 1.6 | 0.68 | 0.75 | 0.9 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 |
| HSTL_III, HSTL_III_DCI | 1.4 | 1.5 | 1.6 | – | 0.9 | – | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 |
| HSTL_I_18, HSTL_I_DCI_18 | 1.7 | 1.8 | 1.9 | 0.8 | 0.9 | 1.1 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 |
| HSTL_II_18, HSTL_II_DCI_18 | 1.7 | 1.8 | 1.9 | – | 0.9 | – | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 |
| HSTL_III_18, HSTL_III_DCI_18 | 1.7 | 1.8 | 1.9 | – | 1.1 | – | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 |
| LVCMOS12 | 1.14 | 1.2 | 1.3 | – | – | – | $0.37V_{CCO}$ | $0.58V_{CCO}$ |
| LVCMOS15, LVDCI_15, LVDCI_DV2_15 | 1.4 | 1.5 | 1.6 | – | – | – | $0.30V_{CCO}$ | $0.70V_{CCO}$ |
| LVCMOS18, LVDCI_18, LVDCI_DV2_18 | 1.7 | 1.8 | 1.9 | – | – | – | $0.30V_{CCO}$ | $0.70V_{CCO}$ |
| LVCMOS25[4,5], LVDCI_25, LVDCI_DV2_25[4] | 2.3 | 2.5 | 2.7 | – | – | – | 0.7 | 1.7 |
| LVCMOS33, LVDCI_33, LVDCI_DV2_33[4] | 3.0 | 3.3 | 3.465 | – | – | – | 0.8 | 2.0 |
| LVTTL | 3.0 | 3.3 | 3.465 | – | – | – | 0.8 | 2.0 |
| PCI33_3[7] | 3.0 | 3.3 | 3.465 | – | – | – | $0.30V_{CCO}$ | $0.50V_{CCO}$ |
| SSTL18_I, SSTL18_I_DCI | 1.7 | 1.8 | 1.9 | 0.833 | 0.900 | 0.969 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 |
| SSTL18_II | 1.7 | 1.8 | 1.9 | 0.833 | 0.900 | 0.969 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 |
| SSTL2_I, SSTL2_I_DCI | 2.3 | 2.5 | 2.7 | 1.15 | 1.25 | 1.35 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 |
| SSTL2_II, SSTL2_II_DCI | 2.3 | 2.5 | 2.7 | 1.15 | 1.25 | 1.35 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 |

**Notes:**

1. Descriptions of the symbols used in this table are as follows:
   $V_{CCO}$ – the supply voltage for output drivers as well as LVCMOS, LVTTL, and PCI inputs
   $V_{REF}$ – the reference voltage for setting the input switching threshold
   $V_{IL}$ – the input voltage that indicates a Low logic level
   $V_{IH}$ – the input voltage that indicates a High logic level
2. For device operation, the maximum signal voltage ($V_{IH}$ max) may be as high as $V_{IN}$ max. See Table 28.
3. Because the GTL and GTLP standards employ open-drain output buffers, $V_{CCO}$ lines do not supply current to the I/O circuit, rather this current is provided using an external pull-up resistor connected from the I/O pin to a termination voltage ($V_{TT}$). Nevertheless, the voltage applied to the associated $V_{CCO}$ lines must always be at or above $V_{TT}$ and I/O pad voltages.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS25 or LVCMOS33 standards.
5. All dedicated pins (M0-M2, CCLK, PROG_B, DONE, HSWAP_EN, TCK, TDI, TDO, and TMS) use the LVCMOS standard and draw power from the $V_{CCAUX}$ rail (2.5V). The dual-purpose configuration pins (DIN/D0, D1-D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B) use the LVCMOS standard before the user mode. For these pins, apply 2.5V to the $V_{CCO}$ Bank 4 and $V_{CCO}$ Bank 5 rails at power-on and throughout configuration. For information concerning the use of 3.3V signals, see 3.3V-Tolerant Configuration Interface, page 47.
6. The Global Clock Inputs (GCLK0-GCLK7) are dual-purpose pins to which any signal standard can be assigned.
7. For more information, see XAPP457.

*Table 41:* **System-Synchronous Pin-to-Pin Setup and Hold Times for the IOB Input Path**

| Symbol | Description | Conditions | Device | Speed Grade | | Units |
|---|---|---|---|---|---|---|
| | | | | -5 | -4 | |
| | | | | Min | Min | |
| **Setup Times** | | | | | | |
| $T_{PSDCM}$ | When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed. | LVCMOS25(2), IOBDELAY = NONE, with DCM(4) | XC3S50 | 2.37 | 2.71 | ns |
| | | | XC3S200 | 2.13 | 2.35 | ns |
| | | | XC3S400 | 2.15 | 2.36 | ns |
| | | | XC3S1000 | 2.58 | 2.95 | ns |
| | | | XC3S1500 | 2.55 | 2.91 | ns |
| | | | XC3S2000 | 2.59 | 2.96 | ns |
| | | | XC3S4000 | 2.76 | 3.15 | ns |
| | | | XC3S5000 | 2.69 | 3.08 | ns |
| $T_{PSFD}$ | When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed. | LVCMOS25(2), IOBDELAY = IFD, without DCM | XC3S50 | 3.00 | 3.46 | ns |
| | | | XC3S200 | 2.63 | 3.02 | ns |
| | | | XC3S400 | 2.50 | 2.87 | ns |
| | | | XC3S1000 | 3.50 | 4.03 | ns |
| | | | XC3S1500 | 3.78 | 4.35 | ns |
| | | | XC3S2000 | 4.98 | 5.73 | ns |
| | | | XC3S4000 | 5.25 | 6.05 | ns |
| | | | XC3S5000 | 5.37 | 6.18 | ns |
| **Hold Times** | | | | | | |
| $T_{PHDCM}$ | When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed. | LVCMOS25(3), IOBDELAY = NONE, with DCM(4) | XC3S50 | –0.45 | –0.40 | ns |
| | | | XC3S200 | –0.12 | –0.05 | ns |
| | | | XC3S400 | –0.12 | –0.05 | ns |
| | | | XC3S1000 | –0.43 | –0.38 | ns |
| | | | XC3S1500 | –0.45 | –0.40 | ns |
| | | | XC3S2000 | –0.47 | –0.42 | ns |
| | | | XC3S4000 | –0.61 | –0.56 | ns |
| | | | XC3S5000 | –0.62 | –0.57 | ns |

*Table 50:* **Recommended Number of Simultaneously Switching Outputs per $V_{CCO}$/GND Pair *(Cont'd)***

| Signal Standard (IOSTANDARD) | | | Package | | | | |
|---|---|---|---|---|---|---|---|
| | | | VQ100 | TQ144 | PQ208 | CP132 | FT256, FG320, FG456, FG676, FG900, FG1156 |
| LVCMOS33 | Slow | 2 | 34 | 24 | 24 | 52 | 76 |
| | | 4 | 17 | 14 | 14 | 26 | 46 |
| | | 6 | 17 | 11 | 11 | 26 | 27 |
| | | 8 | 10 | 10 | 10 | 13 | 20 |
| | | 12 | 9 | 9 | 9 | 13 | 13 |
| | | 16 | 8 | 8 | 8 | 8 | 10 |
| | | 24 | 8 | 8 | 8 | 8 | 9 |
| | Fast | 2 | 20 | 20 | 20 | 26 | 44 |
| | | 4 | 15 | 15 | 15 | 15 | 26 |
| | | 6 | 11 | 11 | 11 | 13 | 16 |
| | | 8 | 10 | 10 | 10 | 10 | 12 |
| | | 12 | 8 | 8 | 8 | 8 | 10 |
| | | 16 | 8 | 8 | 8 | 8 | 8 |
| | | 24 | 7 | 7 | 7 | 7 | 7 |
| LVDCI_33 | | | 10 | 10 | 10 | 10 | 10 |
| LVDCI_DV2_33 | | | 10 | 10 | 10 | 10 | 10 |
| HSLVDCI_33 | | | 10 | 10 | 10 | 10 | 10 |
| LVTTL | Slow | 2 | 34 | 25 | 25 | 52 | 60 |
| | | 4 | 17 | 16 | 16 | 26 | 41 |
| | | 6 | 17 | 15 | 15 | 26 | 29 |
| | | 8 | 12 | 12 | 12 | 13 | 22 |
| | | 12 | 10 | 10 | 10 | 13 | 13 |
| | | 16 | 10 | 10 | 10 | 10 | 11 |
| | | 24 | 8 | 8 | 8 | 8 | 9 |
| | Fast | 2 | 20 | 20 | 20 | 26 | 34 |
| | | 4 | 13 | 13 | 13 | 13 | 20 |
| | | 6 | 11 | 11 | 11 | 13 | 15 |
| | | 8 | 10 | 10 | 10 | 10 | 12 |
| | | 12 | 9 | 9 | 9 | 9 | 10 |
| | | 16 | 8 | 8 | 8 | 8 | 9 |
| | | 24 | 7 | 7 | 7 | 7 | 7 |

*Table 59:* **Switching Characteristics for the DLL *(Cont'd)***

| Symbol | Description | Frequency Mode / FCLKIN Range | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | -5 | | -4 | | |
| | | | | Min | Max | Min | Max | |
| **Lock Time** | | | | | | | | |
| LOCK_DLL | When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase | 18 MHz ≤ $F_{CLKIN}$ ≤ 30 MHz | All | – | 2.88 | – | 2.88 | ms |
| | | 30 MHz < $F_{CLKIN}$ ≤ 40 MHz | | – | 2.16 | – | 2.16 | ms |
| | | 40 MHz < $F_{CLKIN}$ ≤ 50 MHz | | – | 1.20 | – | 1.20 | ms |
| | | 50 MHz < $F_{CLKIN}$ ≤ 60 MHz | | – | 0.60 | – | 0.60 | ms |
| | | $F_{CLKIN}$ > 60 MHz | | – | 0.48 | – | 0.48 | ms |
| **Delay Lines** | | | | | | | | |
| DCM_TAP | Delay tap resolution | All | All | 30.0 | 60.0 | 30.0 | 60.0 | ps |

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 32 and Table 58.
2. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
3. Only mask revision 'E' and later devices (see Mask and Fab Revisions, page 58) and all revisions of the XC3S50 and the XC3S1000 support DLL feedback using the CLK2X output. For all other Spartan-3 devices, use feedback from the CLK0 output (instead of the CLK2X output) and set the CLK_FEEDBACK attribute to 1X.
4. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
5. This specification only applies if the attribute DUTY_CYCLE_CORRECTION = TRUE.

## Digital Frequency Synthesizer (DFS)

*Table 60:* **Recommended Operating Conditions for the DFS**

| Symbol | | Description | Frequency Mode | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | -5 | | -4 | | |
| | | | | Min | Max | Min | Max | |
| **Input Frequency Ranges**(2) | | | | | | | | |
| $F_{CLKIN}$ | CLKIN_FREQ_FX | Frequency for the CLKIN input | All | 1 | 280 | 1 | 280 | MHz |
| **Input Clock Jitter Tolerance**(3) | | | | | | | | |
| CLKIN_CYC_JITT_FX_LF | | Cycle-to-cycle jitter at the CLKIN input | Low | – | ±300 | – | ±300 | ps |
| CLKIN_CYC_JITT_FX_HF | | | High | – | ±150 | – | ±150 | ps |
| CLKIN_PER_JITT_FX | | Period jitter at the CLKIN input | All | – | ±1 | – | ±1 | ns |

**Notes:**

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 58.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.

*Table 71:* **Dual-Purpose Pins Used in Master or Slave Serial Mode**

| Pin Name | Direction | Description |
|---|---|---|
| DIN | Input | **Serial Data Input:**<br>During the Master or Slave Serial configuration modes, DIN is the serial configuration data input, and all data is synchronized to the rising CCLK edge. After configuration, this pin is available as a user I/O.<br>This signal is located in Bank 4 and its output voltage determined by VCCO_4.<br>The BitGen option ***Persist*** permits this pin to retain its configuration function in the User mode. |
| DOUT | Output | **Serial Data Output:**<br>In a multi-FPGA design where all the FPGAs use serial mode, connect the DOUT output of one FPGA—in either Master or Slave Serial mode—to the DIN input of the next FPGA—in Slave Serial mode—so that configuration data passes from one to the next, in daisy-chain fashion. This "daisy chain" permits sequential configuration of multiple FPGAs.<br>This signal is located in Bank 4 and its output voltage determined by VCCO_4.<br>The BitGen option ***Persist*** permits this pin to retain its configuration function in the User mode. |
| INIT_B | Bidirectional (open-drain) | **Initializing Configuration Memory/Configuration Error:**<br>Just after power is applied, the FPGA produces a Low-to-High transition on this pin indicating that initialization (*i.e.*, clearing) of the configuration memory has finished. Before entering the User mode, this pin functions as an open-drain output, which requires a pull-up resistor in order to produce a High logic level. In a multi-FPGA design, tie (wire AND) the INIT_B pins from all FPGAs together so that the common node transitions High only after all of the FPGAs have been successfully initialized.<br>Externally holding this pin Low beyond the initialization phase delays the start of configuration. This action stalls the FPGA at the configuration step just before the mode select pins are sampled.<br>During configuration, the FPGA indicates the occurrence of a data (i.e., CRC) error by asserting INIT_B Low.<br>This signal is located in Bank 4 and its output voltage determined by VCCO_4.<br>The BitGen option ***Persist*** permits this pin to retain its configuration function in the User mode. |

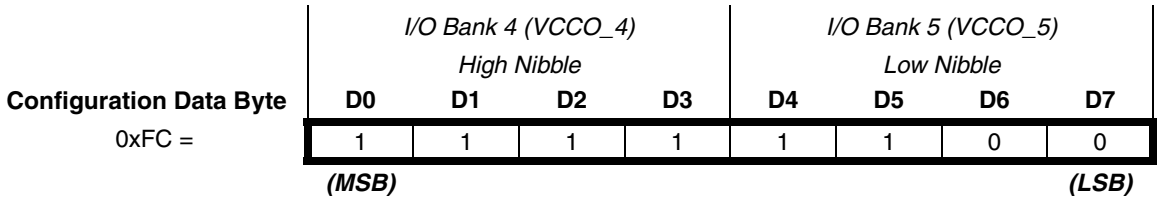


*Figure 41:* **Configuration Data Byte Mapping to D0-D7 Bits**

## Parallel Configuration Modes (SelectMAP)

This section describes the dual-purpose configuration pins used during the Master and Slave Parallel configuration modes, sometimes also called the SelectMAP modes. In both Master and Slave Parallel configuration modes, D0-D7 form the byte-wide configuration data input. See Table 75 for Mode Select pin settings required for Parallel modes.

As shown in Figure 41, D0 is the most-significant bit while D7 is the least-significant bit. Bits D0-D3 form the high nibble of the byte and bits D4-D7 form the low nibble.

In the Parallel configuration modes, both the VCCO_4 and VCCO_5 voltage supplies are required and must both equal the voltage of the attached configuration device, typically either 2.5V or 3.3V.

Assert Low both the chip-select pin, CS_B, and the read/write control pin, RDWR_B, to write the configuration data byte presented on the D0-D7 pins to the FPGA on a rising-edge of the configuration clock, CCLK. The order of CS_B and RDWR_B does not matter, although RDWR_B must be asserted throughout the configuration process. If RDWR_B is de-asserted during configuration, the FPGA aborts the configuration operation.

After configuration, these pins are available as general-purpose user I/O. However, the SelectMAP configuration interface is optionally available for debugging and dynamic reconfiguration. To use these SelectMAP pins after configuration, set the Persist bitstream generation option.

The Readback debugging option, for example, requires the Persist bitstream generation option. During Readback mode, assert CS_B Low, along with RDWR_B High, to read a configuration data byte from the FPGA to the D0-D7 bus on a rising CCLK edge. During Readback mode, D0-D7 are output pins.

In all the cases, the configuration data and control signals are synchronized to the rising edge of the CCLK clock signal.

*Table 72:* **Dual-Purpose Configuration Pins for Parallel (SelectMAP) Configuration Modes *(Cont'd)***

<table>
<tr><th>Pin Name</th><th>Direction</th><th>Description</th></tr>
<tr><td>BUSY</td><td>Output</td><td>Configuration Data Rate Control for Parallel Mode:<br>In the Slave and Master Parallel modes, BUSY throttles the rate at which configuration data is loaded. BUSY is only necessary if CCLK operates at greater than 50 MHz. Ignore BUSY for frequencies of 50 MHz and below.<br>When BUSY is Low, the FPGA accepts the next configuration data byte on the next rising CCLK edge for which CS_B and RDWR_B are Low. When BUSY is High, the FPGA ignores the next configuration data byte. The next configuration data value must be held or reloaded until the next rising CCLK edge when BUSY is Low. When CS_B is High, BUSY is in a high impedance state.<br><table><tr><th>BUSY</th><th>Function</th></tr><tr><td>0</td><td>The FPGA is ready to accept the next configuration data byte.</td></tr><tr><td>1</td><td>The FPGA is busy processing the current configuration data byte and is not ready to accept the next byte.</td></tr><tr><td>Hi-Z</td><td>If CS_B is High, then BUSY is high impedance.</td></tr></table>This signal is located in Bank 4 and its output voltage is determined by VCCO_4. The BitGen option Persist permits this pin to retain its configuration function in the User mode.</td></tr>
<tr><td>INIT_B</td><td>Bidirectional (open-drain)</td><td>Initializing Configuration Memory/Configuration Error (active-Low):<br>See description under Serial Configuration Modes, page 112.</td></tr>
</table>

### JTAG Configuration Mode

In the JTAG configuration mode all dual-purpose configuration pins are unused and behave exactly like user-I/O pins, as shown in Table 79. See Table 75 for Mode Select pin settings required for JTAG mode.

### Dual-Purpose Pin I/O Standard During Configuration

During configuration, the dual-purpose pins default to CMOS input and output levels for the associated VCCO voltage supply pins. For example, in the Parallel configuration modes, both VCCO_4 and VCCO_5 are required. If connected to +2.5V, then the associated pins conform to the LVCMOS25 I/O standard. If connected to +3.3V, then the pins drive LVCMOS output levels and accept either LVTTL or LVCMOS input levels.

### Dual-Purpose Pin Behavior After Configuration

After the configuration process completes, these pins, if they were borrowed during configuration, become user-I/O pins available to the application. If a dual-purpose configuration pin is not used during the configuration process—*i.e.*, the parallel configuration pins when using serial mode—then the pin behaves exactly like a general-purpose I/O. See I/O Type: Unrestricted, General-purpose I/O Pins section.

## DCI: User I/O or Digitally Controlled Impedance Resistor Reference Input

These pins are individual user-I/O pins unless one of the I/O standards used in the bank requires the Digitally Controlled Impedance (DCI) feature. If DCI is used, then 1% precision resistors connected to the VRP_# and VRN_# pins match the impedance on the input or output buffers of the I/O standards that use DCI within the bank. The '#' character in the pin name indicates the associated I/O bank and is an integer, 0 through 7.

There are two DCI pins per I/O bank, except in the CP132 and TQ144 packages, which do not have any DCI inputs for Bank 5.

### VRP and VRN Impedance Resistor Reference Inputs

The 1% precision impedance-matching resistor attached to the VRP_# pin controls the pull-up impedance of PMOS transistor in the input or output buffer. Consequently, the VRP_# pin must connect to ground. The 'P' character in "VRP" indicates that this pin controls the I/O buffer's PMOS transistor impedance. The VRP_# pin is used for both single and split termination.

# CP132: 132-Ball Chip-Scale Package

**Note:** The CP132 and CPG132 packages are discontinued. See www.xilinx.com/support/documentation/spartan-3.htm#19600.

The pinout and footprint for the XC3S50 in the 132-ball chip-scale package, CP132, appear in Table 89 and Figure 45.

All the package pins appear in Table 89 and are sorted by bank number, then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The CP132 footprint has eight I/O banks. However, the voltage supplies for the two I/O banks along an edge are connected together internally. Consequently, there are four output voltage supplies, labeled VCCO_TOP, VCCO_RIGHT, VCCO_BOTTOM, and VCCO_LEFT.

## Pinout Table

*Table 89:* **CP132 Package Pinout**

| Bank | XC3S50 Pin Name | CP132 Ball | Type |
|---|---|---|---|
| 0 | IO_L01N_0/VRP_0 | A3 | DCI |
| 0 | IO_L01P_0/VRN_0 | C4 | DCI |
| 0 | IO_L27N_0 | C5 | I/O |
| 0 | IO_L27P_0 | B5 | I/O |
| 0 | IO_L30N_0 | B6 | I/O |
| 0 | IO_L30P_0 | A6 | I/O |
| 0 | IO_L31N_0 | C7 | I/O |
| 0 | IO_L31P_0/VREF_0 | B7 | VREF |
| 0 | IO_L32N_0/GCLK7 | A7 | GCLK |
| 0 | IO_L32P_0/GCLK6 | C8 | GCLK |
| 1 | IO_L01N_1/VRP_1 | A13 | DCI |
| 1 | IO_L01P_1/VRN_1 | B13 | DCI |
| 1 | IO_L27N_1 | C11 | I/O |
| 1 | IO_L27P_1 | A12 | I/O |
| 1 | IO_L28N_1 | A11 | I/O |
| 1 | IO_L28P_1 | B11 | I/O |
| 1 | IO_L31N_1/VREF_1 | C9 | VREF |
| 1 | IO_L31P_1 | A10 | I/O |
| 1 | IO_L32N_1/GCLK5 | A8 | GCLK |
| 1 | IO_L32P_1/GCLK4 | A9 | GCLK |
| 2 | IO_L01N_2/VRP_2 | D12 | DCI |
| 2 | IO_L01P_2/VRN_2 | C14 | DCI |
| 2 | IO_L20N_2 | E12 | I/O |
| 2 | IO_L20P_2 | E13 | I/O |
| 2 | IO_L21N_2 | E14 | I/O |
| 2 | IO_L21P_2 | F12 | I/O |
| 2 | IO_L23N_2/VREF_2 | F13 | VREF |
| 2 | IO_L23P_2 | F14 | I/O |
| 2 | IO_L24N_2 | G12 | I/O |

## User I/Os by Bank

Table 92 indicates how the available user-I/O pins are distributed between the eight I/O banks on the TQ144 package.

*Table 92:* **User I/Os Per Bank in TQ144 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | DUAL | DCI | VREF | GCLK |
| Top | 0 | 10 | 5 | 0 | 2 | 1 | 2 |
| | 1 | 9 | 4 | 0 | 2 | 1 | 2 |
| Right | 2 | 14 | 10 | 0 | 2 | 2 | 0 |
| | 3 | 15 | 11 | 0 | 2 | 2 | 0 |
| Bottom | 4 | 11 | 0 | 6 | 2 | 1 | 2 |
| | 5 | 9 | 0 | 6 | 0 | 1 | 2 |
| Left | 6 | 14 | 10 | 0 | 2 | 2 | 0 |
| | 7 | 15 | 11 | 0 | 2 | 2 | 0 |

## TQ144 Footprint

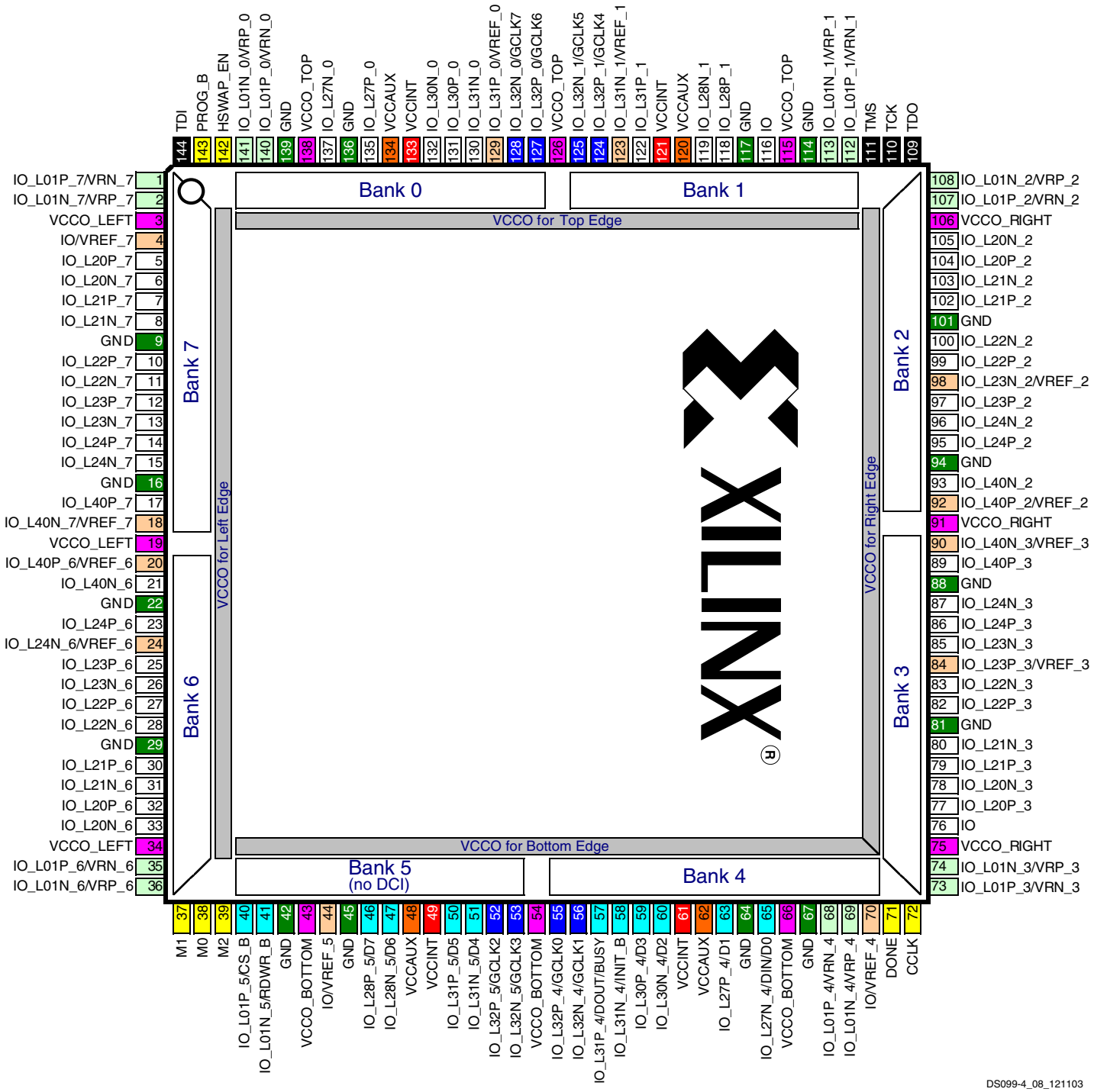


*Figure 46:* **TQ144 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

| | | |
|---|---|---|
| 51 **I/O:** Unrestricted, general-purpose user I/O | 12 **DUAL:** Configuration pin, then possible user I/O | 12 **VREF:** User I/O or input voltage reference for bank |
| 14 **DCI:** User I/O or reference resistor input for bank | 8 **GCLK:** User I/O or global clock buffer input | 12 **VCCO:** Output voltage supply for bank |
| 7 **CONFIG:** Dedicated configuration pins | 4 **JTAG:** Dedicated JTAG port pins | 4 **VCCINT:** Internal core voltage supply (+1.2V) |
| 0 **N.C.:** No unconnected pins in this package | 16 **GND:** Ground | 4 **VCCAUX:** Auxiliary voltage supply (+2.5V) |

*Table 100:* **FG456 Package Pinout *(Cont'd)***

| Bank | 3S400 Pin Name | 3S1000, 3S1500, 3S2000 Pin Name | FG456 Pin Number | Type |
|---|---|---|---|---|
| 6 | N.C. (◆) | IO_L28N_6 | R5 | I/O |
| 6 | N.C. (◆) | IO_L28P_6 | P6 | I/O |
| 6 | N.C. (◆) | IO_L29N_6 | R2 | I/O |
| 6 | N.C. (◆) | IO_L29P_6 | R1 | I/O |
| 6 | N.C. (◆) | IO_L31N_6 | P5 | I/O |
| 6 | N.C. (◆) | IO_L31P_6 | P4 | I/O |
| 6 | N.C. (◆) | IO_L32N_6 | P2 | I/O |
| 6 | N.C. (◆) | IO_L32P_6 | P1 | I/O |
| 6 | N.C. (◆) | IO_L33N_6 | N6 | I/O |
| 6 | N.C. (◆) | IO_L33P_6 | N5 | I/O |
| 6 | IO_L34N_6/VREF_6 | IO_L34N_6/VREF_6 | N4 | VREF |
| 6 | IO_L34P_6 | IO_L34P_6 | N3 | I/O |
| 6 | IO_L35N_6 | IO_L35N_6 | N2 | I/O |
| 6 | IO_L35P_6 | IO_L35P_6 | N1 | I/O |
| 6 | IO_L38N_6 | IO_L38N_6 | M6 | I/O |
| 6 | IO_L38P_6 | IO_L38P_6 | M5 | I/O |
| 6 | IO_L39N_6 | IO_L39N_6 | M4 | I/O |
| 6 | IO_L39P_6 | IO_L39P_6 | M3 | I/O |
| 6 | IO_L40N_6 | IO_L40N_6 | M2 | I/O |
| 6 | IO_L40P_6/VREF_6 | IO_L40P_6/VREF_6 | M1 | VREF |
| 6 | VCCO_6 | VCCO_6 | M7 | VCCO |
| 6 | VCCO_6 | VCCO_6 | N7 | VCCO |
| 6 | VCCO_6 | VCCO_6 | P7 | VCCO |
| 6 | VCCO_6 | VCCO_6 | R3 | VCCO |
| 6 | VCCO_6 | VCCO_6 | R6 | VCCO |
| 7 | IO | IO | C2 | I/O |
| 7 | IO_L01N_7/VRP_7 | IO_L01N_7/VRP_7 | C3 | DCI |
| 7 | IO_L01P_7/VRN_7 | IO_L01P_7/VRN_7 | C4 | DCI |
| 7 | IO_L16N_7 | IO_L16N_7 | D1 | I/O |
| 7 | IO_L16P_7/VREF_7 | IO_L16P_7/VREF_7 | C1 | VREF |
| 7 | IO_L17N_7 | IO_L17N_7 | E4 | I/O |
| 7 | IO_L17P_7 | IO_L17P_7 | D4 | I/O |
| 7 | IO_L19N_7/VREF_7 | IO_L19N_7/VREF_7 | D3 | VREF |
| 7 | IO_L19P_7 | IO_L19P_7 | D2 | I/O |
| 7 | IO_L20N_7 | IO_L20N_7 | F4 | I/O |
| 7 | IO_L20P_7 | IO_L20P_7 | E3 | I/O |
| 7 | IO_L21N_7 | IO_L21N_7 | E1 | I/O |
| 7 | IO_L21P_7 | IO_L21P_7 | E2 | I/O |
| 7 | IO_L22N_7 | IO_L22N_7 | G6 | I/O |
| 7 | IO_L22P_7 | IO_L22P_7 | F5 | I/O |

## User I/Os by Bank

Table 101 indicates how the available user-I/O pins are distributed between the eight I/O banks for the XC3S400 in the FG456 package. Similarly, Table 102 shows how the available user-I/O pins are distributed between the eight I/O banks for the XC3S1000, XC3S1500, and XC3S2000 in the FG456 package.

*Table 101:* **User I/Os Per Bank for XC3S400 in FG456 Package**

| Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | DUAL | DCI | VREF | GCLK |
| Top | 0 | 35 | 27 | 0 | 2 | 4 | 2 |
| | 1 | 35 | 27 | 0 | 2 | 4 | 2 |
| Right | 2 | 31 | 25 | 0 | 2 | 4 | 0 |
| | 3 | 31 | 25 | 0 | 2 | 4 | 0 |
| Bottom | 4 | 35 | 21 | 6 | 2 | 4 | 2 |
| | 5 | 35 | 21 | 6 | 2 | 4 | 2 |
| Left | 6 | 31 | 25 | 0 | 2 | 4 | 0 |
| | 7 | 31 | 25 | 0 | 2 | 4 | 0 |

*Table 102:* **User I/Os Per Bank for XC3S1000, XC3S1500, and XC3S2000 in FG456 Package**

| Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | DUAL | DCI | VREF | GCLK |
| Top | 0 | 40 | 31 | 0 | 2 | 5 | 2 |
| | 1 | 40 | 31 | 0 | 2 | 5 | 2 |
| Right | 2 | 43 | 37 | 0 | 2 | 4 | 0 |
| | 3 | 43 | 37 | 0 | 2 | 4 | 0 |
| Bottom | 4 | 41 | 26 | 6 | 2 | 5 | 2 |
| | 5 | 40 | 25 | 6 | 2 | 5 | 2 |
| Left | 6 | 43 | 37 | 0 | 2 | 4 | 0 |
| | 7 | 43 | 37 | 0 | 2 | 4 | 0 |

*Table 107:* **FG900 Package Pinout *(Cont'd)***

| Bank | XC3S2000 Pin Name | XC3S4000, XC3S5000 Pin Name | FG900 Pin Number | Type |
|---|---|---|---|---|
| 2 | VCCO_2 | VCCO_2 | J28 | VCCO |
| 2 | VCCO_2 | VCCO_2 | N28 | VCCO |
| 3 | IO | IO | AB25 | I/O |
| 3 | IO_L01N_3/VRP_3 | IO_L01N_3/VRP_3 | AH30 | DCI |
| 3 | IO_L01P_3/VRN_3 | IO_L01P_3/VRN_3 | AH29 | DCI |
| 3 | IO_L02N_3/VREF_3 | IO_L02N_3/VREF_3 | AG28 | VREF |
| 3 | IO_L02P_3 | IO_L02P_3 | AG27 | I/O |
| 3 | IO_L03N_3 | IO_L03N_3 | AG30 | I/O |
| 3 | IO_L03P_3 | IO_L03P_3 | AG29 | I/O |
| 3 | IO_L04N_3 | IO_L04N_3 | AF30 | I/O |
| 3 | IO_L04P_3 | IO_L04P_3 | AF29 | I/O |
| 3 | IO_L05N_3 | IO_L05N_3 | AE26 | I/O |
| 3 | IO_L05P_3 | IO_L05P_3 | AF27 | I/O |
| 3 | IO_L06N_3 | IO_L06N_3 | AE29 | I/O |
| 3 | IO_L06P_3 | IO_L06P_3 | AE28 | I/O |
| 3 | IO_L07N_3 | IO_L07N_3 | AD28 | I/O |
| 3 | IO_L07P_3 | IO_L07P_3 | AD27 | I/O |
| 3 | IO_L08N_3 | IO_L08N_3 | AD30 | I/O |
| 3 | IO_L08P_3 | IO_L08P_3 | AD29 | I/O |
| 3 | IO_L09N_3 | IO_L09N_3 | AC24 | I/O |
| 3 | IO_L09P_3/VREF_3 | IO_L09P_3/VREF_3 | AD25 | VREF |
| 3 | IO_L10N_3 | IO_L10N_3 | AC26 | I/O |
| 3 | IO_L10P_3 | IO_L10P_3 | AC25 | I/O |
| 3 | IO_L11N_3 | IO_L11N_3 | AC28 | I/O |
| 3 | IO_L11P_3 | IO_L11P_3 | AC27 | I/O |
| 3 | IO_L13N_3/VREF_3 | IO_L13N_3/VREF_3 | AC30 | VREF |
| 3 | IO_L13P_3 | IO_L13P_3 | AC29 | I/O |
| 3 | IO_L14N_3 | IO_L14N_3 | AB27 | I/O |
| 3 | IO_L14P_3 | IO_L14P_3 | AB26 | I/O |
| 3 | IO_L15N_3 | IO_L15N_3 | AB30 | I/O |
| 3 | IO_L15P_3 | IO_L15P_3 | AB29 | I/O |
| 3 | IO_L16N_3 | IO_L16N_3 | AA22 | I/O |
| 3 | IO_L16P_3 | IO_L16P_3 | AB23 | I/O |
| 3 | IO_L17N_3 | IO_L17N_3 | AA25 | I/O |
| 3 | IO_L17P_3/VREF_3 | IO_L17P_3/VREF_3 | AA24 | VREF |
| 3 | IO_L19N_3 | IO_L19N_3 | AA29 | I/O |
| 3 | IO_L19P_3 | IO_L19P_3 | AA28 | I/O |
| 3 | IO_L20N_3 | IO_L20N_3 | Y21 | I/O |
| 3 | IO_L20P_3 | IO_L20P_3 | AA21 | I/O |
| 3 | IO_L21N_3 | IO_L21N_3 | Y24 | I/O |

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| 2 | IO_L19N_2 | IO_L19N_2 | M29 | I/O |
| 2 | IO_L19P_2 | IO_L19P_2 | M30 | I/O |
| 2 | IO_L20N_2 | IO_L20N_2 | M31 | I/O |
| 2 | IO_L20P_2 | IO_L20P_2 | M32 | I/O |
| 2 | IO_L21N_2 | IO_L21N_2 | M26 | I/O |
| 2 | IO_L21P_2 | IO_L21P_2 | N25 | I/O |
| 2 | IO_L22N_2 | IO_L22N_2 | N27 | I/O |
| 2 | IO_L22P_2 | IO_L22P_2 | N28 | I/O |
| 2 | IO_L23N_2/VREF_2 | IO_L23N_2VREF_2 | N31 | VREF |
| 2 | IO_L23P_2 | IO_L23P_2 | N32 | I/O |
| 2 | IO_L24N_2 | IO_L24N_2 | N24 | I/O |
| 2 | IO_L24P_2 | IO_L24P_2 | P24 | I/O |
| 2 | IO_L26N_2 | IO_L26N_2 | P29 | I/O |
| 2 | IO_L26P_2 | IO_L26P_2 | P30 | I/O |
| 2 | IO_L27N_2 | IO_L27N_2 | P31 | I/O |
| 2 | IO_L27P_2 | IO_L27P_2 | P32 | I/O |
| 2 | IO_L28N_2 | IO_L28N_2 | P33 | I/O |
| 2 | IO_L28P_2 | IO_L28P_2 | P34 | I/O |
| 2 | IO_L29N_2 | IO_L29N_2 | R24 | I/O |
| 2 | IO_L29P_2 | IO_L29P_2 | R25 | I/O |
| 2 | IO_L30N_2 | IO_L30N_2 | R28 | I/O |
| 2 | IO_L30P_2 | IO_L30P_2 | R29 | I/O |
| 2 | IO_L31N_2 | IO_L31N_2 | R31 | I/O |
| 2 | IO_L31P_2 | IO_L31P_2 | R32 | I/O |
| 2 | IO_L32N_2 | IO_L32N_2 | R33 | I/O |
| 2 | IO_L32P_2 | IO_L32P_2 | R34 | I/O |
| 2 | IO_L33N_2 | IO_L33N_2 | R26 | I/O |
| 2 | IO_L33P_2 | IO_L33P_2 | T25 | I/O |
| 2 | IO_L34N_2/VREF_2 | IO_L34N_2/VREF_2 | T28 | VREF |
| 2 | IO_L34P_2 | IO_L34P_2 | T29 | I/O |
| 2 | IO_L35N_2 | IO_L35N_2 | T32 | I/O |
| 2 | IO_L35P_2 | IO_L35P_2 | T33 | I/O |
| 2 | IO_L37N_2 | IO_L37N_2 | U27 | I/O |
| 2 | IO_L37P_2 | IO_L37P_2 | U28 | I/O |
| 2 | IO_L38N_2 | IO_L38N_2 | U29 | I/O |
| 2 | IO_L38P_2 | IO_L38P_2 | U30 | I/O |
| 2 | IO_L39N_2 | IO_L39N_2 | U31 | I/O |
| 2 | IO_L39P_2 | IO_L39P_2 | U32 | I/O |
| 2 | IO_L40N_2 | IO_L40N_2 | U33 | I/O |
| 2 | IO_L40P_2/VREF_2 | IO_L40P_2/VREF_2 | U34 | VREF |

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| 4 | IO_L01N_4/VRP_4 | IO_L01N_4/VRP_4 | AN32 | DCI |
| 4 | IO_L01P_4/VRN_4 | IO_L01P_4/VRN_4 | AP32 | DCI |
| 4 | IO_L02N_4 | IO_L02N_4 | AN31 | I/O |
| 4 | IO_L02P_4 | IO_L02P_4 | AP31 | I/O |
| 4 | IO_L03N_4 | IO_L03N_4 | AM30 | I/O |
| 4 | IO_L03P_4 | IO_L03P_4 | AN30 | I/O |
| 4 | IO_L04N_4 | IO_L04N_4 | AN27 | I/O |
| 4 | IO_L04P_4 | IO_L04P_4 | AP27 | I/O |
| 4 | IO_L05N_4 | IO_L05N_4 | AH26 | I/O |
| 4 | IO_L05P_4 | IO_L05P_4 | AJ26 | I/O |
| 4 | IO_L06N_4/VREF_4 | IO_L06N_4/VREF_4 | AL26 | VREF |
| 4 | IO_L06P_4 | IO_L06P_4 | AM26 | I/O |
| 4 | IO_L07N_4 | IO_L07N_4 | AF25 | I/O |
| 4 | IO_L07P_4 | IO_L07P_4 | AG25 | I/O |
| 4 | IO_L08N_4 | IO_L08N_4 | AH25 | I/O |
| 4 | IO_L08P_4 | IO_L08P_4 | AJ25 | I/O |
| 4 | IO_L09N_4 | IO_L09N_4 | AL25 | I/O |
| 4 | IO_L09P_4 | IO_L09P_4 | AM25 | I/O |
| 4 | IO_L10N_4 | IO_L10N_4 | AN25 | I/O |
| 4 | IO_L10P_4 | IO_L10P_4 | AP25 | I/O |
| 4 | IO_L11N_4 | IO_L11N_4 | AD23 | I/O |
| 4 | IO_L11P_4 | IO_L11P_4 | AE23 | I/O |
| 4 | IO_L12N_4 | IO_L12N_4 | AF23 | I/O |
| 4 | IO_L12P_4 | IO_L12P_4 | AG23 | I/O |
| 4 | IO_L13N_4 | IO_L13N_4 | AJ23 | I/O |
| 4 | IO_L13P_4 | IO_L13P_4 | AK23 | I/O |
| 4 | IO_L14N_4 | IO_L14N_4 | AL23 | I/O |
| 4 | IO_L14P_4 | IO_L14P_4 | AM23 | I/O |
| 4 | IO_L15N_4 | IO_L15N_4 | AN23 | I/O |
| 4 | IO_L15P_4 | IO_L15P_4 | AP23 | I/O |
| 4 | IO_L16N_4 | IO_L16N_4 | AG22 | I/O |
| 4 | IO_L16P_4 | IO_L16P_4 | AH22 | I/O |
| 4 | IO_L17N_4 | IO_L17N_4 | AL22 | I/O |
| 4 | IO_L17P_4 | IO_L17P_4 | AM22 | I/O |
| 4 | IO_L18N_4 | IO_L18N_4 | AD21 | I/O |
| 4 | IO_L18P_4 | IO_L18P_4 | AE21 | I/O |
| 4 | IO_L19N_4 | IO_L19N_4 | AG21 | I/O |
| 4 | IO_L19P_4 | IO_L19P_4 | AH21 | I/O |
| 4 | IO_L20N_4 | IO_L20N_4 | AJ21 | I/O |
| 4 | IO_L20P_4 | IO_L20P_4 | AK21 | I/O |

*Table 110:* **FG1156 Package Pinout *(Cont'd)***

| Bank | XC3S4000 Pin Name | XC3S5000 Pin Name | FG1156 Pin Number | Type |
|---|---|---|---|---|
| 5 | VCCO_5 | VCCO_5 | AJ13 | VCCO |
| 5 | VCCO_5 | VCCO_5 | AL11 | VCCO |
| 5 | VCCO_5 | VCCO_5 | AL16 | VCCO |
| 5 | VCCO_5 | VCCO_5 | AM4 | VCCO |
| 5 | VCCO_5 | VCCO_5 | AM8 | VCCO |
| 5 | VCCO_5 | VCCO_5 | AN13 | VCCO |
| 6 | IO | IO | AH1 | I/O |
| 6 | IO | IO | AH2 | I/O |
| 6 | IO | IO | V9 | I/O |
| 6 | IO | IO | V10 | I/O |
| 6 | IO_L01N_6/VRP_6 | IO_L01N_6/VRP_6 | AM2 | DCI |
| 6 | IO_L01P_6/VRN_6 | IO_L01P_6/VRN_6 | AM1 | DCI |
| 6 | IO_L02N_6 | IO_L02N_6 | AL2 | I/O |
| 6 | IO_L02P_6 | IO_L02P_6 | AL1 | I/O |
| 6 | IO_L03N_6/VREF_6 | IO_L03N_6/VREF_6 | AK3 | VREF |
| 6 | IO_L03P_6 | IO_L03P_6 | AK2 | I/O |
| 6 | IO_L04N_6 | IO_L04N_6 | AJ4 | I/O |
| 6 | IO_L04P_6 | IO_L04P_6 | AJ3 | I/O |
| 6 | IO_L05N_6 | IO_L05N_6 | AJ2 | I/O |
| 6 | IO_L05P_6 | IO_L05P_6 | AJ1 | I/O |
| 6 | IO_L06N_6 | IO_L06N_6 | AH6 | I/O |
| 6 | IO_L06P_6 | IO_L06P_6 | AH5 | I/O |
| 6 | IO_L07N_6 | IO_L07N_6 | AG6 | I/O |
| 6 | IO_L07P_6 | IO_L07P_6 | AG5 | I/O |
| 6 | IO_L08N_6 | IO_L08N_6 | AG2 | I/O |
| 6 | IO_L08P_6 | IO_L08P_6 | AG1 | I/O |
| 6 | IO_L09N_6/VREF_6 | IO_L09N_6/VREF_6 | AF7 | VREF |
| 6 | IO_L09P_6 | IO_L09P_6 | AF6 | I/O |
| 6 | IO_L10N_6 | IO_L10N_6 | AG4 | I/O |
| 6 | IO_L10P_6 | IO_L10P_6 | AF4 | I/O |
| 6 | IO_L11N_6 | IO_L11N_6 | AF3 | I/O |
| 6 | IO_L11P_6 | IO_L11P_6 | AF2 | I/O |
| 6 | IO_L12N_6 | IO_L12N_6 | AF8 | I/O |
| 6 | IO_L12P_6 | IO_L12P_6 | AE9 | I/O |
| 6 | IO_L13N_6 | IO_L13N_6 | AE8 | I/O |
| 6 | IO_L13P_6/VREF_6 | IO_L13P_6/VREF_6 | AE7 | VREF |
| 6 | IO_L14N_6 | IO_L14N_6 | AE6 | I/O |
| 6 | IO_L14P_6 | IO_L14P_6 | AE5 | I/O |
| 6 | IO_L15N_6 | IO_L15N_6 | AE4 | I/O |
| 6 | IO_L15P_6 | IO_L15P_6 | AE3 | I/O |