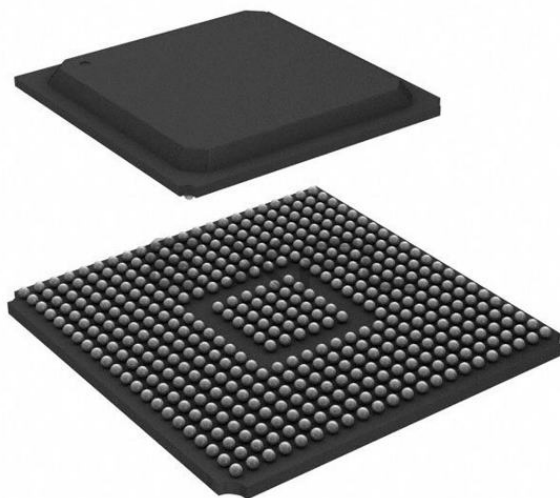




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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	294912
Number of I/O	264
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s400-5fgg456c

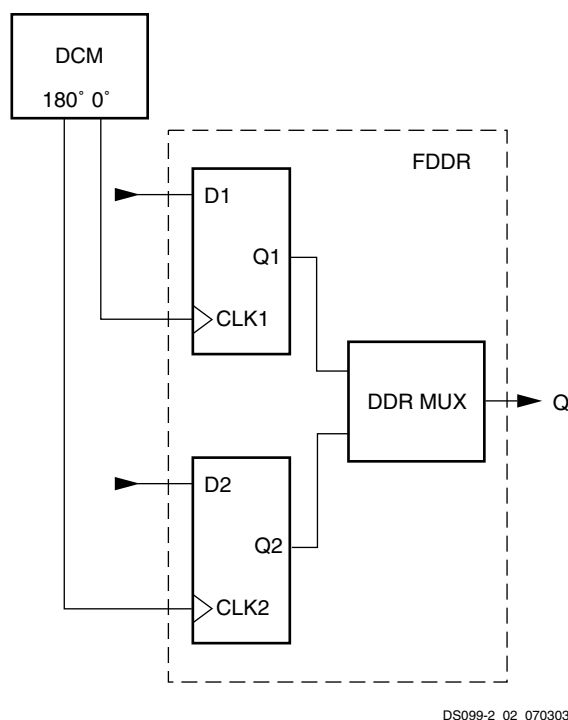


Figure 8: Clocking the DDR Register

Aside from high bandwidth data transfers, DDR can also be used to reproduce, or “mirror”, a clock signal on the output. This approach is used to transmit clock and data signals together. A similar approach is used to reproduce a clock signal at multiple outputs. The advantage for both approaches is that skew across the outputs will be minimal.

Some adjacent I/O blocks (IOBs) share common routing connecting the ICLK1, ICLK2, OTCLK1, and OTCLK2 clock inputs of both IOBs. These IOB pairs are identified by their differential pair names IO_LxxN_# and IO_LxxP_#, where “xx” is an I/O pair number and “#” is an I/O bank number. Two adjacent IOBs containing DDR registers must share common clock inputs, otherwise one or more of the clock signals will be unroutable.

Pull-Up and Pull-Down Resistors

The optional pull-up and pull-down resistors are intended to establish High and Low levels, respectively, at unused I/Os. The pull-up resistor optionally connects each IOB pad to V_{CCO} . A pull-down resistor optionally connects each pad to GND. These resistors are placed in a design using the PULLUP and PULLDOWN symbols in a schematic, respectively. They can also be instantiated as components, set as constraints or passed as attributes in HDL code. These resistors can also be selected for all unused I/O using the Bitstream Generator (BitGen) option UnusedPin. A Low logic level on HSWAP_EN activates the pull-up resistors on all I/Os during configuration (see [The I/Os During Power-On, Configuration, and User Mode, page 21](#)).

The Spartan-3 FPGAs I/O pull-up and pull-down resistors are significantly stronger than the “weak” pull-up/pull-down resistors used in previous Xilinx FPGA families. See [Table 33, page 61](#) for equivalent resistor strengths.

Keeper Circuit

Each I/O has an optional keeper circuit that retains the last logic level on a line after all drivers have been turned off. This is useful to keep bus lines from floating when all connected drivers are in a high-impedance state. This function is placed in a design using the KEEPER symbol. Pull-up and pull-down resistors override the keeper circuit.

Table 20: PS Attributes

Attribute	Description	Values
CLKOUT_PHASE_SHIFT	Disables PS component or chooses between Fixed Phase and Variable Phase modes.	NONE, FIXED, VARIABLE
PHASE_SHIFT	Determines size and direction of initial fine phase shift.	Integers from –255 to +255 ⁽¹⁾

Notes:

- The practical range of values will be less when $T_{CLKIN} > FINE_SHIFT_RANGE$ in the Fixed Phase mode, also when $T_{CLKIN} > (FINE_SHIFT_RANGE)/2$ in the Variable Phase mode. the $FINE_SHIFT_RANGE$ represents the sum total delay of all taps.

The Variable Phase Mode

The “Variable Phase” mode dynamically adjusts the fine phase shift over time using three inputs to the PS component, namely PSEN, PSCLK and PSINCDEC, as defined in [Table 21](#).

After device configuration, the PS component initially determines T_{PS} by evaluating Equation (4) for the value assigned to the PHASE_SHIFT attribute. Then to dynamically adjust that phase shift, use the three PS inputs to increase or decrease the fine phase shift.

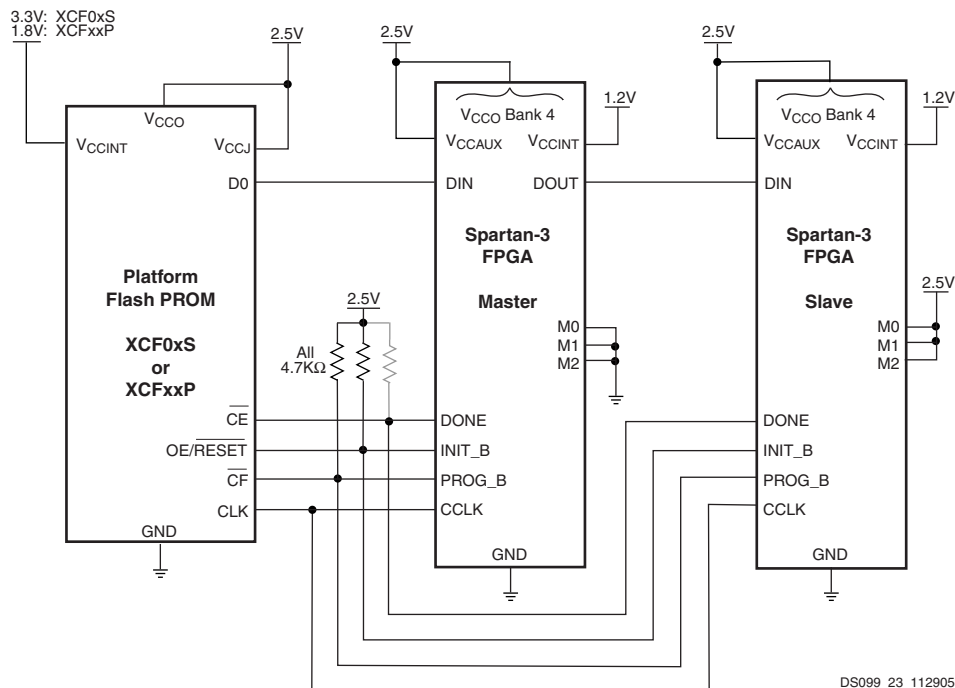
PSINCDEC is synchronized to the PSCLK clock signal, which is enabled by asserting PSEN. It is possible to drive the PSCLK input with the CLKIN signal or any other clock signal. A request for phase adjustment is entered as follows: For each PSCLK cycle that PSINCDEC is High, the PS component adds 1/256 of a CLKIN cycle to T_{PS} . Similarly, for each enabled PSCLK cycle that PSINCDEC is Low, the PS component subtracts 1/256 of a CLKIN cycle from T_{PS} . The phase adjustment may require as many as 100 CLKIN cycles plus three PSCLK cycles to take effect, at which point the output PSDONE goes High for one PSCLK cycle. This pulse indicates that the PS component has finished the present adjustment and is now ready for the next request. Asserting the Reset (RST) input, returns T_{PS} to its original shift time, as determined by the PHASE_SHIFT attribute value. The set of waveforms in section [c] of [Figure 23, page 41](#) illustrates the relationship between CLKFB and CLKIN in the Variable Phase mode.

Table 21: Signals for Variable Phase Mode

Signal	Direction	Description
PSEN ⁽¹⁾	Input	Enables PSCLK for variable phase adjustment.
PSCLK ⁽¹⁾	Input	Clock to synchronize phase shift adjustment.
PSINCDEC ⁽¹⁾	Input	Chooses between increment and decrement for phase adjustment. It is synchronized to the PSCLK signal.
PSDONE	Output	Goes High to indicate that present phase adjustment is complete and PS component is ready for next phase adjustment request. It is synchronized to the PSCLK signal.

Notes:

- It is possible to program this input for either a true or inverted polarity



Notes:

- There are two ways to use the DONE line. First, one may set the BitGen option DriveDone to "Yes" only for the last FPGA to be configured in the chain shown above (or for the single FPGA as may be the case). This enables the DONE pin to drive High; thus, no pull-up resistor is necessary. DriveDone is set to "No" for the remaining FPGAs in the chain. Second, DriveDone can be set to "No" for all FPGAs. Then all DONE lines are open-drain and require the pull-up resistor shown in grey. In most cases, a value between 3.3KΩ to 4.7KΩ is sufficient. However, when using DONE synchronously with a long chain of FPGAs, cumulative capacitance may necessitate lower resistor values (e.g. down to 330Ω) in order to ensure a rise time within one clock cycle.
- For information on how to program the FPGA using 3.3V signals and power, see [3.3V-Tolerant Configuration Interface](#).

Figure 26: Connection Diagram for Master and Slave Serial Configuration

Slave Serial mode is selected by applying <111> to the mode pins (M0, M1, and M2). A pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

Master Serial Mode

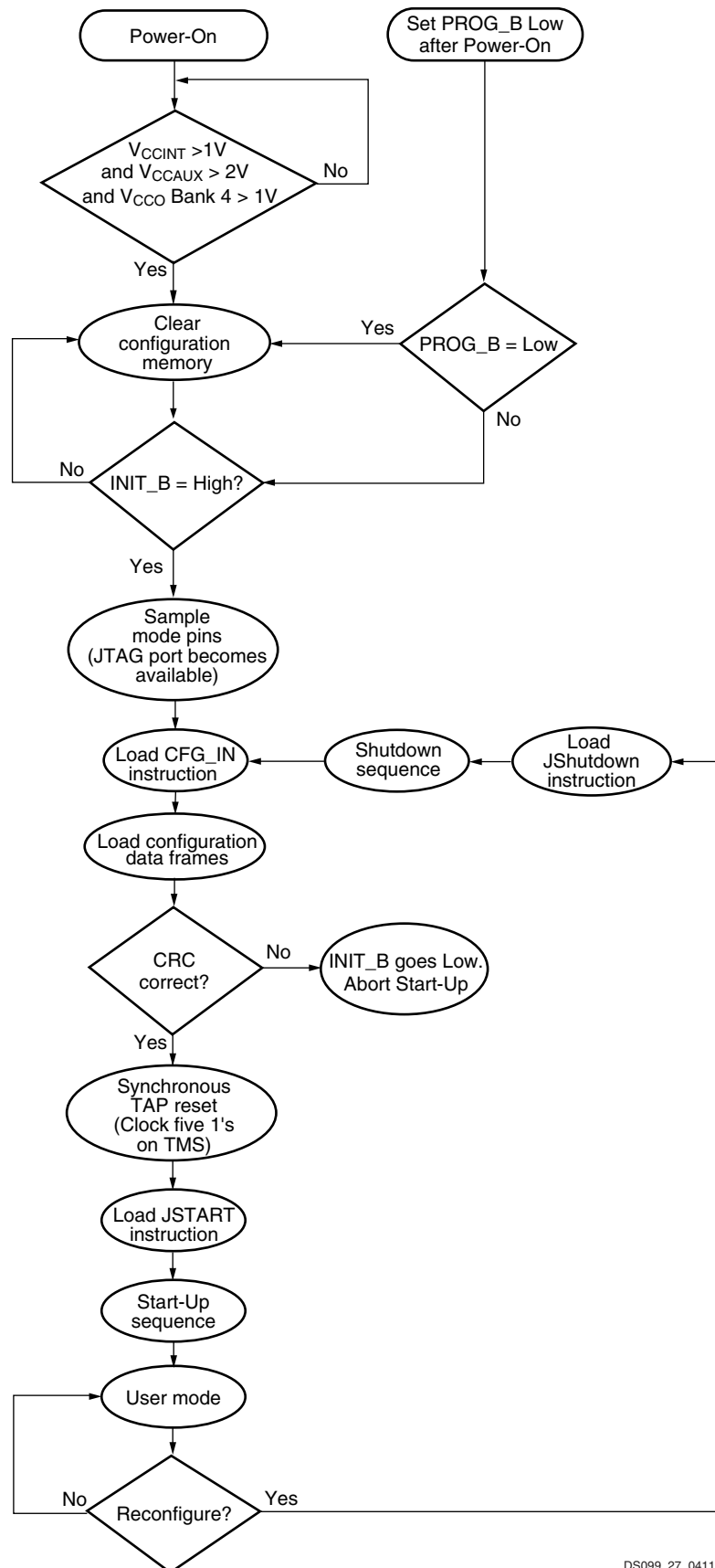
In Master Serial mode, the FPGA drives CCLK pin, which behaves as a bidirectional I/O pin. The FPGA in the center of Figure 26 is set for Master Serial mode and connects to the serial configuration PROM and to the CCLK inputs of any slave FPGAs in a configuration daisy-chain. The master FPGA drives the configuration clock on the CCLK pin to the Xilinx Serial PROM, which, in response, provides bit-serial data to the FPGA's DIN input. The FPGA accepts this data on each rising CCLK edge. After the master FPGA finishes configuring, it passes data on its DOUT pin to the next FPGA device in a daisy-chain. The DOUT data appears after the falling CCLK clock edge.

The Master Serial mode interface is identical to Slave Serial except that an internal oscillator generates the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK, which always starts at a default frequency of 6 MHz. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

Slave Parallel Mode (SelectMAP)

The Parallel or SelectMAP modes support the fastest configuration. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data. An external source provides 8-bit-wide data, CCLK, an active-Low Chip Select (CS_B) signal and an active-Low Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the Slave Parallel mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, it is possible to use any of the Multipurpose pins (DIN/D0-D7, DOUT/BUSY, INIT_B, CS_B, and RDWR_B) as User I/Os. To do this, simply set the BitGen option *Persist* to *No* and assign the desired signals to multipurpose configuration pins using the Xilinx development software. Alternatively, it is possible to continue using the configuration port



DS099_27_041103

Figure 30: Boundary-Scan Configuration Flow Diagram

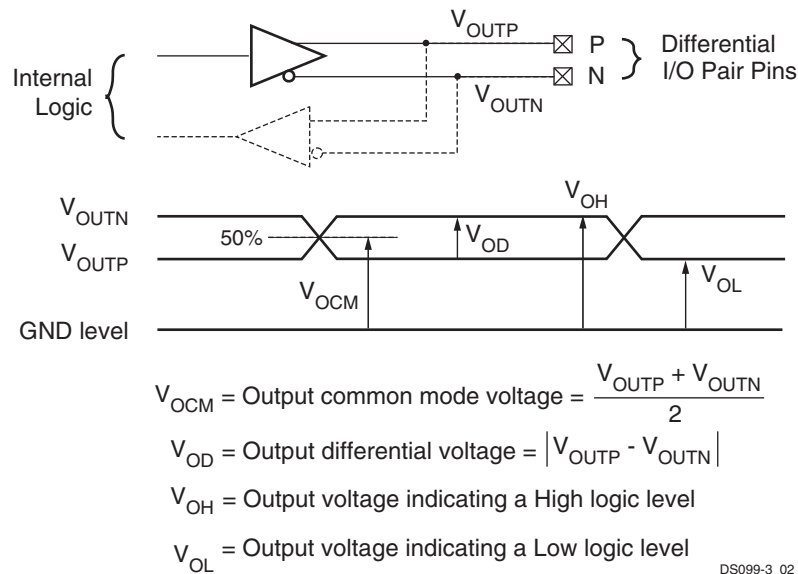


Figure 33: Differential Output Voltages

Table 38: DC Characteristics of User I/Os Using Differential Signal Standards

Signal Standard	Mask ⁽³⁾ Revision	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
		Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LDT_25 (ULVDS_25)	All	430 ⁽⁴⁾	600	670	0.495	0.600	0.715	0.71	0.50
LVDS_25	All	100	—	600	0.80	—	1.6	0.85	1.55
	'E'	200	—	500	1.0	—	1.5	1.10	1.40
BLVDS_25 ⁽⁵⁾	All	250	350	450	—	1.20	—	—	—
LVDSEXT_25	All	100	—	600	0.80	—	1.6	0.85	1.55
	'E'	300	—	700	1.0	—	1.5	1.15	1.35
LVPECL_25 ⁽⁵⁾	All	—	—	—	—	—	—	1.35	1.005
RSDS_25 ⁽⁶⁾	All	100	—	600	0.80	—	1.6	0.85	1.55
	'E'	200	—	500	1.0	—	1.5	1.10	1.40
DIFF_HSTL_II_18	All	—	—	—	—	—	—	$V_{CCO} - 0.40$	0.40
DIFF_SSTL2_II	All	—	—	—	—	—	—	$V_{TT} + 0.80$	$V_{TT} - 0.80$

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32 and Table 37.
2. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100 Ω across the N and P pins of the differential signal pair.
3. Mask revision E devices have tighter output ranges but can be used in any design that was in a previous revision. See Mask and Fab Revisions, page 58.
4. This value must be compatible with the receiver to which the FPGA's output pair is connected.
5. Each LVPECL_25 or BLVDS_25 output-pair requires three external resistors for proper output operation as shown in Figure 34. Each LVPECL_25 or BLVDS_25 input-pair uses a 100W termination resistor at the receiver.
6. Only one of the differential standards RSDS_25, LDT_25, LVDS_25, and LVDSEXT_25 may be used for outputs within a bank. Each differential standard input-pair requires an external 100 Ω termination resistor.

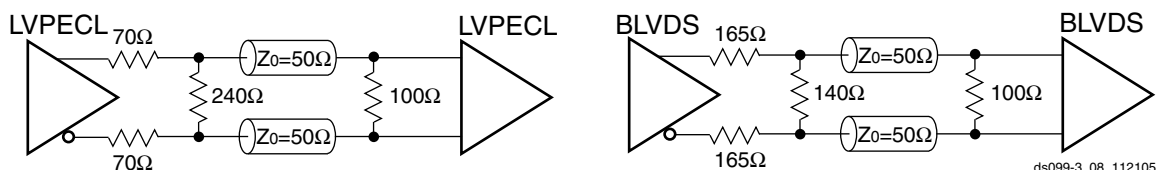


Figure 34: External Termination Required for LVPECL and BLVDS Output and Input

Table 41: System-Synchronous Pin-to-Pin Setup and Hold Times for the IOB Input Path (Cont'd)

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
T _{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25 ⁽³⁾ , IOBDELAY = IFD, without DCM	XC3S50	-0.98	-0.93	ns
			XC3S200	-0.40	-0.35	ns
			XC3S400	-0.27	-0.22	ns
			XC3S1000	-1.19	-1.14	ns
			XC3S1500	-1.43	-1.38	ns
			XC3S2000	-2.33	-2.28	ns
			XC3S4000	-2.47	-2.42	ns
			XC3S5000	-2.66	-2.61	ns

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 48](#) and are based on the operating conditions set forth in [Table 32](#) and [Table 35](#).
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *subtract* the appropriate adjustment from [Table 44](#). If this is true of the data Input, *add* the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *add* the appropriate Input adjustment from [Table 44](#). If this is true of the data Input, *subtract* the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Table 42: Setup and Hold Times for the IOB Input Path

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Setup Times						
T _{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25 ⁽²⁾ , IOBDELAY = NONE	XC3S50	1.65	1.89	ns
			XC3S200	1.37	1.57	ns
			XC3S400	1.37	1.57	ns
			XC3S1000	1.65	1.89	ns
			XC3S1500	1.65	1.89	ns
			XC3S2000	1.65	1.89	ns
			XC3S4000	1.73	1.99	ns
			XC3S5000	1.82	2.09	ns
T _{IOPICKD}	Time from the setup of data at the Input pin to the active transition at the IFF's ICLK input. The Input Delay is programmed.	LVCMOS25 ⁽²⁾ , IOBDELAY = IFD	XC3S50	4.39	5.04	ns
			XC3S200	4.76	5.47	ns
			XC3S400	4.63	5.32	ns
			XC3S1000	5.02	5.76	ns
			XC3S1500	5.40	6.20	ns
			XC3S2000	6.68	7.68	ns
			XC3S4000	7.16	8.24	ns
			XC3S5000	7.33	8.42	ns

Table 47: Output Timing Adjustments for IOB (Cont'd)

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
PCI33_3	0.74	0.85	ns
SSTL18_I	0.07	0.07	ns
SSTL18_I_DCI	0.22	0.25	ns
SSTL18_II	0.30	0.34	ns
SSTL2_I	0.23	0.26	ns
SSTL2_I_DCI	0.19	0.22	ns
SSTL2_II	0.13	0.15	ns
SSTL2_II_DCI	0.10	0.11	ns
Differential Standards			
LDT_25 (ULVDS_25)	−0.06	−0.05	ns
LVDS_25	−0.09	−0.07	ns
BLVDS_25	0.02	0.04	ns
LVDSEXT_25	−0.15	−0.13	ns
LVPECL_25	0.16	0.18	ns
RSDS_25	0.05	0.06	ns
DIFF_HSTL_II_18	−0.02	−0.01	ns
DIFF_HSTL_II_18_DCI	0.75	0.86	ns
DIFF_SSTL2_II	0.13	0.15	ns
DIFF_SSTL2_II_DCI	0.10	0.11	ns

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 48](#) and are based on the operating conditions set forth in [Table 32](#), [Table 35](#), and [Table 37](#).
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.
3. For minimums, use the values reported by the Xilinx timing analyzer.

Table 48: Test Methods for Timing Measurement at I/Os (Cont'd)

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V _{REF} (V)	V _L (V)	V _H (V)	R _T (Ω)	V _T (V)	V _M (V)
HSTL_III_18		1.1	V _{REF} − 0.5	V _{REF} + 0.5	50	1.8	V _{REF}
HSTL_III_DCI_18							
LVCMOS12		-	0	1.2	1M	0	0.6
LVCMOS15		-	0	1.5	1M	0	0.75
LVDCI_15							
LVDCI_DV2_15							
HSLVDCI_15							
LVCMOS18		-	0	1.8	1M	0	0.9
LVDCI_18							
LVDCI_DV2_18							
HSLVDCI_18							
LVCMOS25		-	0	2.5	1M	0	1.25
LVDCI_25							
LVDCI_DV2_25							
HSLVDCI_25							
LVCMOS33		-	0	3.3	1M	0	1.65
LVDCI_33							
LVDCI_DV2_33							
HSLVDCI_33							
LVTTL		-	0	3.3	1M	0	1.4
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
SSTL18_I		0.9	V _{REF} − 0.5	V _{REF} + 0.5	50	0.9	V _{REF}
SSTL18_I_DCI							
SSTL18_II		0.9	V _{REF} − 0.5	V _{REF} + 0.5	50	0.9	V _{REF}
SSTL2_I		1.25	V _{REF} − 0.75	V _{REF} + 0.75	50	1.25	V _{REF}
SSTL2_I_DCI							
SSTL2_II		1.25	V _{REF} − 0.75	V _{REF} + 0.75	25	1.25	V _{REF}
SSTL2_II_DCI					50	1.25	
Differential							
LDT_25 (ULVDS_25)		-	V _{ICM} − 0.125	V _{ICM} + 0.125	60	0.6	V _{ICM}
LVDS_25		-	V _{ICM} − 0.125	V _{ICM} + 0.125	50	1.2	V _{ICM}
LVDS_25_DCI					N/A	N/A	
BLVDS_25		-	V _{ICM} − 0.125	V _{ICM} + 0.125	1M	0	V _{ICM}
LVDSEXT_25		-	V _{ICM} − 0.125	V _{ICM} + 0.125	50	1.2	V _{ICM}
LVDSEXT_25_DCI					N/A	N/A	
LVPECL_25		-	V _{ICM} − 0.3	V _{ICM} + 0.3	1M	0	V _{ICM}
RSDS_25		-	V _{ICM} − 0.1	V _{ICM} + 0.1	50	1.2	V _{ICM}
DIFF_HSTL_II_18		-	V _{ICM} − 0.5	V _{ICM} + 0.5	50	1.8	V _{ICM}
DIFF_HSTL_II_18_DCI							

Table 56: Block RAM Timing

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T _{BCKO}	When reading from the Block RAM, the time from the active transition at the CLK input to data appearing at the DOUT output	–	2.09	–	2.40	ns
Setup Times						
T _{BDCK}	Time from the setup of data at the DIN inputs to the active transition at the CLK input of the Block RAM	0.43	–	0.49	–	ns
Hold Times						
T _{BCKD}	Time from the active transition at the Block RAM's CLK input to the point where data is last held at the DIN inputs	0	–	0	–	ns
Clock Timing						
T _{BPWH}	Block RAM CLK signal High pulse width	1.19	∞	1.37	∞	ns
T _{BPWL}	Block RAM CLK signal Low pulse width	1.19	∞	1.37	∞	ns

Notes:

- The numbers in this table are based on the operating conditions set forth in [Table 32](#).
- For minimums, use the values reported by the Xilinx timing analyzer.

Clock Distribution Switching Characteristics
Table 57: Clock Distribution Switching Characteristics

Description	Symbol	Maximum		Units
		Speed Grade		
		-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I-input to O-output delay	T _{GIO}	0.36	0.41	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0- and I1-inputs. Same as BUFGCE enable CE-input	T _{GSI}	0.53	0.60	ns

Notes:

- For minimums, use the values reported by the Xilinx timing analyzer.

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables ([Table 58](#) and [Table 59](#)) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables ([Table 60](#) through [Table 63](#)) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in [Table 58](#) and [Table 59](#).

Period jitter and cycle-cycle jitter are two (of many) different ways of characterizing clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the average clock period of all clock cycles in the collection of clock periods sampled (usually from 100,000 to more than a million samples for specification purposes). In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Delay-Locked Loop (DLL)

Table 58: Recommended Operating Conditions for the DLL

Symbol		Description	Frequency Mode/ F _{CLKIN} Range	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges								
F _{CLKIN}	CLKIN_FREQ_DLL_LF	Frequency for the CLKIN input	Low	18 ⁽²⁾	167 ⁽³⁾	18 ⁽²⁾	167 ⁽³⁾	MHz
	CLKIN_FREQ_DLL_HF		High	48	280 ⁽³⁾	48	280 ⁽³⁾⁽⁴⁾	MHz
Input Pulse Requirements								
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	F _{CLKIN} ≤ 100 MHz	40%	60%	40%	60%	-
			F _{CLKIN} > 100 MHz	45%	55%	45%	55%	-
Input Clock Jitter Tolerance and Delay Path Variation ⁽⁵⁾								
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	Low	—	±300	—	±300	ps
CLKIN_CYC_JITT_DLL_HF			High	—	±150	—	±150	ps
CLKIN_PER_JITT_DLL_LF		Period jitter at the CLKIN input	All	—	±1	—	±1	ns
CLKIN_PER_JITT_DLL_HF			—	—	—	—		
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input	All	—	±1	—	±1	ns

Notes:

- DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
- The DFS, when operating independently of the DLL, supports lower F_{CLKIN} frequencies. See [Table 60](#).
- The CLKIN_DIVIDE_BY_2 attribute can be used to increase the effective input frequency range up to F_{BUFG} . When set to TRUE, CLKIN_DIVIDE_BY_2 divides the incoming clock frequency by two as it enters the DCM.
- Industrial temperature range devices have additional requirements for continuous clocking, as specified in [Table 64](#).
- CLKIN input jitter beyond these limits may cause the DCM to lose lock. See [UG331](#) for more details.

All VCCAUX inputs must be connected together and to the +2.5V voltage supply. Furthermore, there must be sufficient supply decoupling to guarantee problem-free operation, as described in [XAPP623](#).

Because VCCAUX connects to the DCMs and the DCMs are sensitive to voltage changes, be sure that the VCCAUX supply and the ground return paths are designed for low noise and low voltage drop, especially that caused by a large number of simultaneous switching I/Os.

GND Type: Ground

All GND pins must be connected and have a low resistance path back to the various VCCO, VCCINT, and VCCAUX supplies.

Pin Behavior During Configuration

[Table 79](#) shows how various pins behave during the FPGA configuration process. The actual behavior depends on the values applied to the M2, M1, and M0 mode select pins and the HSWAP_EN pin. The mode select pins determine which of the DUAL type pins are active during configuration. In JTAG configuration mode, none of the DUAL-type pins are used for configuration and all behave as user-I/O pins.

All DUAL-type pins not actively used during configuration and all I/O-type, DCI-type, VREF-type, GCLK-type pins are high impedance (floating, three-stated, Hi-Z) during the configuration process. These pins are indicated in [Table 79](#) as shaded table entries or cells. These pins have a pull-up resistor to their associated VCCO if the HSWAP_EN pin is Low. When HSWAP_EN is High, these pull-up resistors are disabled during configuration.

Some pins always have an active pull-up resistor during configuration, regardless of the value applied to the HSWAP_EN pin. After configuration, these pull-up resistors are controlled by [Bitstream Options](#).

- All the dedicated CONFIG-type configuration pins (CCLK, PROG_B, DONE, M2, M1, M0, and HSWAP_EN) have a pull-up resistor to VCCAUX.
- All JTAG-type pins (TCK, TDI, TMS, TDO) have a pull-up resistor to VCCAUX.
- The INIT_B DUAL-purpose pin has a pull-up resistor to VCCO_4 or VCCO_BOTTOM, depending on package style.

After configuration completes, some pins have optional behavior controlled by the configuration bitstream loaded into the part. For example, via the bitstream, all unused I/O pins can be collectively configured as input pins with either a pull-up resistor, a pull-down resistor, or be left in a high-impedance state.

Table 79: Pin Behavior After Power-Up, During Configuration

Pin Name	Configuration Mode Settings <M2:M1:M0>					Bitstream Configuration Option
	Serial Modes		SelectMap Parallel Modes		JTAG Mode <1:0:1>	
	Master <0:0:0>	Slave <1:1:1>	Master <0:1:1>	Slave <1:1:0>		
I/O: General-purpose I/O pins						
IO						UnusedPin
IO_Lxxy_#						UnusedPin
DUAL: Dual-purpose configuration pins						
IO_Lxxy_#/ DIN/D0	DIN (I)	DIN (I)	D0 (I/O)	D0 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D1			D1 (I/O)	D1 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D2			D2 (I/O)	D2 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D3			D3 (I/O)	D3 (I/O)		Persist UnusedPin
IO_Lxxy_#/ D4			D4 (I/O)	D4 (I/O)		Persist UnusedPin

Table 87: VQ100 Package Pinout (Cont'd)

Bank	XC3S50 XC3S200 Pin Name	VQ100 Pin Number	Type
VCCAUX	TDO	P76	JTAG
VCCAUX	TMS	P78	JTAG

User I/Os by Bank

Table 88 indicates how the available user-I/O pins are distributed between the eight I/O banks on the VQ100 package.

Table 88: User I/Os Per Bank in VQ100 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	6	1	0	2	1	2
	1	7	2	0	2	1	2
Right	2	8	5	0	2	1	0
	3	8	5	0	2	1	0
Bottom	4	10	0	6	2	0	2
	5	8	0	6	0	0	2
Left	6	8	4	0	2	2	0
	7	8	5	0	2	1	0

Table 98: FG320 Package Pinout (Cont'd)

Bank	XC3S400, XC3S1000, XC3S1500 Pin Name	FG320 Pin Number	Type
7	IO_L20P_7	E1	I/O
7	IO_L21N_7	E4	I/O
7	IO_L21P_7	F4	I/O
7	IO_L22N_7	G5	I/O
7	IO_L22P_7	F5	I/O
7	IO_L23N_7	G1	I/O
7	IO_L23P_7	F2	I/O
7	IO_L24N_7	G4	I/O
7	IO_L24P_7	G3	I/O
7	IO_L27N_7	H5	I/O
7	IO_L27P_7/VREF_7	H6	VREF
7	IO_L34N_7	H4	I/O
7	IO_L34P_7	H3	I/O
7	IO_L35N_7	H1	I/O
7	IO_L35P_7	H2	I/O
7	IO_L39N_7	J1	I/O
7	IO_L39P_7	J2	I/O
7	IO_L40N_7/VREF_7	J5	VREF
7	IO_L40P_7	J4	I/O
7	VCCO_7	F3	VCCO
7	VCCO_7	H7	VCCO
7	VCCO_7	J7	VCCO
N/A	GND	A1	GND
N/A	GND	A13	GND
N/A	GND	A18	GND
N/A	GND	A6	GND
N/A	GND	B17	GND
N/A	GND	B2	GND
N/A	GND	C10	GND
N/A	GND	C9	GND
N/A	GND	F1	GND
N/A	GND	F18	GND
N/A	GND	G12	GND
N/A	GND	G7	GND
N/A	GND	H10	GND
N/A	GND	H11	GND
N/A	GND	H8	GND
N/A	GND	H9	GND
N/A	GND	J11	GND
N/A	GND	J16	GND

Table 100: FG456 Package Pinout (Cont'd)

Bank	3S400 Pin Name	3S1000, 3S1500, 3S2000 Pin Name	FG456 Pin Number	Type
2	IO_L21P_2	IO_L21P_2	E22	I/O
2	IO_L22N_2	IO_L22N_2	G17	I/O
2	IO_L22P_2	IO_L22P_2	G18	I/O
2	IO_L23N_2/VREF_2	IO_L23N_2/VREF_2	F19	VREF
2	IO_L23P_2	IO_L23P_2	G19	I/O
2	IO_L24N_2	IO_L24N_2	F20	I/O
2	IO_L24P_2	IO_L24P_2	F21	I/O
2	N.C. (◆)	IO_L26N_2	G20	I/O
2	N.C. (◆)	IO_L26P_2	H19	I/O
2	IO_L27N_2	IO_L27N_2	G21	I/O
2	IO_L27P_2	IO_L27P_2	G22	I/O
2	N.C. (◆)	IO_L28N_2	H18	I/O
2	N.C. (◆)	IO_L28P_2	J17	I/O
2	N.C. (◆)	IO_L29N_2	H21	I/O
2	N.C. (◆)	IO_L29P_2	H22	I/O
2	N.C. (◆)	IO_L31N_2	J18	I/O
2	N.C. (◆)	IO_L31P_2	J19	I/O
2	N.C. (◆)	IO_L32N_2	J21	I/O
2	N.C. (◆)	IO_L32P_2	J22	I/O
2	N.C. (◆)	IO_L33N_2	K17	I/O
2	N.C. (◆)	IO_L33P_2	K18	I/O
2	IO_L34N_2/VREF_2	IO_L34N_2/VREF_2	K19	VREF
2	IO_L34P_2	IO_L34P_2	K20	I/O
2	IO_L35N_2	IO_L35N_2	K21	I/O
2	IO_L35P_2	IO_L35P_2	K22	I/O
2	IO_L38N_2	IO_L38N_2	L17	I/O
2	IO_L38P_2	IO_L38P_2	L18	I/O
2	IO_L39N_2	IO_L39N_2	L19	I/O
2	IO_L39P_2	IO_L39P_2	L20	I/O
2	IO_L40N_2	IO_L40N_2	L21	I/O
2	IO_L40P_2/VREF_2	IO_L40P_2/VREF_2	L22	VREF
2	VCCO_2	VCCO_2	H17	VCCO
2	VCCO_2	VCCO_2	H20	VCCO
2	VCCO_2	VCCO_2	J16	VCCO
2	VCCO_2	VCCO_2	K16	VCCO
2	VCCO_2	VCCO_2	L16	VCCO
3	IO	IO	Y21	I/O
3	IO_L01N_3/VRP_3	IO_L01N_3/VRP_3	Y20	DCI
3	IO_L01P_3/VRN_3	IO_L01P_3/VRN_3	Y19	DCI
3	IO_L16N_3	IO_L16N_3	W22	I/O

Table 103: FG676 Package Pinout (Cont'd)

Bank	XC3S1000 Pin Name	XC3S1500 Pin Name	XC3S2000 Pin Name	XC3S4000 Pin Name	XC3S5000 Pin Name	FG676 Pin Number	Type
4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	IO_L22N_4/VREF_4	AD17	VREF
4	IO_L22P_4	IO_L22P_4	IO_L22P_4	IO_L22P_4	IO_L22P_4	AB17	I/O
4	N.C. (◆)	IO_L23N_4	IO_L23N_4	IO_L23N_4	IO_L23N_4	AE17	I/O
4	N.C. (◆)	IO_L23P_4	IO_L23P_4	IO_L23P_4	IO_L23P_4	AF17	I/O
4	IO_L24N_4	IO_L24N_4	IO_L24N_4	IO_L24N_4	IO_L24N_4	Y16	I/O
4	IO_L24P_4	IO_L24P_4	IO_L24P_4	IO_L24P_4	IO_L24P_4	AA16	I/O
4	IO_L25N_4	IO_L25N_4	IO_L25N_4	IO_L25N_4	IO_L25N_4	AB16	I/O
4	IO_L25P_4	IO_L25P_4	IO_L25P_4	IO_L25P_4	IO_L25P_4	AC16	I/O
4	N.C. (◆)	IO_L26N_4	IO_L26N_4	IO_L26N_4	IO_L26N_4	AE16	I/O
4	N.C. (◆)	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	IO_L26P_4/VREF_4	AF16	VREF
4	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	IO_L27N_4/DIN/D0	Y15	DUAL
4	IO_L27P_4/D1	IO_L27P_4/D1	IO_L27P_4/D1	IO_L27P_4/D1	IO_L27P_4/D1	W14	DUAL
4	IO_L28N_4	IO_L28N_4	IO_L28N_4	IO_L28N_4	IO_L28N_4	AA15	I/O
4	IO_L28P_4	IO_L28P_4	IO_L28P_4	IO_L28P_4	IO_L28P_4	AB15	I/O
4	IO_L29N_4	IO_L29N_4	IO_L29N_4	IO_L29N_4	IO_L29N_4	AE15	I/O
4	IO_L29P_4	IO_L29P_4	IO_L29P_4	IO_L29P_4	IO_L29P_4	AF15	I/O
4	IO_L30N_4/D2	IO_L30N_4/D2	IO_L30N_4/D2	IO_L30N_4/D2	IO_L30N_4/D2	Y14	DUAL
4	IO_L30P_4/D3	IO_L30P_4/D3	IO_L30P_4/D3	IO_L30P_4/D3	IO_L30P_4/D3	AA14	DUAL
4	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	IO_L31N_4/INIT_B	AC14	DUAL
4	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	IO_L31P_4/ DOUT/BUSY	AD14	DUAL
4	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	IO_L32N_4/GCLK1	AE14	GCLK
4	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	IO_L32P_4/GCLK0	AF14	GCLK
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	AD16	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	AD20	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	U14	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	V14	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	V15	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	V16	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	W17	VCCO
4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	VCCO_4	W18	VCCO
5	IO	IO	IO	IO	IO	AA7	I/O
5	IO	IO	IO	IO	IO	AA13	I/O
5	IO	IO	IO	IO	IO_L17P_5 ⁽³⁾	AB9	I/O
5	N.C. (◆)	IO	IO	IO	IO_L17N_5 ⁽³⁾	AC9	I/O
5	IO	IO	IO	IO	IO	AC11	I/O
5	IO	IO	IO	IO	IO	AD10	I/O
5	IO	IO	IO	IO	IO	AD12	I/O
5	IO	IO	IO	IO	IO	AF4	I/O
5	IO	IO	IO	IO	IO	Y8	I/O
5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	AF5	VREF
5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	IO/VREF_5	AF13	VREF
5	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	IO_L01N_5/RDWR_B	AC5	DUAL

Table 107: FG900 Package Pinout (Cont'd)

Bank	XC3S2000 Pin Name	XC3S4000, XC3S5000 Pin Name	FG900 Pin Number	Type
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	W12	VCCINT
N/A	VCCINT	VCCINT	M13	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	M14	VCCINT
N/A	VCCINT	VCCINT	W14	VCCINT
N/A	VCCINT	VCCINT	L15	VCCINT
N/A	VCCINT	VCCINT	Y15	VCCINT
N/A	VCCINT	VCCINT	L16	VCCINT
N/A	VCCINT	VCCINT	Y16	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	W17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	W18	VCCINT
N/A	VCCINT	VCCINT	M19	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	P19	VCCINT
N/A	VCCINT	VCCINT	U19	VCCINT
N/A	VCCINT	VCCINT	V19	VCCINT
N/A	VCCINT	VCCINT	W19	VCCINT
N/A	VCCINT	VCCINT	L20	VCCINT
N/A	VCCINT	VCCINT	R20	VCCINT
N/A	VCCINT	VCCINT	T20	VCCINT
N/A	VCCINT	VCCINT	Y20	VCCINT
VCCAUX	CCLK	CCLK	AH28	CONFIG
VCCAUX	DONE	DONE	AJ28	CONFIG
VCCAUX	HSWAP_EN	HSWAP_EN	A3	CONFIG
VCCAUX	M0	M0	AJ3	CONFIG
VCCAUX	M1	M1	AH3	CONFIG
VCCAUX	M2	M2	AK3	CONFIG
VCCAUX	PROG_B	PROG_B	B3	CONFIG
VCCAUX	TCK	TCK	B28	JTAG
VCCAUX	TDI	TDI	C3	JTAG
VCCAUX	TDO	TDO	C28	JTAG
VCCAUX	TMS	TMS	A28	JTAG

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
1	IO_L27N_1	IO_L27N_1	F19	I/O
1	IO_L27P_1	IO_L27P_1	G19	I/O
1	IO_L28N_1	IO_L28N_1	B19	I/O
1	IO_L28P_1	IO_L28P_1	C19	I/O
1	IO_L29N_1	IO_L29N_1	J18	I/O
1	IO_L29P_1	IO_L29P_1	K18	I/O
1	IO_L30N_1	IO_L30N_1	G18	I/O
1	IO_L30P_1	IO_L30P_1	H18	I/O
1	IO_L31N_1/VREF_1	IO_L31N_1/VREF_1	D18	VREF
1	IO_L31P_1	IO_L31P_1	E18	I/O
1	IO_L32N_1/GCLK5	IO_L32N_1/GCLK5	B18	GCLK
1	IO_L32P_1/GCLK4	IO_L32P_1/GCLK4	C18	GCLK
1	N.C. (◆)	IO_L33N_1	C28	I/O
1	N.C. (◆)	IO_L33P_1	D28	I/O
1	N.C. (◆)	IO_L34N_1	A28	I/O
1	N.C. (◆)	IO_L34P_1	B28	I/O
1	N.C. (◆)	IO_L35N_1	J24	I/O
1	N.C. (◆)	IO_L35P_1	K24	I/O
1	N.C. (◆)	IO_L36N_1	F24	I/O
1	N.C. (◆)	IO_L36P_1	G24	I/O
1	IO_L37N_1	IO_L37N_1	J20	I/O
1	IO_L37P_1	IO_L37P_1	K20	I/O
1	IO_L38N_1	IO_L38N_1	F20	I/O
1	IO_L38P_1	IO_L38P_1	G20	I/O
1	IO_L39N_1	IO_L39N_1	C20	I/O
1	IO_L39P_1	IO_L39P_1	D20	I/O
1	IO_L40N_1	IO_L40N_1	A20	I/O
1	IO_L40P_1	IO_L40P_1	B20	I/O
1	VCCO_1	VCCO_1	B22	VCCO
1	VCCO_1	VCCO_1	C27	VCCO
1	VCCO_1	VCCO_1	C31	VCCO
1	VCCO_1	VCCO_1	D19	VCCO
1	VCCO_1	VCCO_1	D24	VCCO
1	VCCO_1	VCCO_1	F22	VCCO
1	VCCO_1	VCCO_1	G27	VCCO
1	VCCO_1	VCCO_1	H20	VCCO
1	VCCO_1	VCCO_1	H24	VCCO
1	VCCO_1	VCCO_1	M19	VCCO
1	VCCO_1	VCCO_1	M20	VCCO
1	VCCO_1	VCCO_1	M21	VCCO

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
3	IO_L24P_3	IO_L24P_3	AC26	I/O
3	IO_L26N_3	IO_L26N_3	AA28	I/O
3	IO_L26P_3	IO_L26P_3	AA27	I/O
3	IO_L27N_3	IO_L27N_3	AA30	I/O
3	IO_L27P_3	IO_L27P_3	AA29	I/O
3	IO_L28N_3	IO_L28N_3	AA32	I/O
3	IO_L28P_3	IO_L28P_3	AA31	I/O
3	IO_L29N_3	IO_L29N_3	AA34	I/O
3	IO_L29P_3	IO_L29P_3	AA33	I/O
3	IO_L30N_3	IO_L30N_3	Y29	I/O
3	IO_L30P_3	IO_L30P_3	Y28	I/O
3	IO_L31N_3	IO_L31N_3	Y32	I/O
3	IO_L31P_3	IO_L31P_3	Y31	I/O
3	IO_L32N_3	IO_L32N_3	Y34	I/O
3	IO_L32P_3	IO_L32P_3	Y33	I/O
3	IO_L33N_3	IO_L33N_3	W25	I/O
3	IO_L33P_3	IO_L33P_3	Y26	I/O
3	IO_L34N_3	IO_L34N_3	W29	I/O
3	IO_L34P_3/VREF_3	IO_L34P_3/VREF_3	W28	VREF
3	IO_L35N_3	IO_L35N_3	W33	I/O
3	IO_L35P_3	IO_L35P_3	W32	I/O
3	IO_L37N_3	IO_L37N_3	V28	I/O
3	IO_L37P_3	IO_L37P_3	V27	I/O
3	IO_L38N_3	IO_L38N_3	V30	I/O
3	IO_L38P_3	IO_L38P_3	V29	I/O
3	IO_L39N_3	IO_L39N_3	V32	I/O
3	IO_L39P_3	IO_L39P_3	V31	I/O
3	IO_L40N_3/VREF_3	IO_L40N_3/VREF_3	V34	VREF
3	IO_L40P_3	IO_L40P_3	V33	I/O
3	N.C. (◆)	IO_L41N_3	AH32	I/O
3	N.C. (◆)	IO_L41P_3	AH31	I/O
3	N.C. (◆)	IO_L44N_3	AD29	I/O
3	N.C. (◆)	IO_L44P_3	AD28	I/O
3	IO_L45N_3	IO_L45N_3	AC34	I/O
3	IO_L45P_3	IO_L45P_3	AC33	I/O
3	IO_L46N_3	IO_L46N_3	AB28	I/O
3	IO_L46P_3	IO_L46P_3	AB27	I/O
3	IO_L47N_3	IO_L47N_3	AB32	I/O
3	IO_L47P_3	IO_L47P_3	AB31	I/O
3	IO_L48N_3	IO_L48N_3	AA24	I/O

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
7	IO_L22P_7	IO_L22P_7	M6	I/O
7	IO_L23N_7	IO_L23N_7	M3	I/O
7	IO_L23P_7	IO_L23P_7	M4	I/O
7	IO_L24N_7	IO_L24N_7	N10	I/O
7	IO_L24P_7	IO_L24P_7	M9	I/O
7	IO_L25N_7	IO_L25N_7	N3	I/O
7	IO_L25P_7	IO_L25P_7	N4	I/O
7	IO_L26N_7	IO_L26N_7	P11	I/O
7	IO_L26P_7	IO_L26P_7	N11	I/O
7	IO_L27N_7	IO_L27N_7	P7	I/O
7	IO_L27P_7/VREF_7	IO_L27P_7/VREF_7	P8	VREF
7	IO_L28N_7	IO_L28N_7	P5	I/O
7	IO_L28P_7	IO_L28P_7	P6	I/O
7	IO_L29N_7	IO_L29N_7	P3	I/O
7	IO_L29P_7	IO_L29P_7	P4	I/O
7	IO_L30N_7	IO_L30N_7	R6	I/O
7	IO_L30P_7	IO_L30P_7	R7	I/O
7	IO_L31N_7	IO_L31N_7	R3	I/O
7	IO_L31P_7	IO_L31P_7	R4	I/O
7	IO_L32N_7	IO_L32N_7	R1	I/O
7	IO_L32P_7	IO_L32P_7	R2	I/O
7	IO_L33N_7	IO_L33N_7	T10	I/O
7	IO_L33P_7	IO_L33P_7	R9	I/O
7	IO_L34N_7	IO_L34N_7	T6	I/O
7	IO_L34P_7	IO_L34P_7	T7	I/O
7	IO_L35N_7	IO_L35N_7	T2	I/O
7	IO_L35P_7	IO_L35P_7	T3	I/O
7	IO_L37N_7	IO_L37N_7	U7	I/O
7	IO_L37P_7/VREF_7	IO_L37P_7/VREF_7	U8	VREF
7	IO_L38N_7	IO_L38N_7	U5	I/O
7	IO_L38P_7	IO_L38P_7	U6	I/O
7	IO_L39N_7	IO_L39N_7	U3	I/O
7	IO_L39P_7	IO_L39P_7	U4	I/O
7	IO_L40N_7/VREF_7	IO_L40N_7/VREF_7	U1	VREF
7	IO_L40P_7	IO_L40P_7	U2	I/O
7	N.C. (◆)	IO_L41N_7	G3	I/O
7	N.C. (◆)	IO_L41P_7	G4	I/O
7	N.C. (◆)	IO_L44N_7	L6	I/O
7	N.C. (◆)	IO_L44P_7	L7	I/O
7	IO_L45N_7	IO_L45N_7	M1	I/O

Table 110: FG1156 Package Pinout (Cont'd)

Bank	XC3S4000 Pin Name	XC3S5000 Pin Name	FG1156 Pin Number	Type
N/A	VCCAUX	VCCAUX	Y5	VCCAUX
N/A	VCCINT	VCCINT	AA13	VCCINT
N/A	VCCINT	VCCINT	AA22	VCCINT
N/A	VCCINT	VCCINT	AB13	VCCINT
N/A	VCCINT	VCCINT	AB14	VCCINT
N/A	VCCINT	VCCINT	AB15	VCCINT
N/A	VCCINT	VCCINT	AB16	VCCINT
N/A	VCCINT	VCCINT	AB19	VCCINT
N/A	VCCINT	VCCINT	AB20	VCCINT
N/A	VCCINT	VCCINT	AB21	VCCINT
N/A	VCCINT	VCCINT	AB22	VCCINT
N/A	VCCINT	VCCINT	AC12	VCCINT
N/A	VCCINT	VCCINT	AC17	VCCINT
N/A	VCCINT	VCCINT	AC18	VCCINT
N/A	VCCINT	VCCINT	AC23	VCCINT
N/A	VCCINT	VCCINT	M12	VCCINT
N/A	VCCINT	VCCINT	M17	VCCINT
N/A	VCCINT	VCCINT	M18	VCCINT
N/A	VCCINT	VCCINT	M23	VCCINT
N/A	VCCINT	VCCINT	N13	VCCINT
N/A	VCCINT	VCCINT	N14	VCCINT
N/A	VCCINT	VCCINT	N15	VCCINT
N/A	VCCINT	VCCINT	N16	VCCINT
N/A	VCCINT	VCCINT	N19	VCCINT
N/A	VCCINT	VCCINT	N20	VCCINT
N/A	VCCINT	VCCINT	N21	VCCINT
N/A	VCCINT	VCCINT	N22	VCCINT
N/A	VCCINT	VCCINT	P13	VCCINT
N/A	VCCINT	VCCINT	P22	VCCINT
N/A	VCCINT	VCCINT	R13	VCCINT
N/A	VCCINT	VCCINT	R22	VCCINT
N/A	VCCINT	VCCINT	T13	VCCINT
N/A	VCCINT	VCCINT	T22	VCCINT
N/A	VCCINT	VCCINT	U12	VCCINT
N/A	VCCINT	VCCINT	U23	VCCINT
N/A	VCCINT	VCCINT	V12	VCCINT
N/A	VCCINT	VCCINT	V23	VCCINT
N/A	VCCINT	VCCINT	W13	VCCINT
N/A	VCCINT	VCCINT	W22	VCCINT
N/A	VCCINT	VCCINT	Y13	VCCINT